The ATLAS Upgrade Programme

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ECFA High Luminosity
LHC Experiments Workshop

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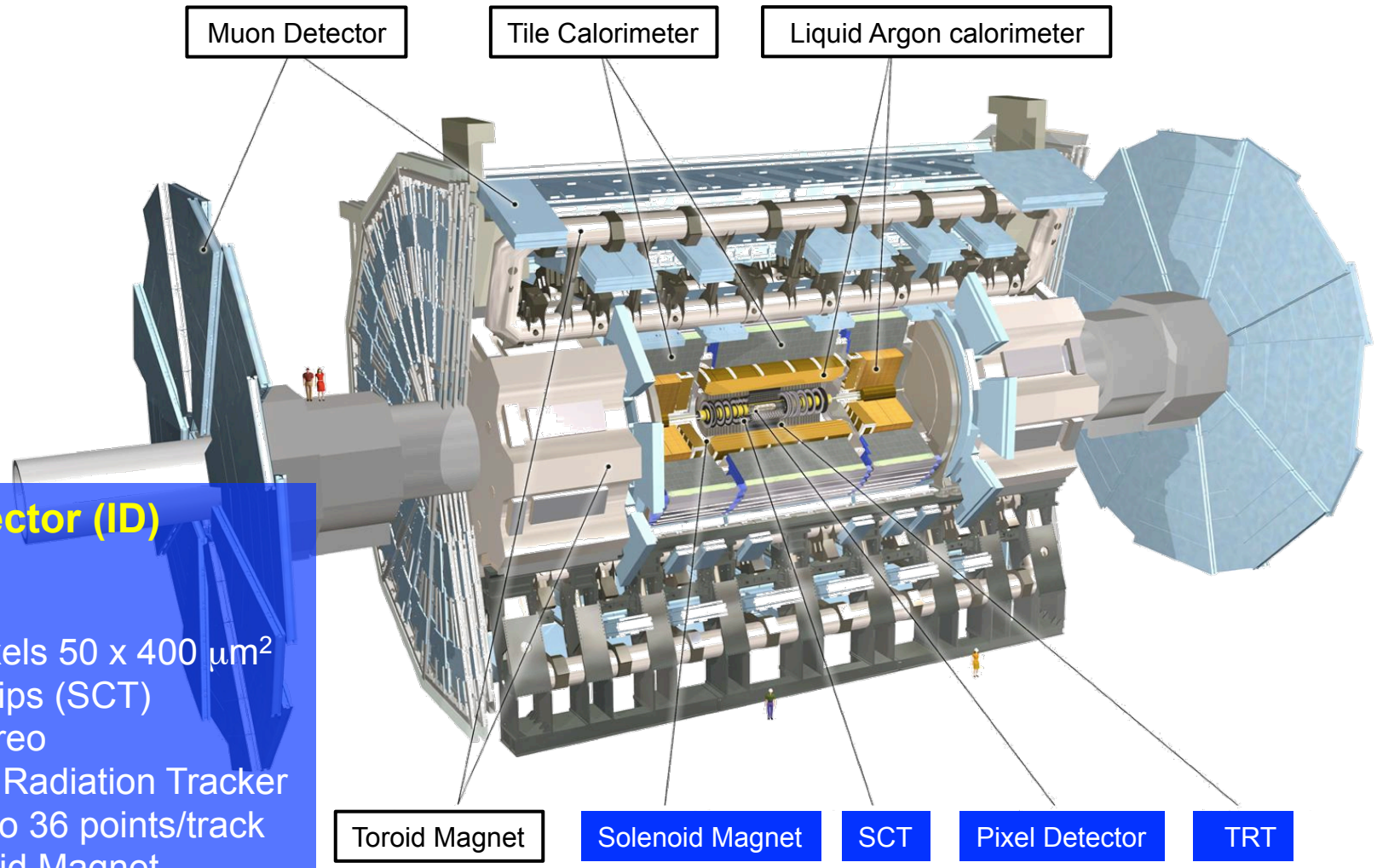
Aix-les-Bains, France

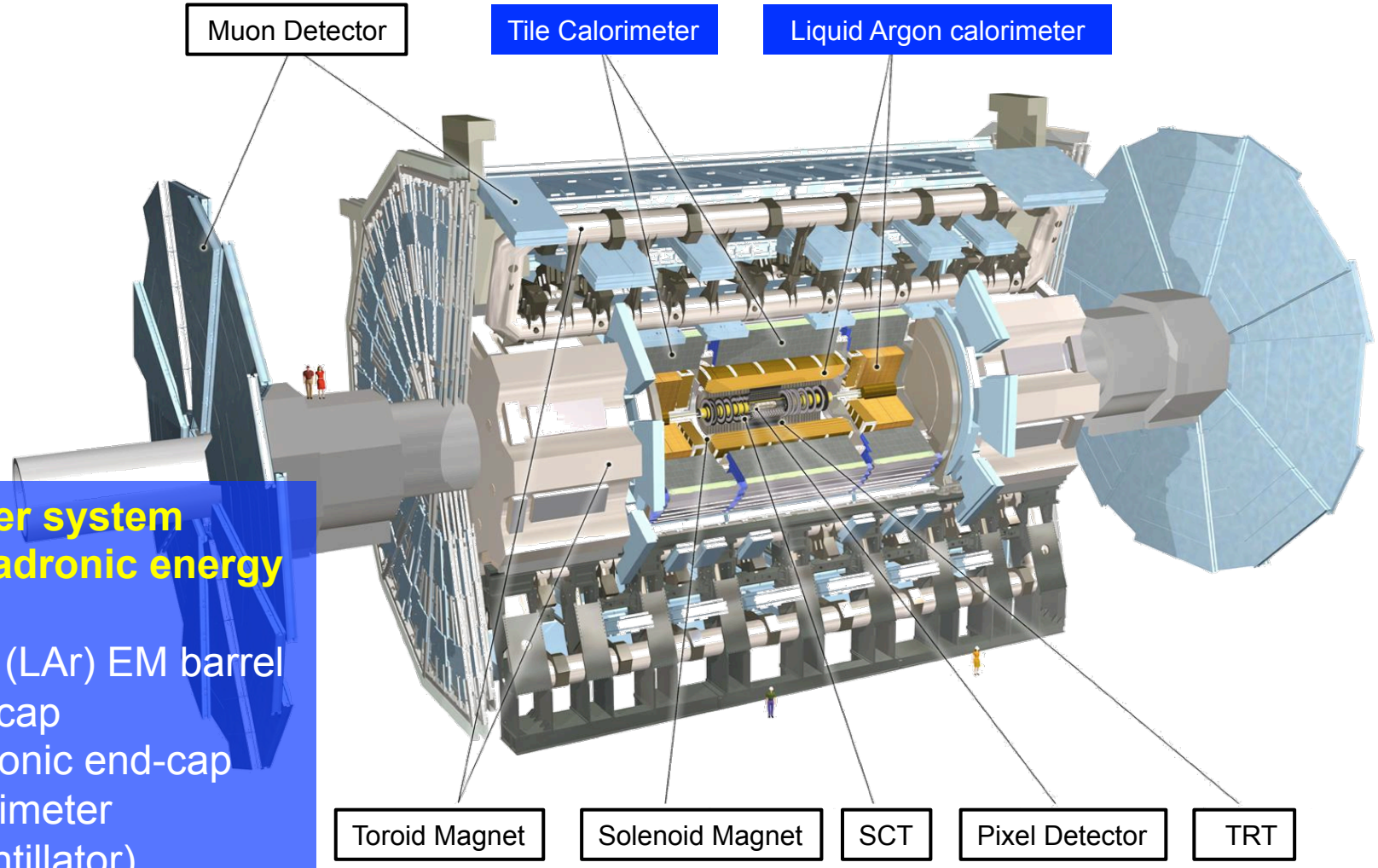
The ATLAS Detector



Inner Detector (ID)
Tracking

- Silicon Pixels 50 x 400 μm^2
- Silicon Strips (SCT) 80 μm stereo
- Transition Radiation Tracker (TRT) up to 36 points/track
- 2T Solenoid Magnet

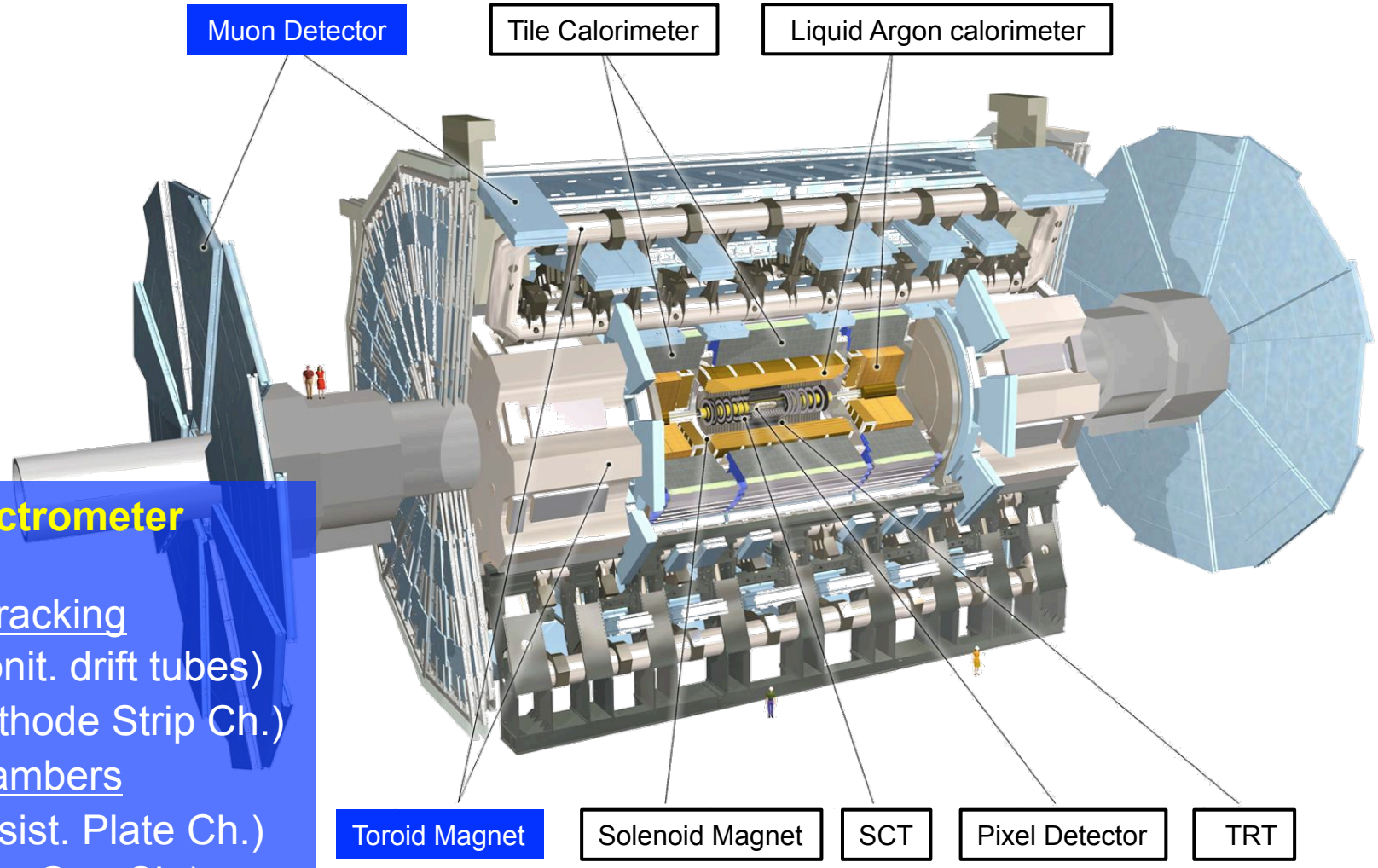
The ATLAS Detector



Calorimeter system
EM and Hadronic energy

- Liquid Ar (LAr) EM barrel and end-cap
- LAr Hadronic end-cap
- Tile calorimeter (Fe – scintillator) hadronic barrel

The ATLAS Detector



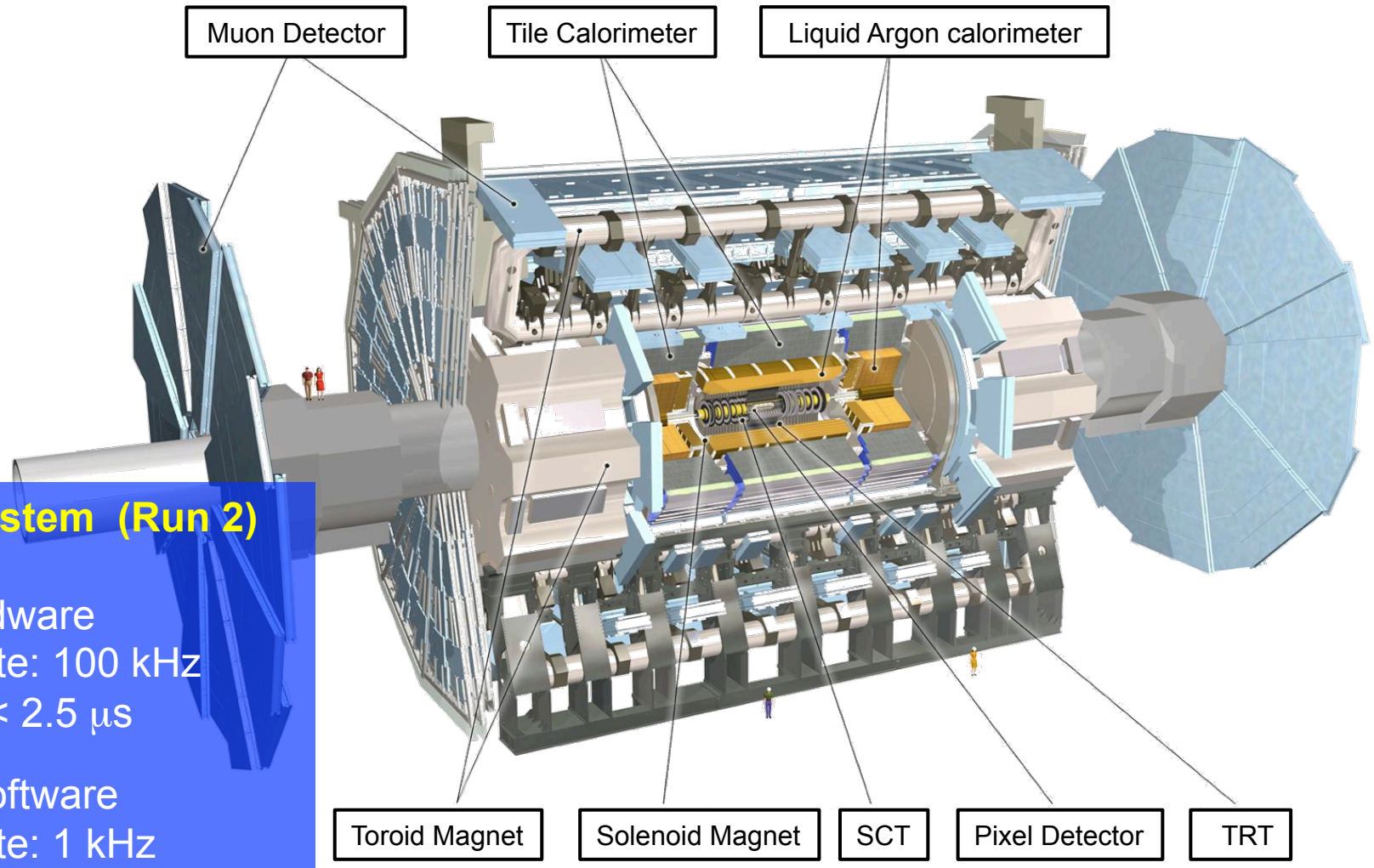
Muon spectrometer
μ tracking

Precision tracking
- MDT (Monit. drift tubes)
- CSC (Cathode Strip Ch.)

Trigger chambers
- RPC (Resist. Plate Ch.)
- TGC (Thin Gap Ch.)

- Toroid Magnet

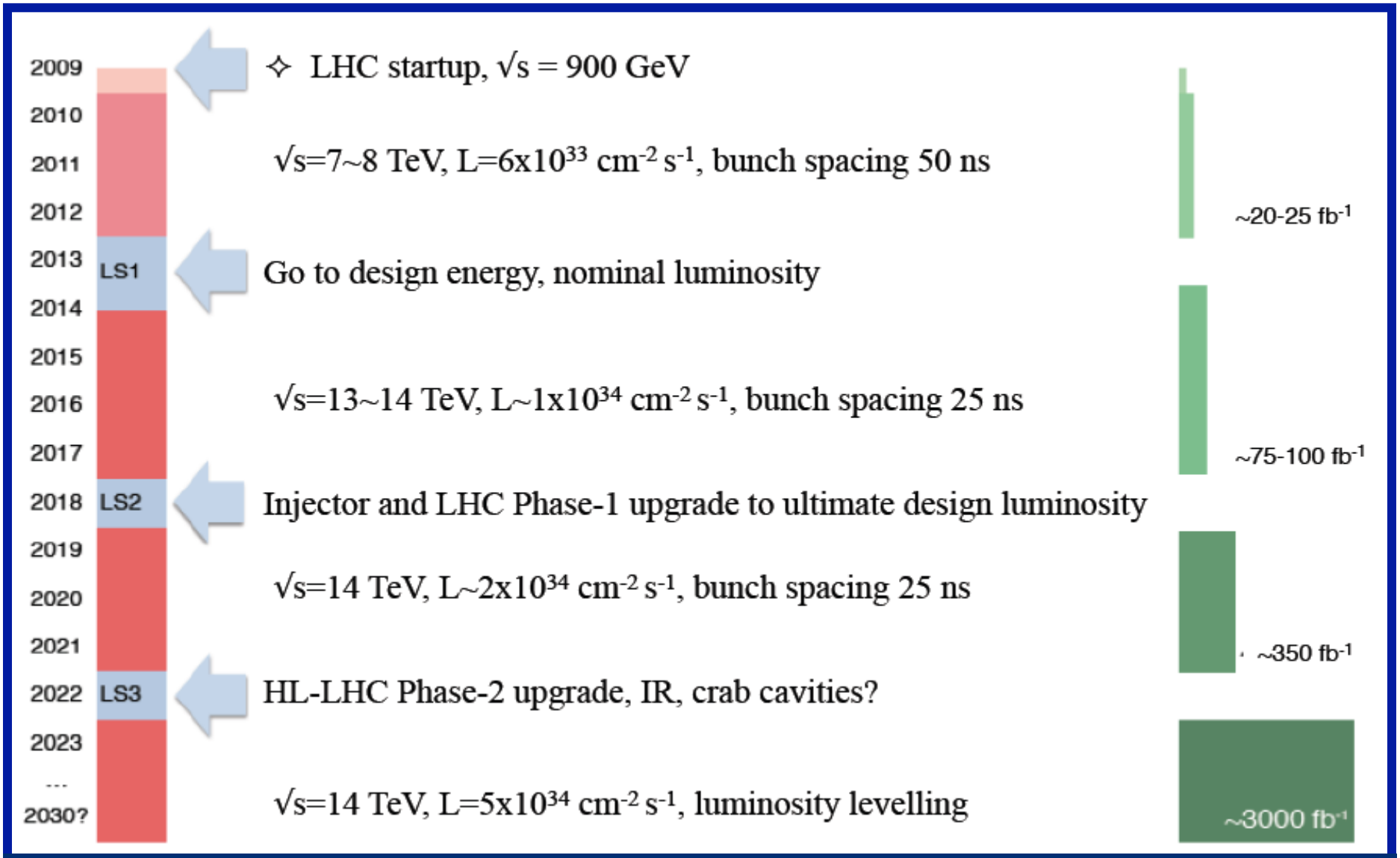
The ATLAS Detector



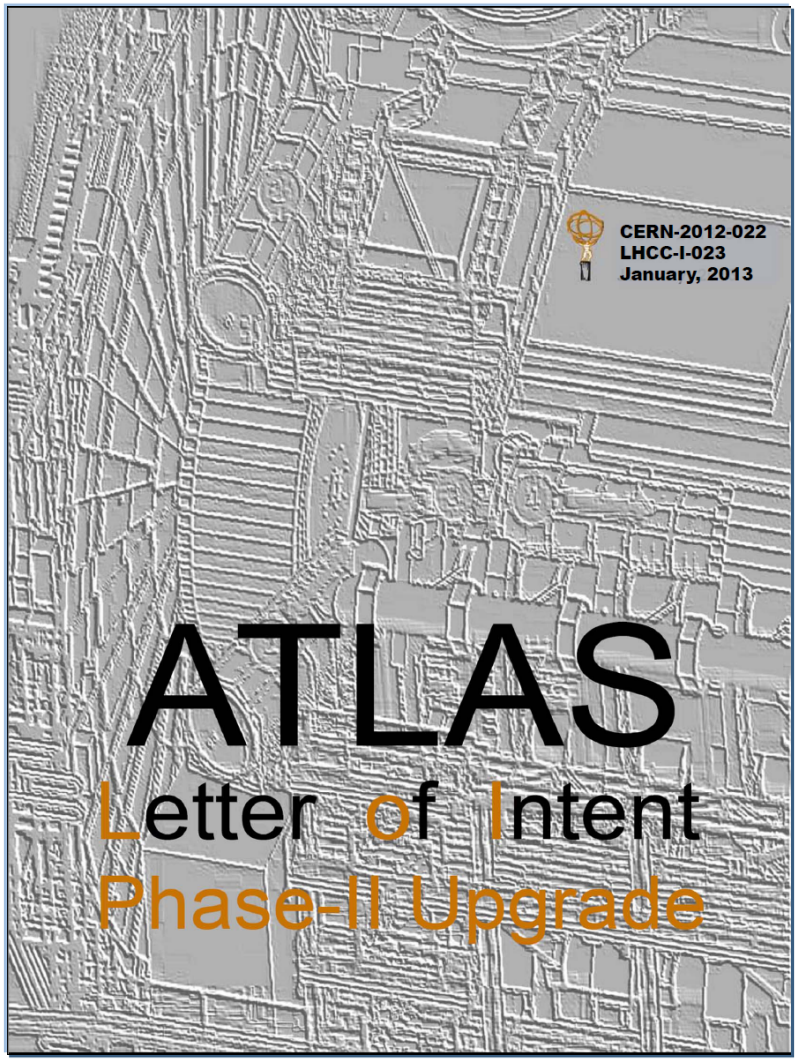
Trigger system (Run 2)

- L1 – hardware
  output rate: 100 kHz
  latency: < 2.5 μs
- HLT – software
  output rate: 1 kHz
  proc. time: ~ 550 ms

The LHC roadmap

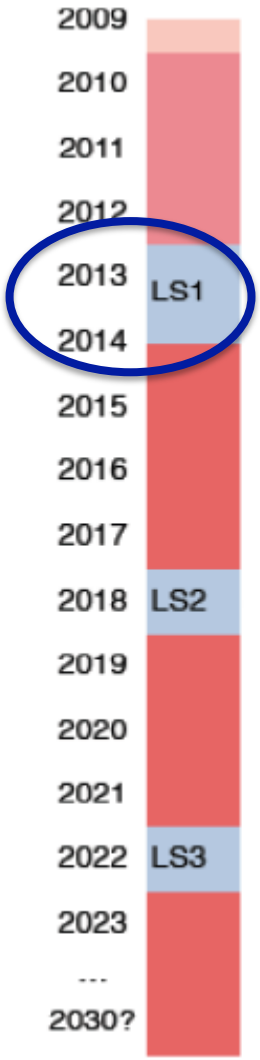


The ATLAS upgrade programme



+ TDR of Insertable B-Layer (Phase-0)

ATLAS Upgrade Plan



$\sqrt{s}$ = 13~14 TeV, 25ns bunch spacing
$L_{inst} \simeq 1 \times 10^{34}$ cm^{-2}s^{-1} ($\mu \simeq 27.5$)
$\int L_{inst} \simeq 50$ fb^{-1}

- New Insertable pixel b-layer (IBL) and pixel services
- New Al/Be beam pipe
- New ID cooling
- Upgrades to L1 Central Trigger
- Detector consolidation (e.g. calorimeter power supplies)
- Add specific neutron shielding
- Finish installation of EE muon chambers staged in 2003
- Upgrade magnet cryogenics

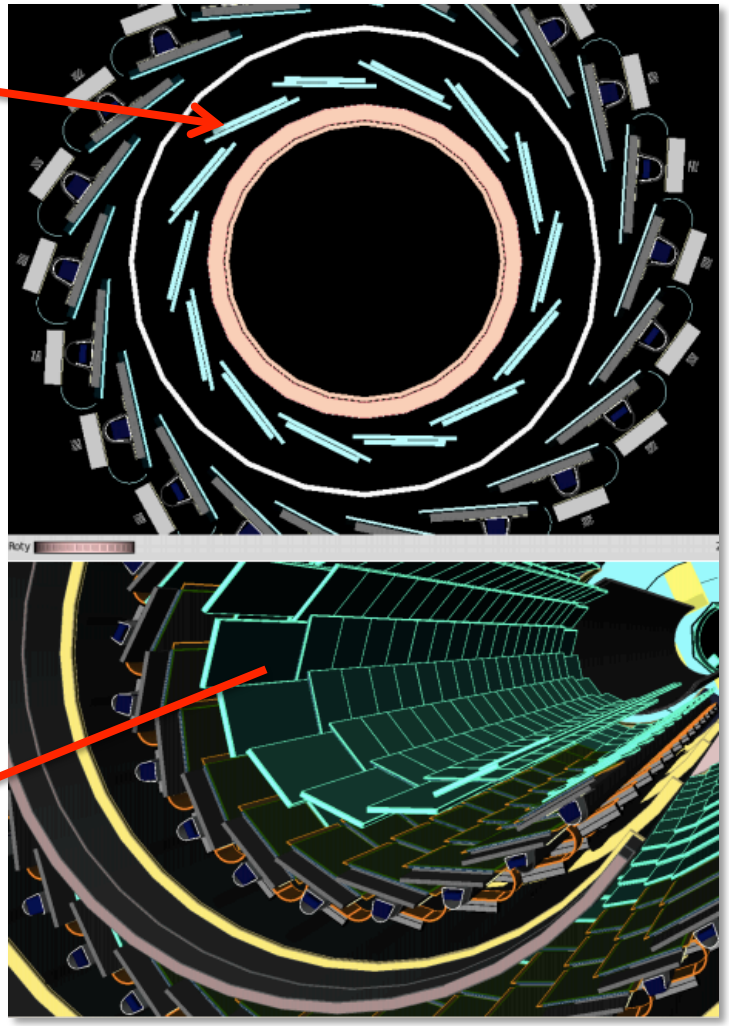
Phase-0

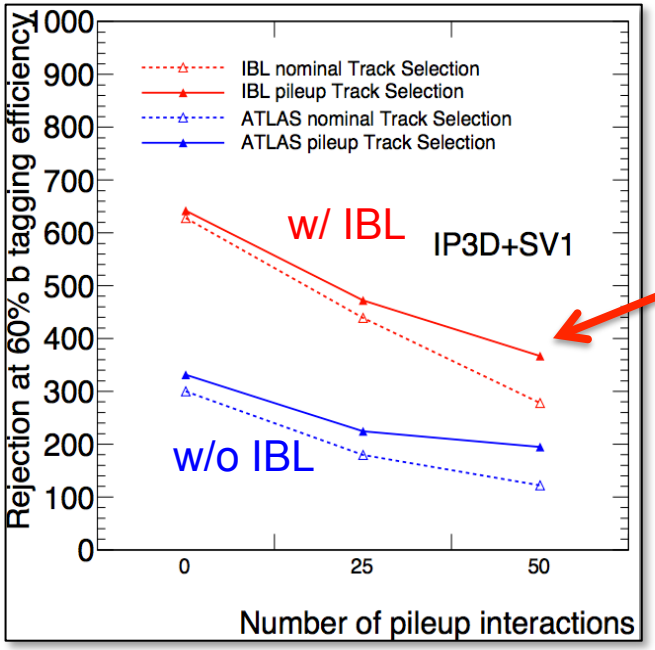
New inner pixel layer

Detector consolidation

Ongoing: Phase-0 upgrades (LS-1)

- Insertable B-Layer
  - Production/Integration on schedule
  - Installation of IBL in the pixel detector, in the pit: March 2014
  - Important ingrediant for low mass, rad-hard construction: 2 cm x 2 cm FE-I4 Pixel Chip, 130 nm CMOS process
  - Will stay until Phase-II

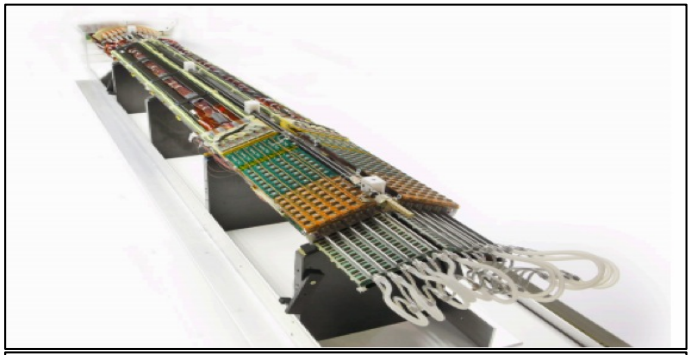


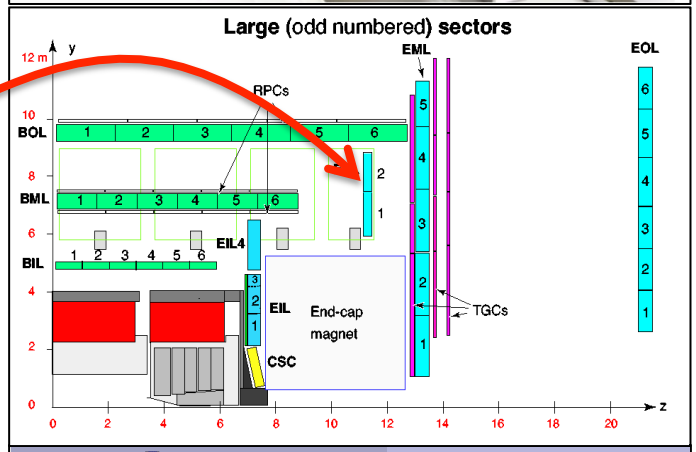


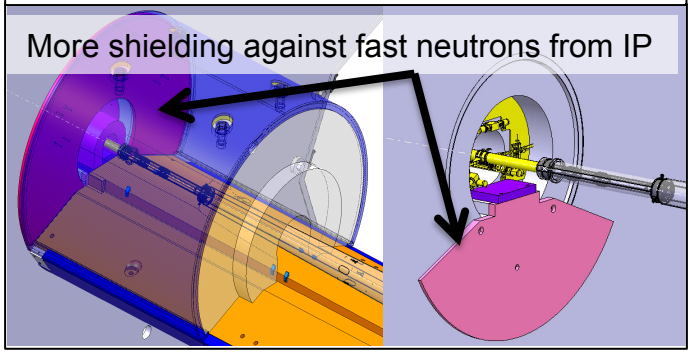
b-tagging rejection vs pile-up

Ongoing: Phase-0 upgrades (LS1)

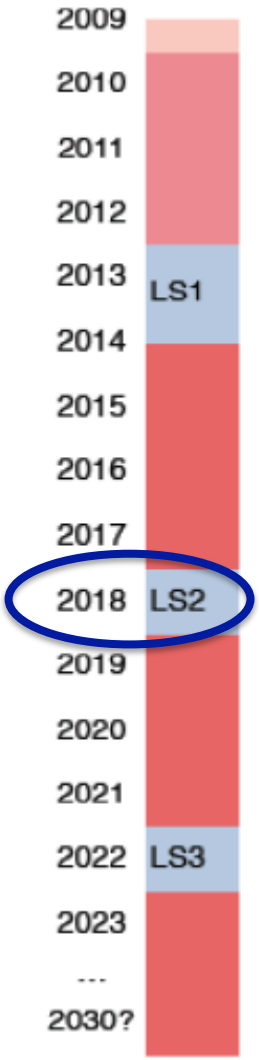
- Pixel Detector
  - new service panels – recover malfunctioning channels, better access, more bandwidth
- Pixel + SCT Detectors
  - New thermoshipon cooling system, keeping evaporative cooling system as backup
- Muon spectrometer
  - Install Muon End-cap Extension (EE) chambers to improve coverage at 1.0 < |n| < 1.3
- Add specific neutron shielding
- Detector consolidation
  - Calorimeter power supplies
  - Optical readout elements, …
  - Magnet cryogenics







ATLAS Upgrade Plan



ultimate luminosity
$L_{inst} \approx 2\text{-}3 \times 10^{34}\ cm^{-2}s^{-1}$ ($\mu \approx 55\text{-}81$)
$\int L_{inst} \gtrsim 350\ fb^{-1}$

- New Small Wheel (NSW) for the forward muon Spectrometer
- High Precision Calorimeter Trigger at Level-1
- Fast TracKing (FTK) for the Level-2 trigger
- Topological Level-1 trigger processors
- Other Trigger and DAQ upgrades, e.g. Muon Trigger interface (MuCTPI)
- ATLAS Forward Physics (AFP), proton det. at ±210 m

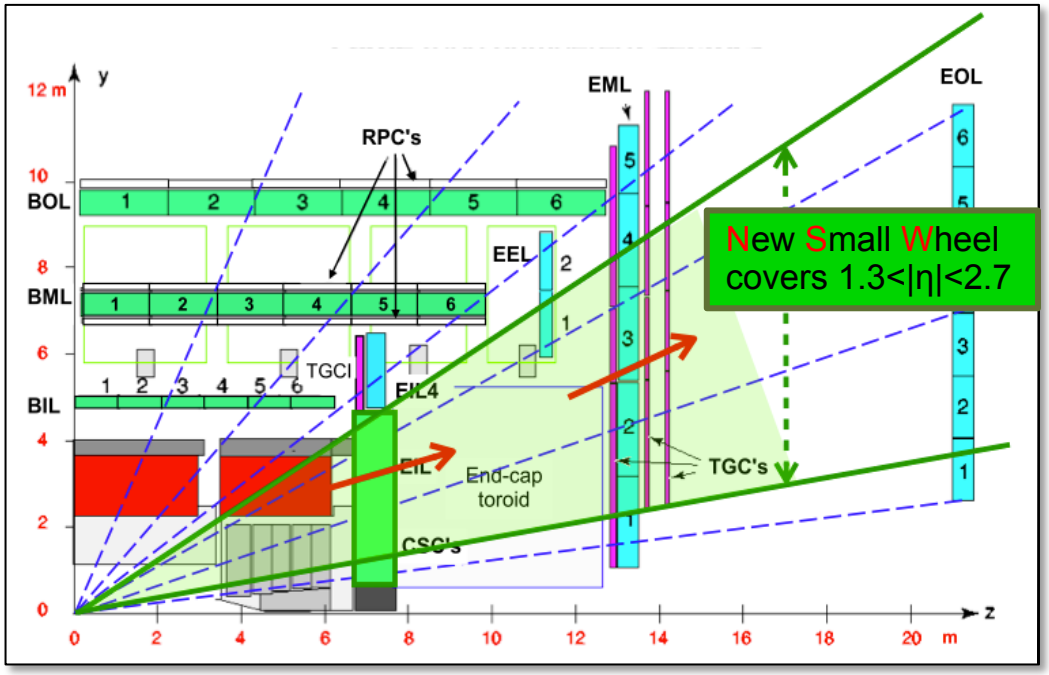
Phase-1

Improve L1 Trigger capabilities to cope with higher rates

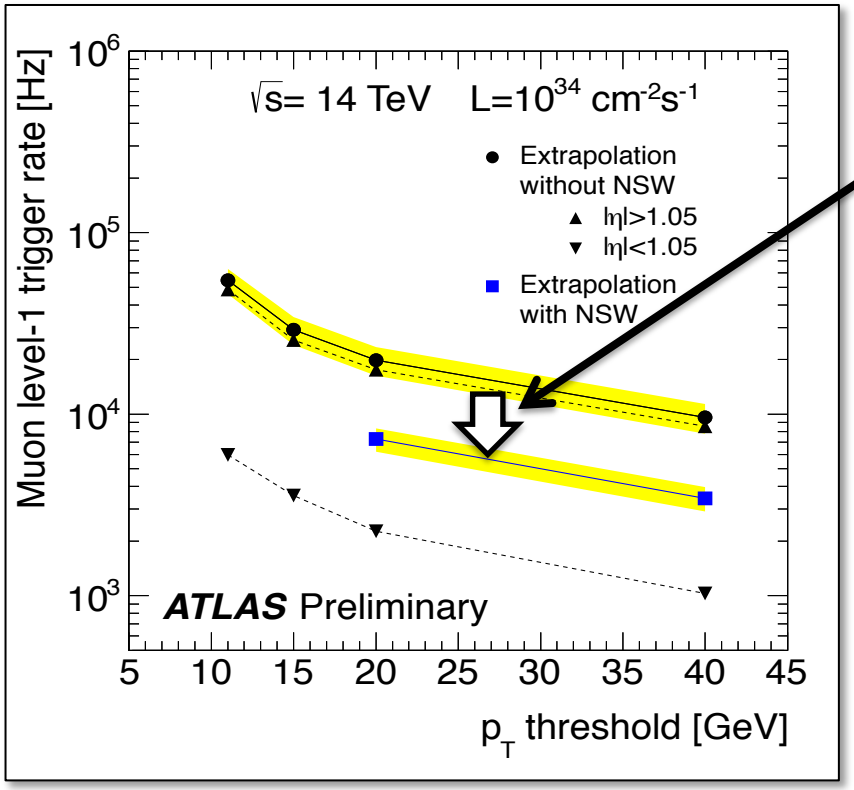
Muons: New Small Wheel

- Consequences of luminosity rising beyond design values for forward muon wheels
  - degradation of the tracking performance (efficiency / resolution)
  - L1 muon trigger bandwidth exceeded unless thresholds are raised

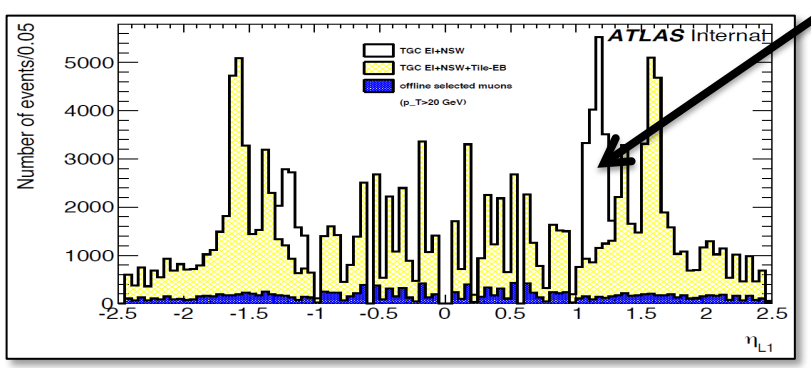
- Replace Muon Small Wheels with New Muon Small Wheels
  - improved tracking and trigger capabilities
  - position resolution < 100 μm
  - IP-pointing segment in NSW with σ_θ~ 1 mrad
  - Meets Phase-II requirements
    - compatible with <μ>=200, up to L~7x10^{34} cm^{-2}s^{-1}
  - Technology: MicroMegas and sTGCs



Muons: New Small Wheel cont.



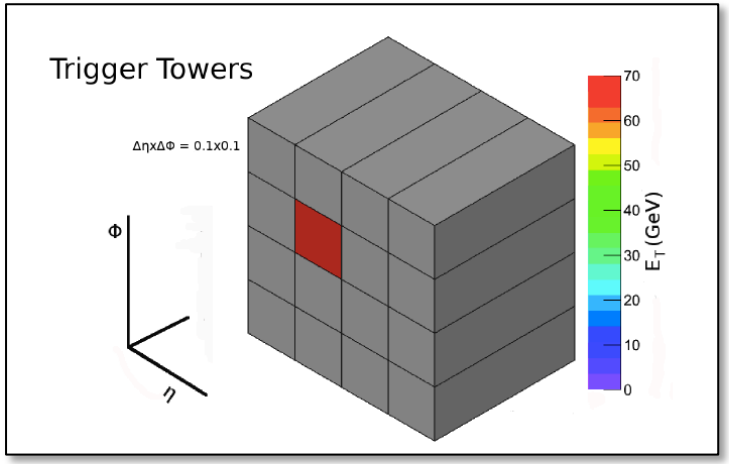
- Strong reduction of muon L1 trigger rate in forward direction
  - Dominated by fakes
- Vital for running at high luminostiy
- In addition smaller improvements during phase-0
  - Additional muon chambers in barrel/end-cap overlap region
  - Coincidences with outer layers of Tile Calorimeter removes peak of muon fakes



Level-1 calorimeter trigger

Run-1 calorimeter trigger input:
Trigger Towers $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$

- Used to calculate core energy, isolation



Run-1 trigger menu
at L_{inst}=3 x 10^{34} $cm^{-2}s^{-1}$

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Total rate for EM triggers would be 270 kHz!
(Total L1 bandwidth is 100kHz)

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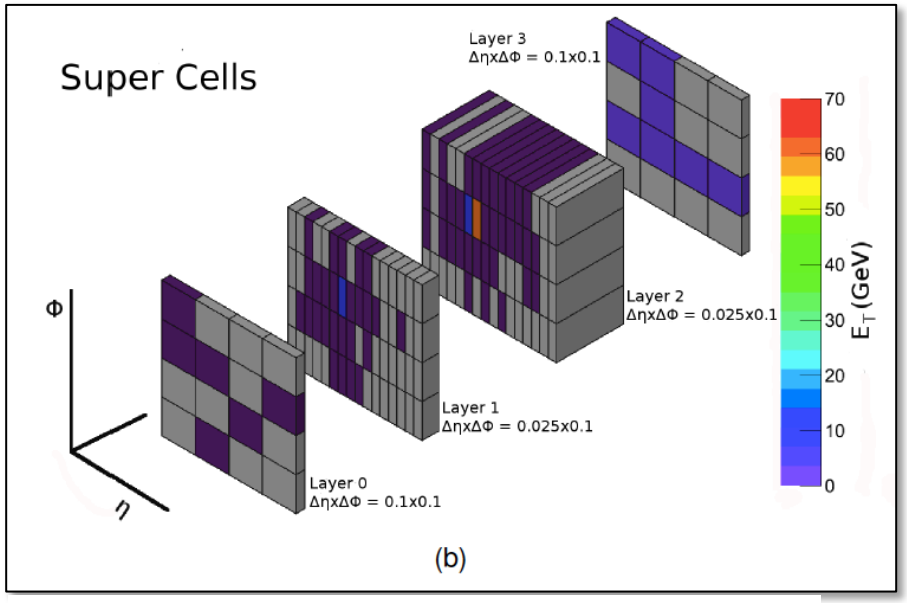
maintain lower thresholds at an acceptable rate

↑

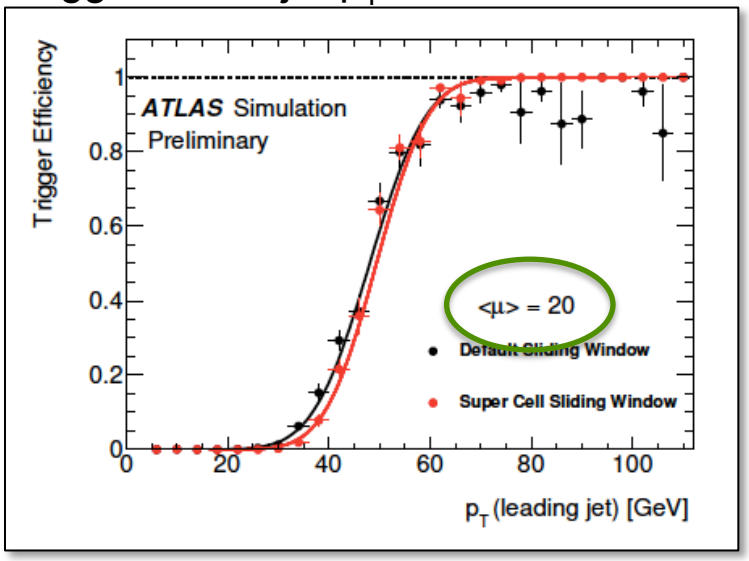
Provide better granularity and better energy resolution



Complemented by new L1Calo trigger processors eFEX and jFEX

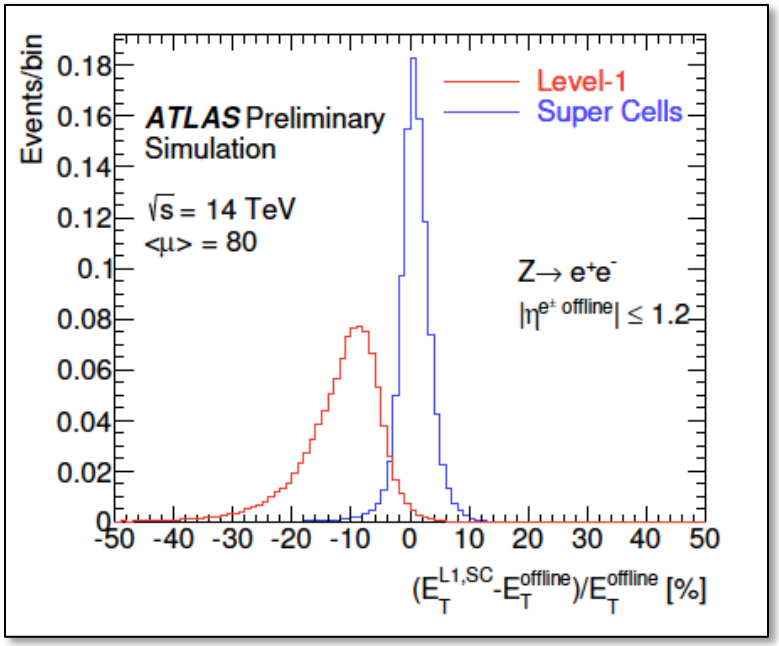
Level-1 calorimeter trigger cont.

Trigger eff. vs jet p_T



Significant degradation of the turn-on curve with pile up (<μ>=80)

- requiring much higher offline threshold (black curve)
- recovered through introduction of super-cells (red curve)



EM Triggers

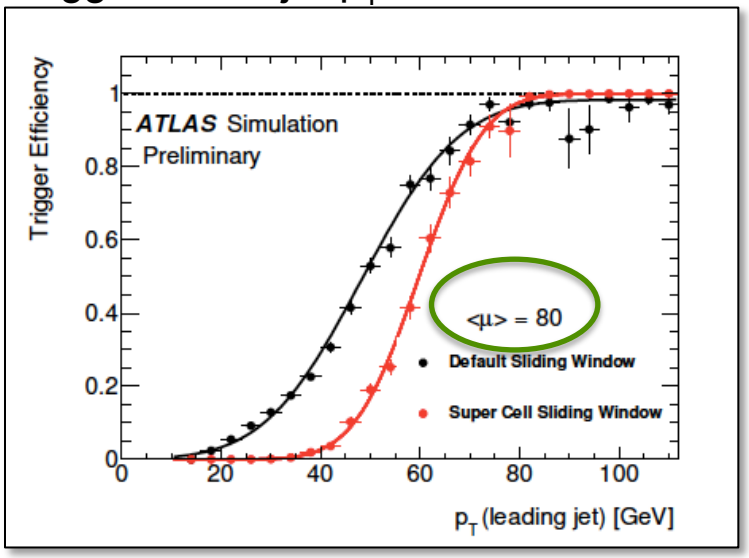
- Better shower shape discrimination
  → lower EM threshold by ~ 7 GeV at same rate
- In addition significantly improved resolution
  → lower EM threshold by another few GeV at same rate

Topological triggering

- Will feed calorimeter trigger input to L1 topological processor (already in Phase-0)

Level-1 calorimeter trigger cont.

Trigger eff. vs jet p_T



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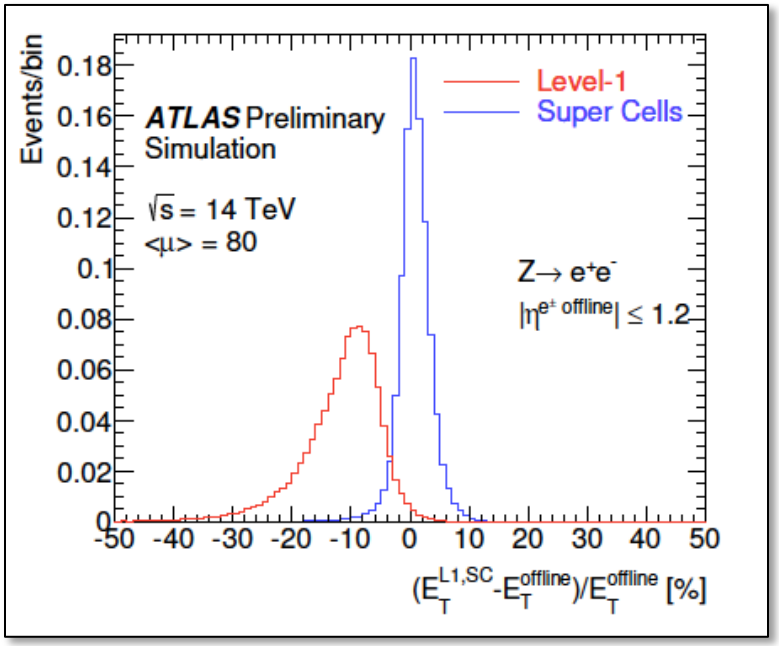


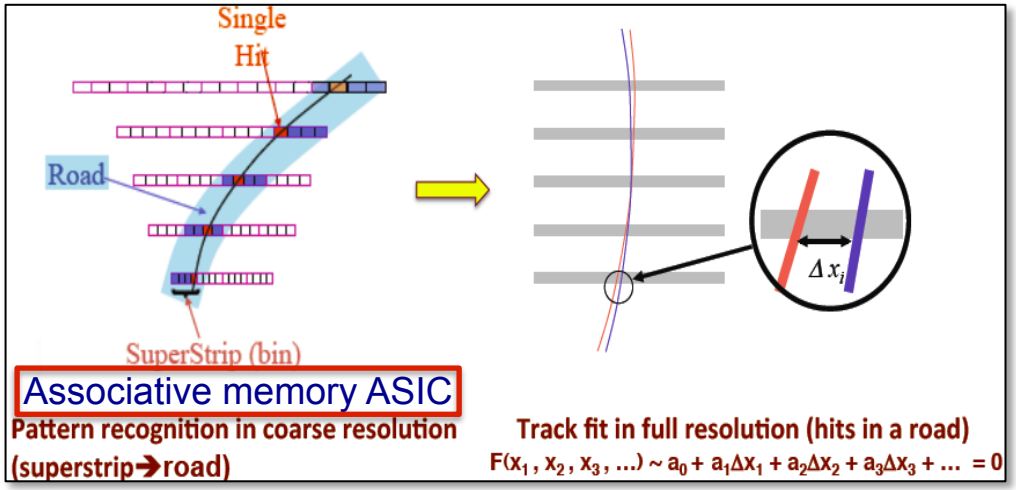
Fast TracK Trigger (FTK)

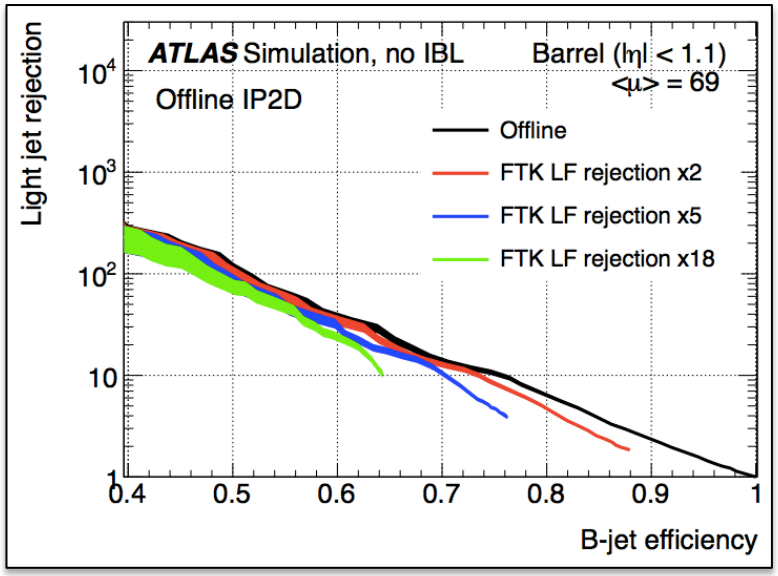
- Dedicated, hardware-based track finder
  - Runs after L1, on duplicated Si-detector read-out links
  - Provides tracking input for L2 for the full event
    - not feasible with software tracking at L2
  - Finds and fits tracks (~ 25 μs) in the ID silicon layers at an "offline precision"

- Processing performed in two steps

hit pattern matching to pre-stored patterns (coarse)

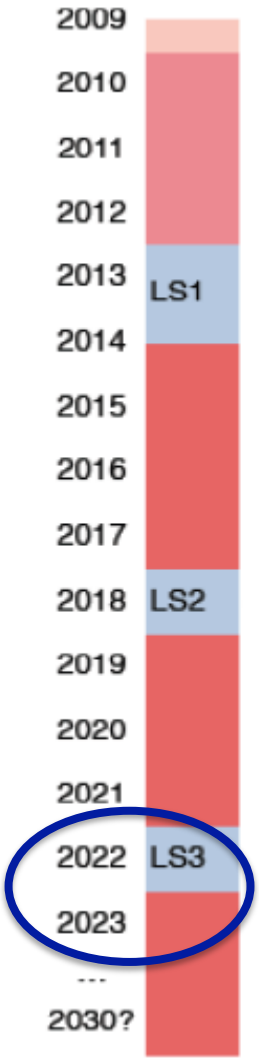
subsequent linear fitting in FPGAs (precise)





Light jet rejection using FTK compared to offline reconstruction
(further improved by addition of IBL)

ATLAS Upgrade Plan



$L_{inst} \simeq 5 \times 10^{34}$ cm^{-2}s^{-1} ($\mu \simeq 140$) w. level.
$\simeq 6\text{-}7 \times 10^{34}$ cm^{-2}s^{-1} ($\mu \simeq 192$) no level.
$\int L_{inst} \simeq 3000$ fb^{-1}

- All new Tracking Detector
- Calorimeter electronics upgrades
- Upgrade muon trigger system
- Possible Level-1 track trigger
- Possible changes to the forward calorimeters

Phase-2

Prepare for $\langle\mu\rangle=200$

Replace Inner Tracker

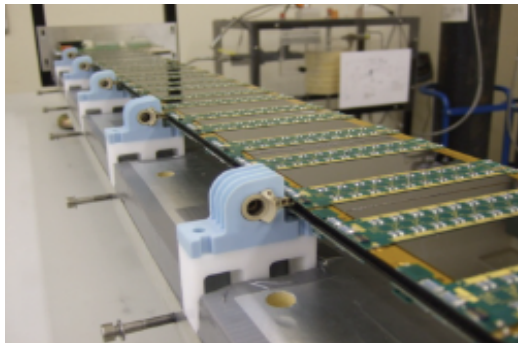
New L0/L1 trigger scheme

Upgrade muon/calorimeter electronics

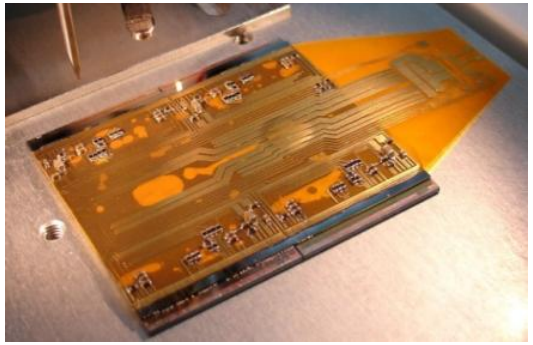
New Tracking detector

- Current Inner Detector (ID)
  - Designed to operate for 10 years at $L=1x10^{34}$ $cm^{-2}s^{-1}$ with <μ>=23, @25ns, L1=100kHz
- Limiting factors at HL-LHC
  - Bandwidth saturation (Pixels, SCT)
  - Too high occupancies (TRT, SCT)
  - Radiation damage (Pixels (SCT) designed for 400 (700) fb^{-1})

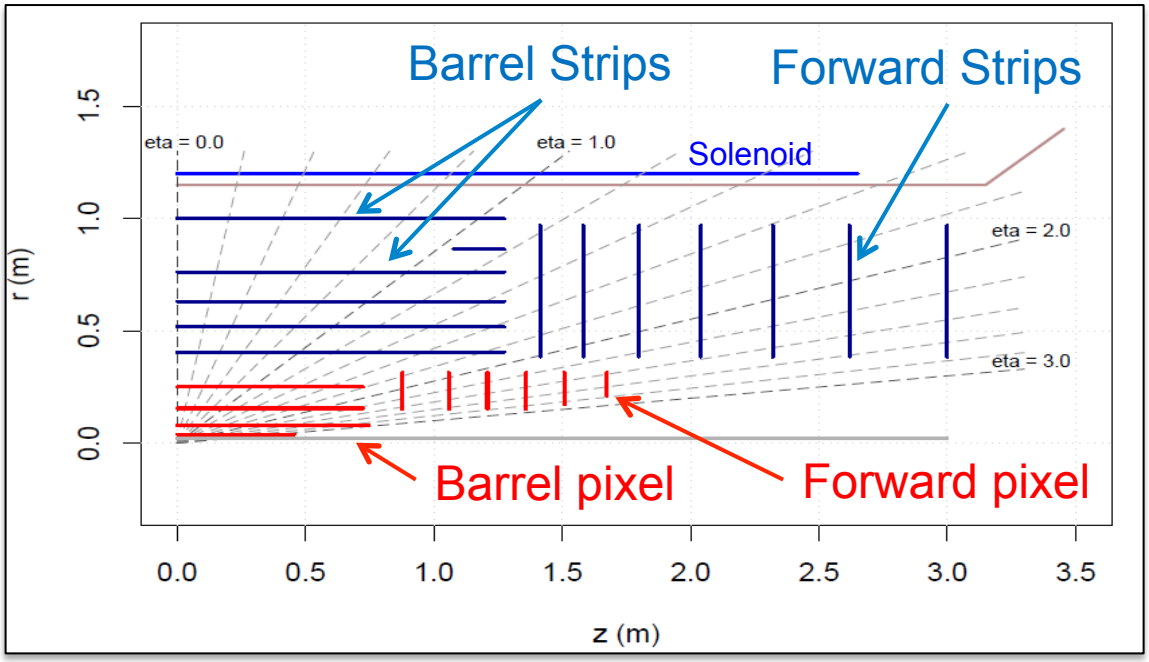
Microstrip Stave Prototype



Quad Pixel Module Prototype



LoI layout new (all Si) ATLAS Inner Tracker for HL-LHC



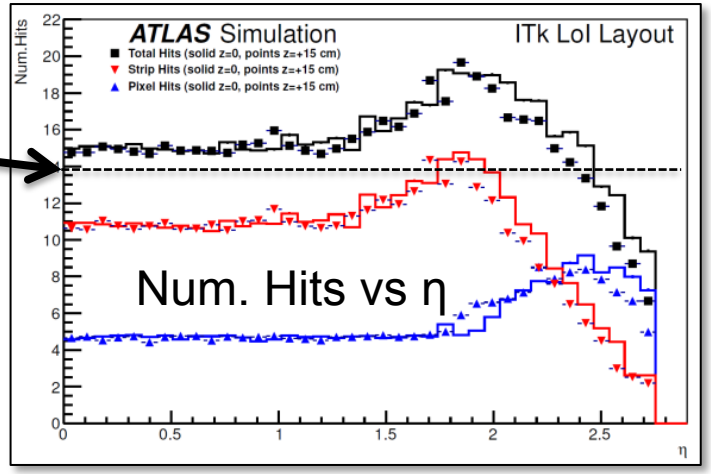
New 130nm prototype strip ASICs in production

- incorporates L0/L1 logic

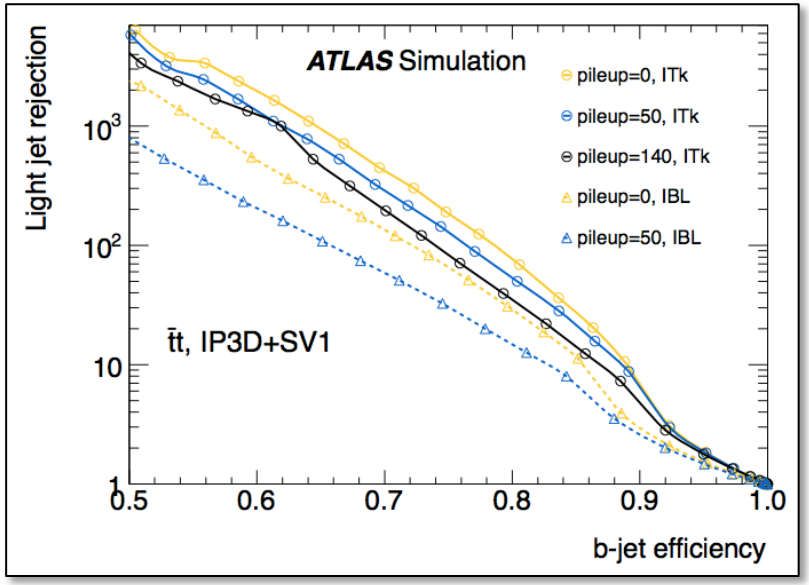
Sensors compatible with 256 channel ASIC being delivered

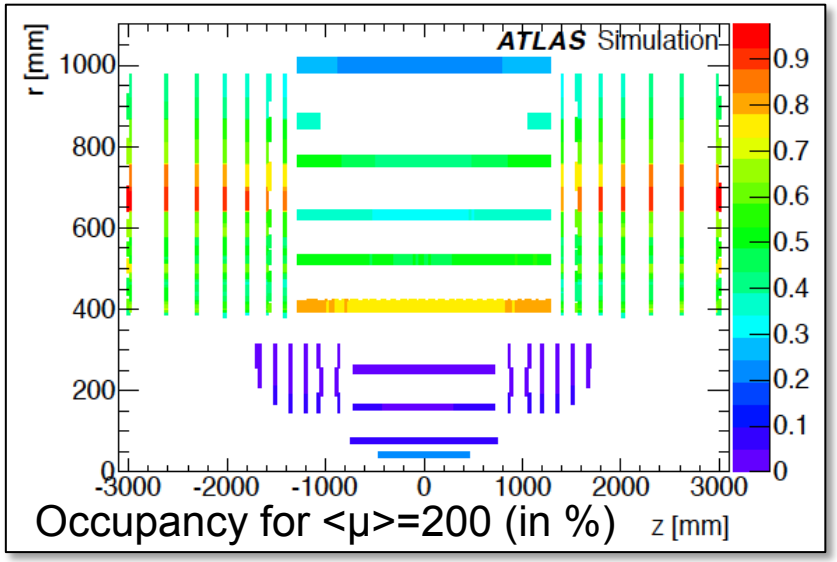
New Tracking detector cont.

- Studies with LOI layout
  - Robust tracking (14 layers)
  - Occupancy <1% for <μ>=200
  - Reduced material wrt current ID
  - Comparable / better tracking performance at <μ>=200 as current ID at <μ>=0
- Prototypes tested to 2x HL-LHC flux
- Solid baseline design
  - working on optimisation



Light jet rejection, ID (w/IBL) and ITk



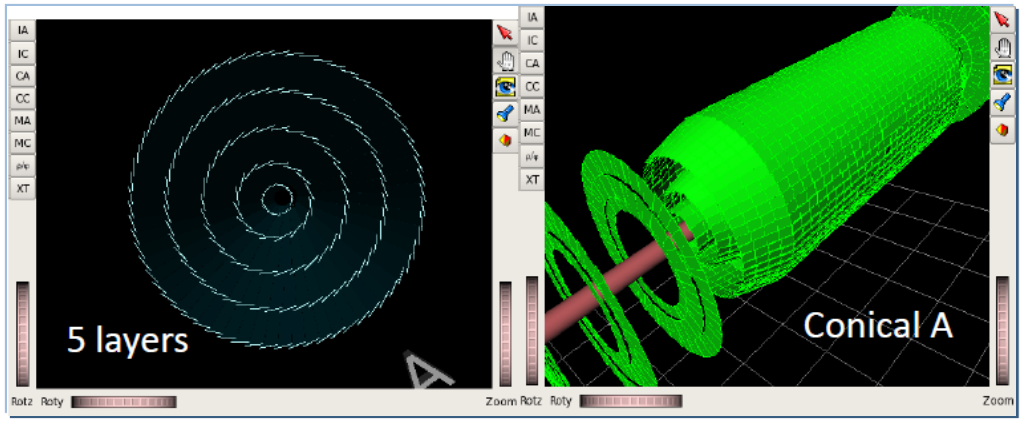


Occupancy for <μ>=200 (in %)

New Tracking detector cont.

- Many topics still to be addressed
  - How can the layout still be optimised?
  - Can all assemblies/components be qualified to the required radiation hardness?
  - How critical is the luminous beam-spot extent in z?
  - Are there physics reasons to significantly extent the coverage in η?
  - Cost / material optimisations with current technologies?
  - Alternative technologies?

- Addressing these questions now is very timely
  - note TDR of current ID was written in 1997 …

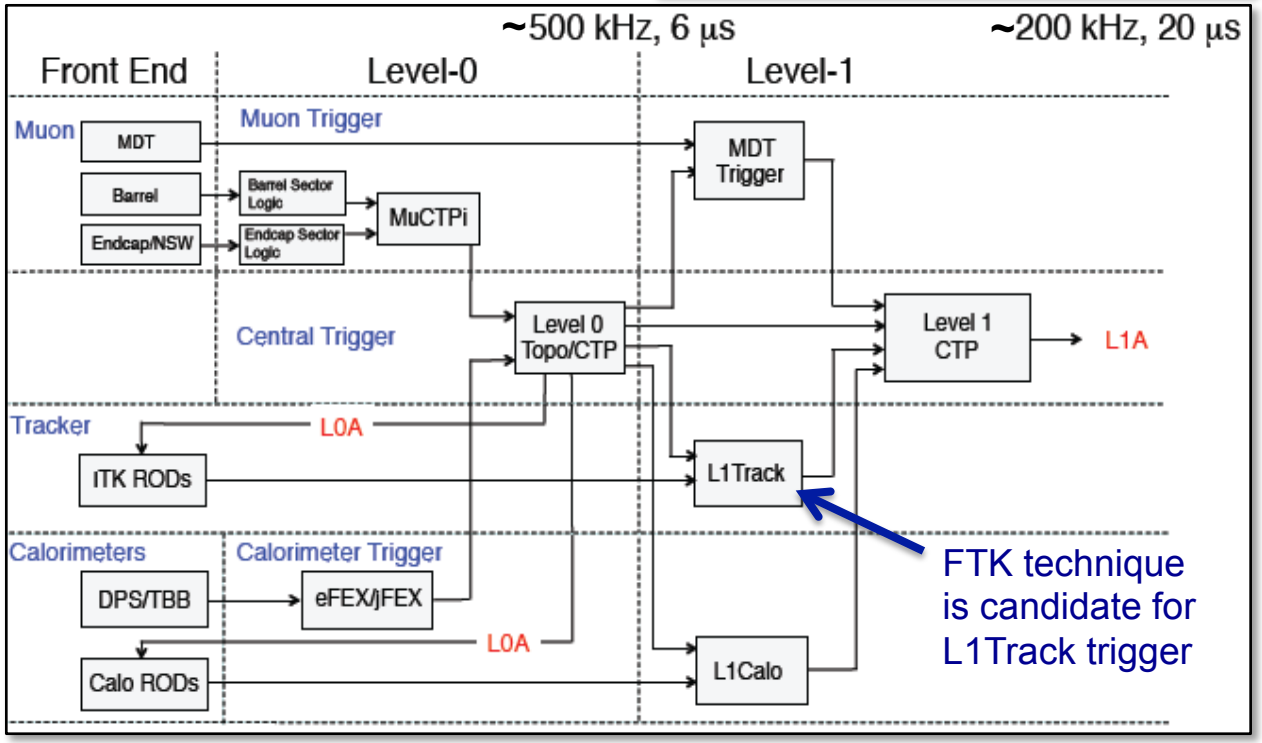


Alternative layouts being considered which include either a further pixel layer or inclined pixel

Trigger system architecture

- New design for Phase II
  - 2-level system, Phase-I L1 becomes Phase-II L0, new L1 includes tracking
  - Make use of improvements made in Phase 1 (NSW, L1Calo) in L0
  - Introduce precision muon and inner tracking information in L1
    - Better muon pT resolution
    - Track matching for electrons,…
  - Requires changes to detector FE electronics feeding trigger system

Will also have new timing/control links and LHC interface system



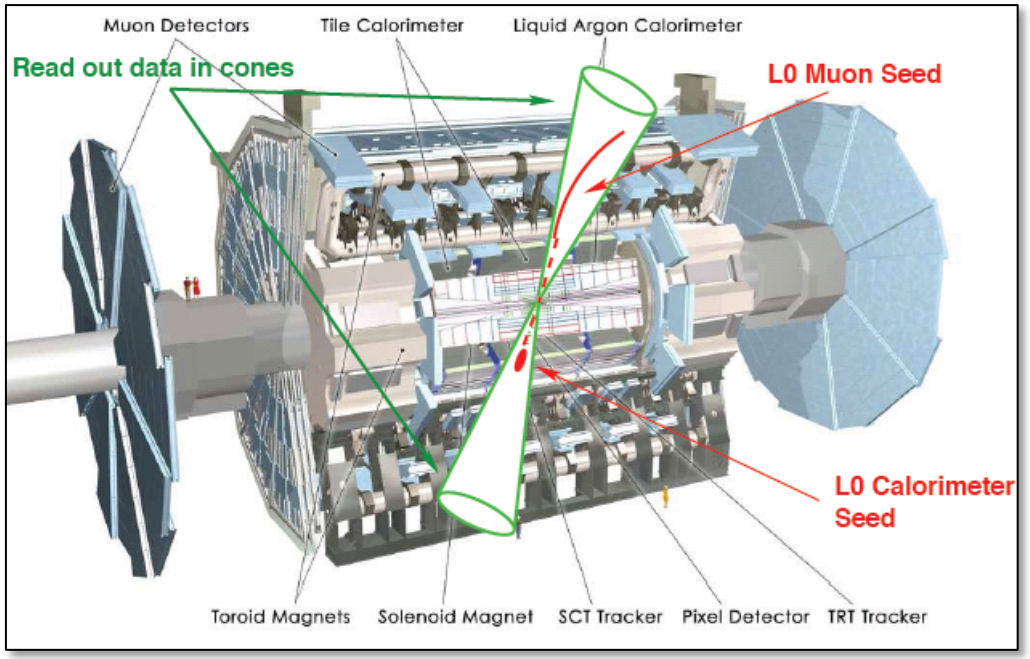
Level-0
Rate ~ 500 kHz, Lat. ~6 μs
Muon + Calo
Level-1
Rate ~200 kHz, Lat. ~20 μs
Muon + Calo + Tracks

L1Track Trigger

- Adding tracking information at Level-1 (L1)
  - Move part of High Level Trigger (HLT) reconstruction into L1
  - Goal: keep thresholds on p_T of triggering leptons and L1 trigger rates low

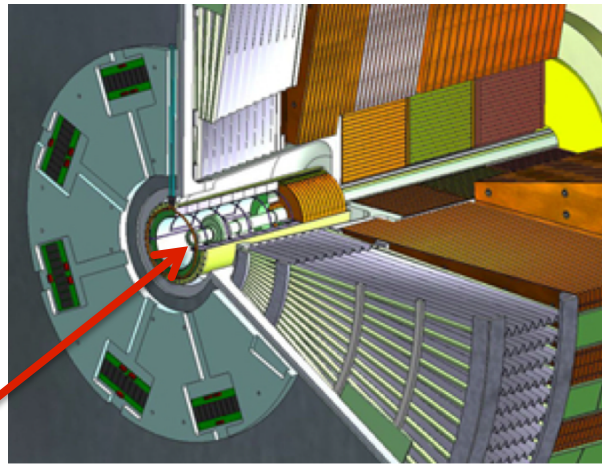
- Triggering sequence
  - L0 trigger (Calo/Muon) reduces rate within ~6 μs to $\gtrsim$ 500 kHz and defines RoIs
  - L1 track trigger extracts tracking info inside RoIs from detector FEs

- Challenge
  - Finish processing within the latency constraints



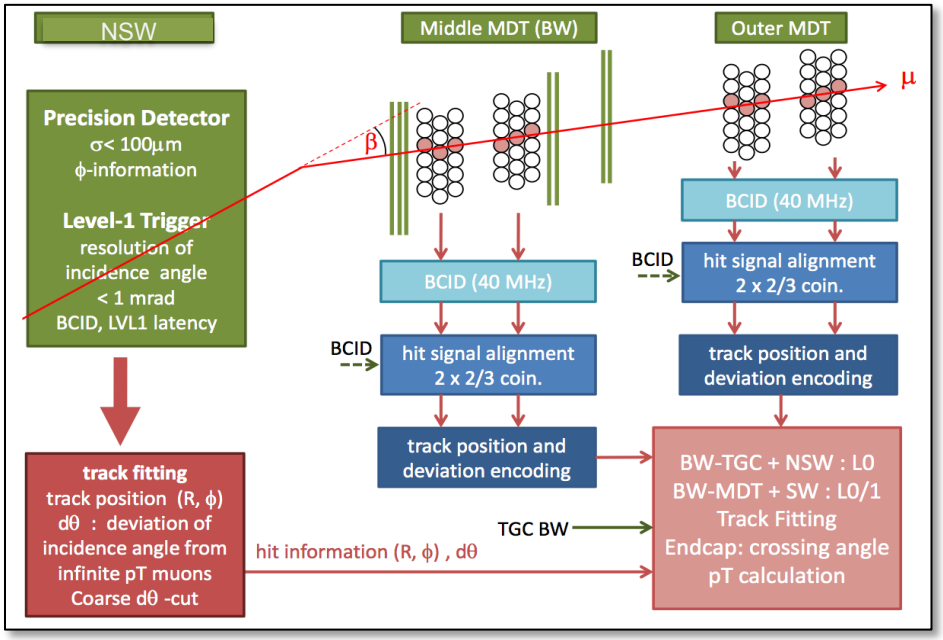
Calorimeter electronics

- Tile Calorimeters
  - No change to detector needed
  - Full replacement of FE and BE electronics
    - New read-out architecture: Full digitisation of data at 40MHz and transmission to off-detector system, digital information to L1/L0 trigger
- LAr Calorimeter
  - Replace FE and BE electronics
    - Aging, radiation limits
    - 40 MHz digitisation, inputs to L0/L1
    - Natural evolution of Phase-I trigger boards
  - Replace HEC cold preamps if required
    - i.e. if significant degradation in performance
  - Replace Forward calorimeter (FCal) if required
    - Install new sFCAL in cryostat or miniFCAL in front of cryostat if significant degradation in current FCAL

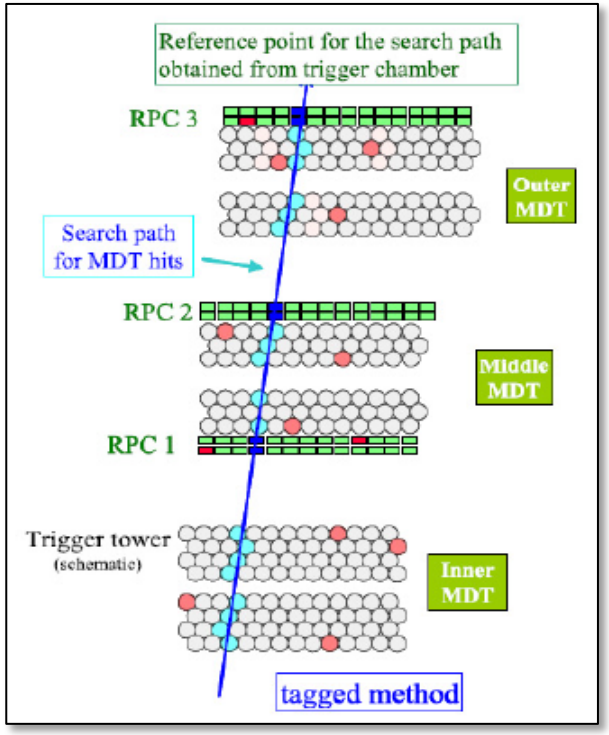


Muon system upgrade

- Upgrade FE electronics
  - accommodate L0/L1 scheme parameters
- Improve L1 p_T resolution
  - Use MDT information possibly seeded by trigger chambers ROIs (RPC/TGC)
  - Another option: add higher precision RPC layer at inner MDT station



Match angle measurement in end-cap MDTs to precision measurement in NSW



RoI of high-p_T track used as a search road for MDT hits of the candidate track

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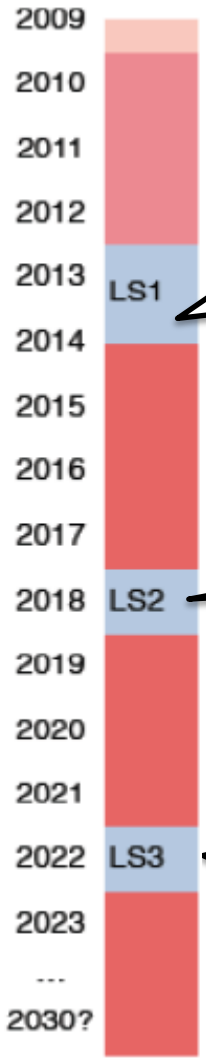
Combine track segments of several MDTs to give precise p_T estimate

Summary



Phase-0

New inner pixel layer

Detector consolidation

Phase-1

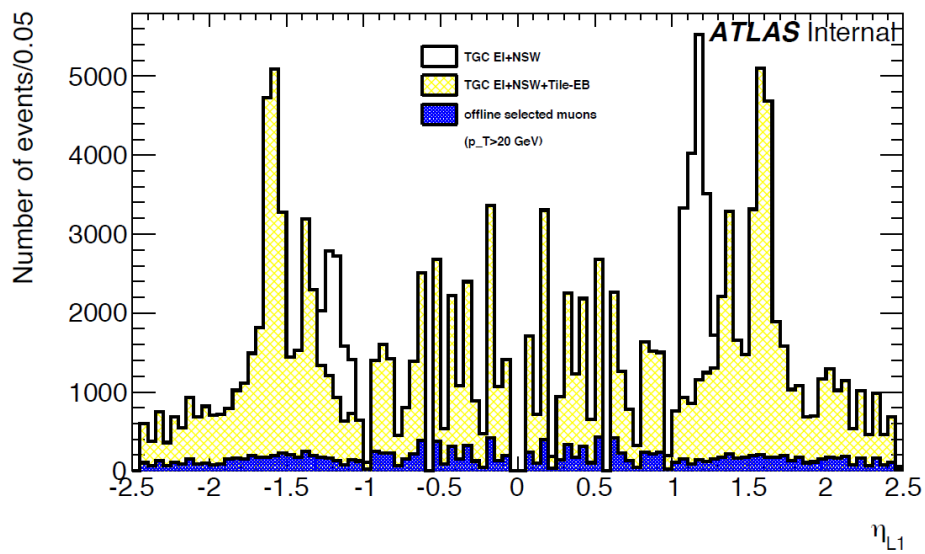
Improve L1 Trigger capabilities to cope with higher rates

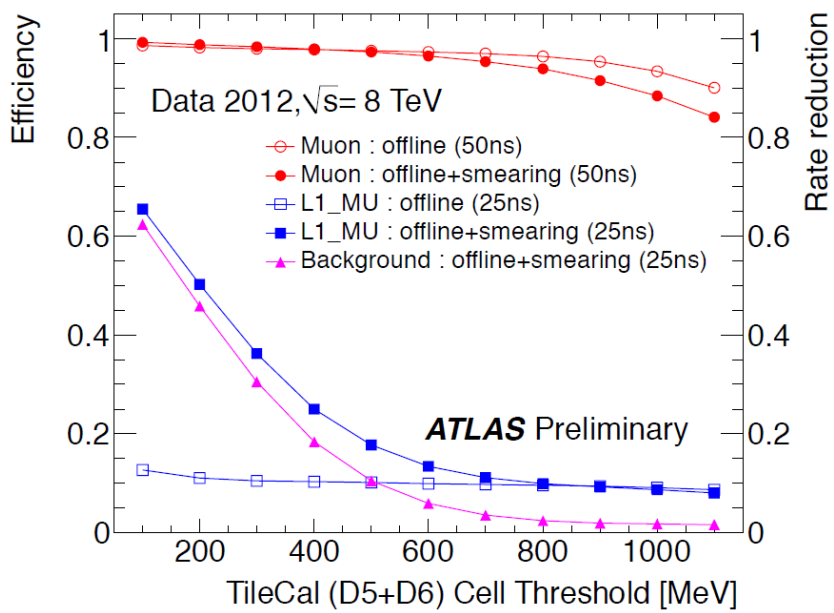
Phase-2

Prepare for <μ>=200
Replace Inner Tracker
New L0/L1 trigger scheme
Upgrade muon/calorimeter electronics

Backup slides

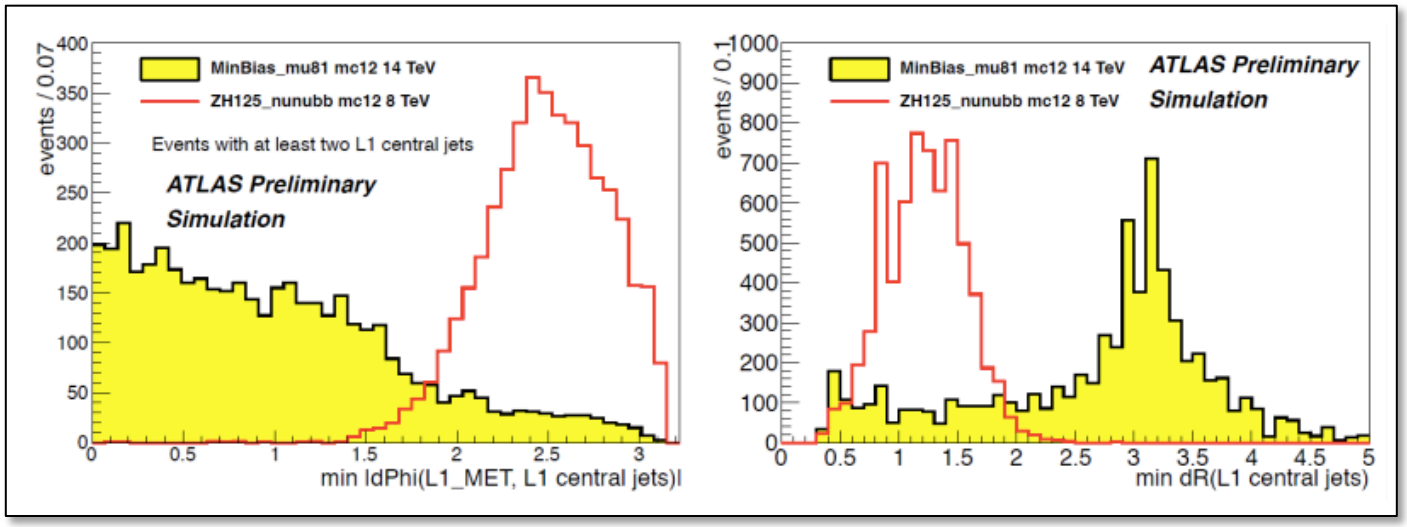
Muon Trigger: Tile coincidence





- Main source of fake triggers are low-momentum protons emanating from endcap toroid and shielding
  - 1.0 < |η| < 1.3 region of Big Wheel TGC not covered by the NSW
- Use hadronic TileCal extended barrel (D-layer) for trigger coincidence
  - Energy resolution smeared by electronics noise in Level-1 read-out path lowers efficiency above 500 MeV
- Tile Muon coincidence reduces rate by 82% at that threshold

Level-1 Topological Trigger

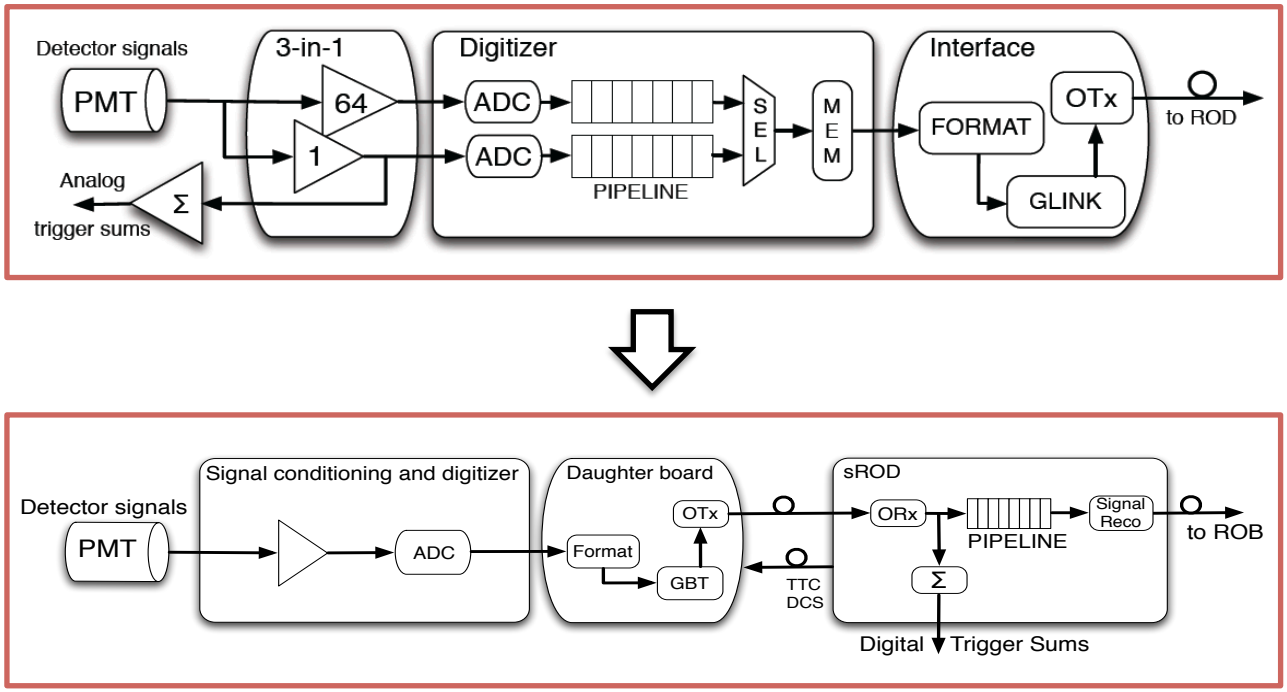


Example: exploit characteristic location of pile-up jets wrt E_T^{miss} vector

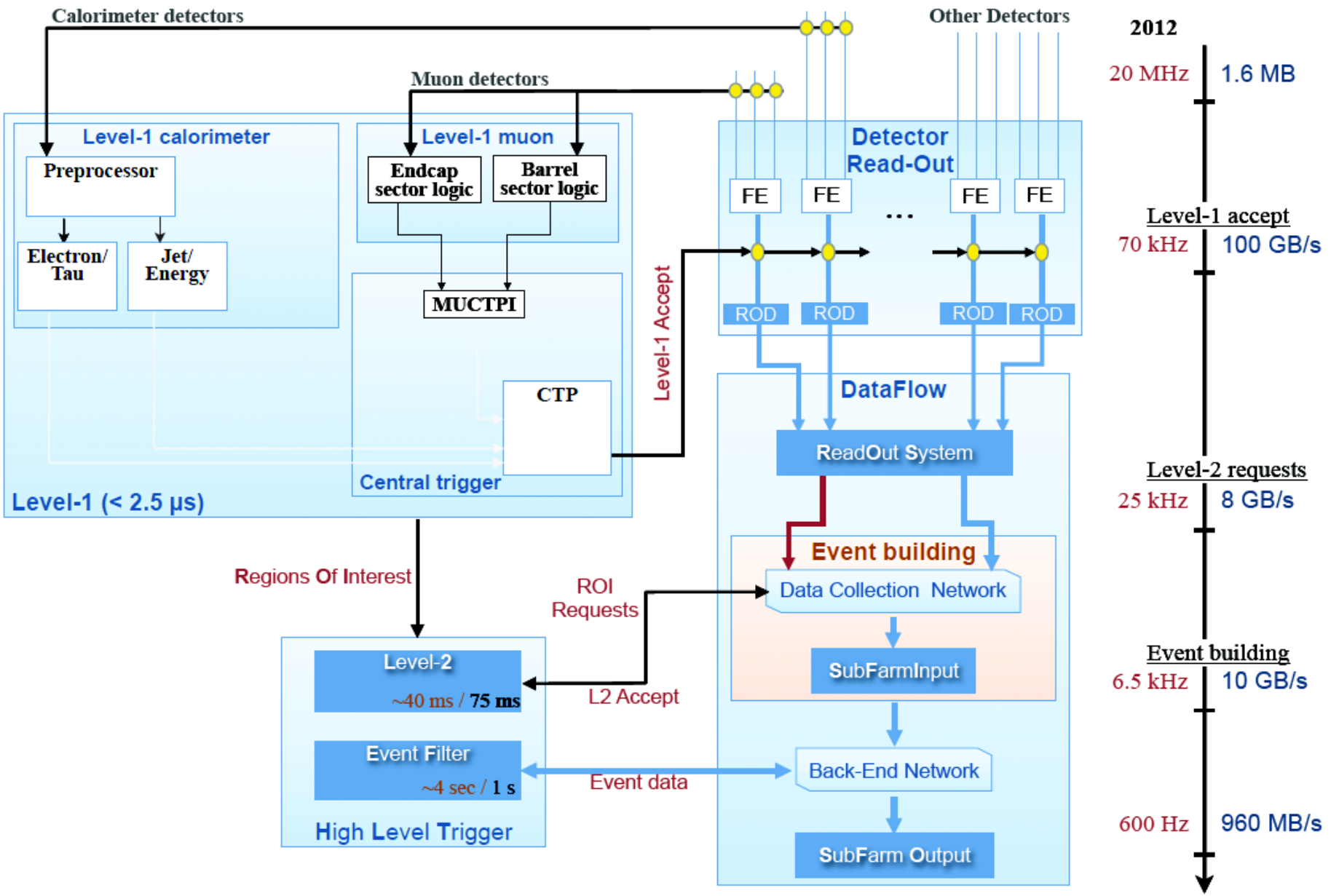
- In Phase-I, ***ZH*** → ***vvbb*** with 160 GeV E_T^{miss} trigger (XE40) would exceed total L1 rate due to pile-up jets faking missing energy
  - Increasing threshold rapidly costs signal efficiency
- Combination with inclusive jet trigger brings rate down to ~10 kHz (still too high)
- L1Topo: cut on azimuthal distance between jet and *E*Tmiss ($\Delta\varphi > 1$) reduces rate by ~45% with negligible loss in signal efficiency
  - radial distance (ΔR) cut could be used to further reduce rate

Tile Calorimeter electronics

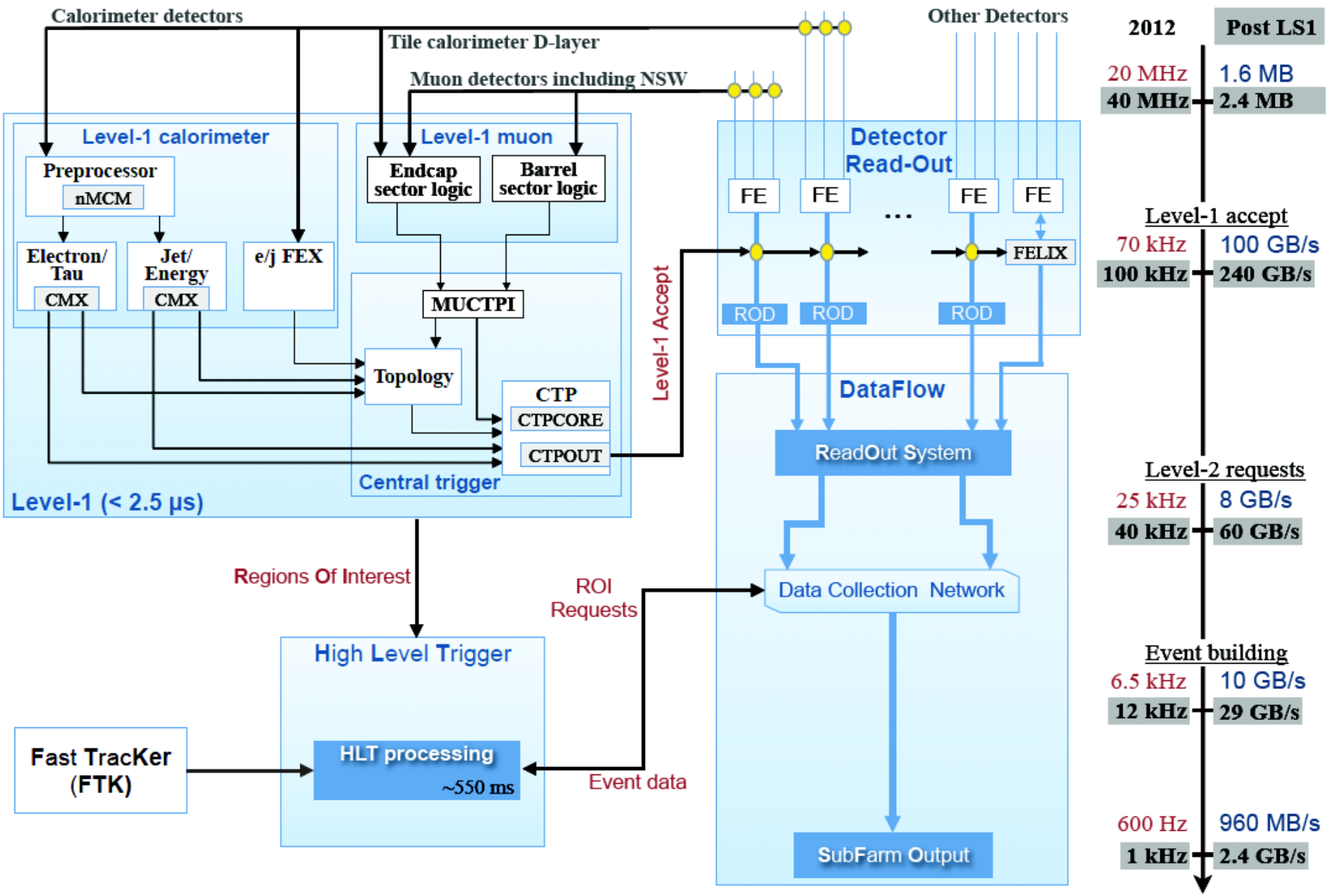
- Change of readout architecture in Phase II



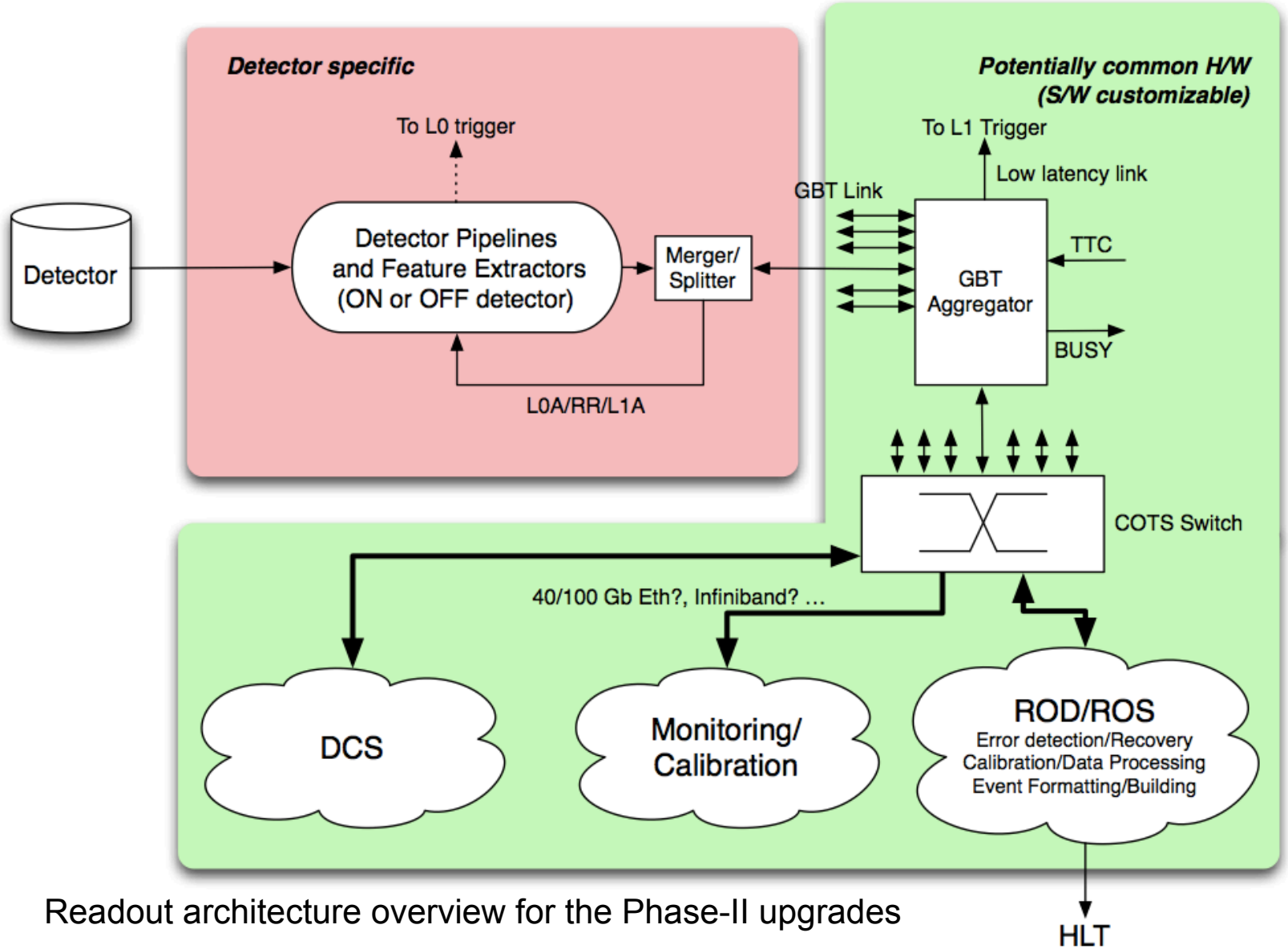
TDAQ system: Run-1



TDAQ system: Run-3



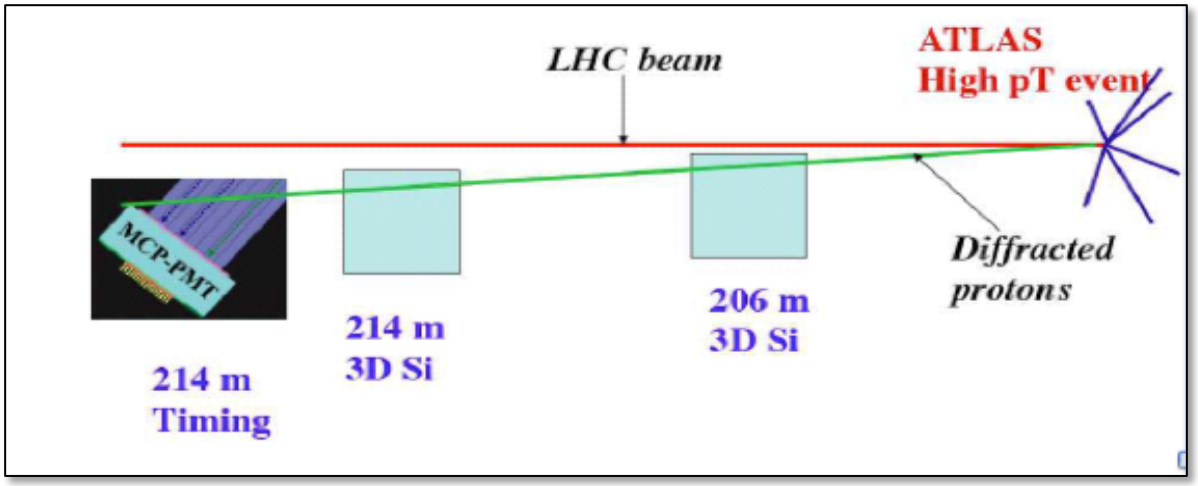
Phase-II Readout architecture

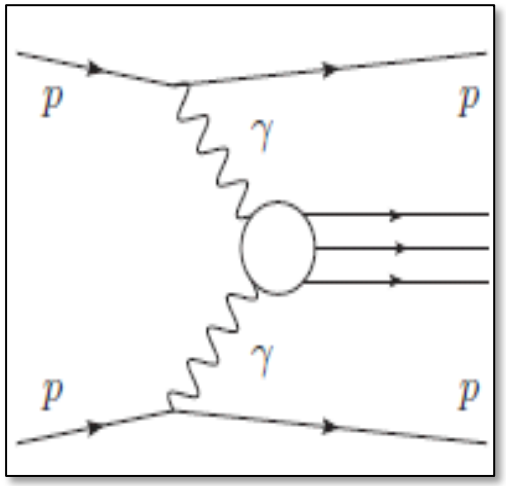


Readout architecture overview for the Phase-II upgrades

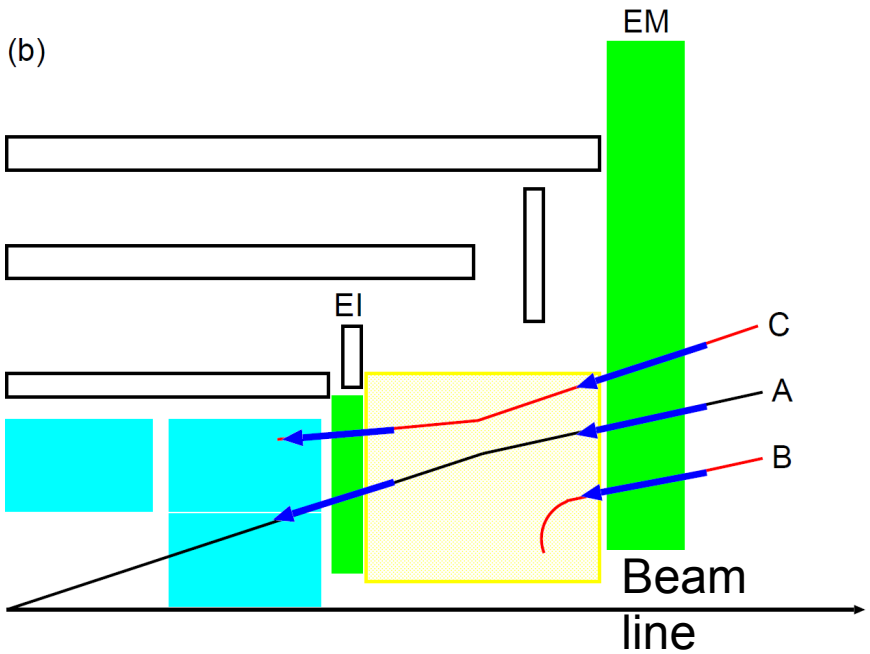
ATLAS Forward Physics (AFP)

- Tag and measure scattered protons at ± 210m
  - Link to system triggered in central ATLAS
  - **Radiation-hard edgeless 3D silicon** developed in IBL context
  - 10ps timing detector for association with high p_T primary vertex
  - Probe hard diffractive physics and central exclusive production of heavy systems/particles
  - Targeted at Phase-I, physics case under evaluation





Background muon forward direction



End-cap muon trigger based on information in the EM layer:

- Correlated background from interactions with the beam pipe can produce fake high p_T triggers.