Calorimetry Electronics

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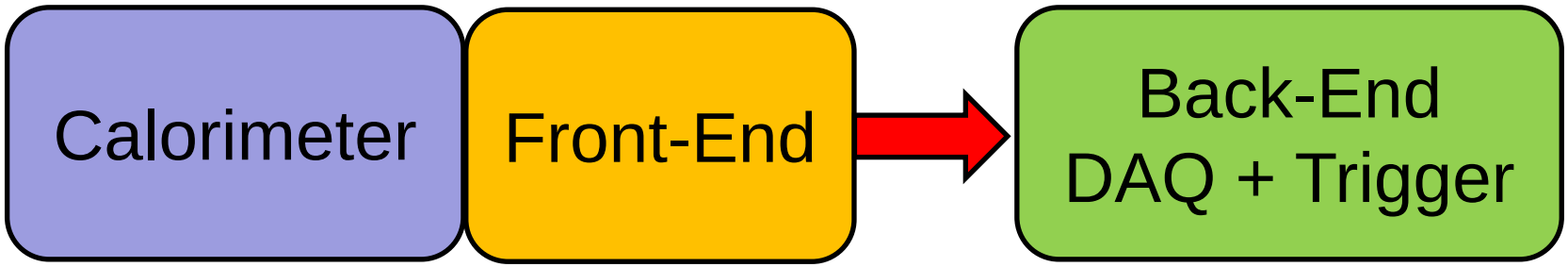
Introduction

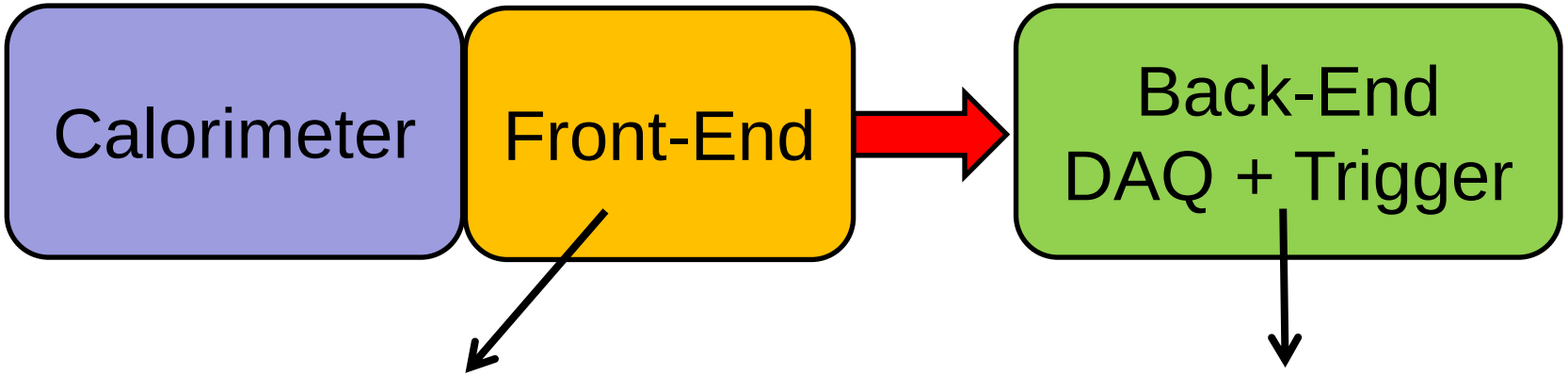
- LHC Phase II luminosity upgrade will bring:
  - instantaneous luminosities of 5 x 10^{34} $cm^{-2}s^{-1}$ → mean pile-up of 130 events
  - total luminosity of 3000 fb^{-1} → high total radiation doses
  - a total of ~30 years of operation since installation instead of anticipated 10 years → longevity of systems and components

- LHC experiments prepare for operating their calorimeter read-out and trigger electronics in these conditions



- General trend for LHC calorimeters:
  - send all data off detector for trigger and read-out at LHC bunch-crossing frequency of 40 MHz
    → apply improved and more complex trigger algorithms
    → off-detector buffers and pipelines allow increased trigger latency or purely software based triggers
  - install front-end components which are more radiation tolerant – if necessary

Overview



- Radiation tolerant ASICs and Commercial-Off-The-Shelf (COTS) components:
  signal amplification and shaping, ADCs, TDCs, signal processing, optical links with 5-10 Gbps
- Trigger, Timing and Control (TTC) distribution
- Power distribution

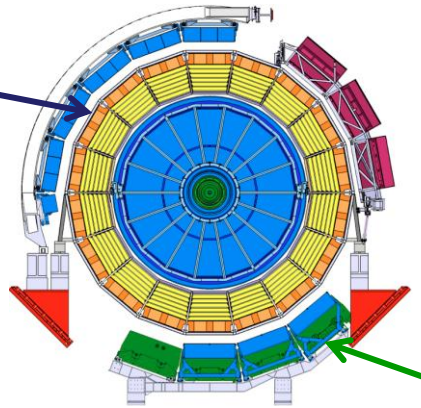
- High-bandwidth, low-latency signal processing
- Data buffering
- Trigger, Timing and Control (TTC) distribution
- High-bandwidth interfaces to hardware trigger and to network based trigger/DAQ systems

Overview

- Requirements, proposed solutions, commonalities and examples for the calorimeter upgrades of

ALICE EMCal/PHOS Front-End Upgrade LS1

EMCal Pb-Scintillator
(after LS1: 17664 towers,
trigger and readout)

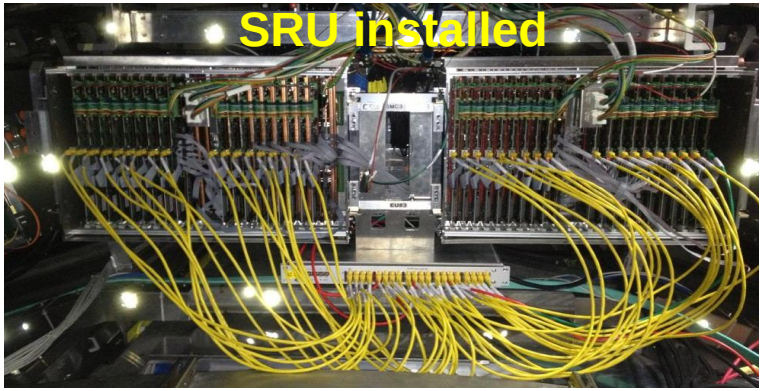


PHOS $PbWO_4$
(after LS1:
14336 channels)

- Readout upgrade with Scalable Readout Unit (SRU) in LS 1 → 40% more readout channels

- Direct front-end to network connection
  - point-to-point connection replaces bus-based readout system
- 40 Mbps input and 1 Gbps Ethernet output

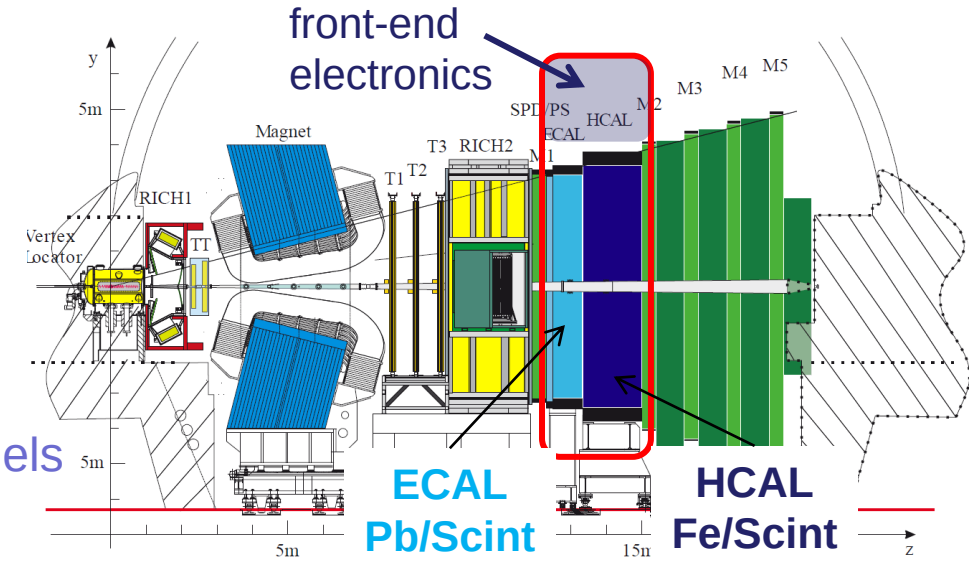
- EMCal equipped with SRUs in May 2013
- SRU installation in Photon Spectrometer (PHOS) read-out in 2014
- No further electronics upgrade foreseen for EMCal and PHOS



- Possible new Forward Calorimeter (FoCAL) after LS2

Upgrade of LHCb Calorimeter Readout

- LHCb upgrade will happen mostly already in LS2 (Phase I)
  - prepare for 5-10 fb^{-1} / year
  - currently 3.2 fb^{-1} recorded



- Expected total ionizing dose at front-end:
  1 Gy/fb → 50-100 Gy

- ECAL: 6016 channels HCAL: 1488 channels
  (pre-shower and scintillator pad detector will be removed)

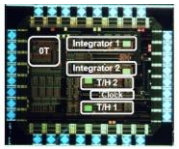
- Front-end upgrade motivation:
  - PMT gain reduction by factor 5 to increase lifetime
    → front-end with higher gain necessary,
    but requirement to keep same level of noise (~1 ADC count for 12-bit ADC)

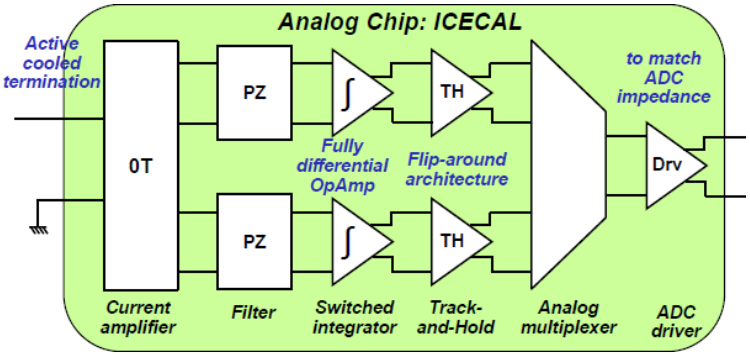
- Back-end upgrade:
  - all-data-out readout system at 40 MHz
  - input to software-based High Level Trigger switched PC-farm

- No further upgrade of calorimeter electronics foreseen after LS2

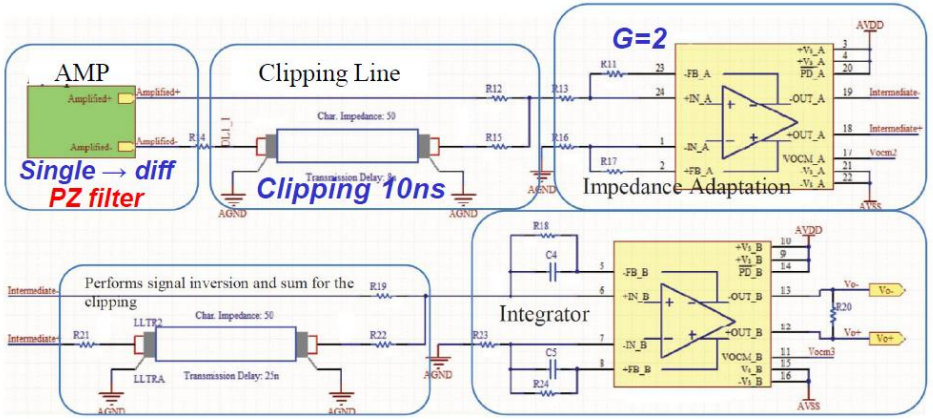
Noise Comparision: LHCb ICECAL and COTS

- ICECAL ASIC: SiGe BiCMOS 0.35µm AMS

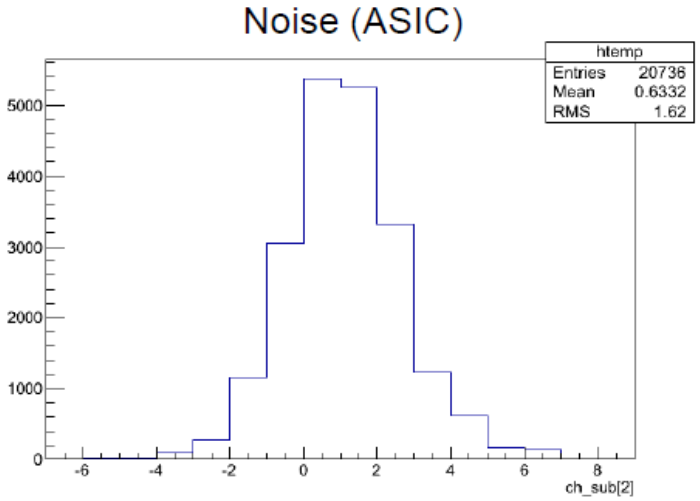


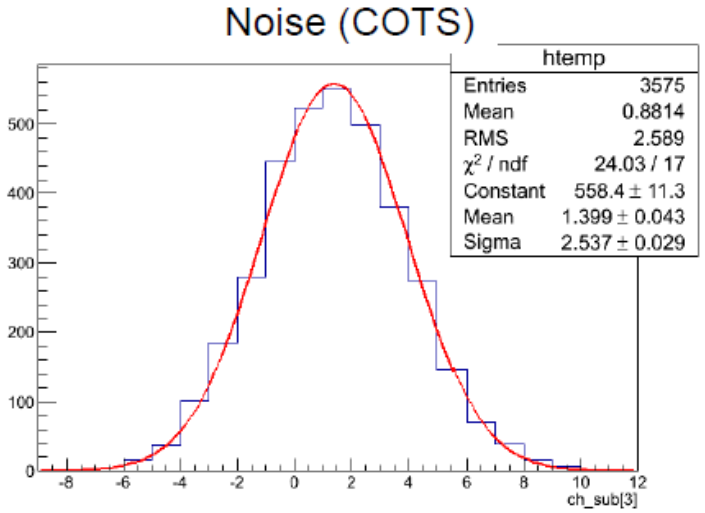


- COTS architecture:



- Testbeam results:

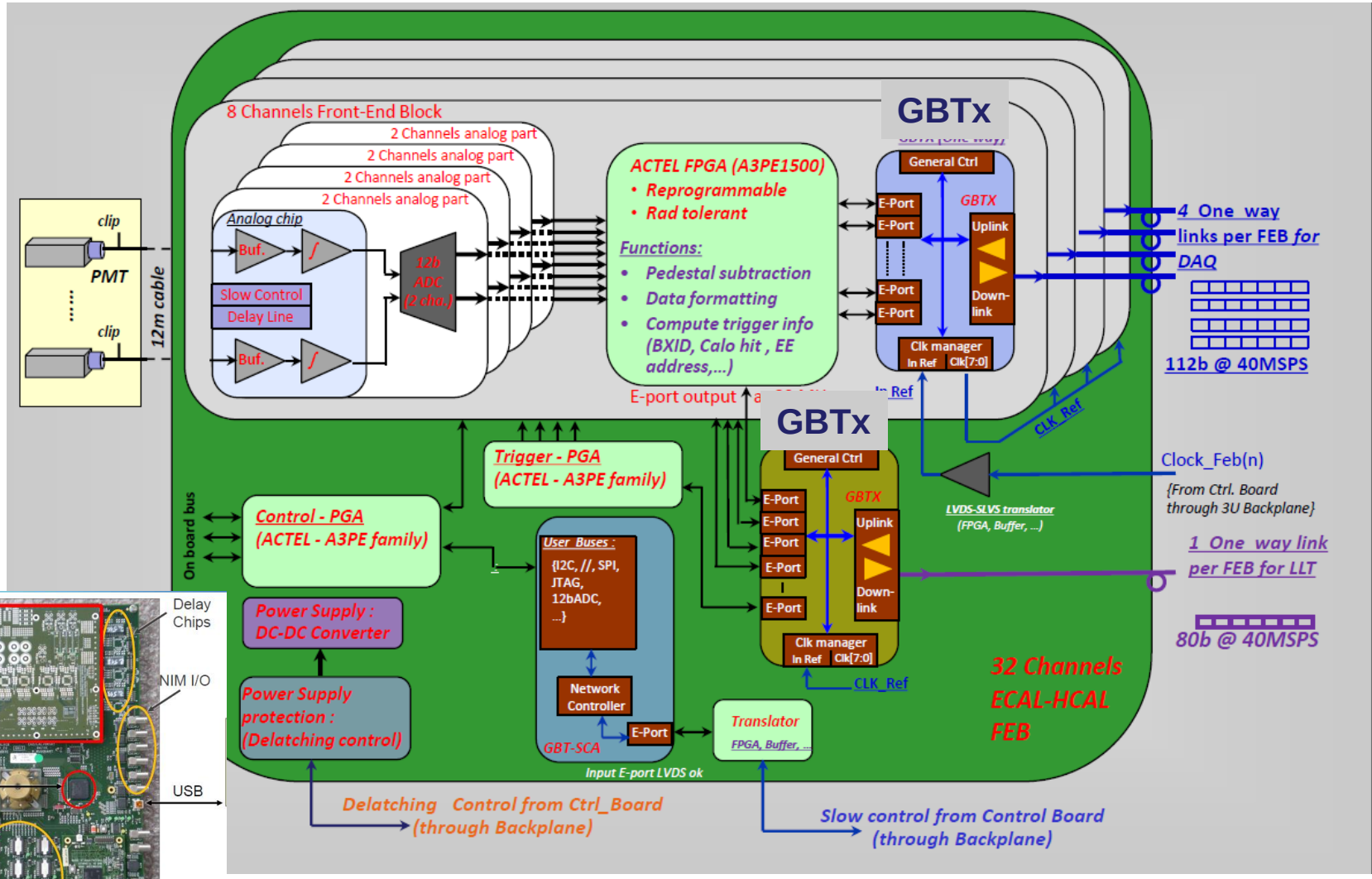




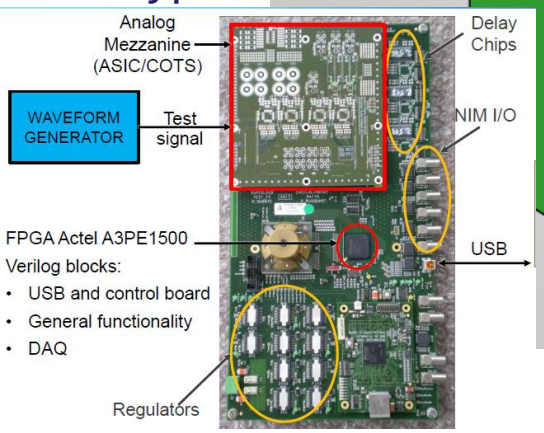
- Noise after pedestal subtraction and corrected for signal distribution: ~1.4 ADC (ASIC) and ~2.3 ADC (COTS)

Upgrade of the LHCb Calorimeter Front-End

- Radiation tolerant commercial ADCs are being evaluated, e.g. Analog Devices AD9238
- Radiation tolerant FPGAs, e.g. reprogrammable Actel A3PE1500
- CERN GBTx/Versatile Links at 5 Gbps link speed are used to transfer data to back-end



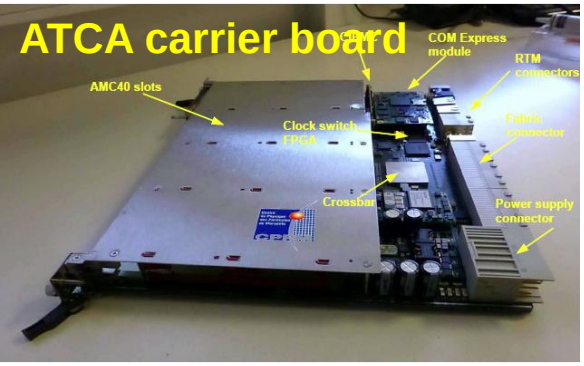
Prototype:

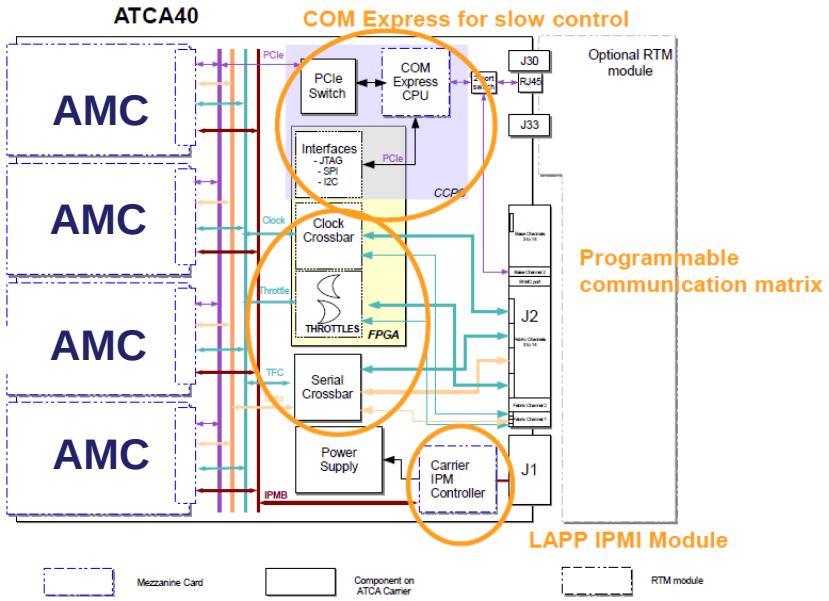


LHCb: Multi-purpose Data Processing Board ATCA40

- ATCA = Advanced Telecommunications Computing Architecture industry standard
- Up to 4 Advanced Mezzanine Cards AMC40 mounted on ATCA carrier board
  - 36 bidirectional optical links per AMC at up to 10.3 Gbps with 10^{-16} BER (10 m)
    → GBTx front-end link runs at 5 Gbps
  - prototype equipped with Stratix V FPGA

- Board can be configured for readout, trigger, and slow-control purposes



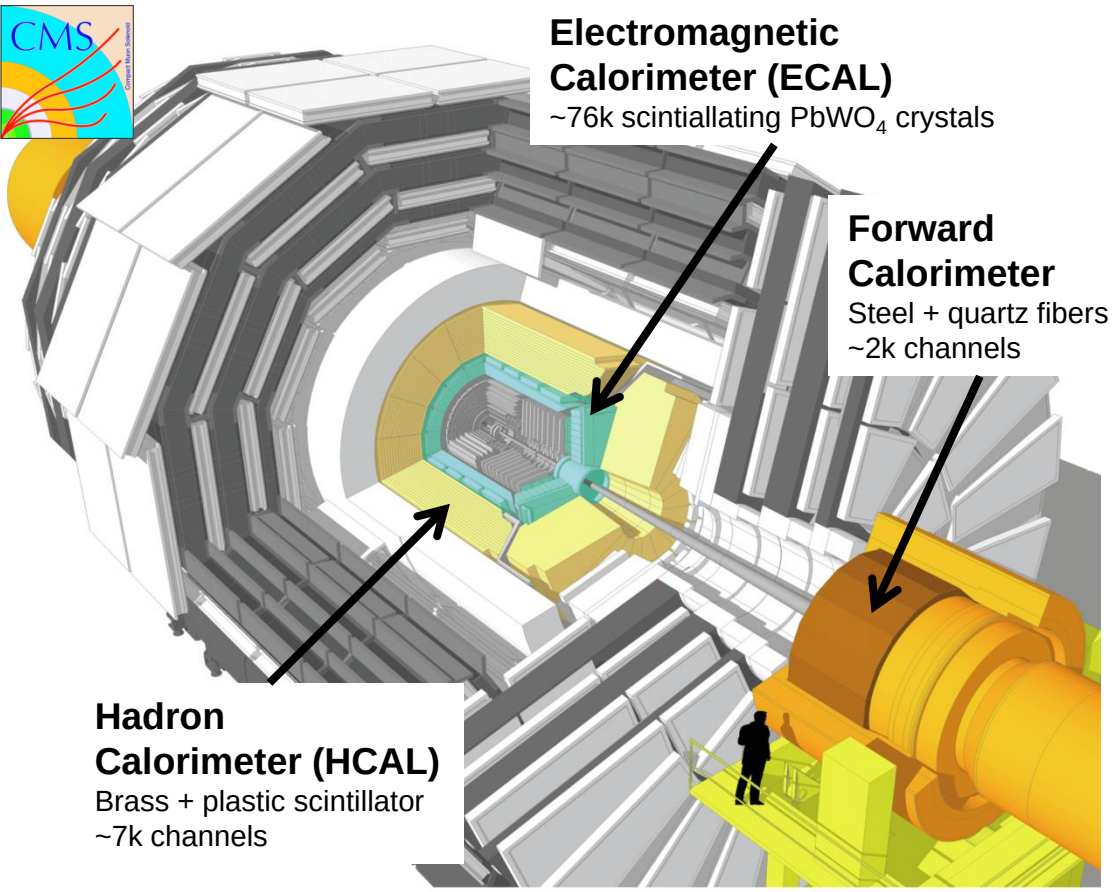


- Many ATCA features typically not used: full redundancy, next-neighbour communication
- ATCA requires board infrastructure: DCDC converters on board, controller interfaces, ...

→ alternative based on PCIe FPGA boards is being developed

→ direct input to PC/network based LHCb High Level Trigger

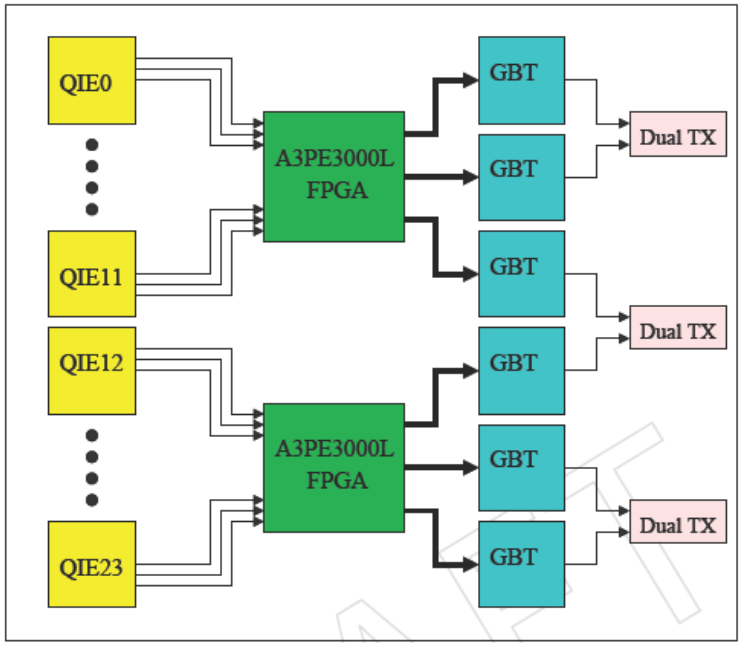
CMS Calorimeter Electronics Upgrade



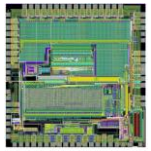
- Thin window, multi-anode PMTs will be installed on Hadronic Forward Calorimeter in LS 1
- Silicon Photomultipliers (SiPM) will replace Hybrid Photon Detectors (HPD) in LS 2 in HCAL Barrel and Endcap
- Finer longitudinal segmentation of HCAL (x 3/x 5 in barrel/endcap):
  - better pile-up treatment
  - improved particle identification (particle flow, electron identification, muon isolation)

- Plan for ECAL and HCAL upgrade for LS 3 (Phase II):
  - upgrade the ECAL Barrel electronics
  - replace ECAL Endcap + PreShower with a new radiation-hard detector

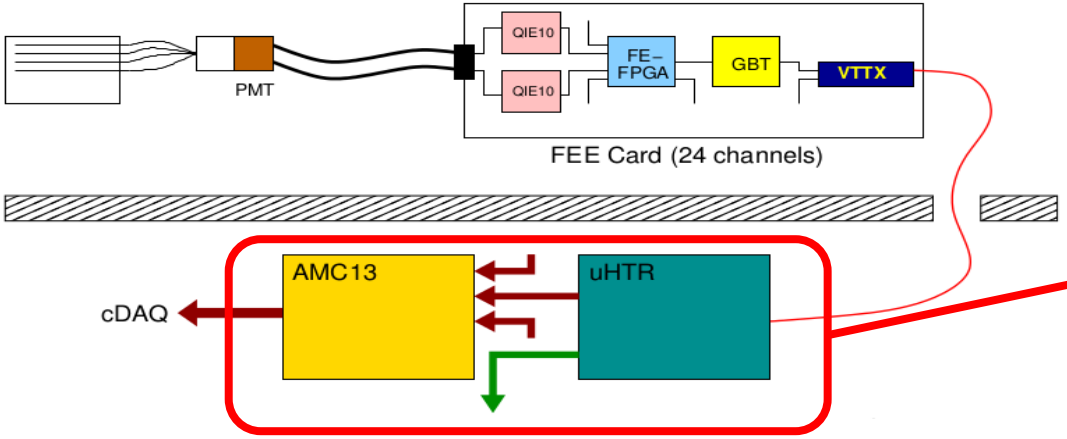
CMS HCAL Electronics Upgrade in LS 1+2

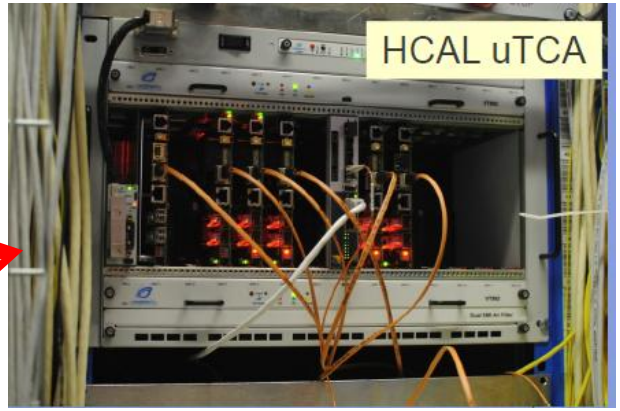


- Required radiation tolerance: 100 Gy
- Data are sent to trigger and read-out at 40 MHz
- HCAL front-end to be equipped with QIE10 chip for charge integration and encoding:
  6 bit ADC, 2 ranges, 2 Capacitor ID
  → 17 bit dynamic range, 6 bit TDC

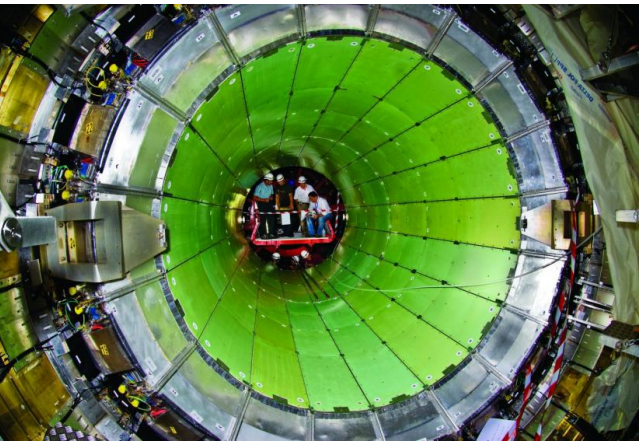


- Better TDC timing (<1 ns resolution) for BC identification, pile-up and background reduction, and anomalous noise identification
- Radiation tolerant FPGAs
- CERN GBTx/Versatile Link to back-end:
  - preprocessing and event building in µTCA modules (uHTR, AMC13)



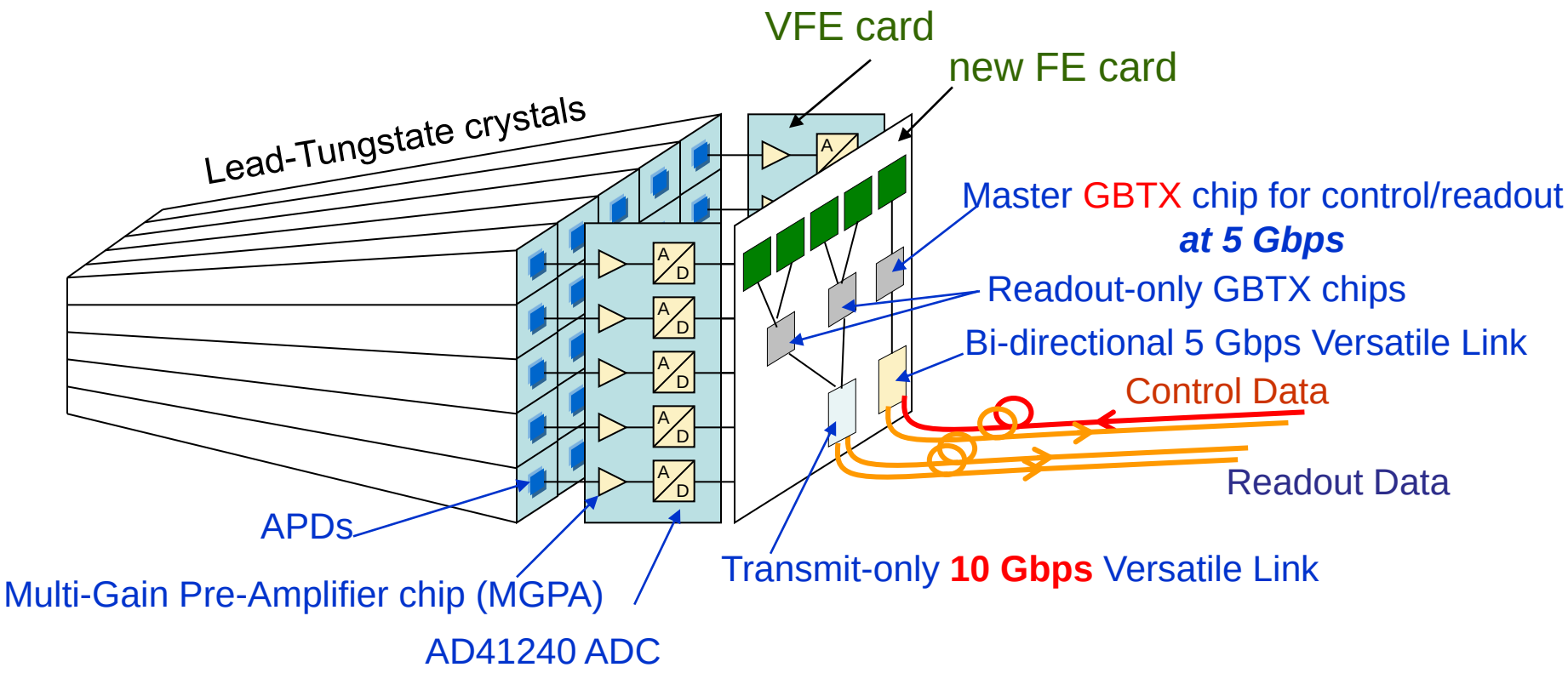


CMS ECAL Barrel Phase II Readout Upgrade



- 61000 $PbWO_4$ scintillating crystals with Avalanche Photodiodes (APDs) to read out the scintillation light
  - energy is currently summed in groups of 25 crystals for trigger information
- Upgrade motivation:
  - read out of all crystals for hardware trigger at 40 MHz
    - level-1 accept rate at 1 MHz
  - present on-detector circular buffer limited to 6.4 μsec
    → remove time limitation for trigger algorithms by by moving all buffers to off-detector electronics
- Electronics upgrade requires:
  - remove all 36 ECAL Barrel supermodules, replace the front-end cards and optical components, then re-install the supermodules
  - replacement of the services (cables, optical fibres)

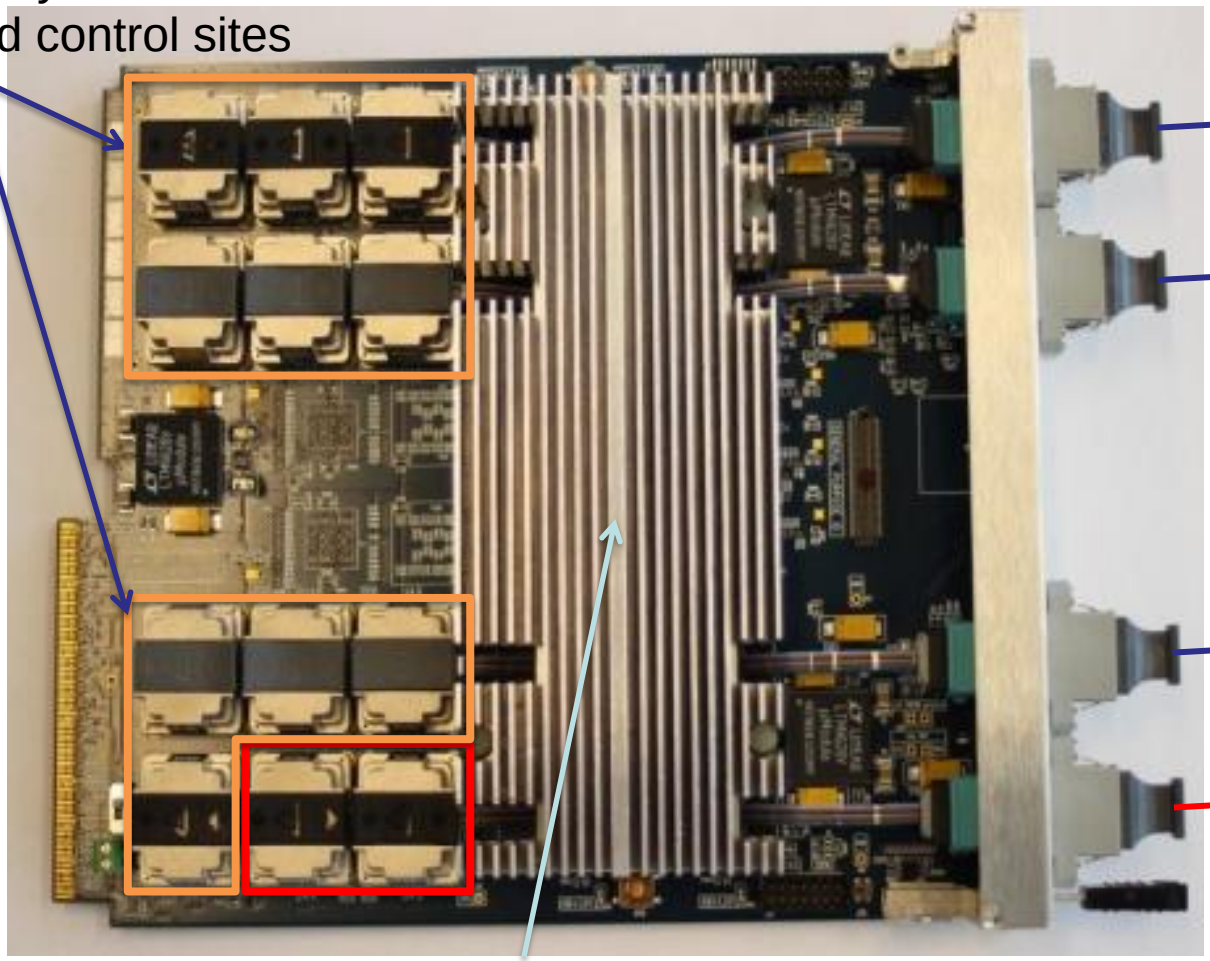
CMS ECAL Barrel Upgrade – Proposed Idea



- Key features:
  - 1 control path and 3 readout paths for 25 crystals at 40 MHz
  - present front-end ASICs are in CMOS 0.25μm → meet radiation tolerance for Phase II
  - replace FE card, including a new ASIC
  - VFE card replacement considered → reject anomalous signals by better signal timing
  - CERN GBTx link for data transfer to back-end and control
  - 10 Gbps rad-tolerant link is required → GBTx evolution needed
  - radiation tolerant power regulation on-detector required

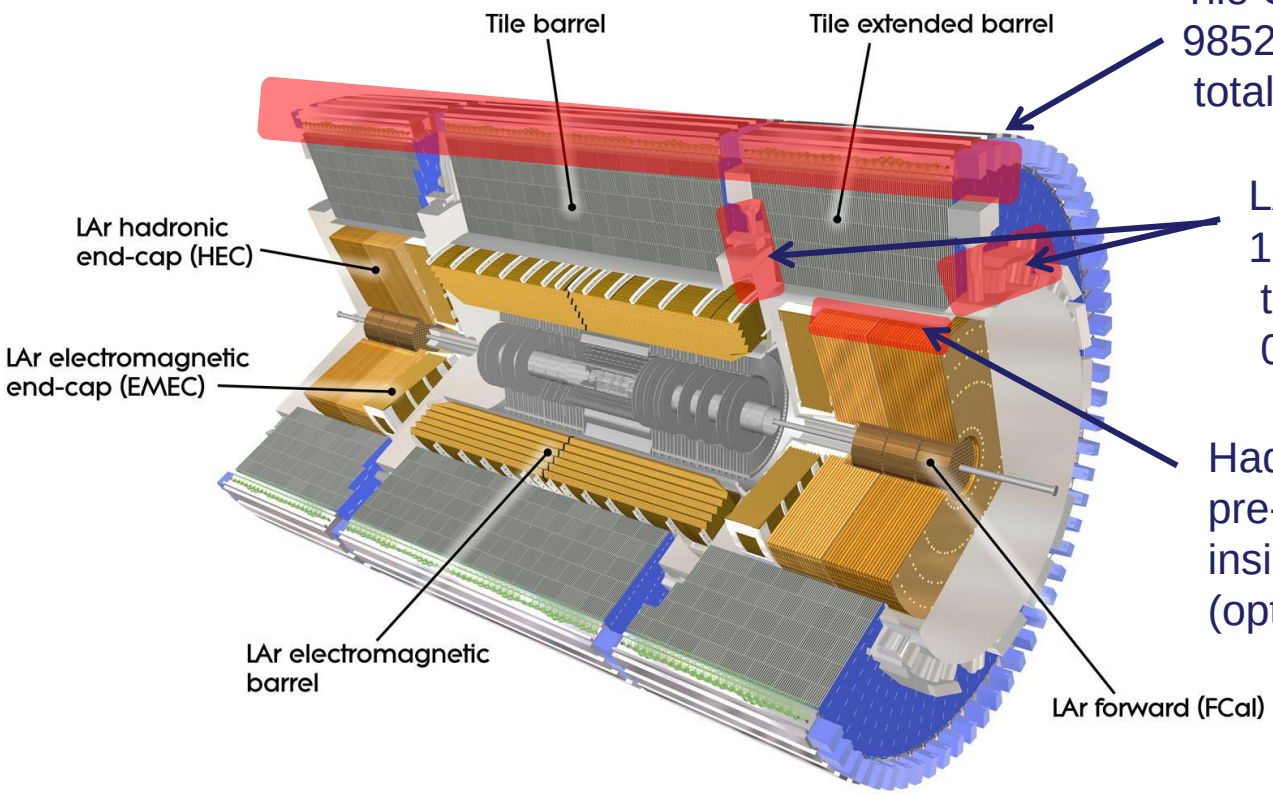
CMS ECAL Back-End with MP7 µTCA Board

- Present idea for back-end: evolution of MP7 µTCA board as developed for Phase I upgrades of the trigger system



ATLAS Upgrade of Calorimeter Electronics

- Reasons for replacement of ATLAS calorimeter electronics in LS 3 (Phase II):
  - Ageing and radiation tolerance of front-end electronics → system longevity
  - Limited on-detector pipelines prevent application of more advanced trigger algorithms
- On-detector digitization of all signals at 40 MHz → input to Level-0/Level-1 triggers
  - Level-0 with accept rate of 500 kHz and latency of 6 μs
  - Level-1 with accept rate of 200 kHz and latency of ~20 μs



Tile Calorimeter front-end:
9852 channels,
total ionizing dose requirement 1kGy

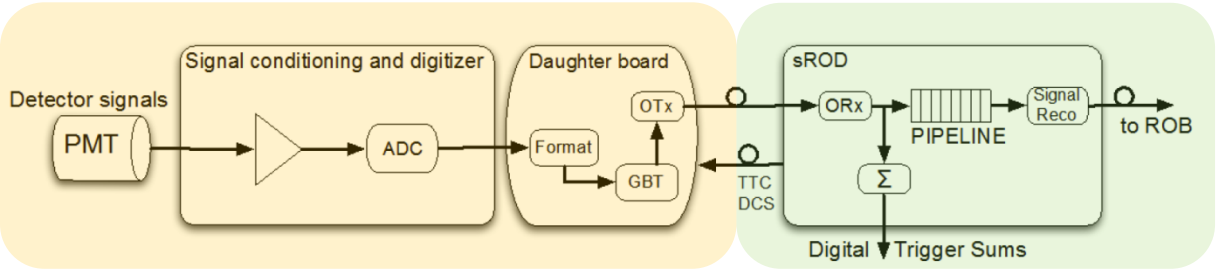
LAr Calorimeter front-end:
182468 channels,
total ionizing dose requirement
0.15-2.8 kGy

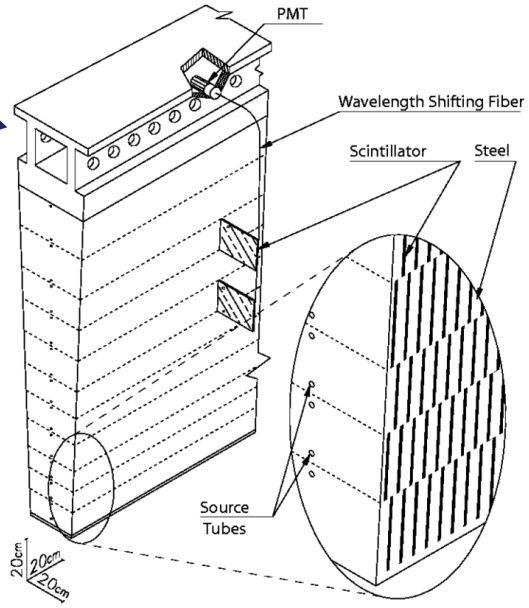
Hadronic LAr Endcap Calorimeter:
pre-amplifier and summing boards
inside endcap cryostat
(optional replacement)

+ new back-end electronics

Upgrade of the ATLAS Tile Calorimeter Readout

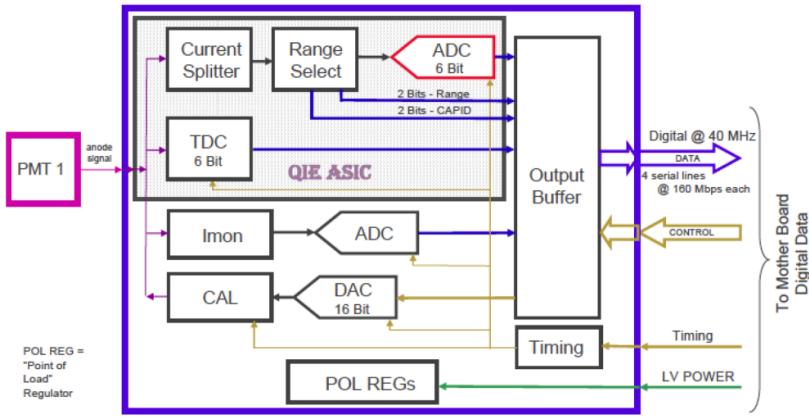
- Front-end electronics installed in 256 drawers
- Free-running design with 40 MHz digitization





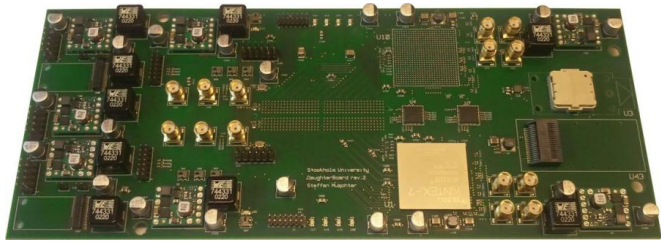
- Main front-end components:
  - Mixed analog/digital Main Board:
    - PMTs will be read-out *redundantly*
    - low voltage power supply will be *redundant*
  - Front-End Board: 3 alternative developments
    - evolution of today's 3-in-1 card: shaper, 2-gain amplifier, 3-gain integrator for Cs calibration
    - QIE10 based design
    - new ASIC development: FATALIC/TACTIC
      - 130 nm IBM process
      - 3 gain shaper, 12-bit pipeline ADC
      - slow integrator for Cs calibration

A Conceptual Design of the QIE Front End Board

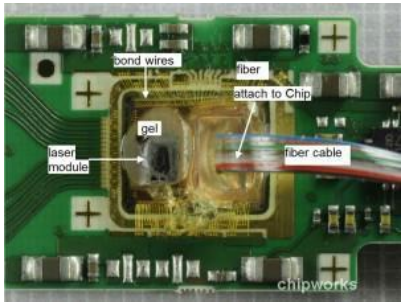


Upgrade of the ATLAS Tile Calorimeter Readout

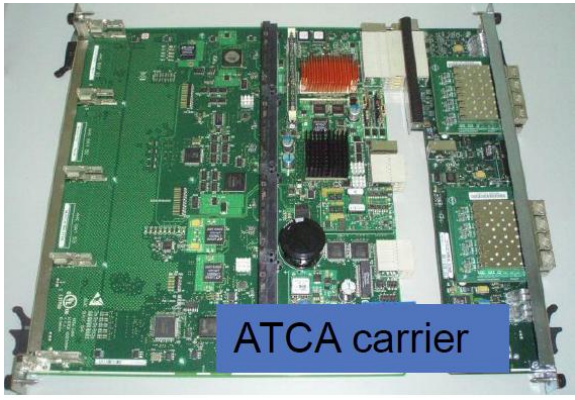
- Daughter boards:
  - 2-fold redundancy
  - Kintex-7 FPGA for data transmission at 10 Gbps
  - Bit Error Rate (BER) better than 10^{-15} at 10 Gbps
  - CERN GBTx is used for TTC data at up to 5 Gbps



- Optical links: Modulator approach is being evaluated in TileCal demonstrator
  - optical transceivers based on light modulators
  - 4 x 10 Gbps with 10^{-18} BER
  - Luxtera chip in 130 nm Silicon-on-Insulator (SoI) CMOS
  - high radiation tolerance of optical device itself
  - however, microcontroller (PIC) needs to be replaced for ATLAS applications



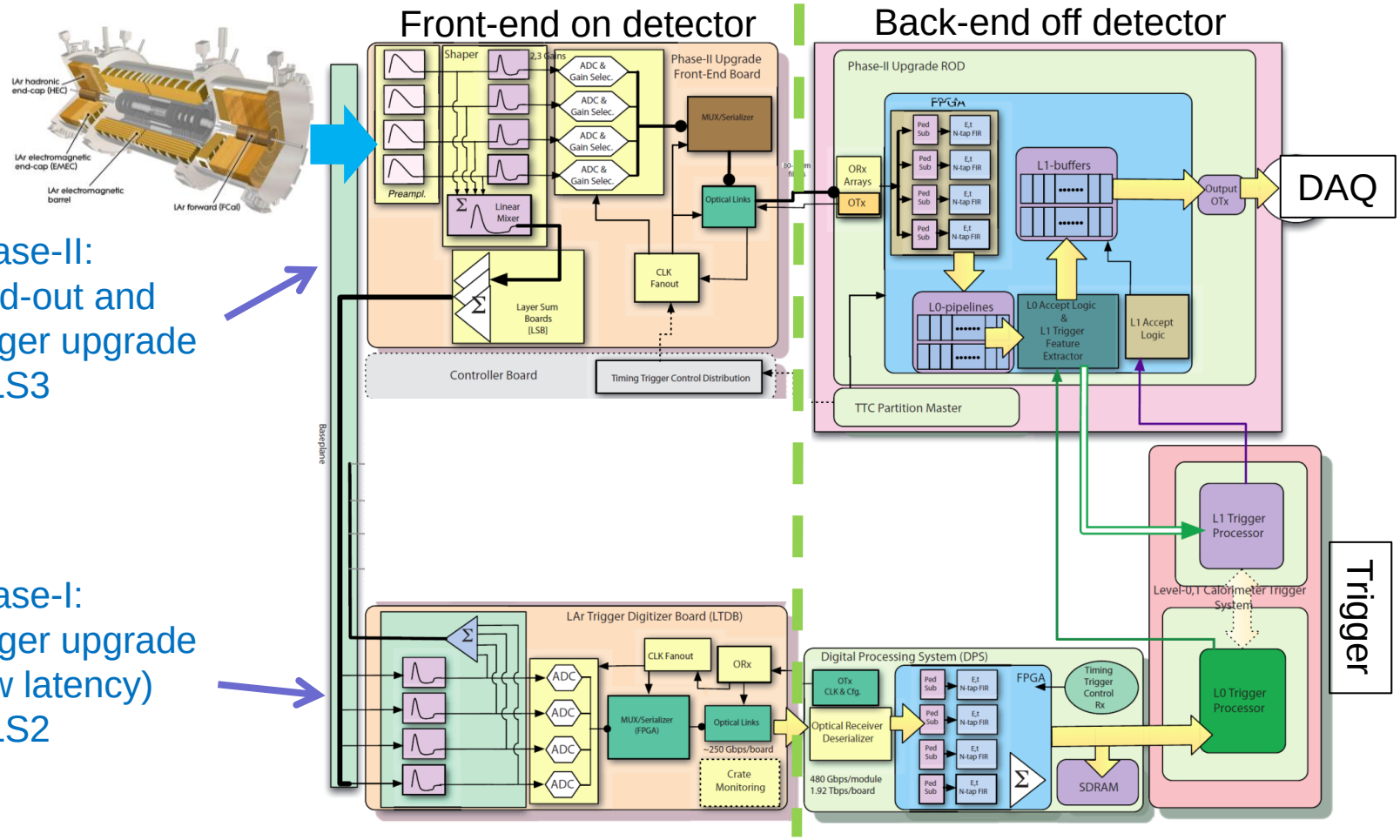
- Back-end: Read-Out Driver in ATCA format
  - full custom ATCA blade design with Virtex7/Kintex7 FPGAs
  - 625 Gbps per Board and 20 Tbps total
  - signal extraction, bunch-crossing identification for trigger, pipeline buffer, TTC signal distribution



- One TileCal drawer is planned to be equipped with a full demonstrator front-end and back-end system in LS 1

Phase II Upgrade of ATLAS LAr Calorimeter Readout

- Free-running readout of all 182468 channels with 40 MHz front-end ADCs and optical transmission to back-end → total bandwidth 140 Tbps
- Front-end with more radiation tolerant components→ trigger buffers will be off-detector
- Upgraded trigger read-out foreseen in LS 2 will be used for low-latency Level-0 trigger in Phase II



ATLAS LAr Calorimeter Front-end Upgrade

- Hadronic Endcap GaAs pre-amplifier and summing chips installed *inside* LAr cryostat
  - delicate operation to open the cryostat if replacement is necessary

  → possible degradation at 3000 fb^{-1} and ageing effects are currently being evaluated
  - replacement decision is planned to be taken in 2014

  → preferred replacement technology available: Si CMOS 250 nm IHP

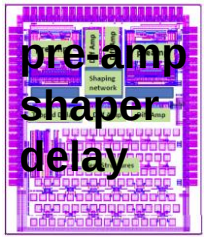
- Front-end electronics *outside* the LAr cryostat is foreseen to be replaced (except new Phase I electronics) → radiation tolerance for 3000 fb^{-1} and system longevity

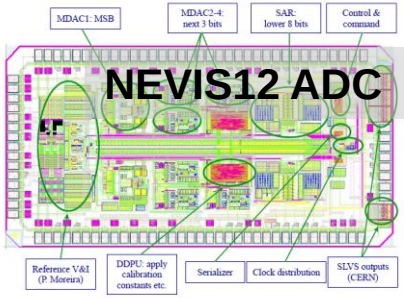
- Custom pre-amplifier, signal shaping and delay ASIC: re-prototyped in cost-effective IHP technology
- Custom ADC development within Phase-I activities:
- NEVIS / PEALL12-bit ADC, IBM 130nm CMOS
  - low power (30-50 mW/channel), low latency (<90 ns)
  - radiation tolerance: 12 kGy, 3.3 x 10^{14} n_{eq}/cm^2, 6.3 x 10^{13} h/cm^2

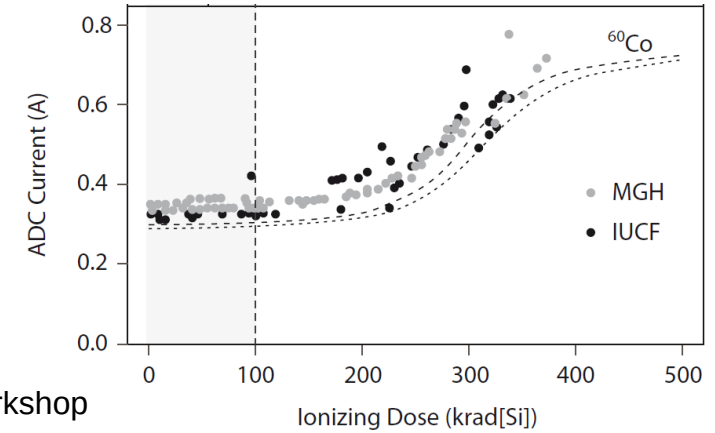
  → will evolve into Phase II applicable ADCs
- Alternative: qualification of commercial 12-bit ADCs for Phase-I/II upgrade applications:

  Texas Instruments ADS5272 performed best

  → radiation tolerant up to 1 kGy (100 krad), low power (113 mW), low latency (163 ns)





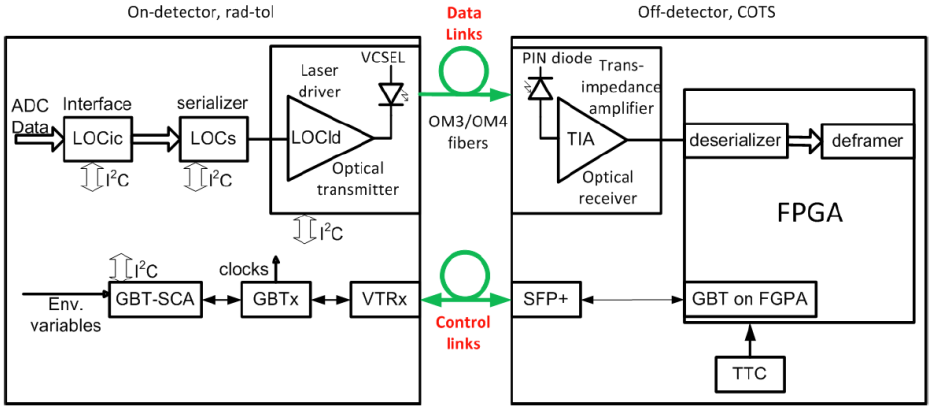


LAr Calorimeter Data Transfer and Processing

- Link-on-chip (LOC) development in Silicon-on-Sapphire (SoS) 0.25 µm
- Technology allows 8 Gbps design - currently applied at 5 Gbps in Phase-I upgrade
  - custom interface and serializer
  - VCSEL pairs from Versatile Link

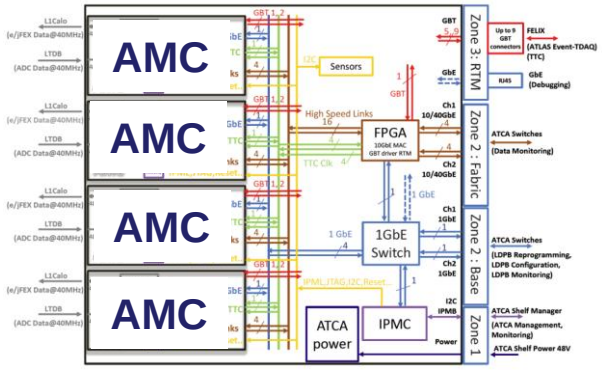
→ Total latency 76 ns (comp. GBTx 220 ns)

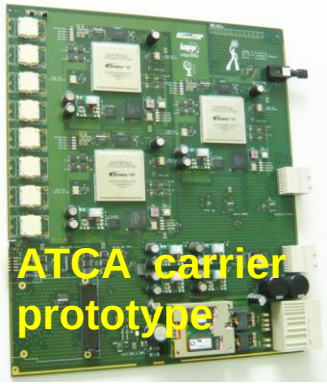
- CERN GBTx is used for TTC data



→ Phase-II requires 12 x 10 Gbps VCSEL arrays and an improved SoS process or a next-generation GBTx

- Data planned to be processed by high-bandwidth ATCA Pre-Processor boards
  - 1.2 Tbps input from front-end and ~250 Gbps trigger information to Level-0
  - tasks: energy reconstruction, bunch-crossing identification, pipeline, trigger sums
- Phase-I ATCA carrier and AMC boards will evolve into Phase II solutions





- example: Intelligent Platform Management Interface (IPMI) development for ATLAS and LHCb

Summary

- Goal of all LHC calorimeter electronic developments is to meet the challenging pile-up and radiation requirements and to ensure longevity of the systems

- General concepts for future calorimeter electronics at LHC detectors:
  - high-bandwidth, all-channel read-out at LHC collision frequency of 40 MHz
    → higher detector granularity, better timing measurement for improved triggers
  - radiation tolerant electronics to sustain up to 3000 fb^{-1} (ATLAS, CMS)

- Many common development paths for Phase I and Phase II for on-detector and off-detector electronics - some examples:
  - qualification of radiation tolerant commercial components: ADCs, FGPAs
  - application and qualification of custom devices, e.g. QIE10 chip explored by ATLAS and CMS
  - CERN GBTx/Versatile Link well received and implemented
    → 10 Gbps radiation tolerant version needed by ATLAS LAr and CMS ECAL
  - development and testing of distributed powering components
  - ATCA , µTCA processing boards and alternatives like PCIe FPGA boards

- A challenging R&D upgrade program is ahead of us:
  → many activities have started already – others need to start now!
  → electronics engineers and associated physicists need to work together as much as possible to exploit the common development paths