ECFA High-Luminosity LHC Experiments Workshop

muon system : #4

Muon detector readout and (hardware) trigger-electronics upgrades for the HL-LHC

Masaya ISHINO (ATLAS , Kyoto Univ.) with the help of ...

Herve Borel (ALICE)

Kerstin Hoepfner (CMS)

Alessandro Cardini (LHCb)

“better” μ-trigger in HL-LHC

maximize **interesting events / time**

different physics **target** → **approach** could be different

ATLAS , CMS : **high-p_T μ** from heavy particles

increase purity of trigger events with sharper turn-on

what is done in Software **→ Hardware Trigger**

LHCb , ALICE : μ from B-meson, J/ψ decays , **...**

simpler Hardware-Trigger, increase events processed

on Software-trigger

→ put more efforts on **readout electronics**


LHCb

LHCb DAQ/Trigger scheme

40 MHz

Calorimeters
Muon

LLT — Hardware Trigger a la **"throttle"**

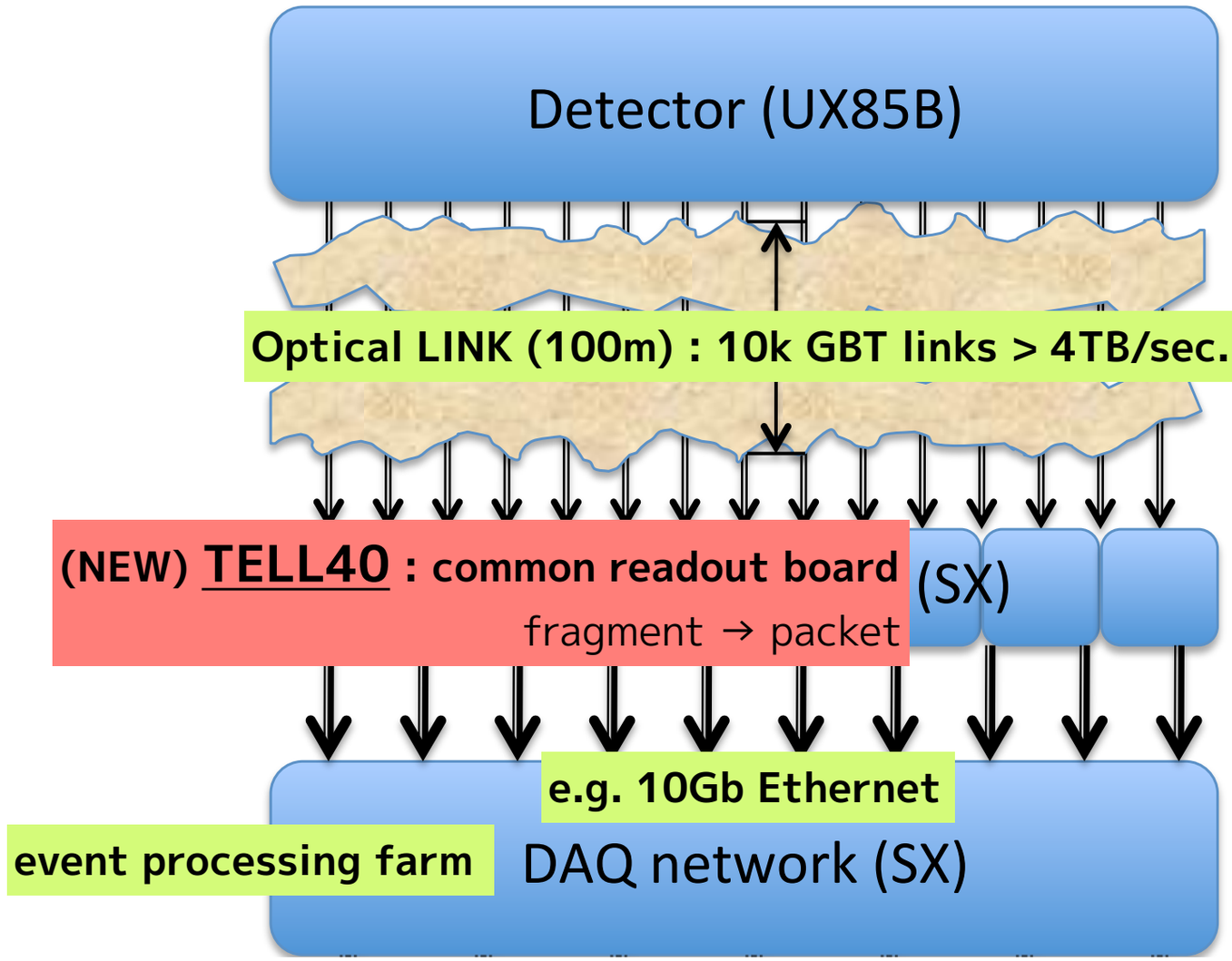
p_T of h, μ, e/γ

1 ~ **40MHz**

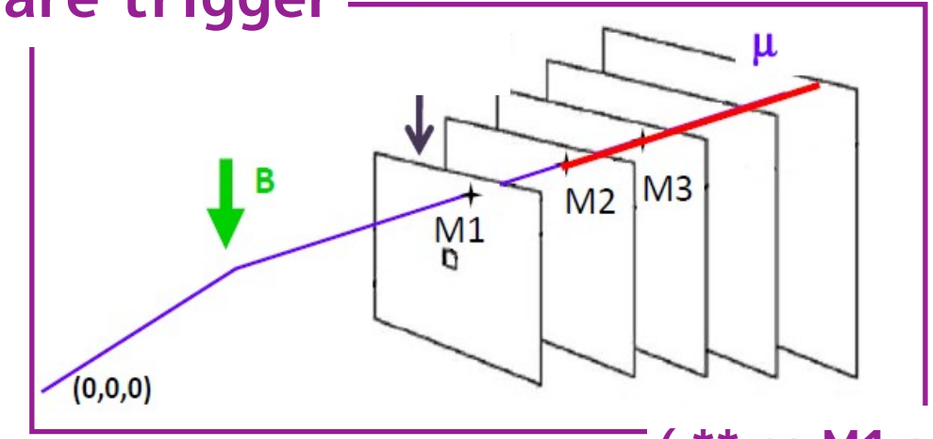
HLT — Software-Trig. (CPU farm)

tracking and vertexing
p_T and impact parameter cuts
inclusive/exclusive selections

20 kHz

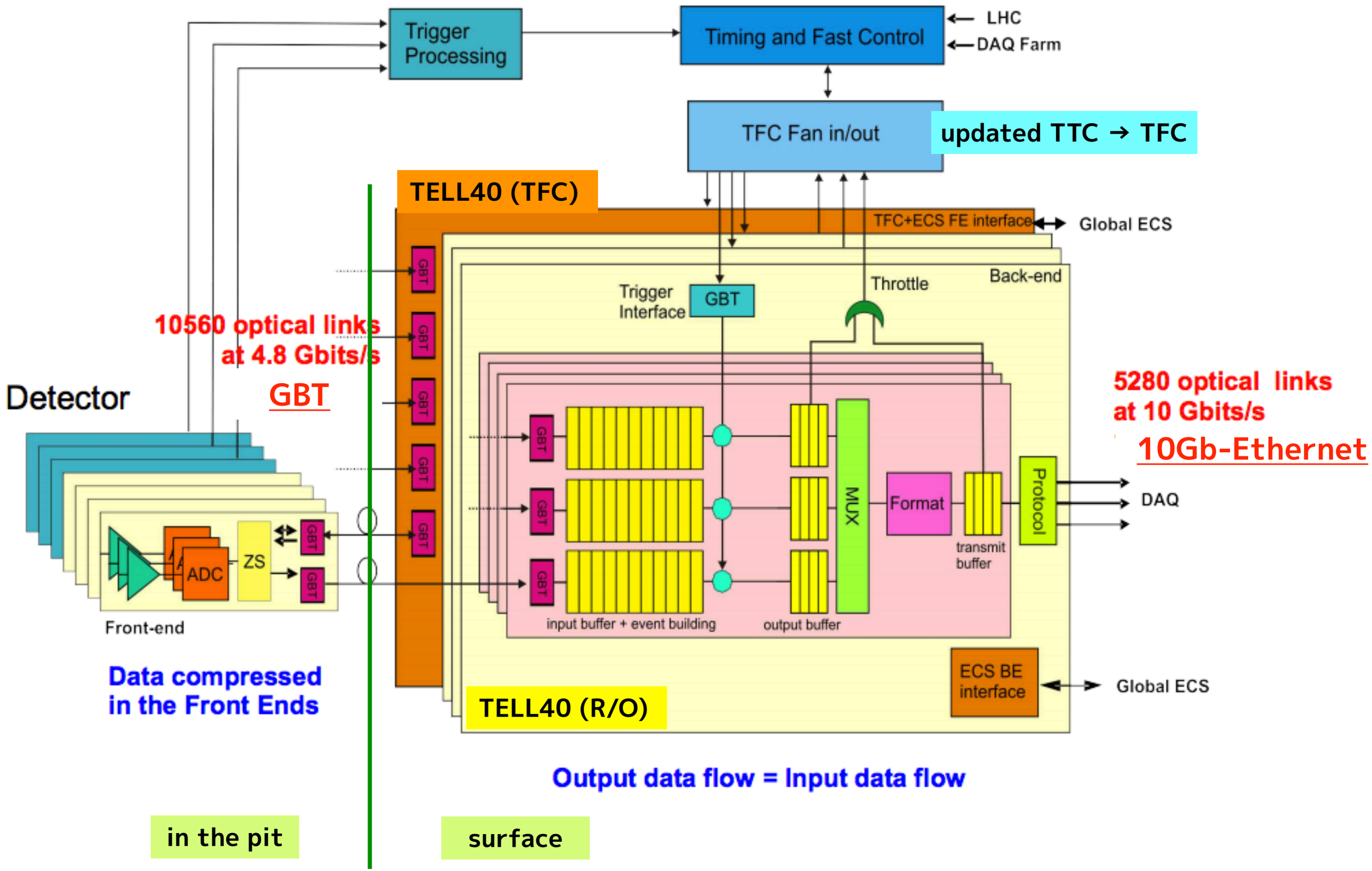


μ hardware trigger

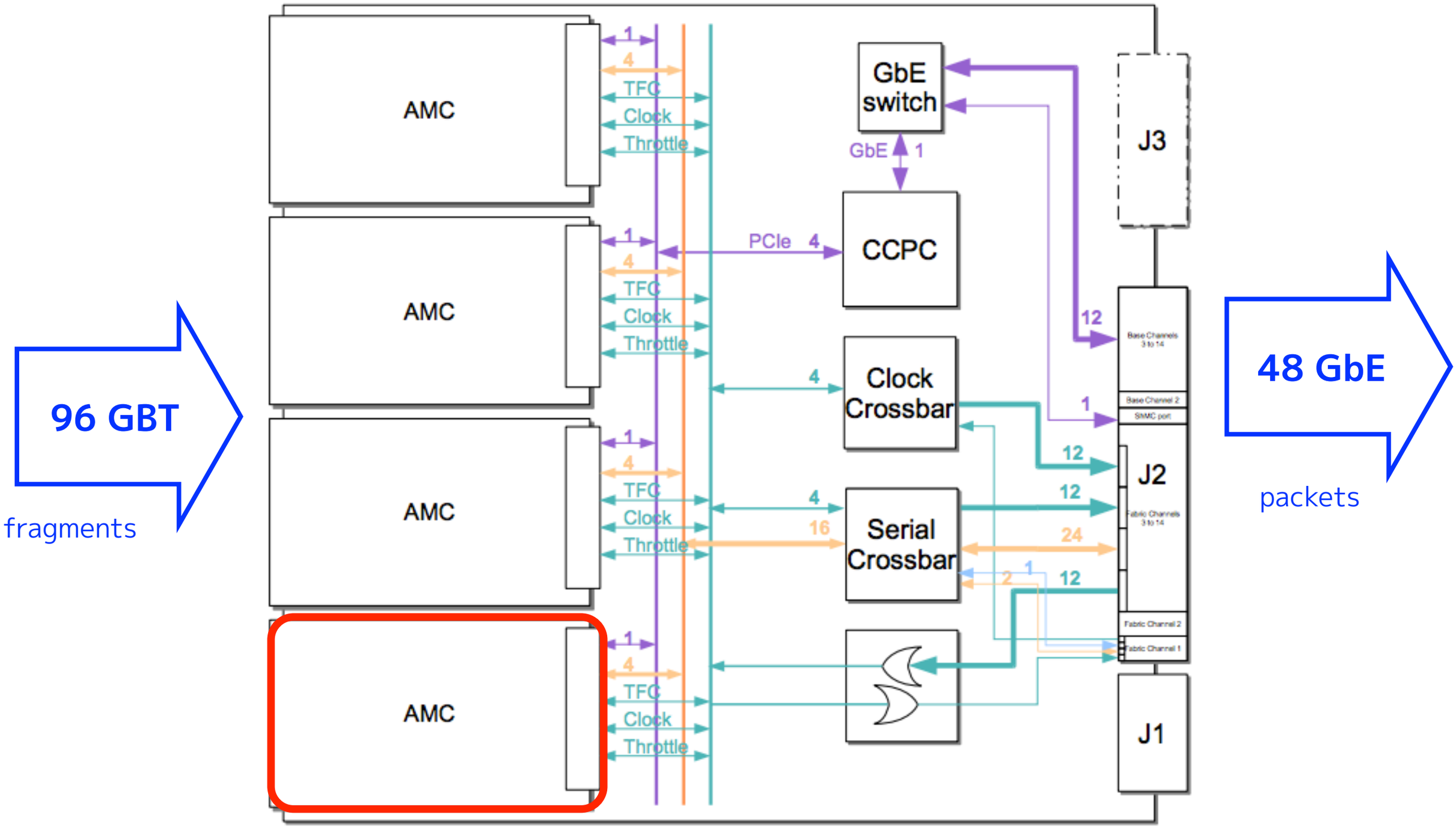


(** no M1 after LS2)

LHCb Readout



LHCb - TELL40 (Readout)

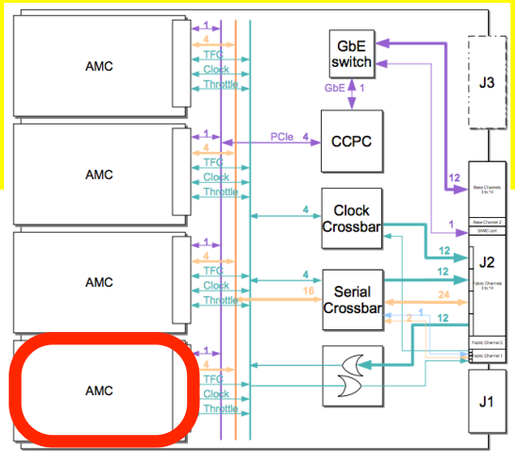


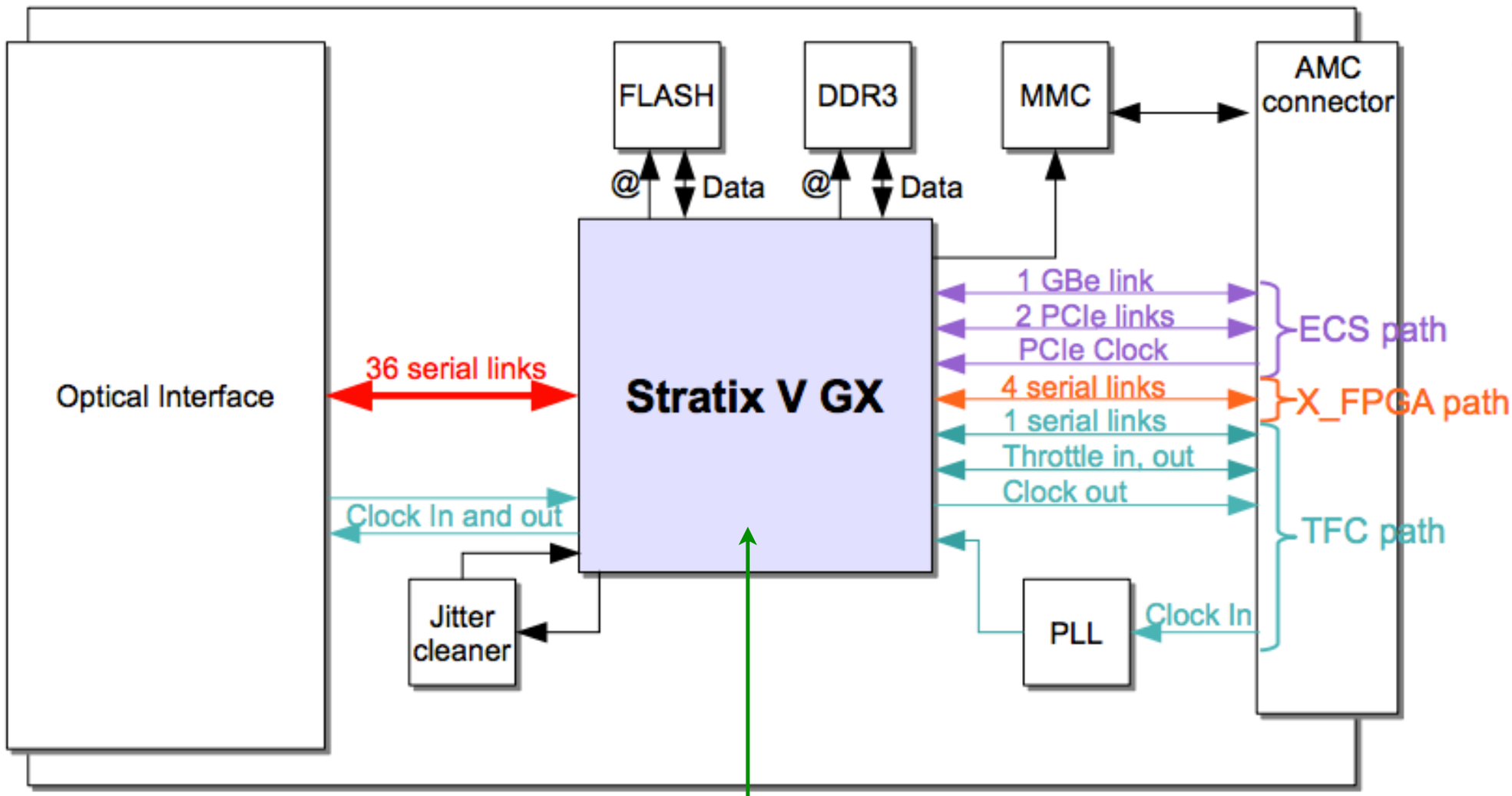
***** 110 boards for the entire LHCb system

*** <u>common hardware for all</u> the sub-system**

(housed in ATCA carrier)

LHCb - AMC (daughter b. of TELL40)





(1) **high density serial link** is available

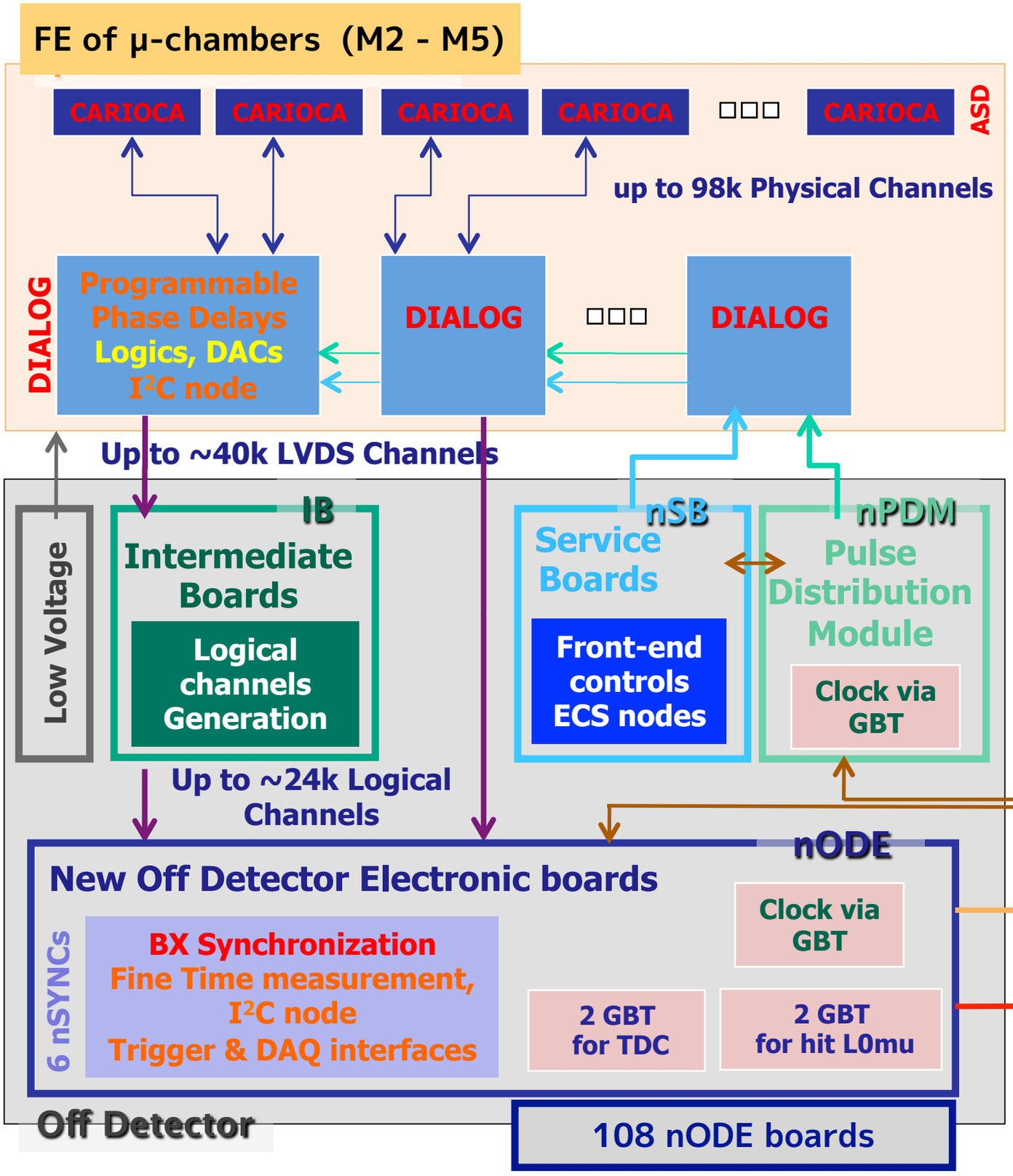
[IN] : FE → TELL40

[OUT] : TELL40 →DAQ network

(2) The FPGA is powerful enough to implement **data processing** algorithm

e.g. Zero-suppression , data formatting , ...

LHCb - μ Readout & μ-LLT



It is performed on **TELL40** !!

* projective algorithm → μ-ID
* p_T cut

Hit or no_HIT (1b/ch.)
to LLTrigger processing

L0 (μ) Trigger on 4 TELL40s (4 AMC)

ECS via duplex GBT

Hit/L0mu: 280 GBT links

NZS @ 40 MHZ

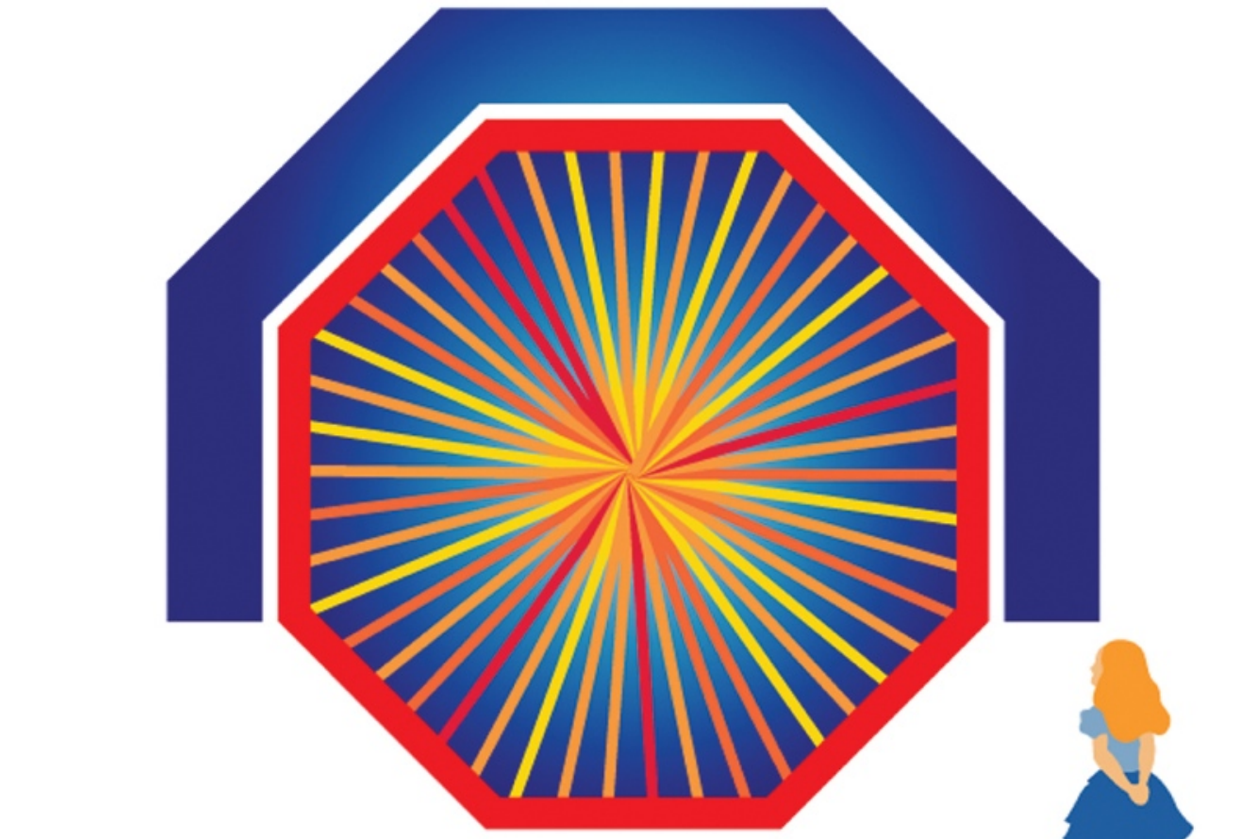
TDC: 280 GBT links

ZS @ 40 MHz

4 TELL40s (4 **AMC**)

TDC

4b/ch. Zero-suppress

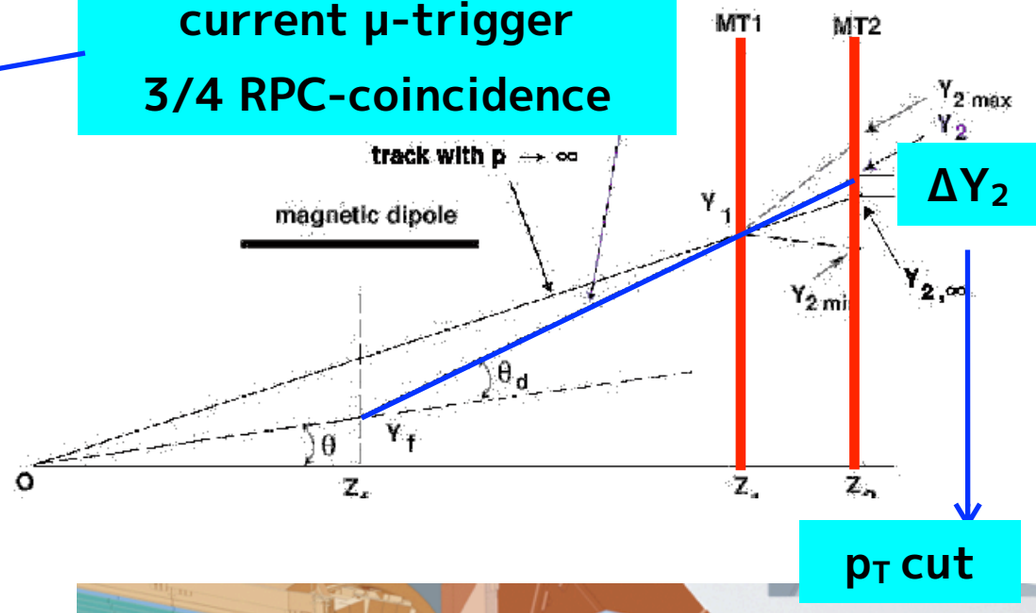


ALICE

ALICE μ-electronics @ HL-LHC

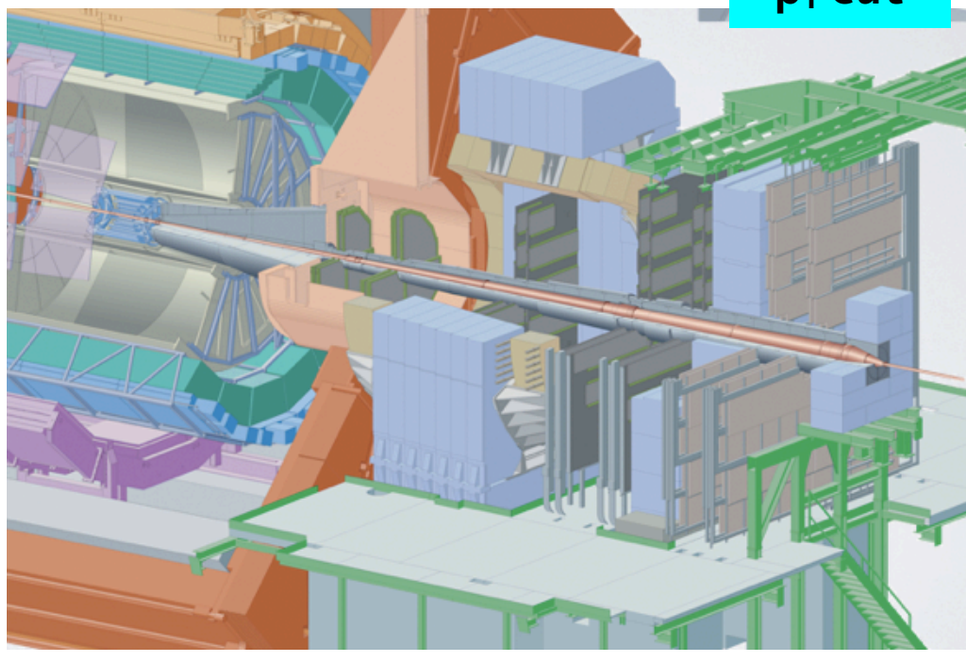
Hardware Trigger : **Minimum-bias**

current μ-trigger
3/4 RPC-coincidence



- data transfer to Software-Trig. **@ 100kHz**
- continuous sampling **10MHz** & pipeline R/O

→ New ASIC chip
common for μ-trackers & TPC



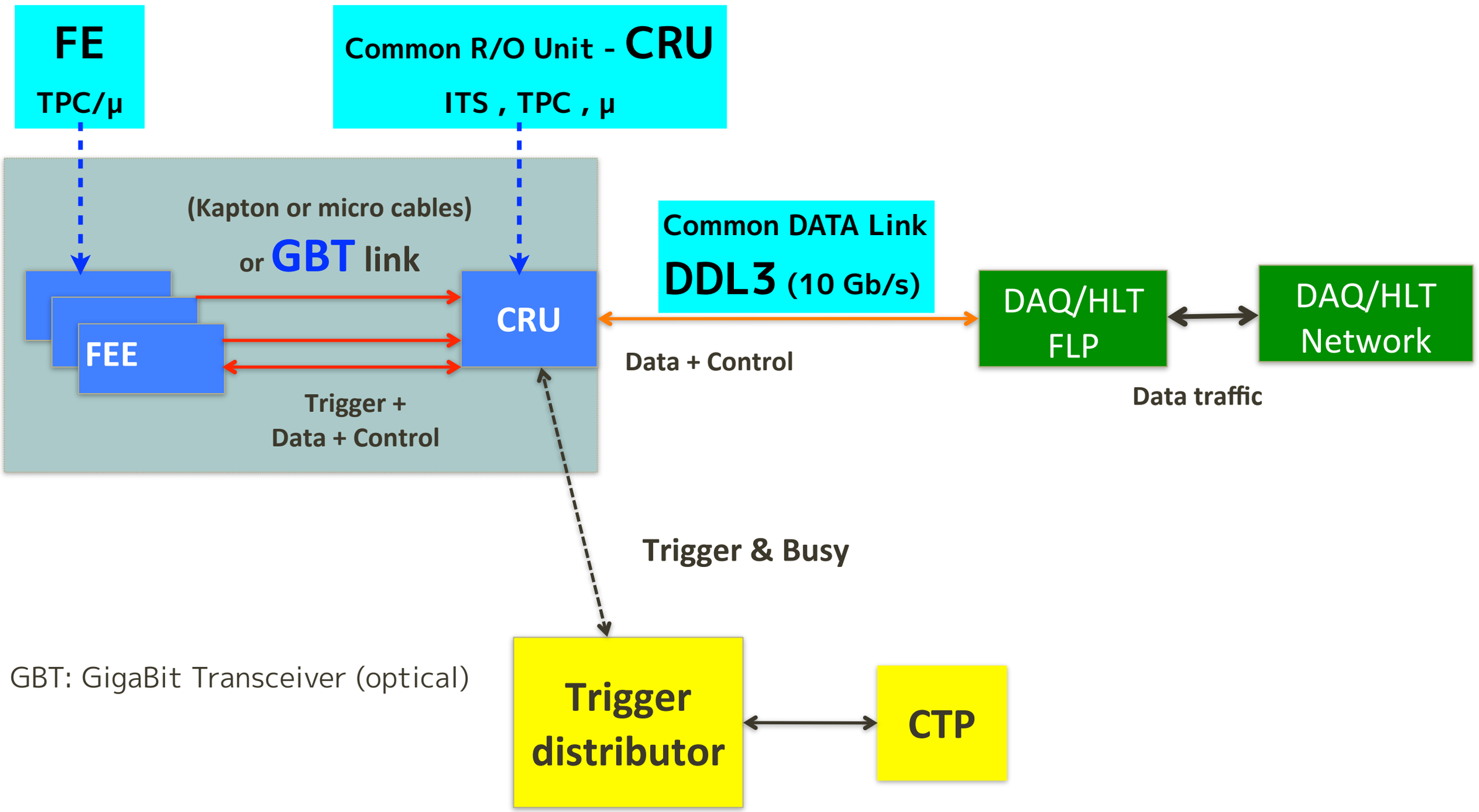
Points

- the range of gain and shaping time is extended
- single sampling and data readout runs independently

notes

- The technology : TSMC 130nm for the ASIC.
- In total 17,000FE cards (1 FE Chip = 32ch. , 1FE Card = 2FE chips)
- Power consumption : 15 to 20mW/ch. (x 1/4 w.r.t. the current chip)

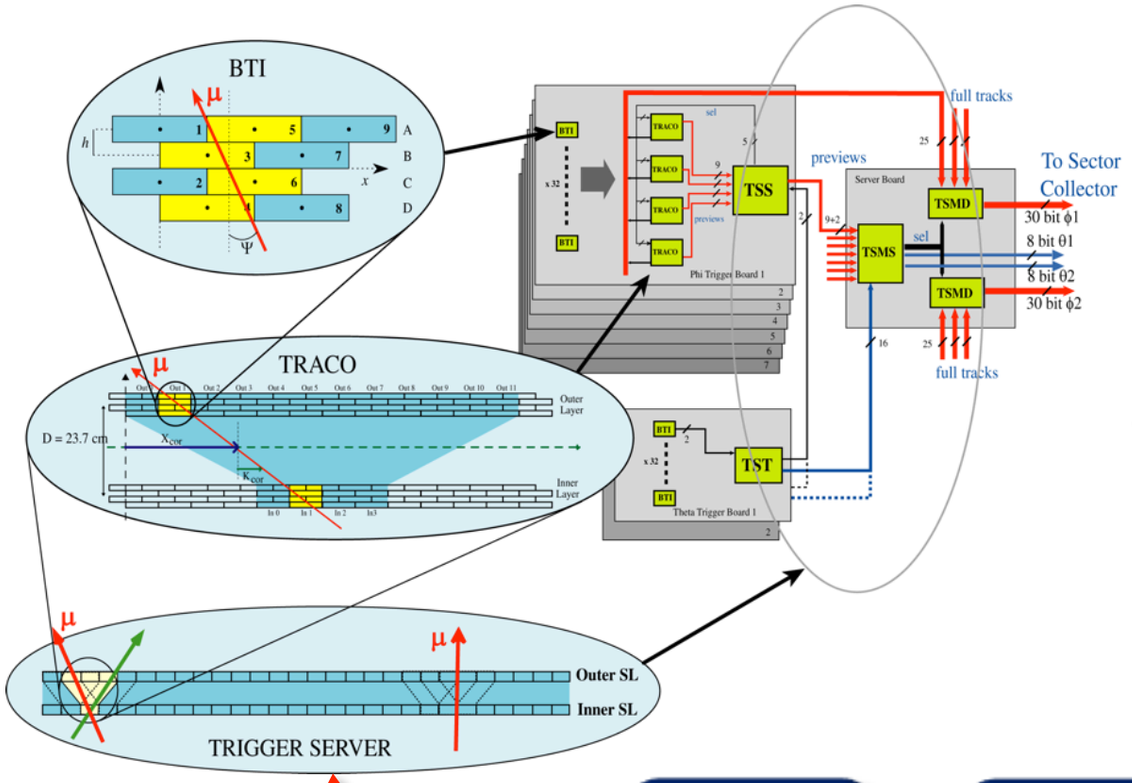
μ-elec. ↔ common ALICE architecture

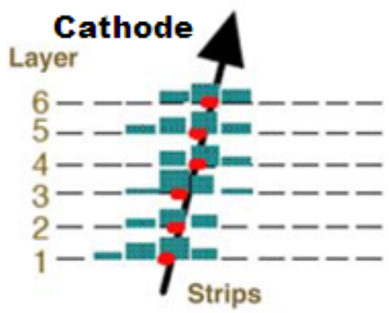


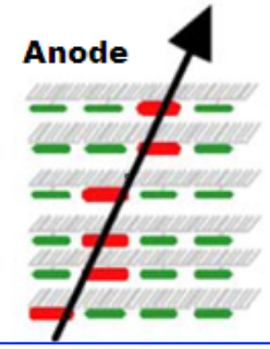
GBT: GigaBit Transceiver (optical)

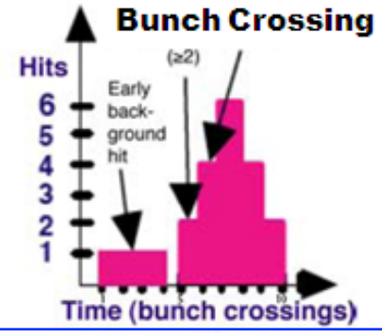

CMS

(current) CMS μ-trigger system







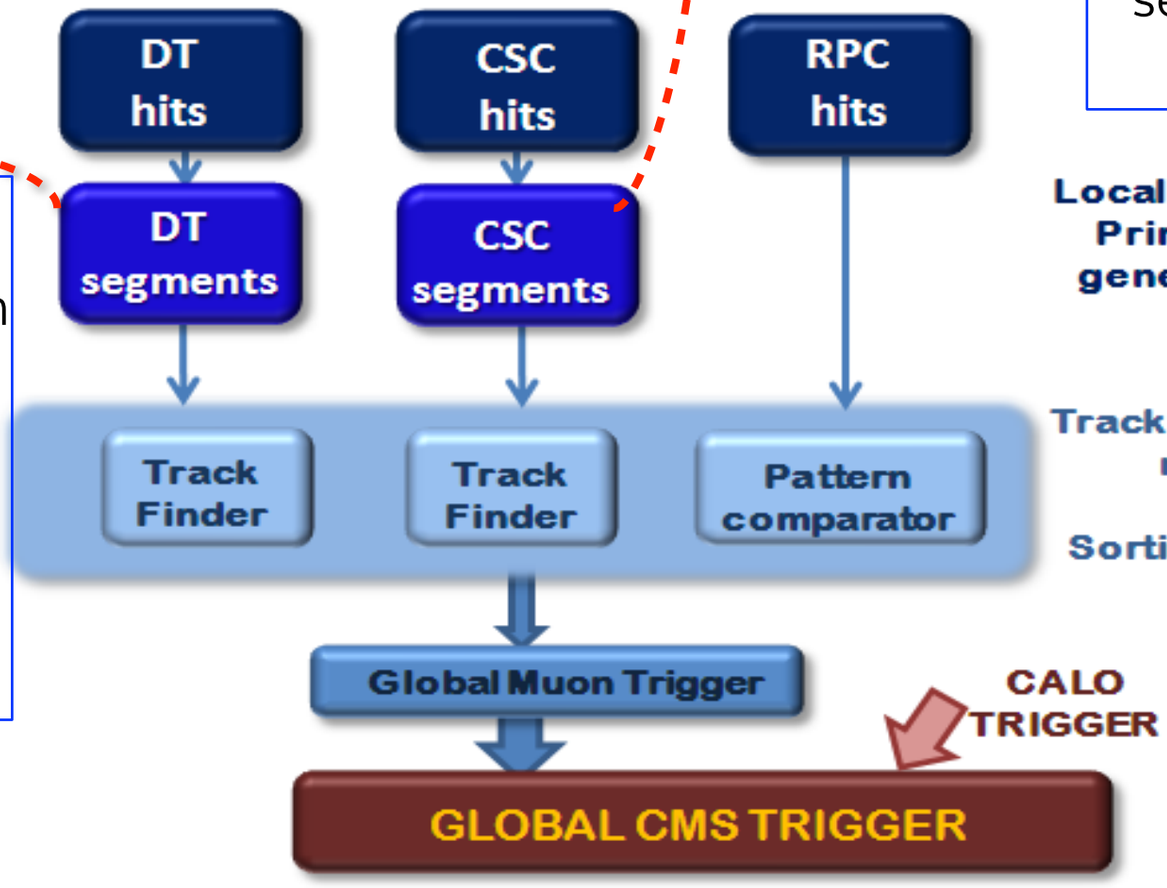


CSC up to 2 local charged tracks built from cathode and anode segments are sent per Bunch-X

RPC spatial coincidence of hits in several layers are compared with predefined patterns

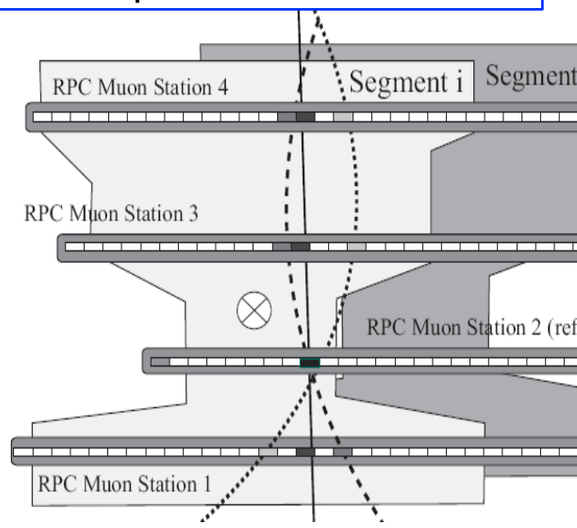
Drift Tube

Segment built through **track-fitting** and further correlation among Super-layers → p_T



Local Trigger Primitive generation

Track Finder, patte matching & Sorting Algorithm



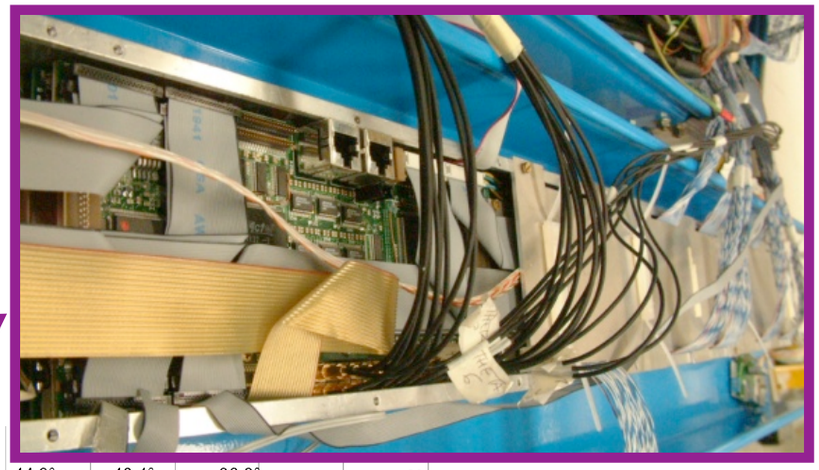
Phase-2 μ-trigger / elec. upgrade

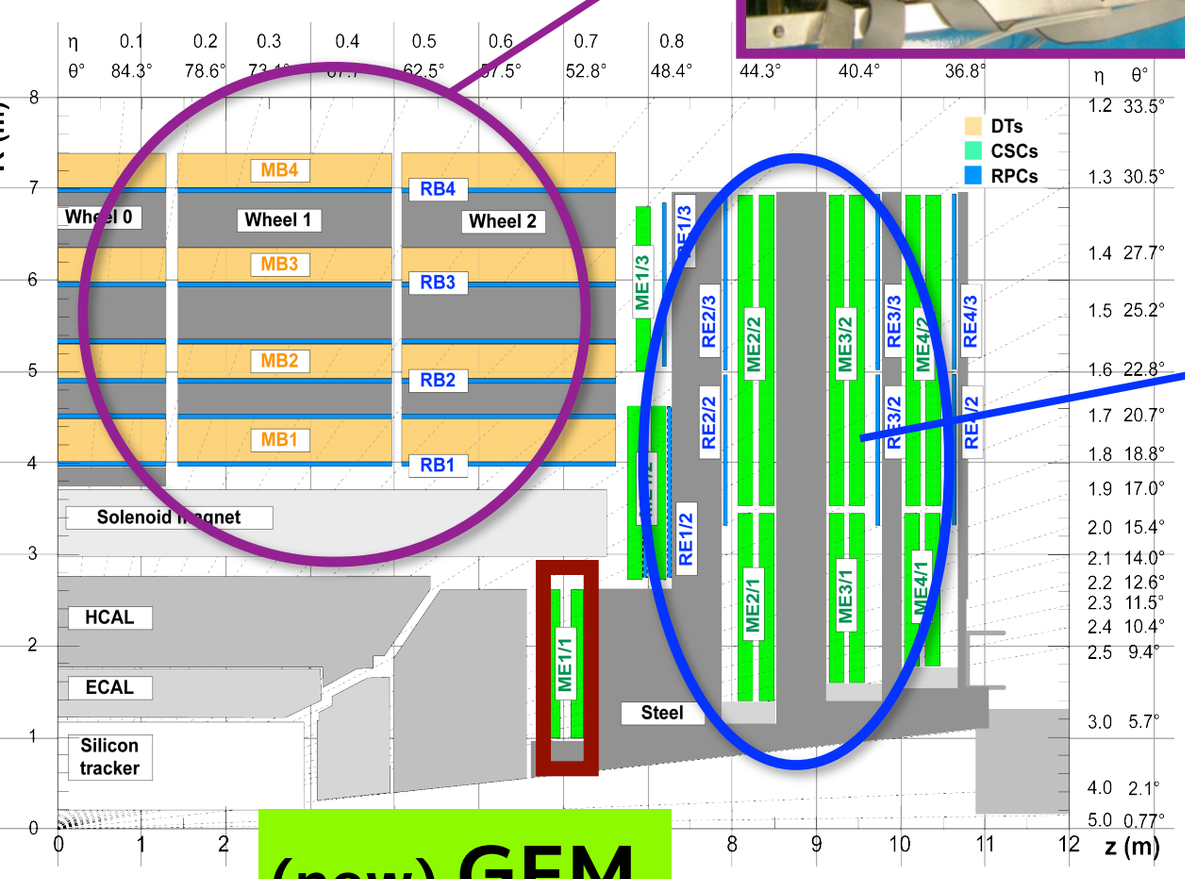
"tracking trigger" impacts LVL1 latency (and rate)

Latency : 3 μs → 10 μs

Rate : 100 kHz → 1 MHz

① replacement of the **Drift Tubes Mini-crates**





(new) **GEM**

② **CSC-GEM μ-trigger**

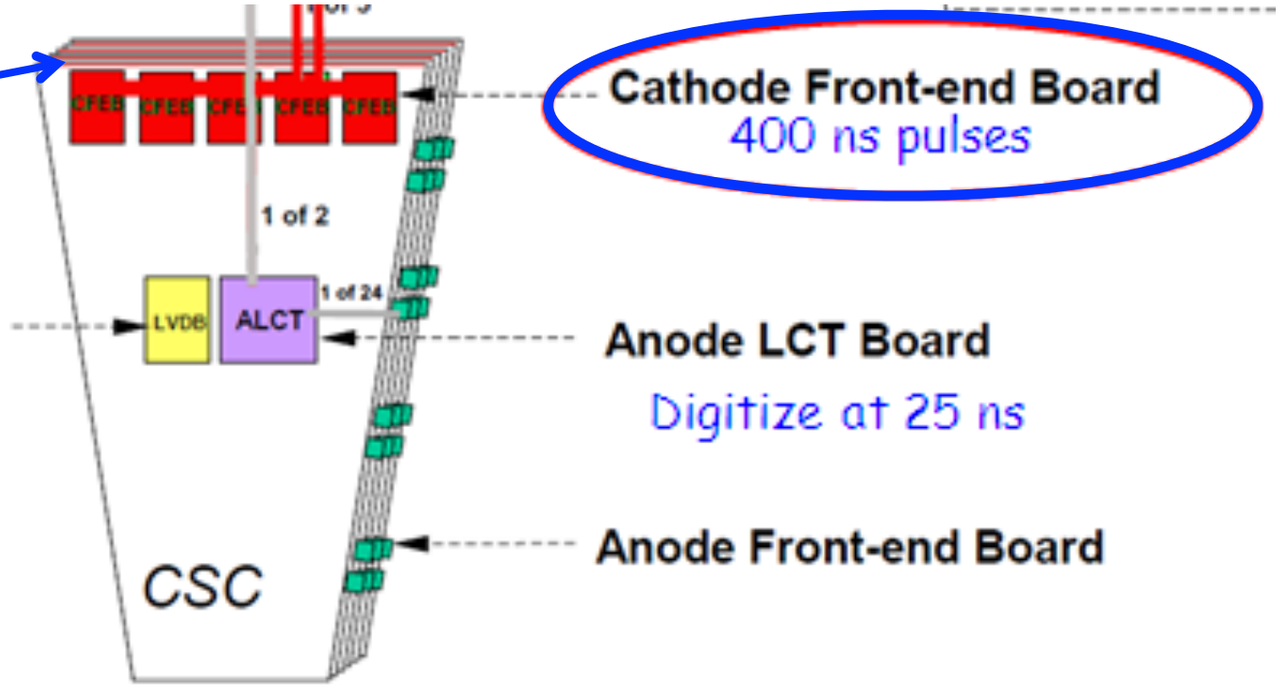
bending-angle

→ improved p_T resolution

(3) **DCFEB** (Digital Cathode Front End Boards) in the **CSC**

chambers to be replaced

(if latency > 10μsec)

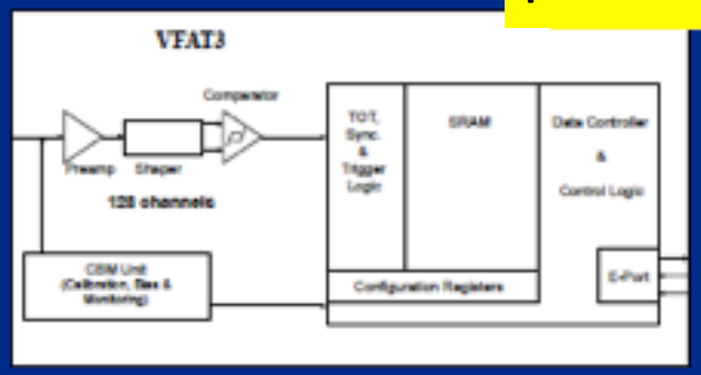


Material colle alk #4 on trigger and electronics

The CMS GEM Electronics System

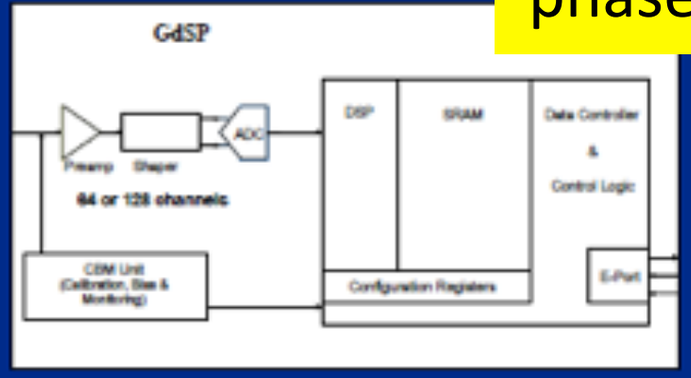
VFAT3

phase-1



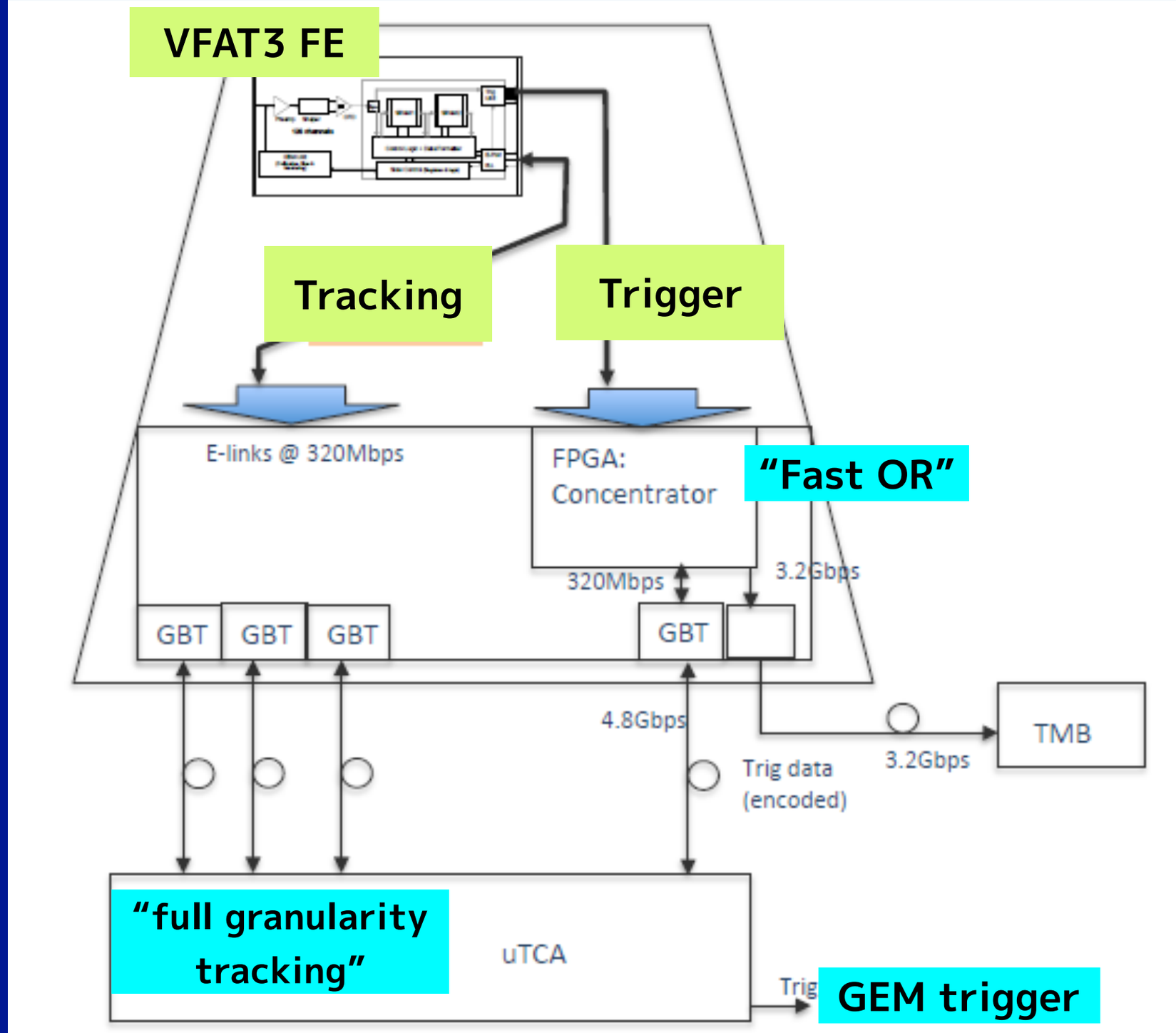
GdSP

phase-2



VFAT3 chosen as baseline for GEM (phase-1)

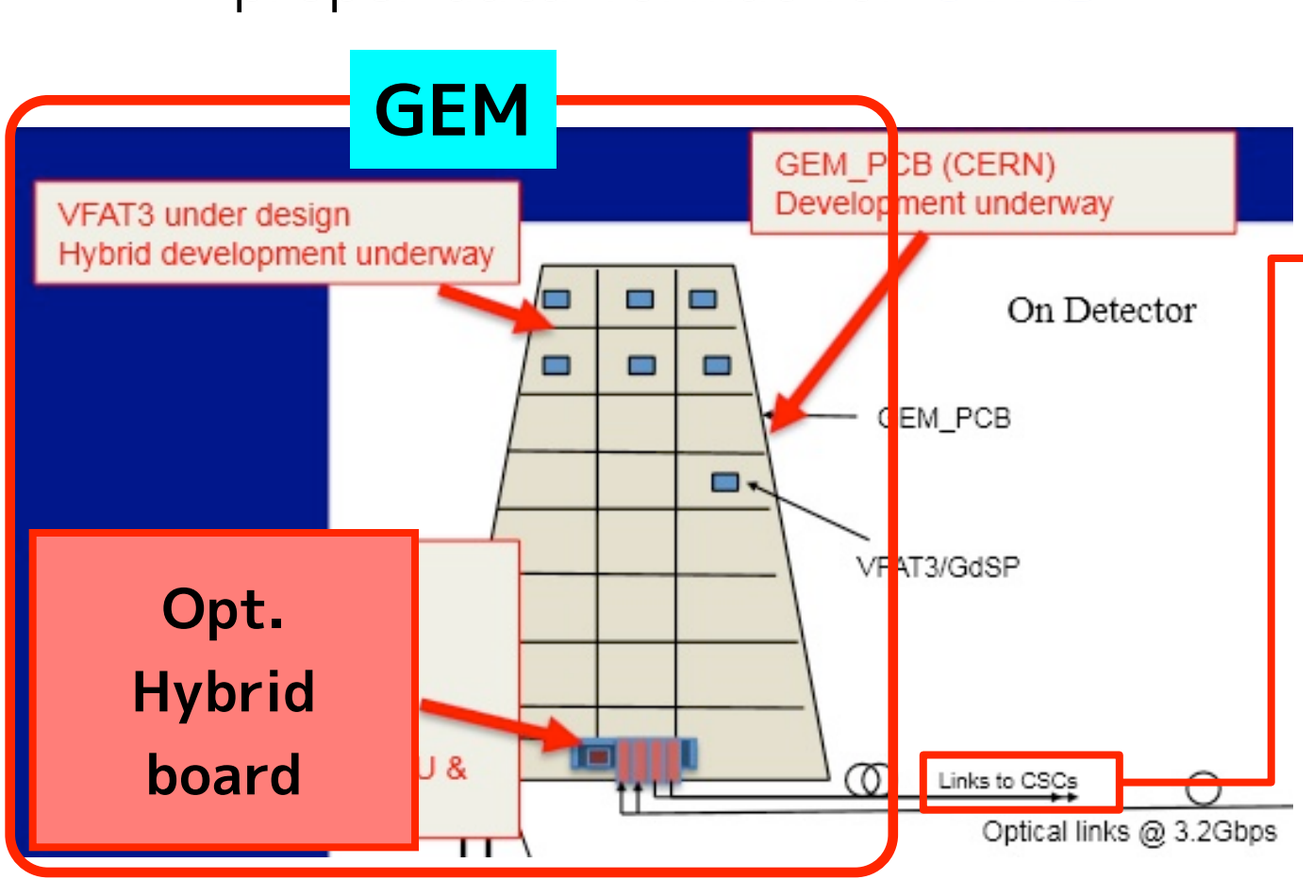
GdSP may be ideal for a number of **Phase-2 upgrades**

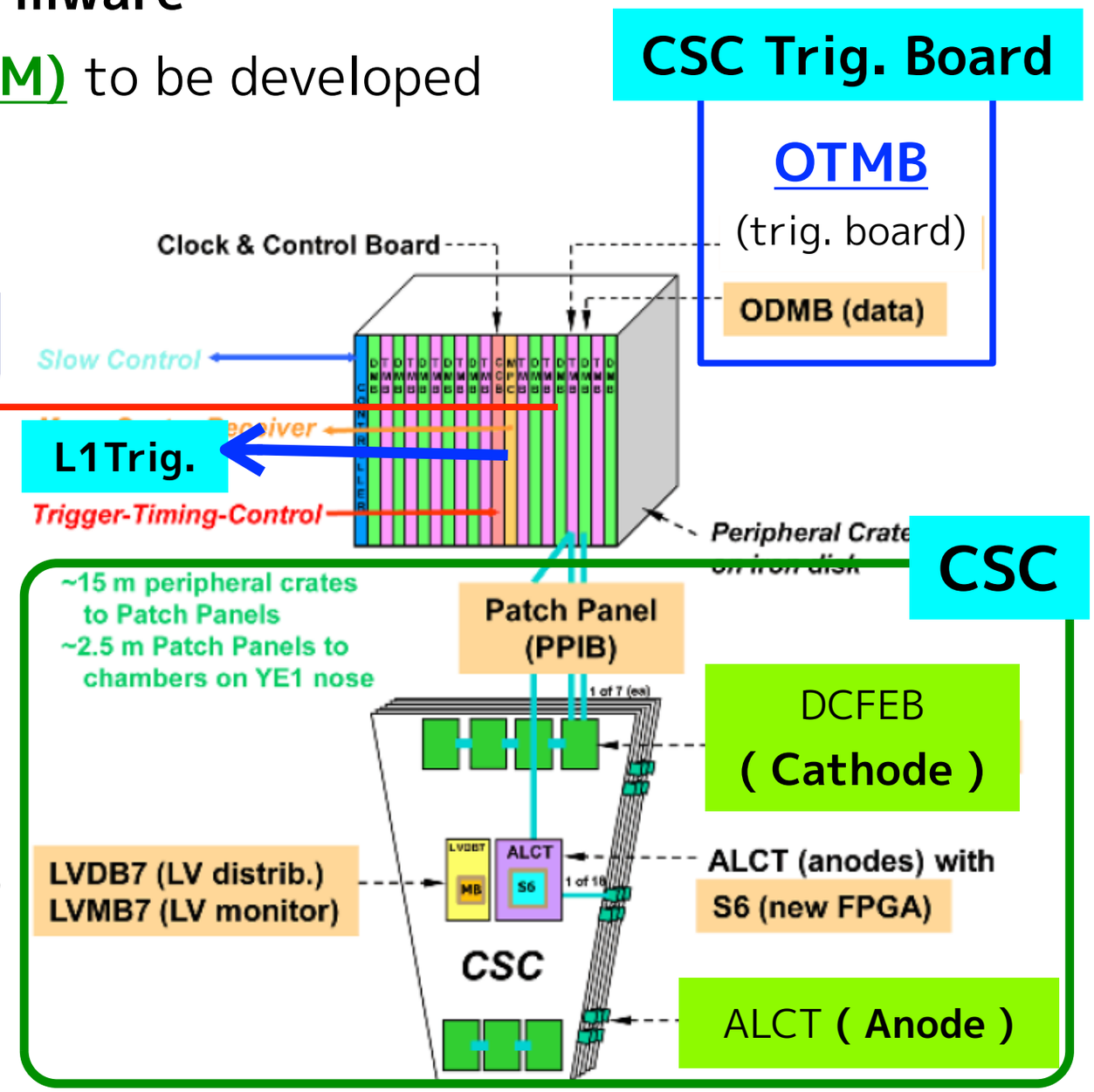


Combined Trigger : GEM-CSC

- **GEM and CSC data processed in a common unit**
  - send **GEM data** **to** **OTMB** **(CSC** Trigger Board) through opt.-hybrid board
  - no changes in CSC scheme needed
- **Requirements**
  - GEM-CSC trigger algorithm in **OTMB** **firmware**
  - firmware for Opt.-hybrid board **(for GEM)** to be developed
    → proper data-format for **OTMB**

cost effective





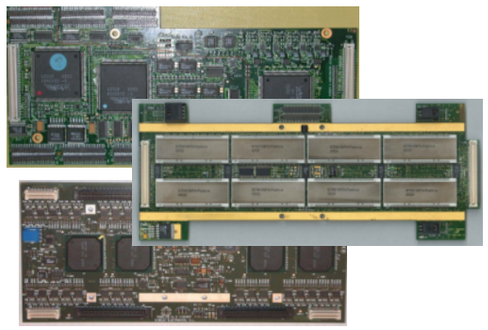
Upgrade of DT on-chamber electronics

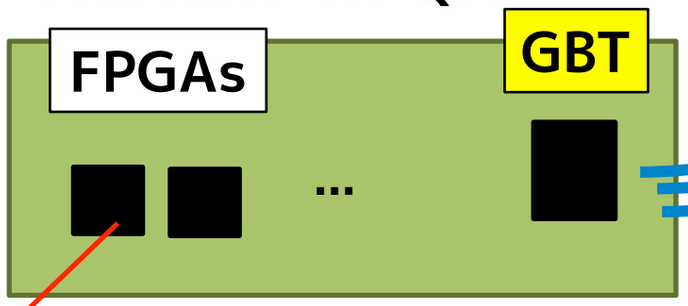
Phase2 Mini-crates : DT

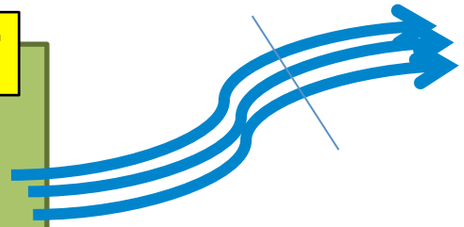
R&D started

- more radiation tolerant / 1MHz readout / improve reliability / …
- **time digitization** & Digital info. sent through **high-speed** optical link
- **Complexity is brought to the counting room**

4 TYPES OF BOARDS → ONE NEW UNIQUE







High speed optical links

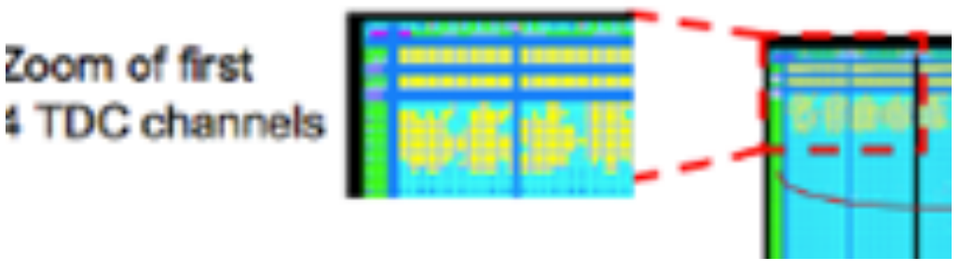
Trigger and Readout electronics

- New electronics in counting room
- **uTCA** technology
- **Trigger primitive algorithms in FPGAs**

Radiation tolerant FPGAs

(MicroSemi ProAsic for prototyping)

time-digitization of all incoming hits (~1 ns)

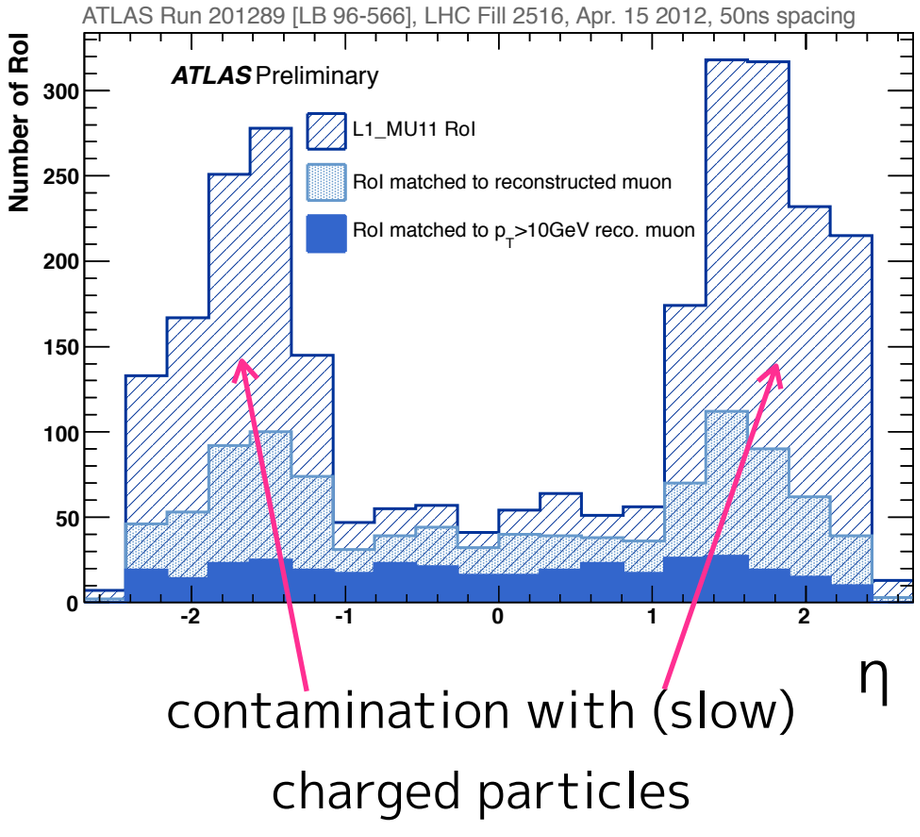


* Readout at **1 MHz and 20μsec** latency

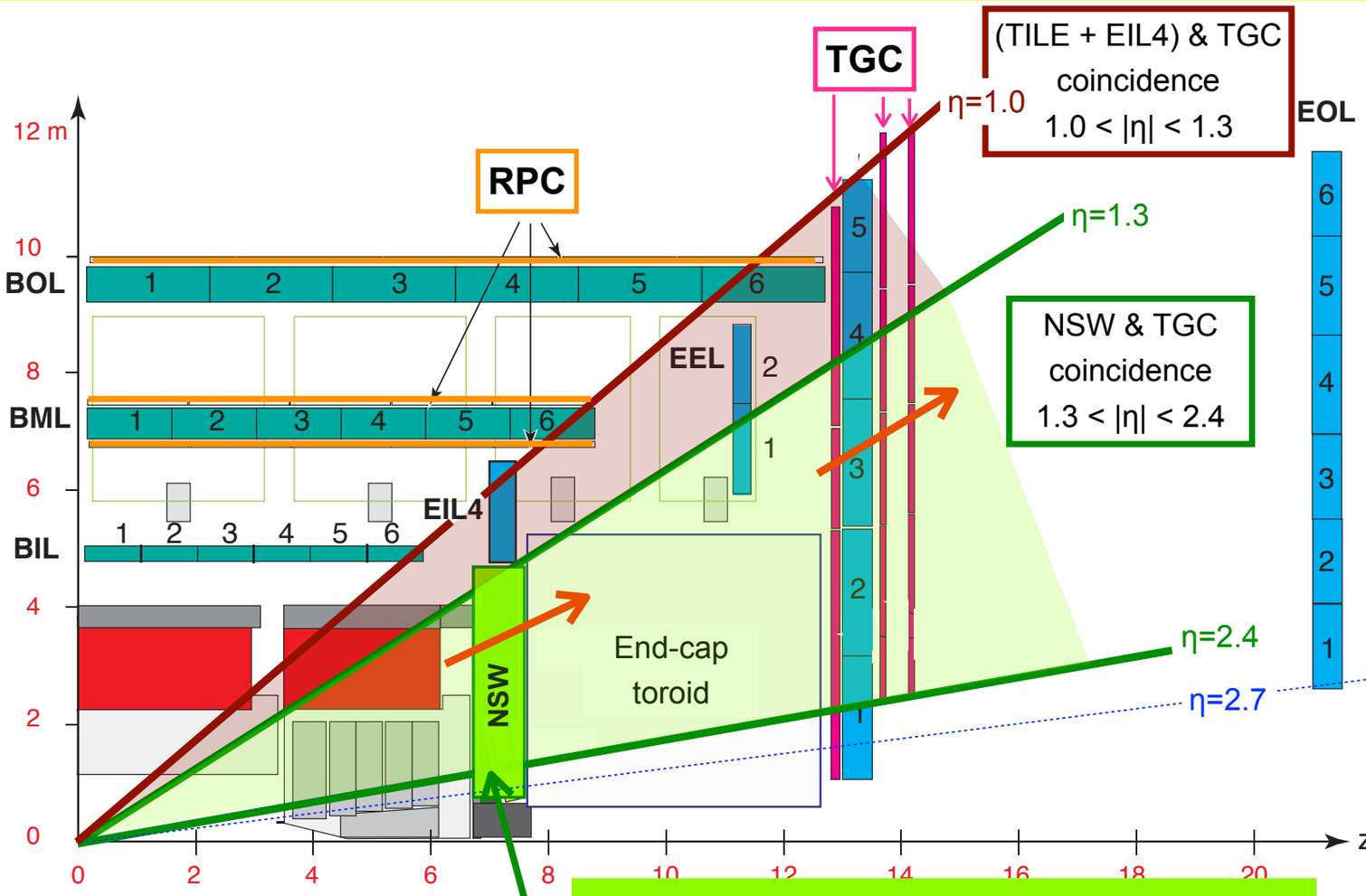
* DT-Trigger primitive generation:
  - **maximum chamber resolution**
    → **better p_T resolution**

ATLAS
EXPERIMENT

ph.2 μ-upgrade - trigger & R/O



contamination with (slow) charged particles



σ(angle)= 1mrad for Trigger

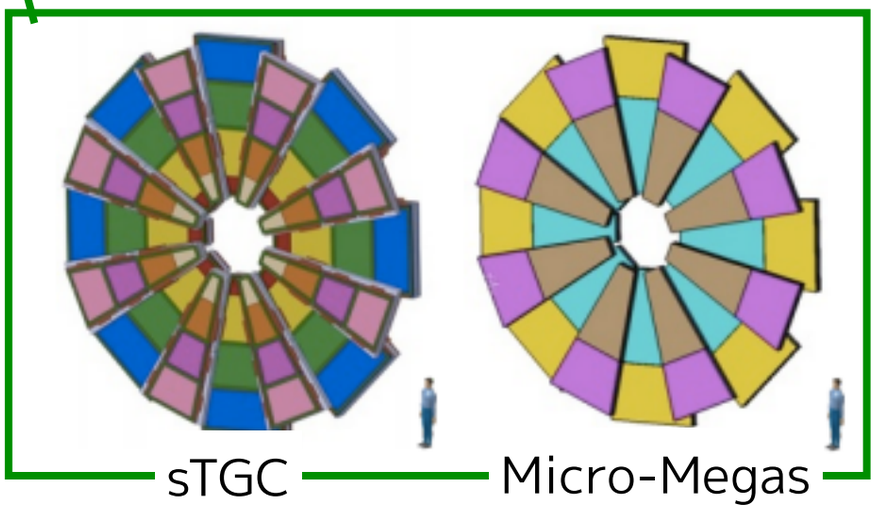
L0-L1 (500kHz → 200kHz) trigger scheme

20μsec. L1-latency

Precision Tracker (**MDT**) to **Hardware** Trigger
→ sharp turn-on with **better p_T resolution**

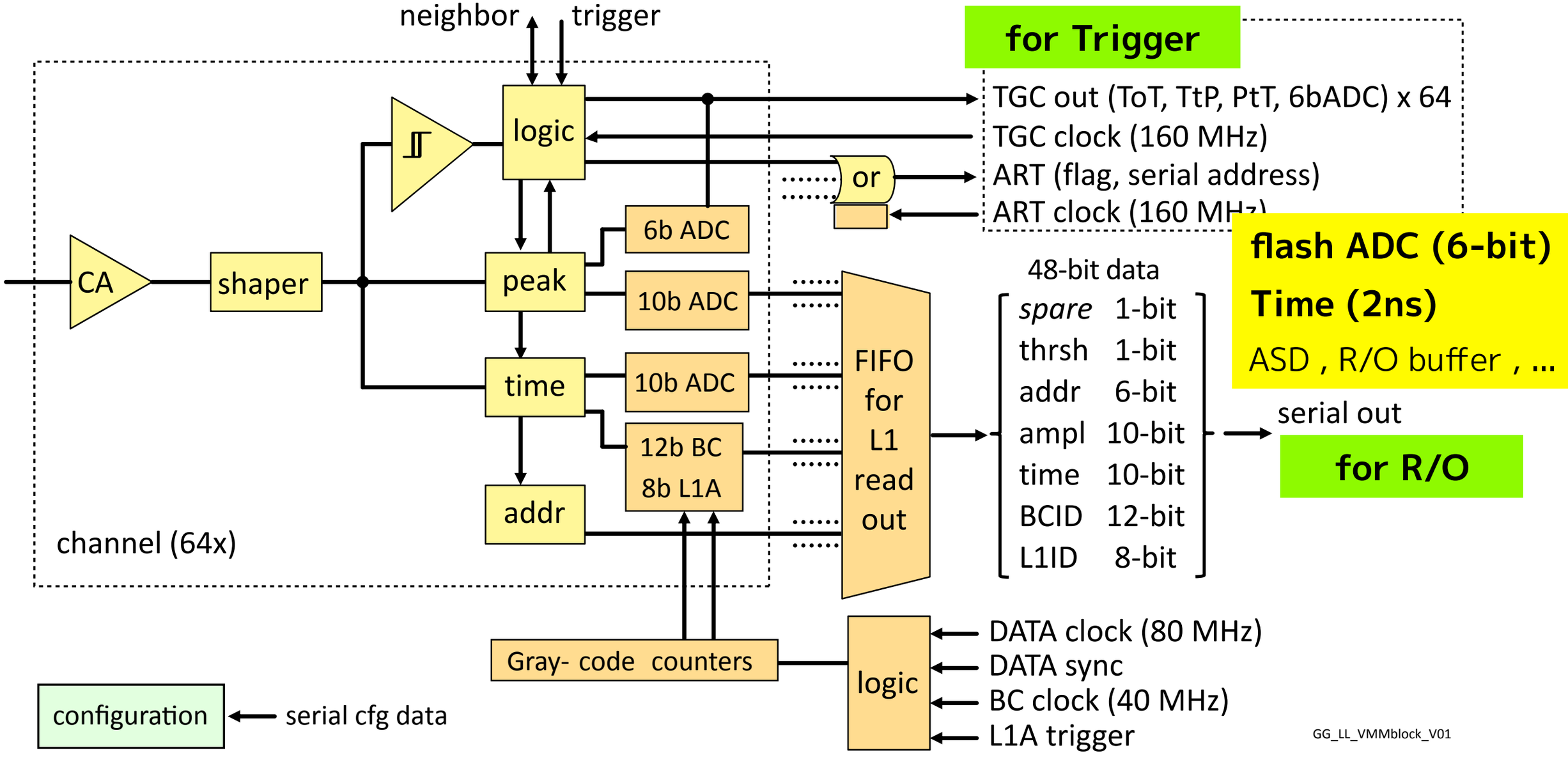
replace **TGC / RPC elec. (latency)**

New Small-Wheel (NSW)



New-SW : Front-End ASIC

common ASIC for sTGC & Micro-Megas : VMM2

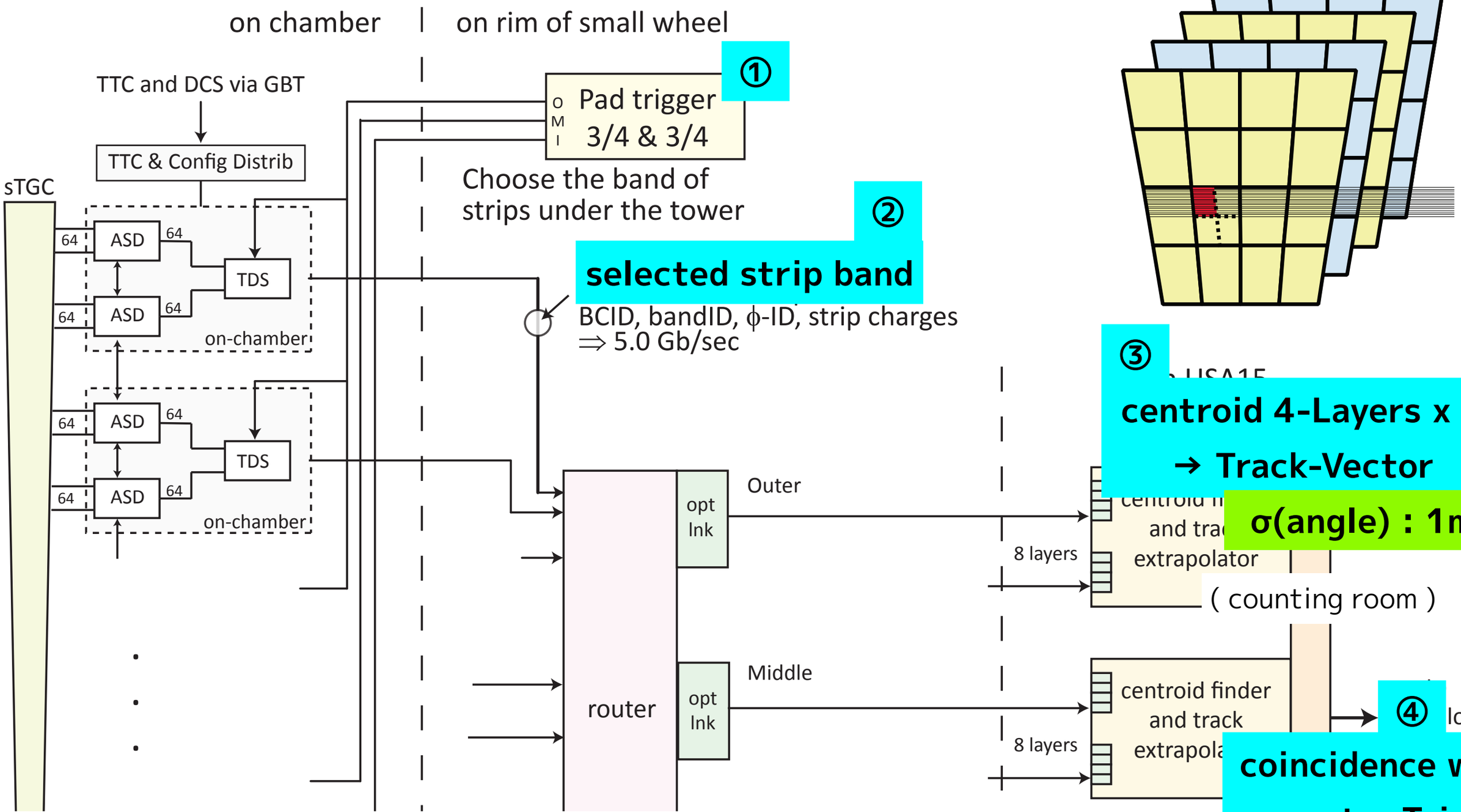


64ch. per chip , 512mW/ch. , ~40k chips

track-vector processor for trigger

the same ATCA cards for both sTGC & MM

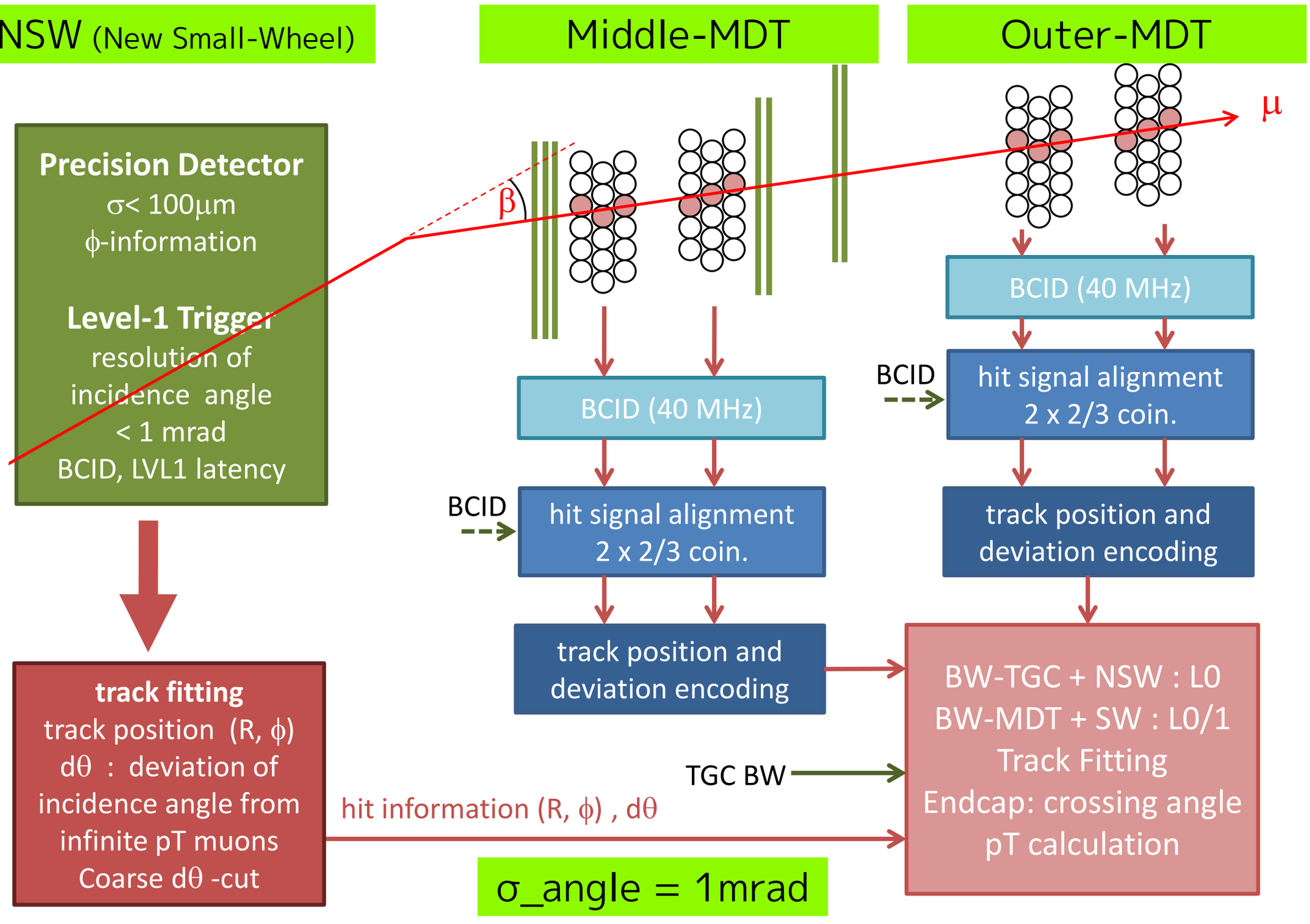
different firmware



sTGC quadruplet

strips	ASDs	TDS's	routers	links	centroid finders
~1030	18	9	1	3	3 (for 8 layers)

ph.2 μ-trigger scheme : **MDT as HW trig.**

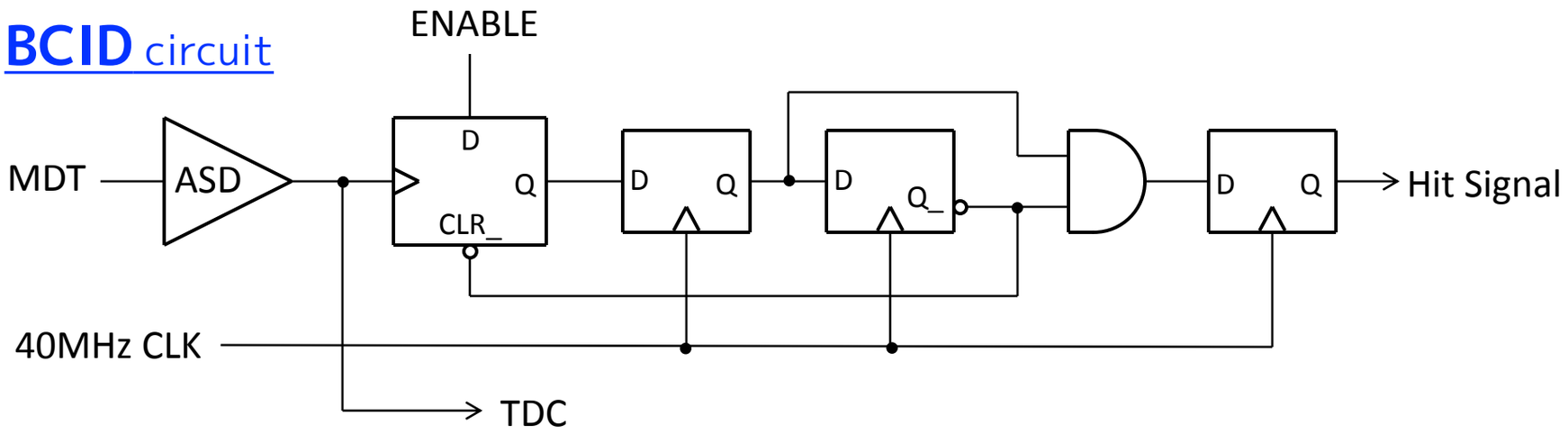


measure drift-time with a precision of LHC-clock (or 0.5 tick)

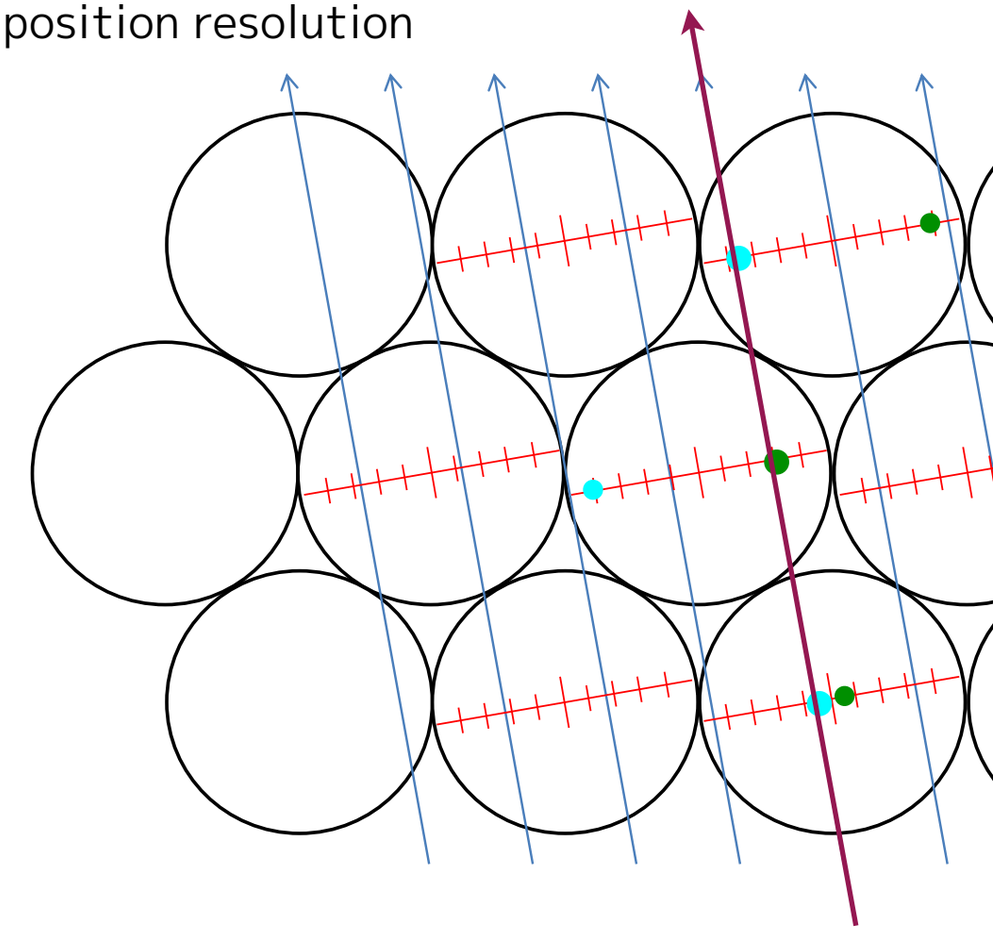
→ deduce angle at each 3-stations → p_T

Drift-Tube as Hardware-Trigger

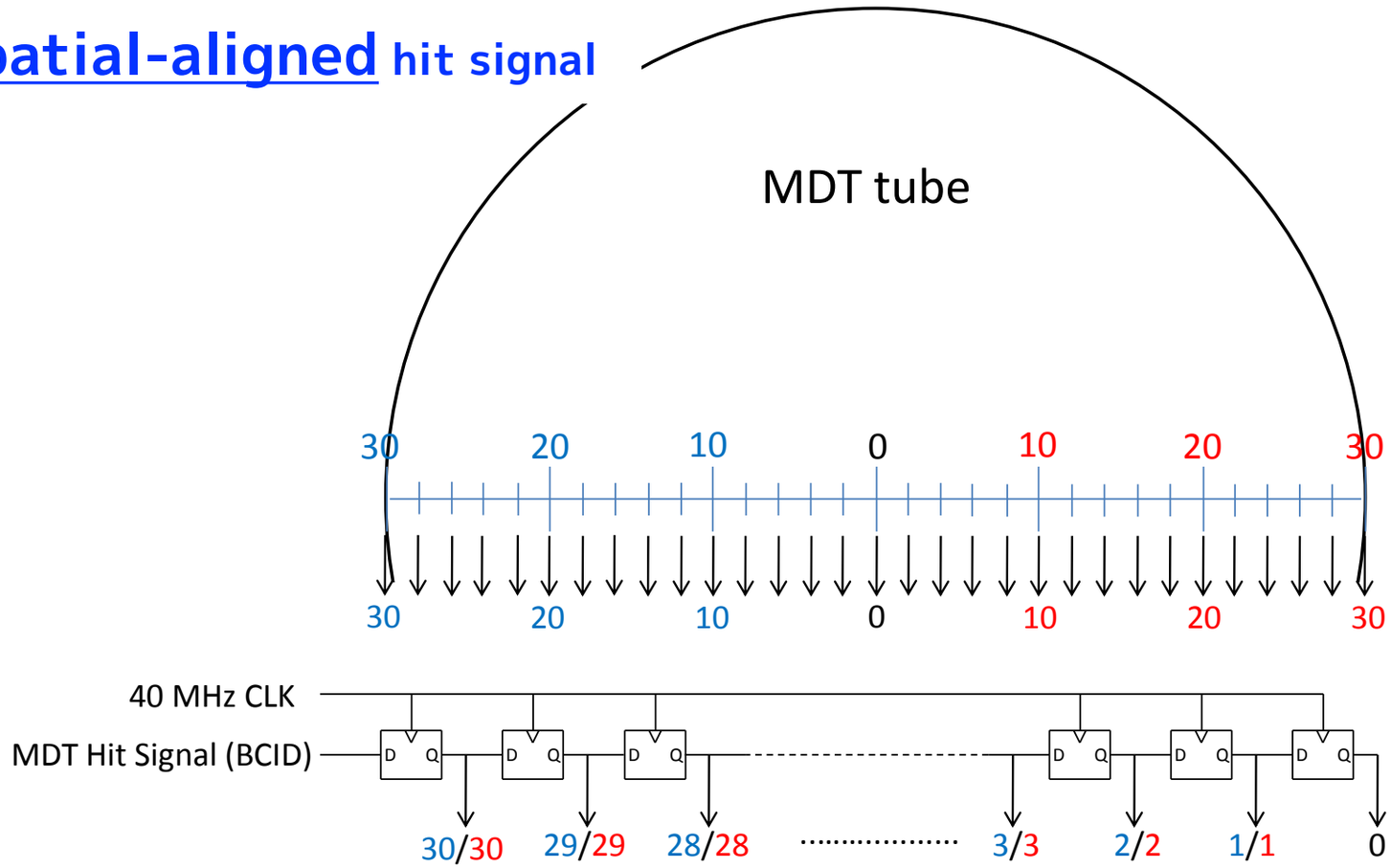
BCID circuit



Leading edges of the hit signals are detected in every 25ns, ~ 0.5mm position resolution



Spatial-aligned hit signal



31 stage shift-register

Summary

Concepts

- common electronics **across multi sub-systems**
- as simple as possible in the pit, **complexities brought to outside**

Technologies

- high-speed optical links (e.g. **GBT**)
- radiation hard Front-End ASICs
- FPGA with high-density serial links & performance
- ATCA (or μTCA) cards

high-rate readout

high-performance μ-trigger → **physics !!**

backup

[Detector systems]

(a) conceptual part

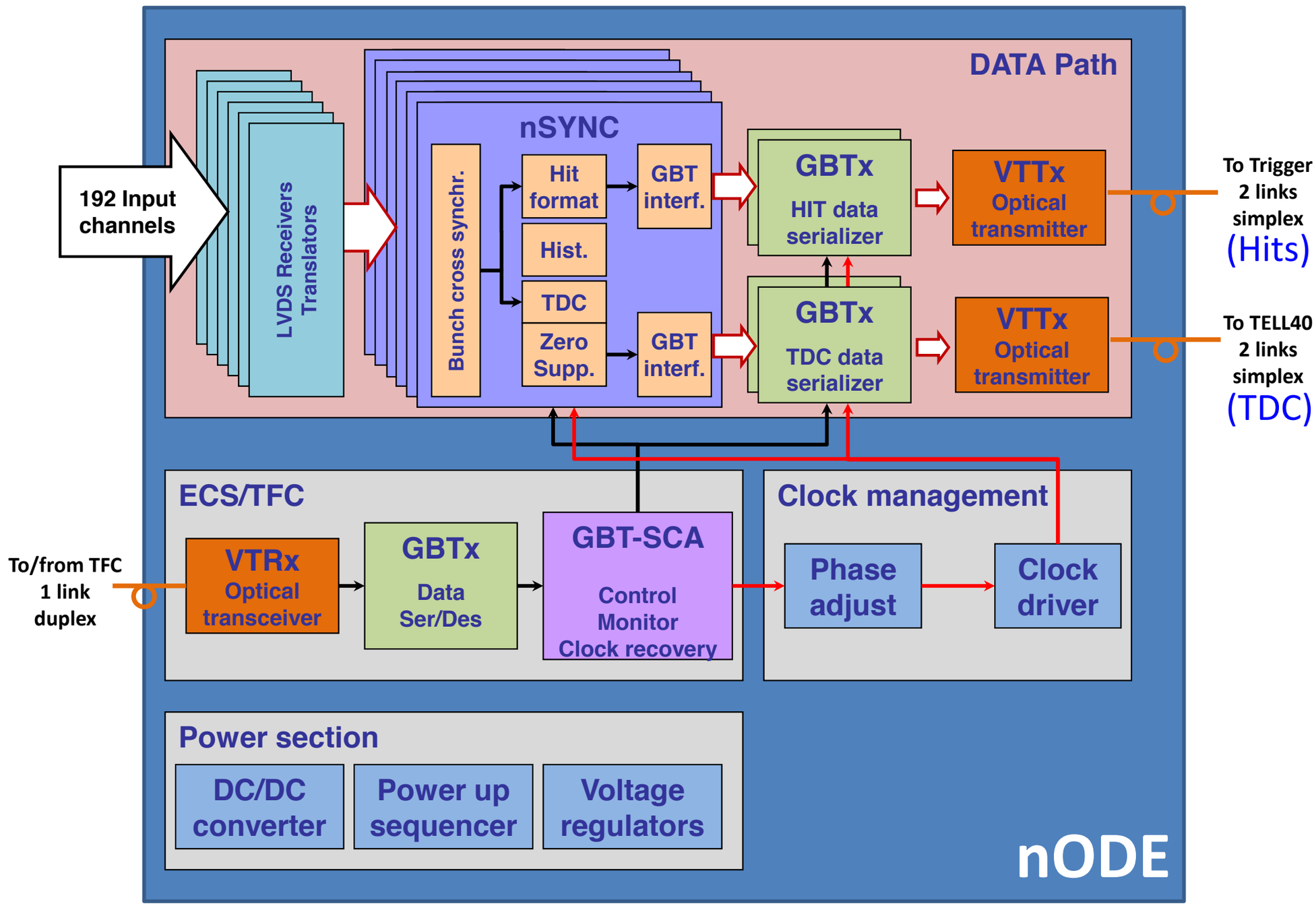
- High level **motivation** for upgrades: longevity
- Important performance **requirements** to achieve the HL-LHC physics program

(b) practical & technical part

- **How to achieve** to the expected performance
- Targeted R&D needs
- technology prospect (including cost considerations)
- ongoing activities & further actions

LHCb - nODE (new Off Detector Elec.)

I may skip this slide … check with Alessandro



6 optical links required / nODE