TOF Upgrade: (few) updates
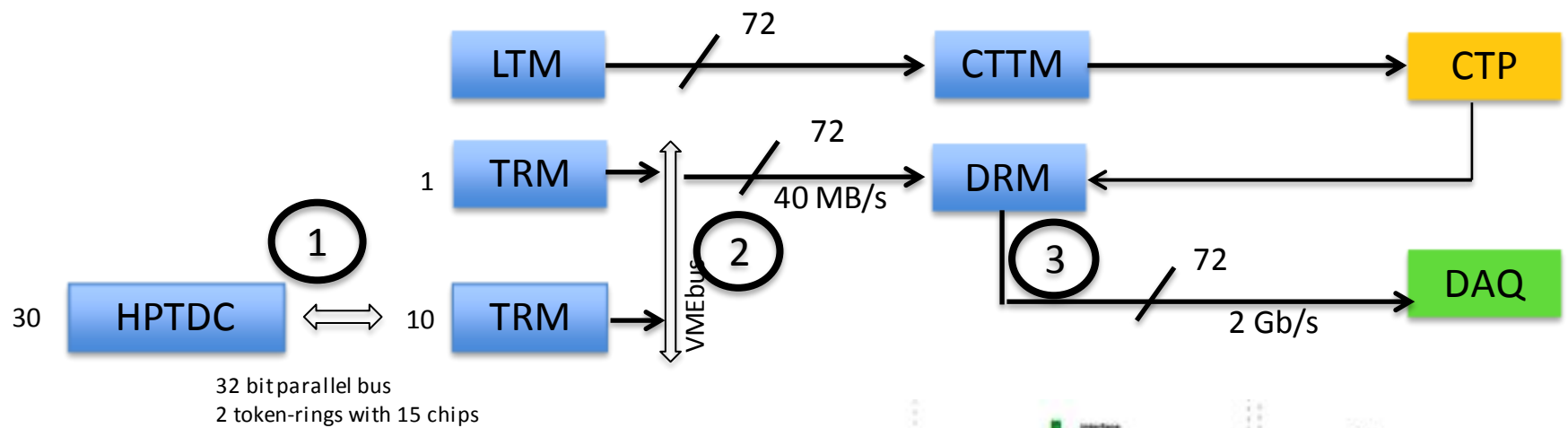
Background docs:
- TOF upgrade (at LoI EB, July 2012)
https://indico.cern.ch/getFile.py/access?contribId=5&resId=0&materialId=slides&confId=200188
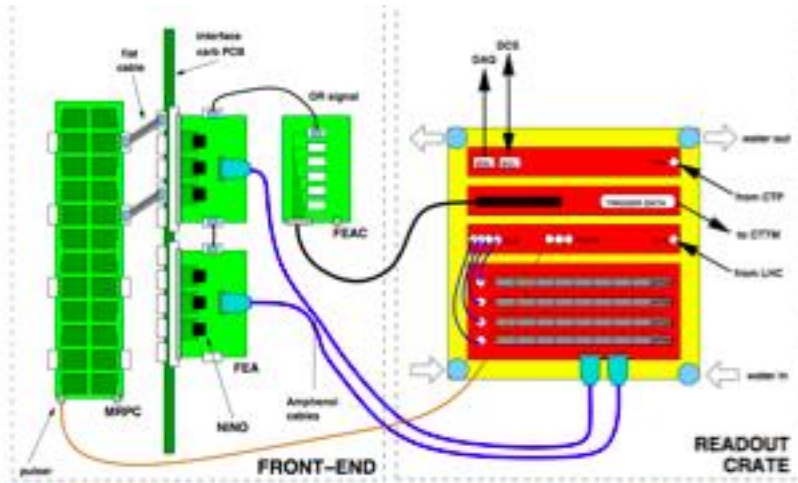
- TOF upgrade (March miniweek)
https://indico.cern.ch/getFile.py/access?contribId=8&resId=0&materialId=slides&confId=241648

P. Antonioli / INFN Bologna

LTM → (72) → CTTM → CTP

TRM (1) → [VMEbus] (72) → DRM ← CTP
40 MB/s

(1)

HPTDC (30) ⟷ TRM (10) → [VMEbus]

(2)

(3) → (72) → DAQ
2 Gb/s

32 bit parallel bus
2 token-rings with 15 chips

Three stages readout:
① from HPTDC to TRM buffers
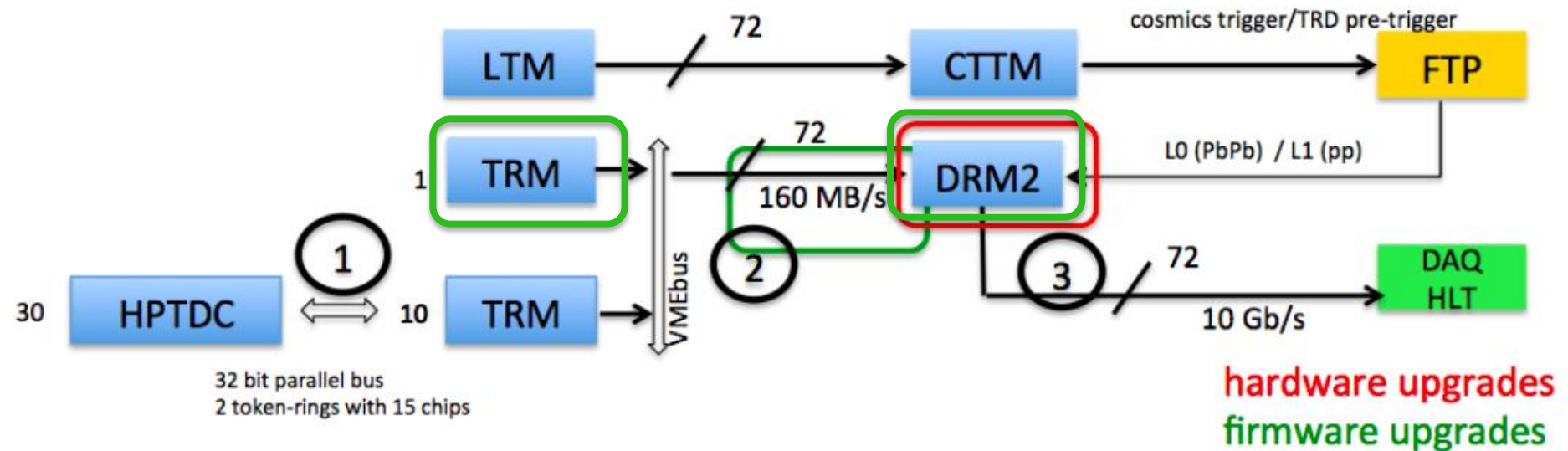② from TRM to DRM
③ from DRM to DAQ

9U VME card (6U width)
water-cooled
VME64X (not completely
standard compliant)

Where we want to intervene with upgrade?

- minimal action principle approach thanks to already satisfactory rates (60 KHz)
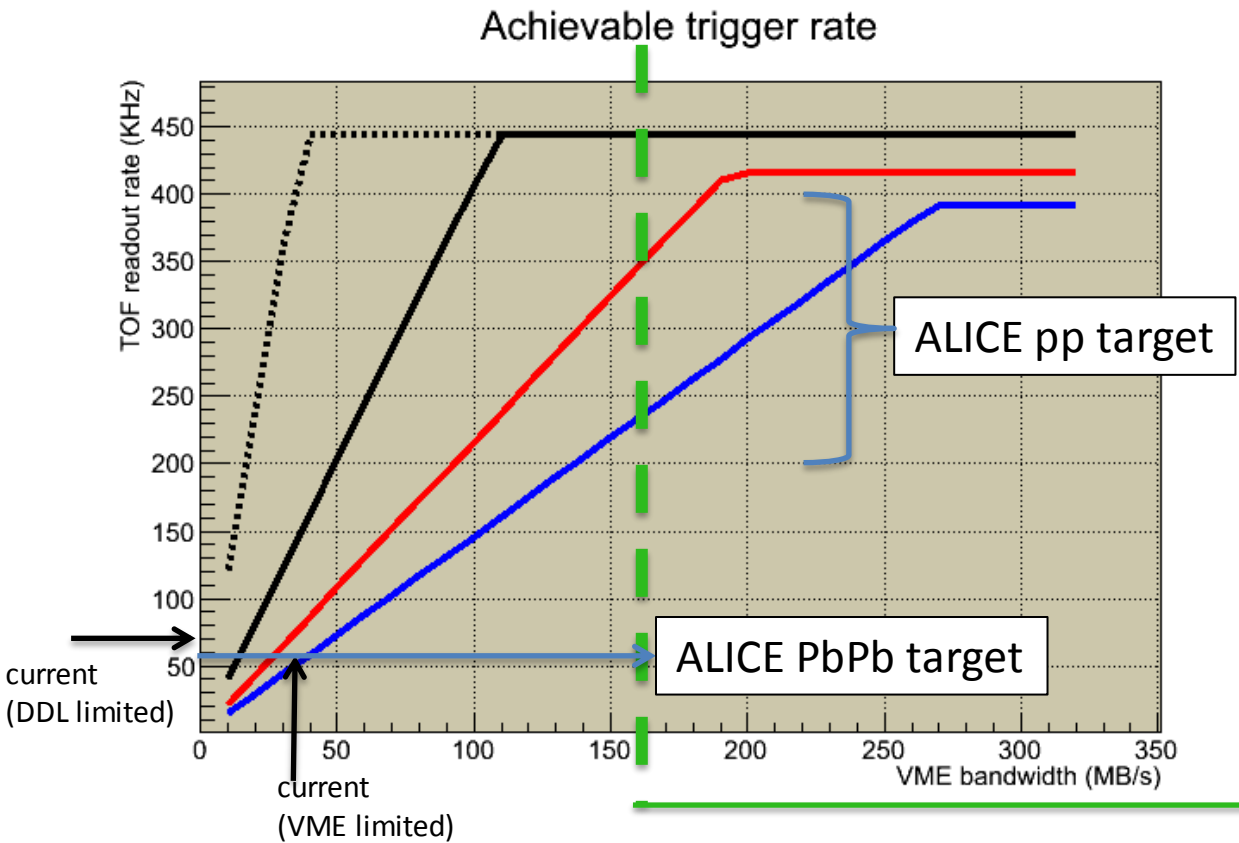- bottlenecks analysis done in 2012 preparing LoI

- DRM links towards ALICE world: TTC, DDL, busy
- Note 1) TOF uses also high-quality clock as additional link: DRM bridges clock domains
- Note 2) on L0: we can work with a L0 (at 900 ns) or with a cleaner L1 (at 5 μs)

What we currently have on DRM
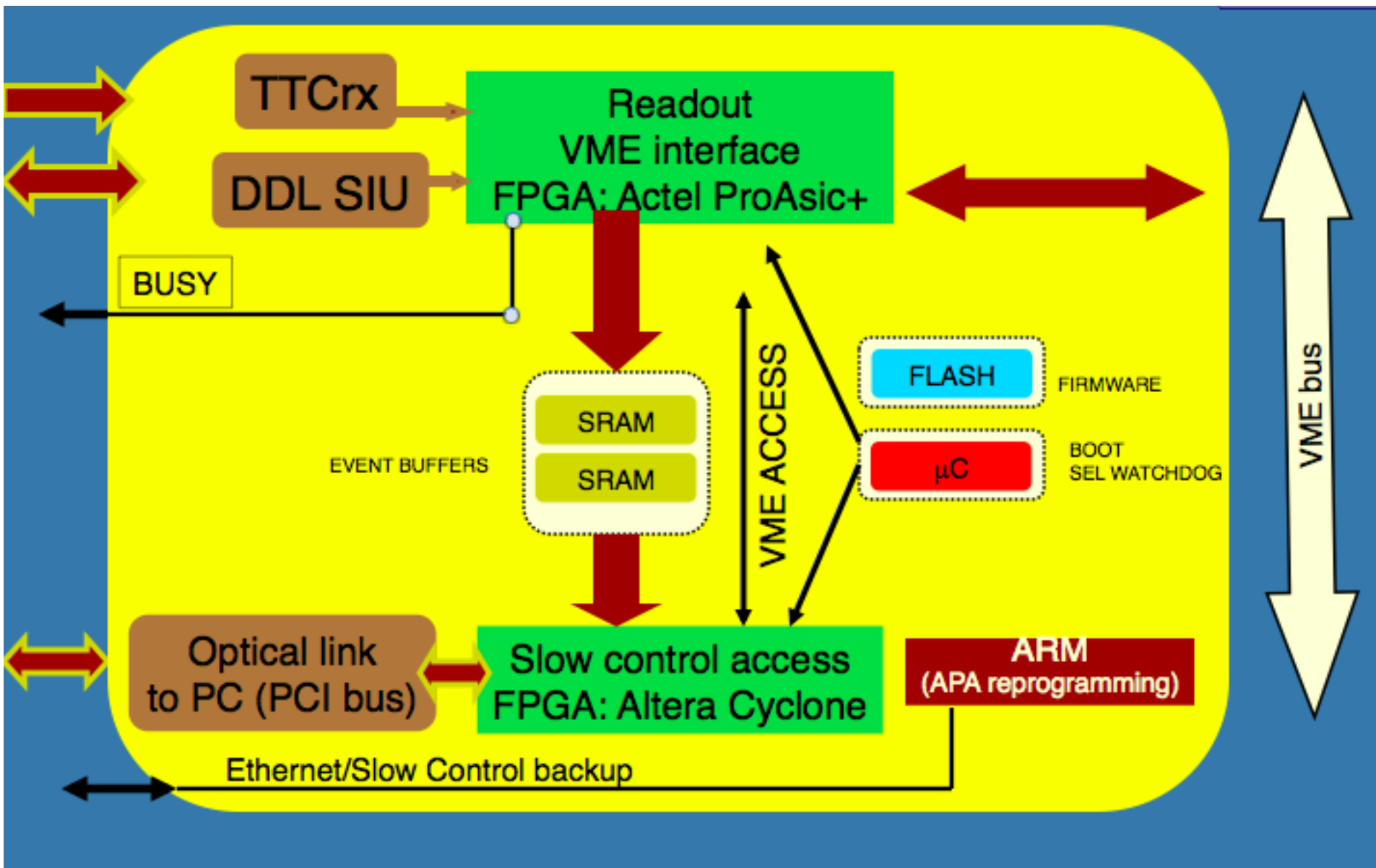
DRM-2: improve readout rate to fit ALICE after LS2

Achievable trigger rate

4000 hit/event @TOF LHC11h
1500 hit/event @TOF LHC10h
50 hit/event @TOF MB pp
--- with data format optimization

Note in upgrade scenario
we will have a minimum
bias trigger, so close to
LHC10h (+ energy increase)

2eSST@160 MB/s

TRM-DRM firmware to be improved to:
- support 2eSST VME transfers (likely at 160 MB/s)
- reduced data size (higher compression of header/trailer)
HPTDC test at high input trigger rate

2013

Development under way.

Test setup facilities at Bologna and CERN.

Hopefully rate achieved will be reported in TDR by August
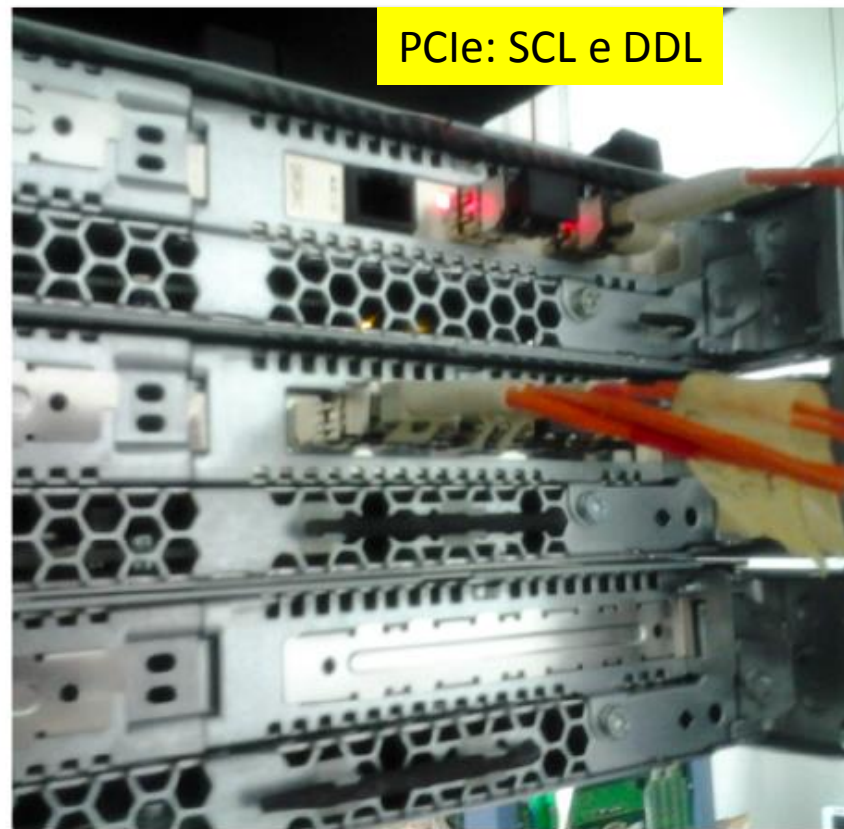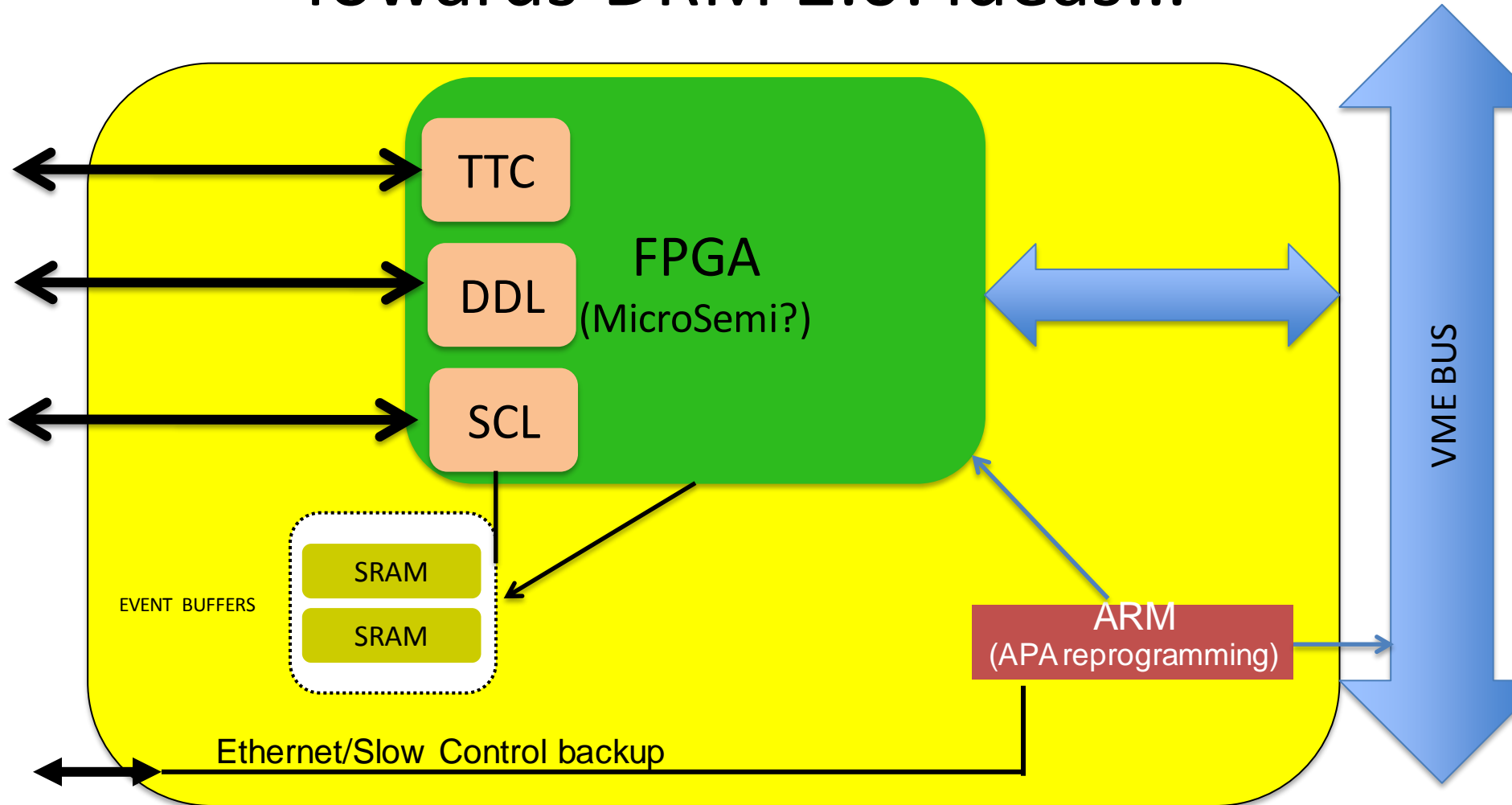
Critical month: June

bre

PCIe: SCL e DDL

Fig. 3: Dettagli setup di test in laboratorio a Bologna: minicrate VME con sistema TTC e scheda DRM su banco (sinistra); interfacce PCIe per link DDL e SlowControl.

Towards DRM 2.0: ideas…

FPGA
(MicroSemi?)

TTC

DDL

SCL

EVENT BUFFERS

SRAM

SRAM

ARM
(APA reprogramming)
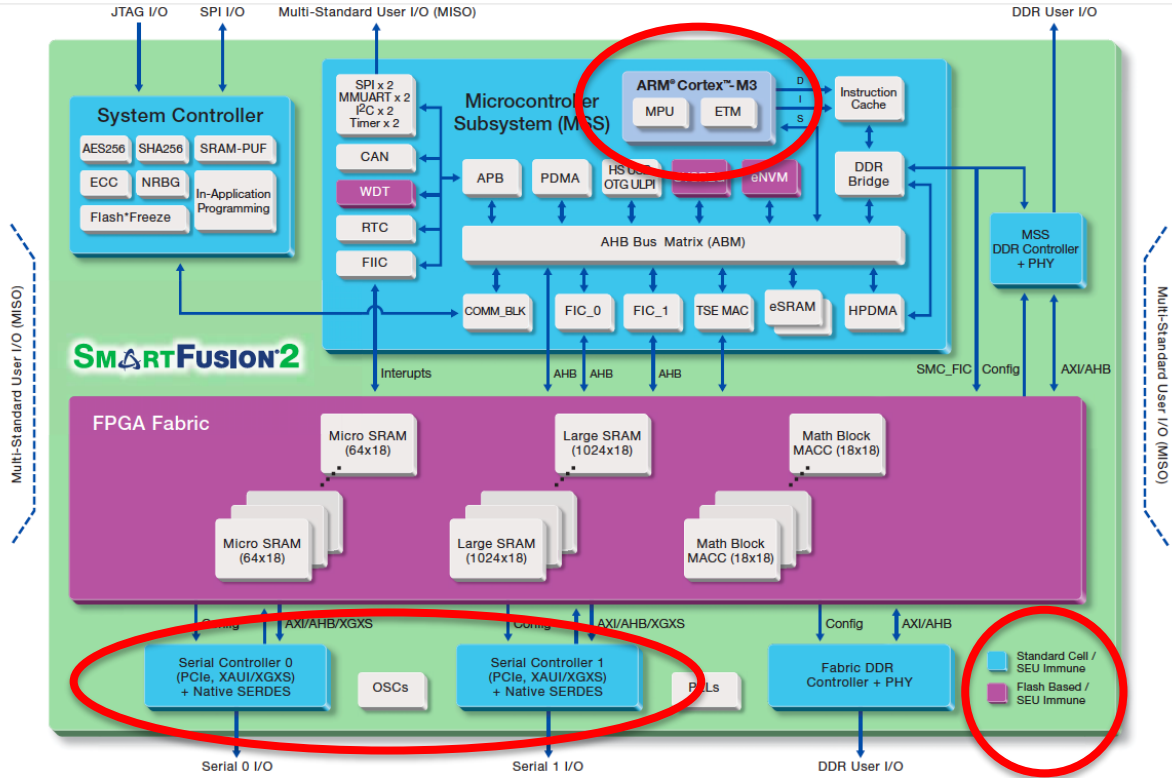
VME BUS

Ethernet/Slow Control backup

- DAQ link?   → DDL2 or DDL3??
- TTC-PON link? → specifications needed!
- FPGA choice + IP cores for TTC/DDL

Verso DRM 2.0

Current main FPGA Candidate for DRM 2.0 (and for CRU for ITS/TPC)

- high speed serial links?
- SEU immune (Flash based)
- ARM processor embedded
- 2013 radiation test (ALICE DAQ group + Wigner)

RELIABILITY

Microsemi's programmable logic solutions are used extensively in military, aviation and space applications due to their high reliability and protection against single event upset (SEU) occurrences, which can cause binary bits to change state and corrupt data and cause hardware malfunction. Industrial and medical safety markets are also requiring SEU protection as vital requirement for their applications.

SmartFusion2 architecture is designed to target reliability applications with the following features:

- SEU immune zero FIT flash FPGA configuration cells
- SEU Protected Memories: eSRAMs, DDR Bridges (MSS, MDDR, FDDR), Instruction Cache, Ethernet, CAN and USB Buffers, PCIe, MMUART and SPI FIFOs
- Hard 667 mbps DDR2/3 controllers with SECDED (aka ECC or EDAC) protection

LOW POWER

.. and doubts (including trigger **from** TOF)

- replace TTC & DDL with a GBT link to CRU (then... 72 CRU to buy???)

- do we really need DRM 2.0? I'm increasingly leaning to keep current DRM!!

- Trigger (Eugenio S. to lead here)
  - make clarity about any 'pre-trigger' thing for TRD involving TOF
  - the UPC dilemma
  - cosmics in general

Funding / planning / etc.

- Funding
- Manpower/institutions
- Connection with T0

Time schedule:
2013: FW development with current cards
2014: prototype development/test
2015: finalize specs + tendering/procurement
2016: start production

	2013	2014	2015	2016	2017
TOF (MCHF)	0.02	0.04	0.06	0.30	0.30

Tab. 1: profilo di spesa per il programma di upgrade per il TOF come riportato nella LoI (da CERN-LHCC-2012-012, pag. 140 Tab. 5.9).

TDR (TOF) contents

- describe readout scheme/how it fits with ALICE readout trigger scheme

- repeat analysis of bottlenecks

- report results of 2013 test

- some detail about new data format

- leave open possibility to don't go to DRM2.0?

- and/or leave open scheme with TTC or GBT?