Upgrade strategies for the ZDC calorimeter

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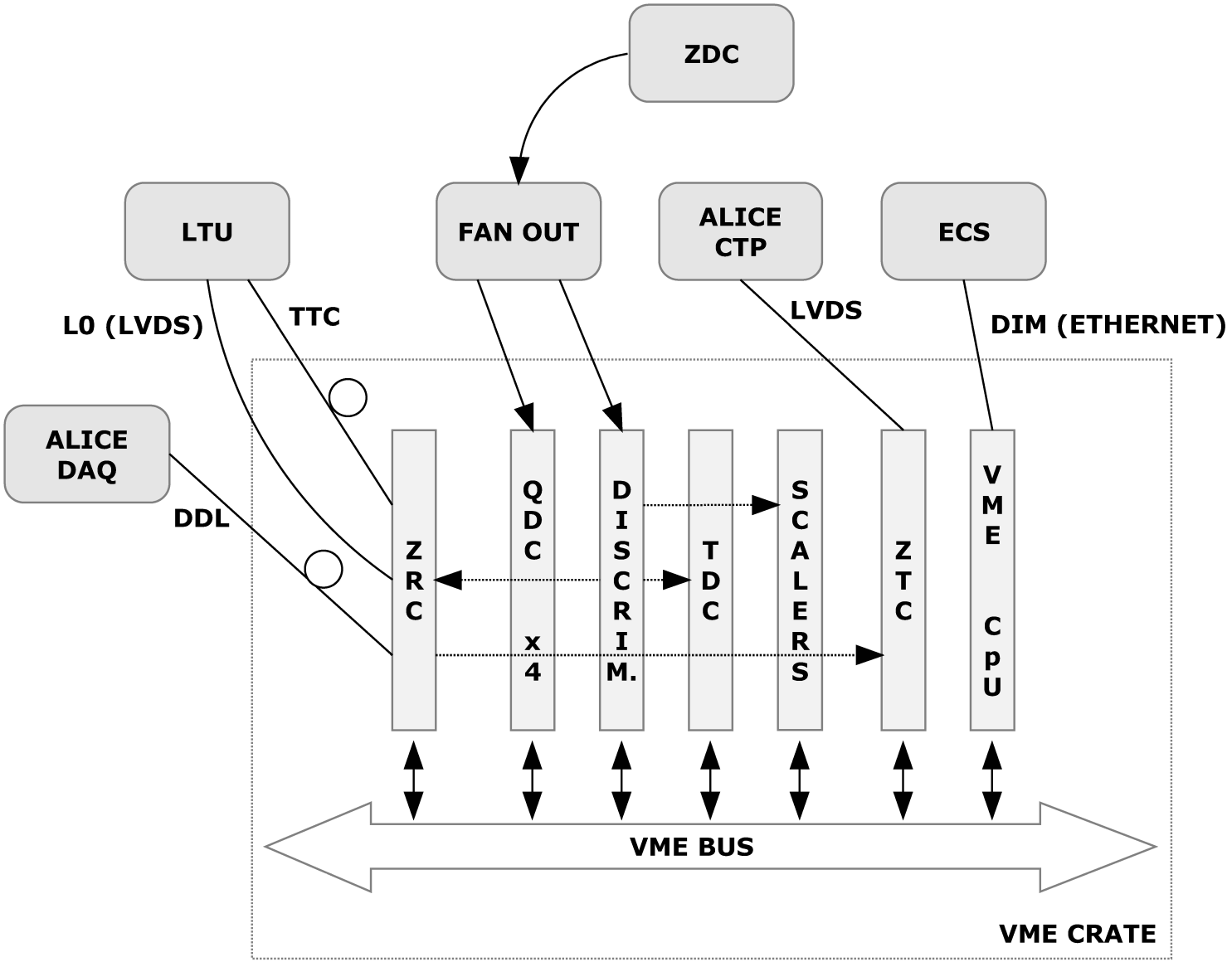
Present DAQ system



Some detail

- Standard FEE
  - QDC V965 (CAEN)
    - multi-event, 12 bit, dual range $\Rightarrow$ 15 bit dynamics
  - Scaler V830 (CAEN)
    - 32 bit, multi-event
  - TDC V1290
    - multi-event, multi-hit
- Custom FEE
  - Differential discriminators (INFN of Torino)
  - Trigger board (INFN of Torino)
- Custom readout board
  - ZDC Readout Card (INFN of Cagliari)
    - receives triggers (LVDS, TTC) and distributes gate (NIM)
    - receives BUSY (NIM) and sends it to LTU (LVDS)
    - reads FEE through VME
    - sends data to DAQ on DDL link

High stability of the readout system

Present performances

- L2a rate: ~8 kHz (meets original ALICE requirements) limited by
  - conversion time of V965 (10 μs)
  - VME transfer rate of V965 (D32 with BLT)
  - not using MEB
- L1r rate: ~100 kHz

During LS1 we will introduce MEB to reduce dead time

No margin of improvement on V965 QDCs

Upgrade LS2 for Pb-Pb

- Hadronic interaction rate: 50 kHz $\Rightarrow$ zero dead time
  - not possible with present QDCs
  - need FEE upgrade ($\sim$20 MB/s)
- trigger-less acquisition
  - electromagnetic interaction rate on ZDC: 2.6 MHz
  - >50 MB/s of background events: is it sustainable on VME?
- triggered acquisition
  - OK with FEE upgrade
  - remaining bandwidth for future increase of collision rate or for p-A

ZDC L1 trigger information

- is it still needed after LS2? In principle not since all the ZDC data should be available for every L0

Test of a digitizer during p-A 2013

- Modern VME digitizers
  - support 2eSST cycles
  - have on-board FPGA
    - signal integration
    - baseline subtraction
    - event time-stamp
- Model CAEN V1751
  - 1Gs/s
  - 10 bit
  - 1Vpp
  - 8 channes

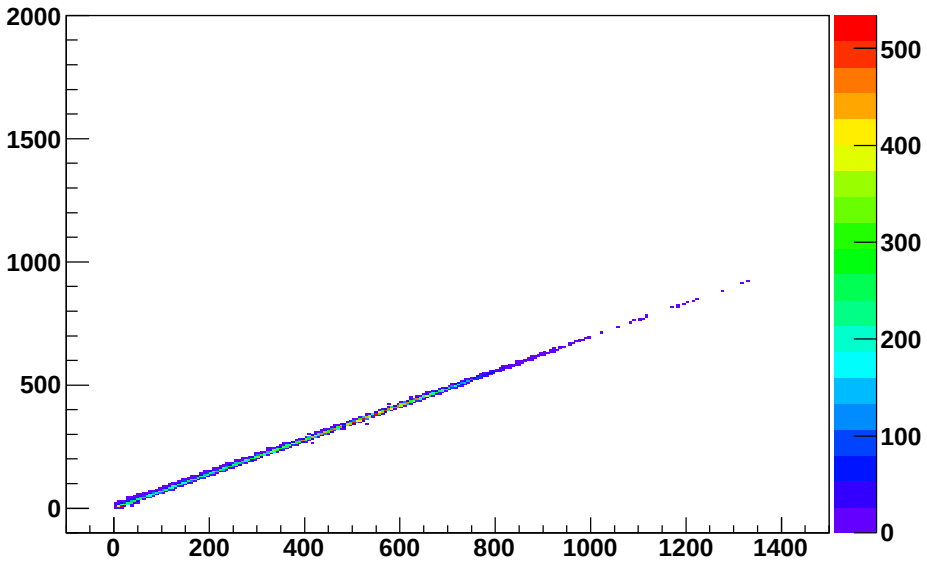
DAQ in parallel to ALICE runs

- Signals attenuated of 4.4 dB to match input dynamics
- $\sim$ 100 samples per channel per event
- numerical integration offline (still to test the FPGA integration feature)

Matching with ALICE data using event timestamp

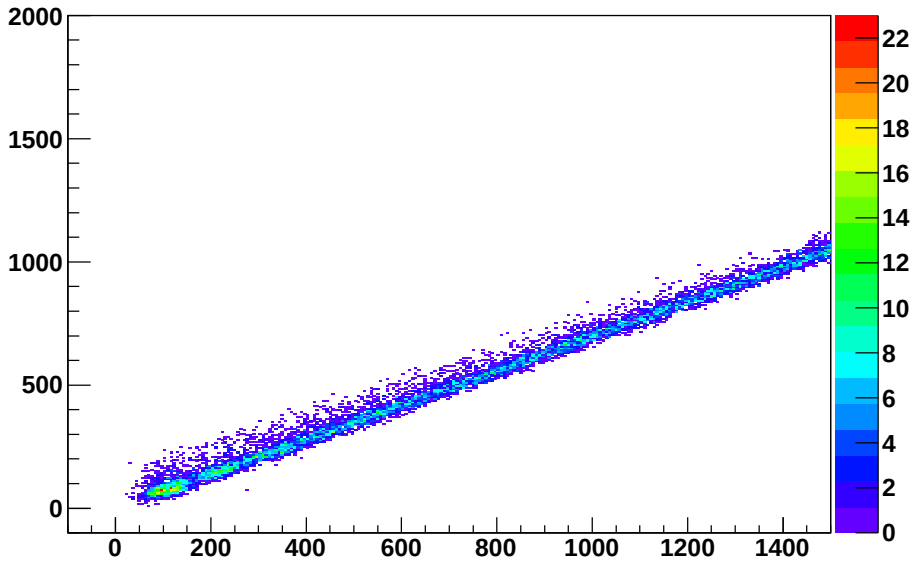
Flash-ADC vs QDC: results (1)

FADC attenuated vs. QDC high range



Charge (pC)

8*FADC attenuated vs. QDC low range

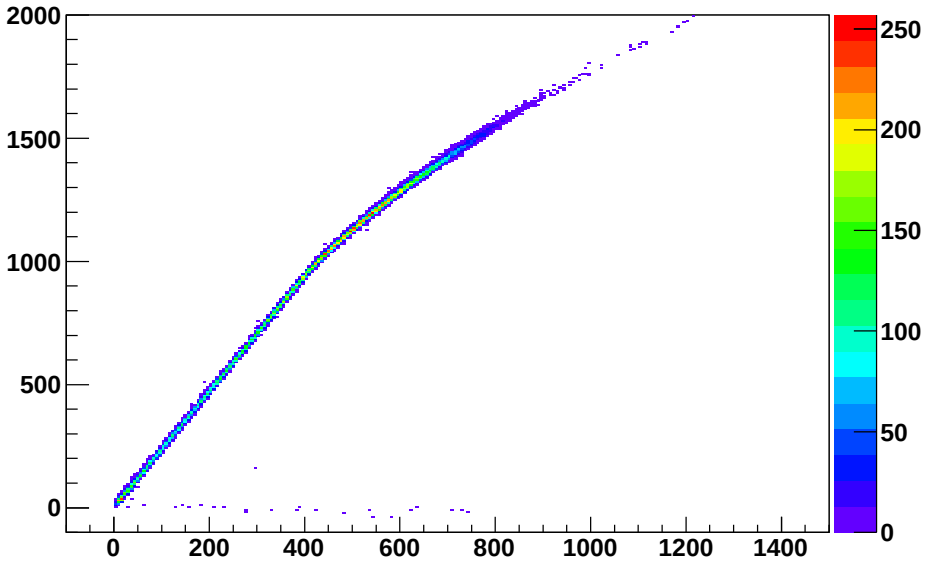


8*charge

- Good linearity
- Separation of 1n and 2n contribution
  - FADC has worse resolution

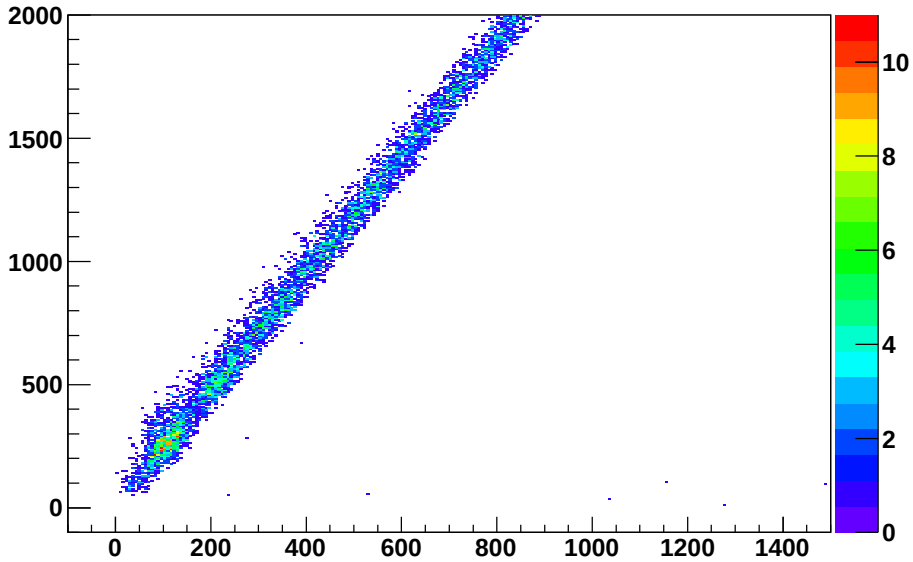
Flash-ADC vs QDC: results (2)

FADC amplified*2 vs. QDC high range



Charge (pC)

8*FADC amplified*2 vs vs QDC low range



8*charge

- Flash ADC saturation
- Good 1n, 2n separation

Need more dynamics on flash ADC $\Rightarrow$ 12 bit

Market survey

- CAEN
  - upgrade of V1751 to 12 bit possible but not in the pipeline
  - possibility to double the number of modules and acquire
    - 22 channels with attenuation
    - 22 copies with amplification
- Struck
  - intended to develop a 1Gs/s 12 bit uTCA FADC in collaboration with GSI
  - they were available to explore the possibility to build also a VME module
  - development stopped due to the high cost of the chip
- TEK Microsystems
  - QuiXilica Atlas-V6 VME/VXS 12 bit ADC a 1Gs/s
  - High cost

All modules can data connections alternative to VME (DDL like but with private protocol, CXP, SFP+, QSFP)

Could we exploit these to send data to DAQ?

Upgrade DAQ and trigger

- ALICE will define new communication standards for what concerns
  - data transfer (new SIU/DDL)
  - trigger reception and busy feedback (new TTC?)
- Upgrade the ZRC board to support faster VME cycles
- Upgrade to support new data/trigger links
  - implement the new links on the board (same/similar to TOF)
    - more complex
    - cannot start development until the links are defined
  - link to the CRU with a standardized protocol (GBTx, e-link ?)
    - probably easier
    - development could probably start sooner
- Is ZDC L1 trigger still needed?