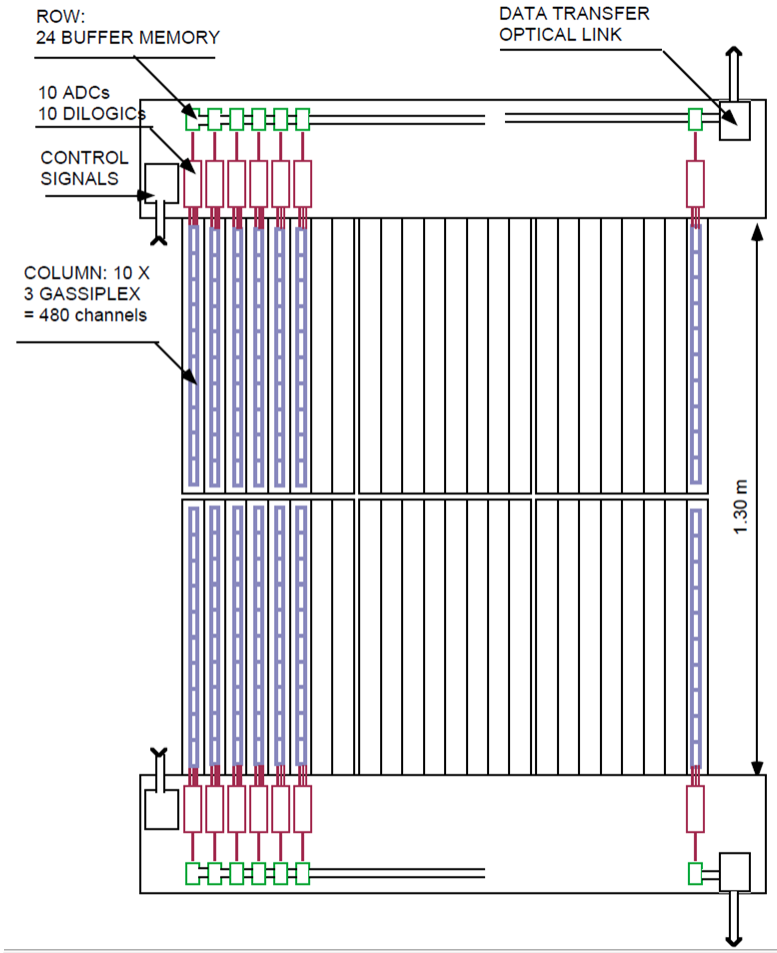
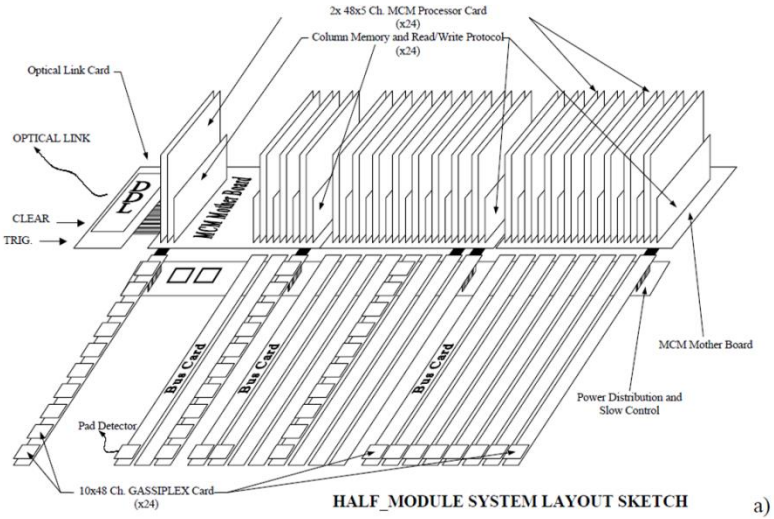
# HMPID readout upgrade for ALICE TDR run3

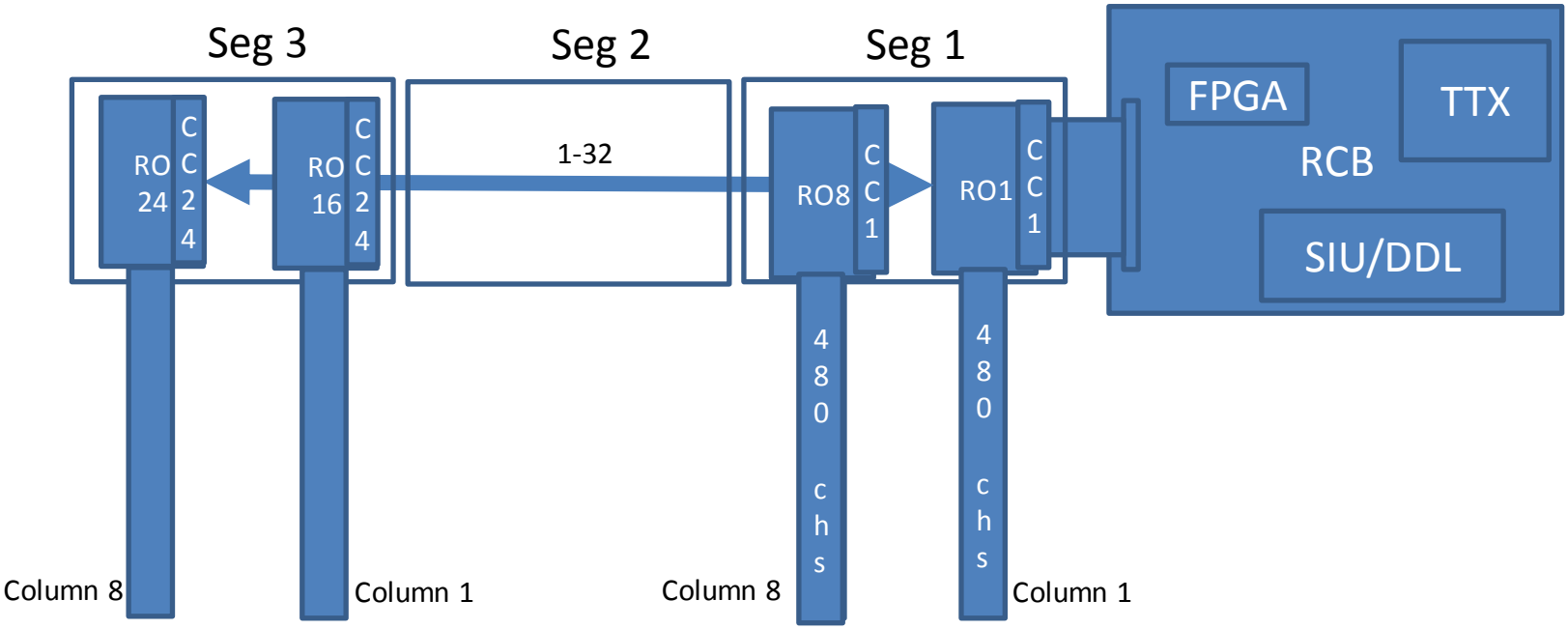
# Present readout layout



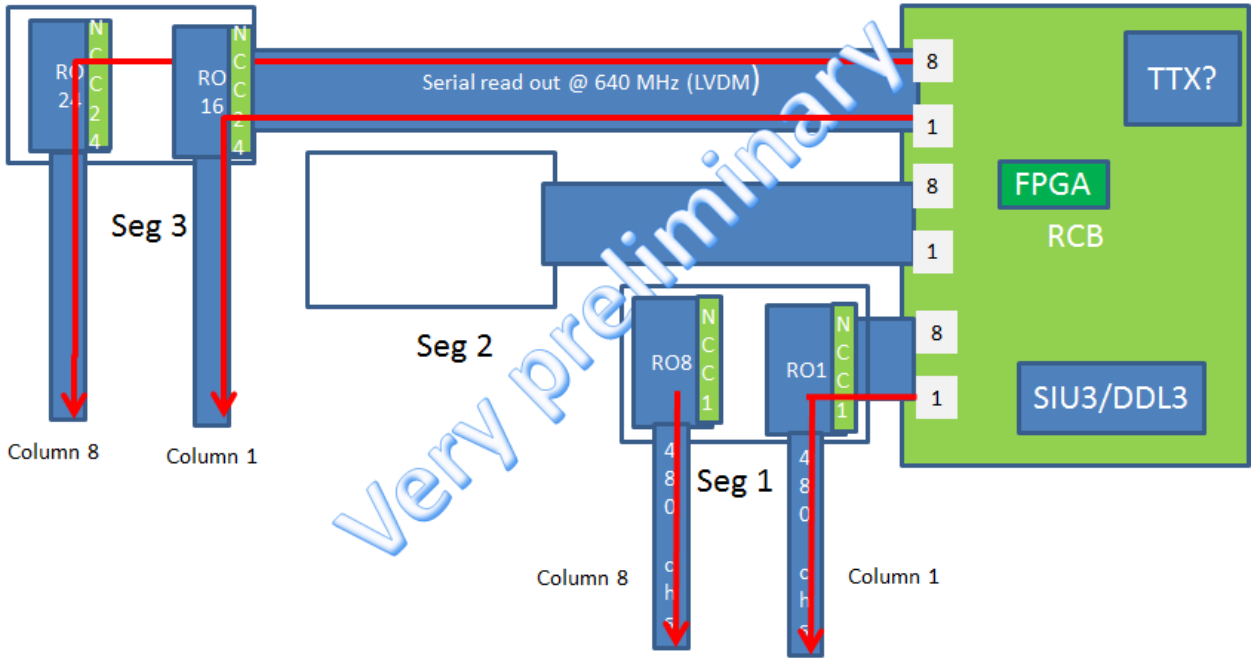
# Present RO scheme

- The present read out scheme is based on a 3 RO Segments (Seg. 1-3) equipped with a total of 24 readout cards (RO), **addressed in series**,; each column is **read out in parallel (ck @10MHz)**; the Column (or Buffer) memory cards are here named Column Control card (CC)
- Each RO card reads 480 channels;
- Max read out rate for a full event: ~0.9 KHZ;



# New RO scheme: Very preliminary

- The new read out scheme should be based on a **parallel read out of the 24 columns** with **serial read out;**
- **Serial read out @ 640 MHz on bipolar lines** (LVDM) **for each column of 480 chs;**
- **For this scheme a new CC card(NCC) , a new RCB board (NRCB) with new FPGA have to be designed;**
- FEE and RO cards do not need to be modified;
- An expected Max read out rate for a full event: ~ 10 KHZ seems reasonable;
- The HMPID remain a triggered detector with the Busy Time as OR of the Seg 1-3 BY;
- The new SIU3 (?) and TTX (?) cards selected by the collaboration, will be adopted.



# Schedule funding and Institute

1. Schedule: as from the SIU3 and TTX(?) cards specifications are available, one year for the design and the production of the first prototype of the NCC and NRCB, is needed;
2. The activity of pto 1) could start as from beginning 2014;
3. Massive tests, debugging and commissioning of the final prototype during 2015;
4. Mass production of boards during 2016;
5. Funding: the project cost is under estimation,
6. Institutes: Bari INFN, CERN (to be confirmed)…and other institutions are not excluded.