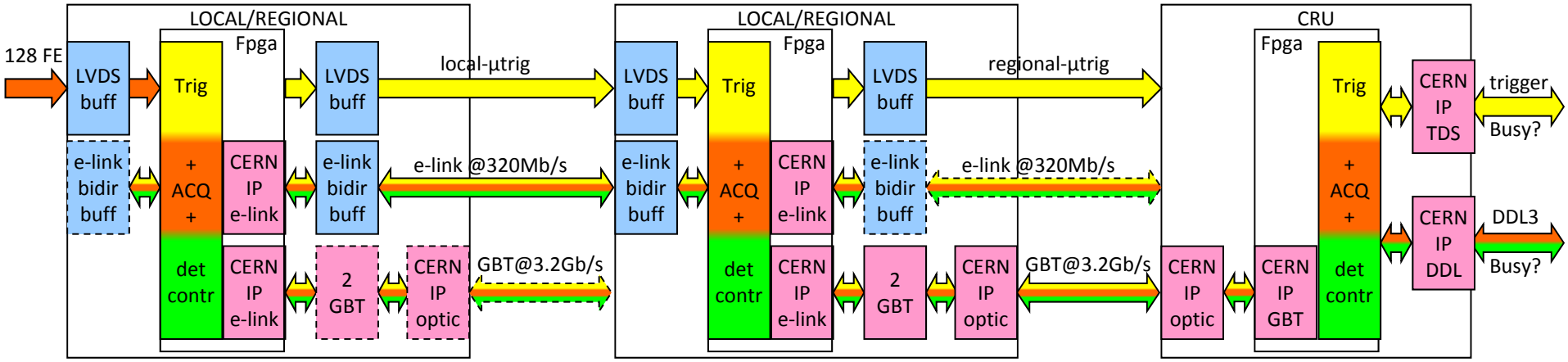
Readout Chain Muon Identifier

Proposition 30sept2013 REGIONAL crate "upgrade" (1/2)

Triggered



LOCAL with 128 LVDS inputs, 17 e-link@320Mb/s, 2 GBT, 2 GBT links @3.2Gb/s, 1 FPGA, 1 LVDS output

REGIONAL with 128 LVDS inputs, 17 e-link@320Mb/s, 2 GBT, 2 GBT links @3.2Gb/s, 1 FPGA, 1 LVDS output

CRU with 32 GBT links @3.2Gb/s ,1 big FPGA, 1 TDS, CDH builder, 1 DDL3

physics event (1+4)*32=160 bits every 5µs (200kHz) + software event (1+4+45)*32=1600 bits every 1s (1Hz) ≤ 1 e-link @320Mb/s / LOCAL

500ns to send a physics event and 5µs to send a software event from LOCAL to CRU.

Physics and software triggers down to LOCAL, multi event buffer in LOCAL, CDH builder in CRU, Busy needed.

•1c CRU in control room, same hardware for LOCAL and REGIONAL

total

-> 234 new-local (128 LVDS inputs, 1 e-link @320Mb/s, *1 FPGA, multi event buffer, 1 LVDS output,* optional[16 e-link @320Mb/s, 2 GBT, 2 GBT links @3.2Gb/s)

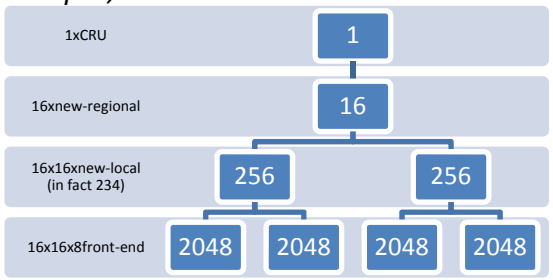
-> 234 short e-link @320Mb/s

-> 16 new-regional (16 e-link @320Mb/s, 2 GBT, 2 GBT links @3.2Gb/s, *16 LVDS inputs, 1 FPGA, 1 LVDS output, optional[112 LVDS inputs*, 1 e-link @320Mb/s])

-> 32 long GBT links @3.2Gb/s

-> 1 CRU (32 GBT links @3.2Gb/s, 1 TDS, CDH builder, 1 DDL3)

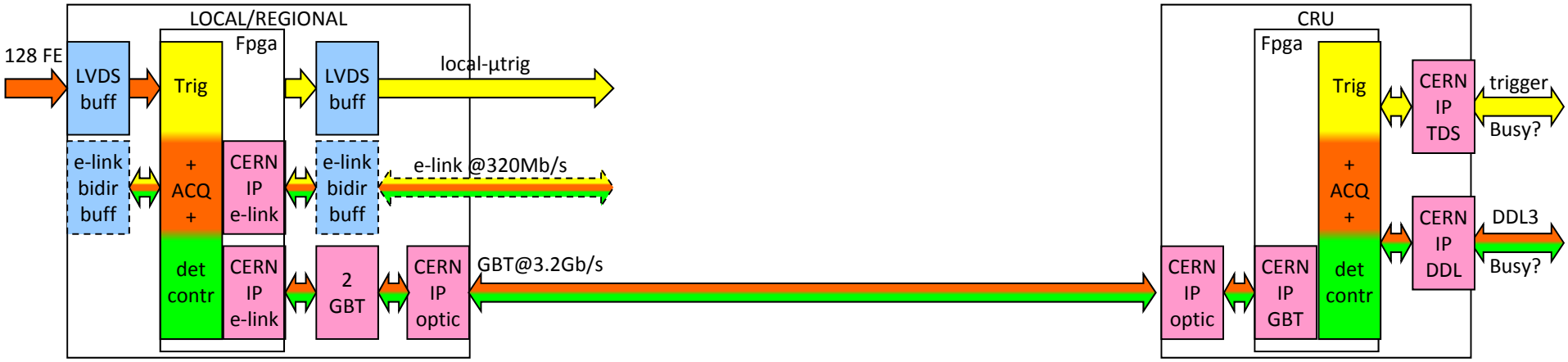
-> 1 short DDL3 to DAQ-FLP



Readout Chain Muon Identifier

Proposition 30sept2013 REGIONAL crate "upgrade" (2/2)

Mixed continuous/triggered



LOCAL with 128 LVDS inputs, 17 e-link@320Mb/s, 2 GBT, 2 GBT links @3.2Gb/s, 1 FPGA, 1 LVDS output

CRU with 32 GBT links @3.2Gb/s ,1 big FPGA, 1 TDS, CDH builder, 1 DDL3

Continuous readout: 128 bit @40MHz = 16 e-link @320Mb/s => 2 GBT links @3.2Gb/s / LOCAL

physics event CDH+16*(1+4)*32=CDH+2560 bits every 5µs (200kHz) + software event CDH+16*(1+4+45)*32=CDH+25600 bits every 1s (1Hz)

Physics and software triggers down to CRU, multi event buffer in CRU, CDH builder in CRU, Busy needed.

•3b CRU in control room, same hardware for LOCAL and REGIONAL, evolution without the REGIONAL

-> 234 new-local (128 LVDS inputs, 2 GBT, 2 GBT links @3.2Gb/s, *1 FPGA, 1 LVDS output,*
optional[17 e-link @320Mb/s)

->

->

total

-> 468 long GBT links @3.2Gb/s

-> 16 CRU (32 GBT links @3.2Gb/s, 1 TDS, multi event buffer, CDH builder, 1 DDL3)

-> 16 short DDL3 to DAQ-FLP