Development of an Indium Bump Bonding Process at PSI

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PSI

Most material presented is taken from

Pixel Conference, Bonn, 2006, NIM A 565 (2006) 303-308

RESMDD, Firenze, 2004, NIM A 552 (2005) 232-238

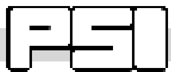
slides of the conference talks at http://www.psi.ch/~rohe

Introduction

- Membership of the PSI group in the CMS pixel project (since 94) required access to bump bonding technology
- Decision to develop in house bump bonding process instead of an industrial contract was taken 1997
  - Fine pitch bumping was not easily available at this time (industrial partners would need R&D)
  - Wanted to have full control on process (parts/most of it can in principle be outsourced)
  - **Fast feedback in case of problems (was very important for the success of the project)**
  - Fast and flexible availability during prototyping
  - Lot of infrastructure is available at PSI (especially the Lab for micro and nano technology), only moderate investments necessary

History

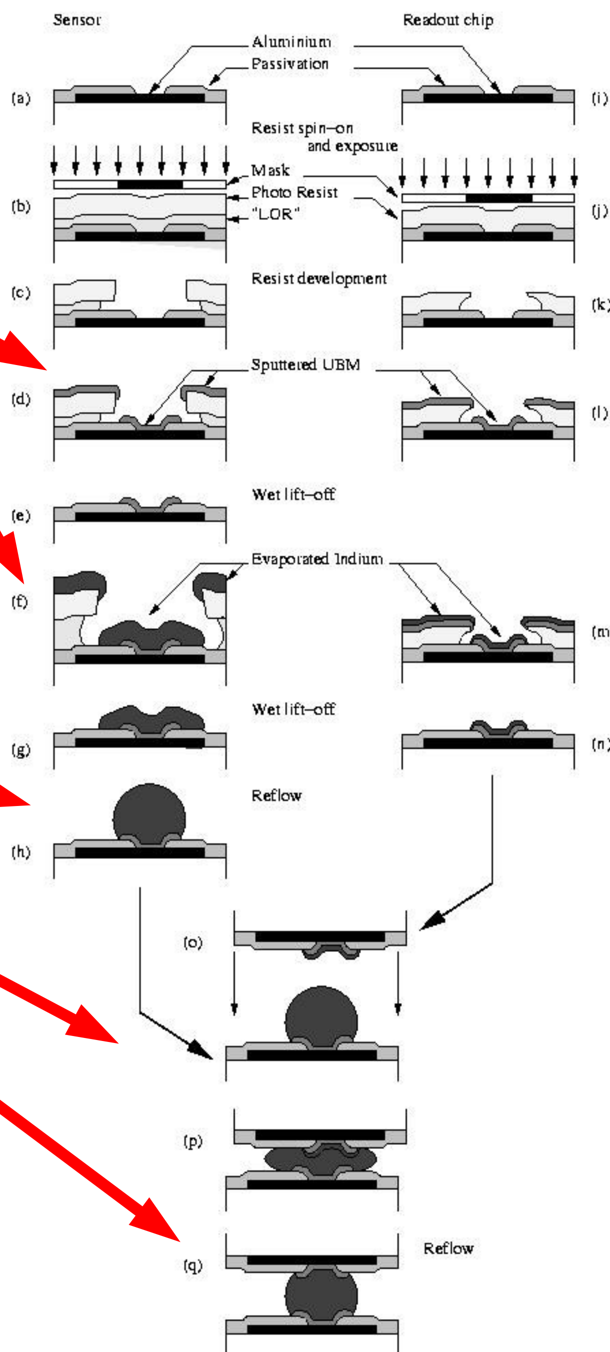
- 1997/98 first trials
  - Sputtering of UBM
  - Construction of In evaporation chamber (optimised version in operation since 2002)
  - Construction of manual chip placer
- Increasing wafer radii 100mm (Honeywell) to **200mm** (2005, DSM)
- 2003 construction of the PILATUS 1M
- 2005 commissioning of a fully automated chip placer
- 2005/06 start of series production for PILATUS 6M and CMS pixel barrel
- 2008 finishing of the construction of the **CMS pixel barrel**



Process Flow

- **Sensor**
  - Test
  - **UBM-Deposition (Lift-off)**
  - **In-Deposition (Lift-off)**
  - Cutting Wafer
  - Test
  - Cleaning
  - **Reflow**

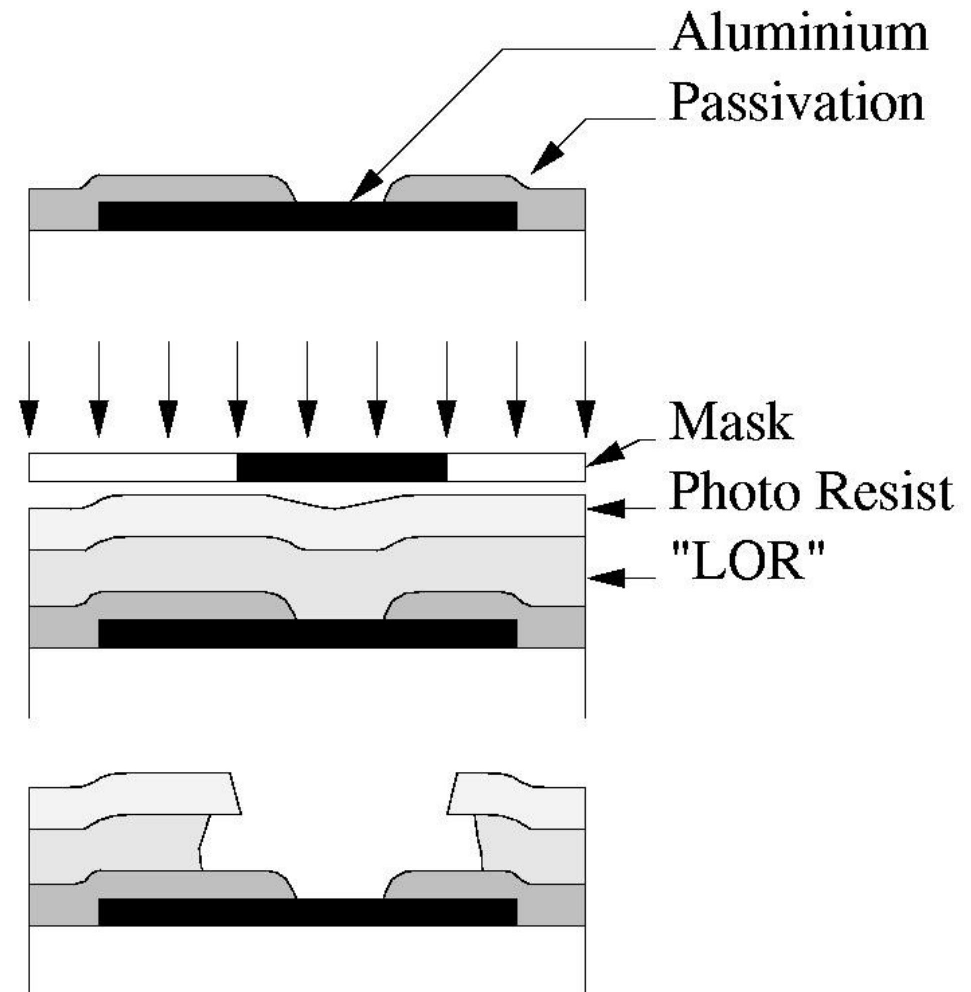
- **Chip flipping**
- **Reflow**
- (Geom. verification + pull test, now omitted)
- Raw module test
- (Potentially: **Rework**)



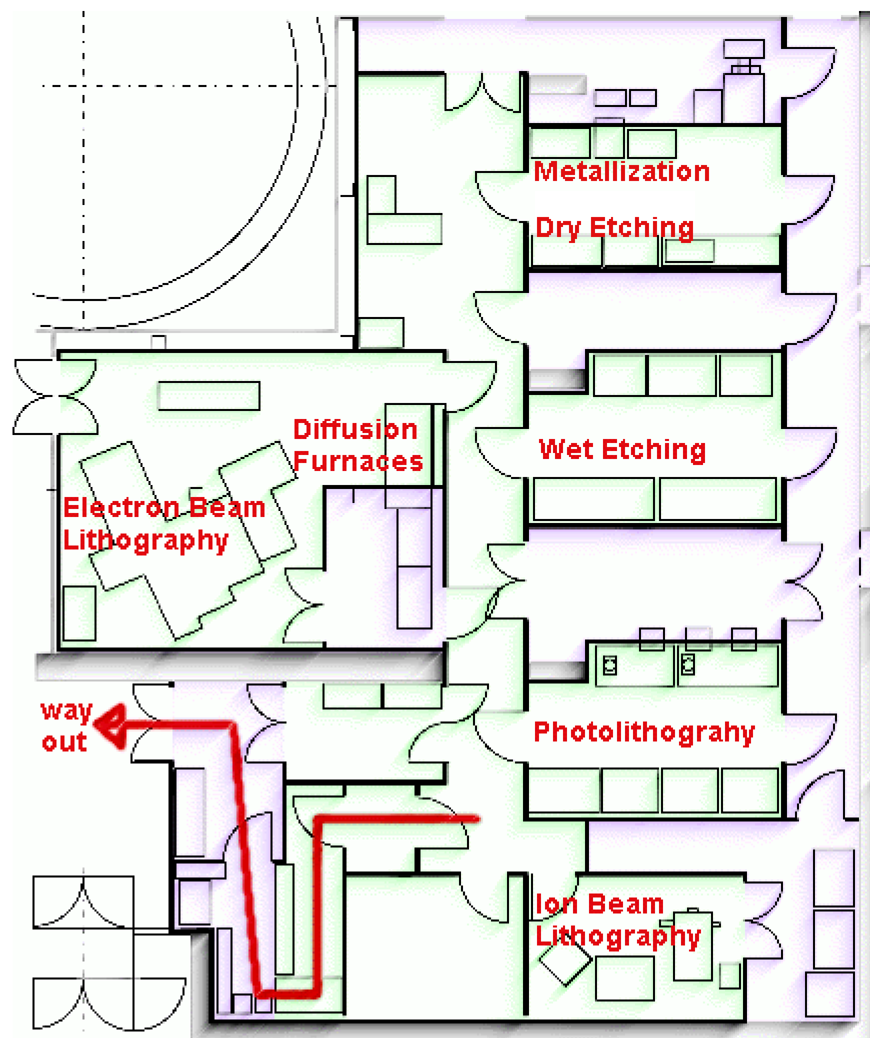
- **ROC**
  - Test
  - **UMB and Indium Deposition (same lift-off)**
  - Wafer thinning (~180μm)
  - Sawing and picking
  - Cleaning
  - Test

UMB: Photolithography

- Use of 2 layer resist
  - Lift-off resist (LOR), not light sensitive, 1.2-1.5μm
    - light scattered from rough metal surface does not harm
    - not removable with acetone
  - Positive resist (parts exposed are developed), ~3.5μm
    - Alignment not possible with bumps only
  - UBM now done by sensor vendor (CiS, Germany)



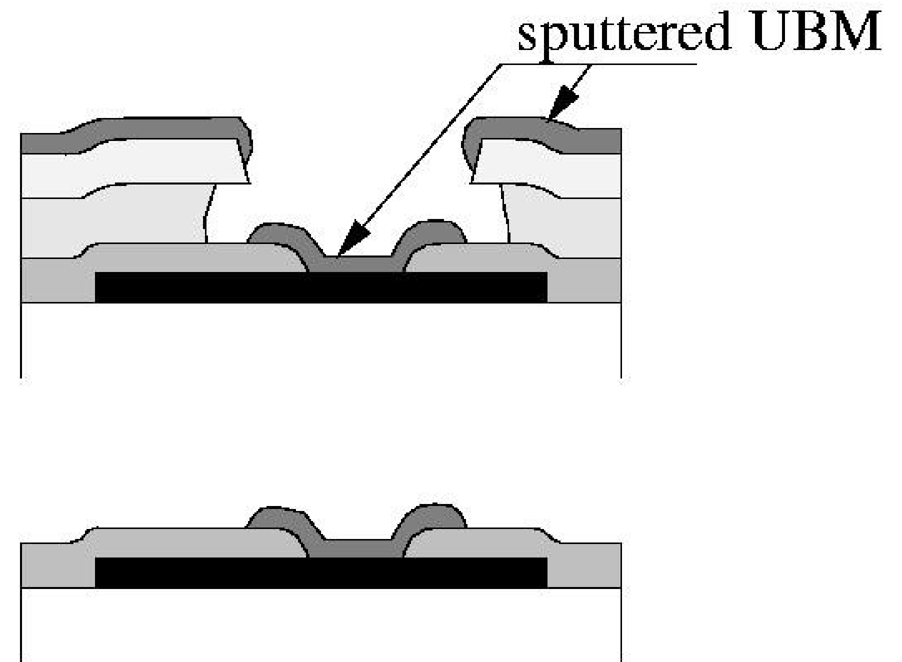
Clean Room Equipment

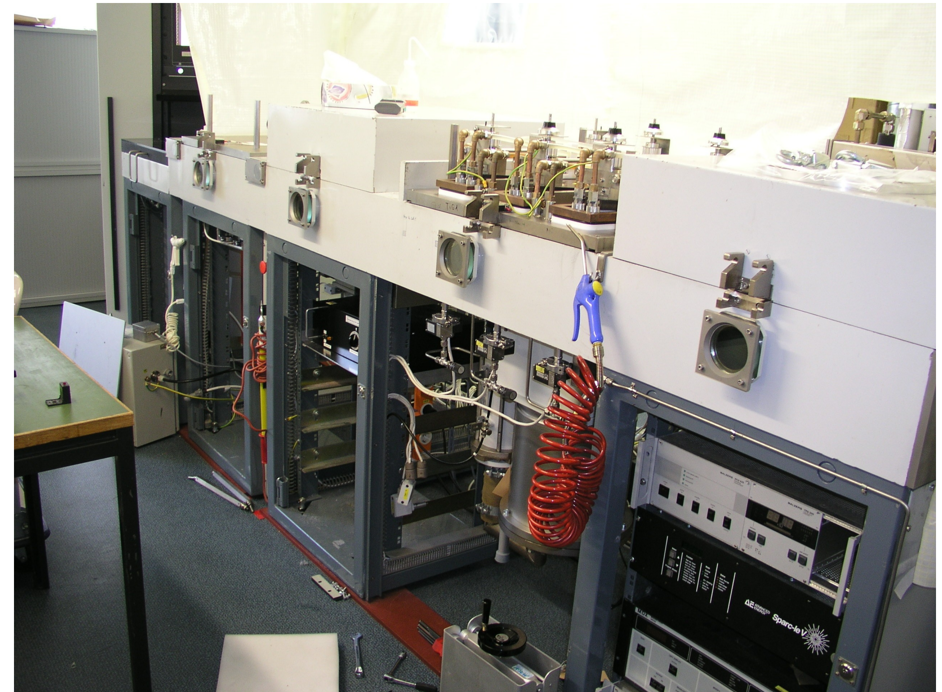


- Area: ~350m^2
- Class 1000 (personal area) to 100 (photolithography) up to 10 (some work spaces)

UBM: Sputtering and Lift-off

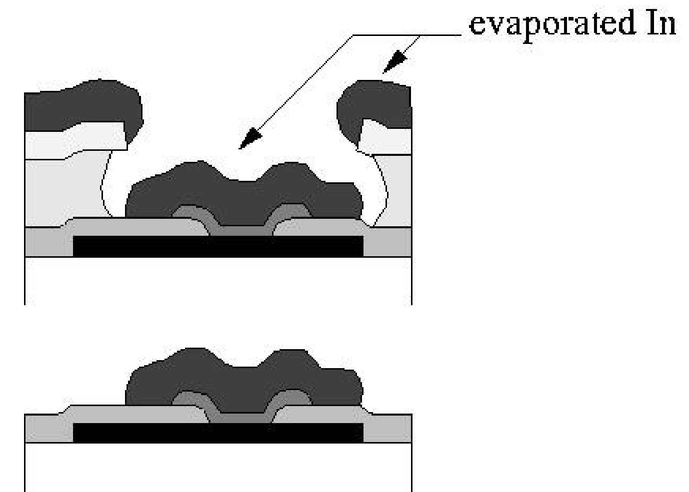
- UBM is sandwich of
  - Ti (adhesion, barrier)
  - Ni (wettable with In)
  - Au (sacrificial, oxidation protection)
- Total thickness ~100nm
- Wet lift-off at ~60°C
- Now done by sensor vendor (CiS)



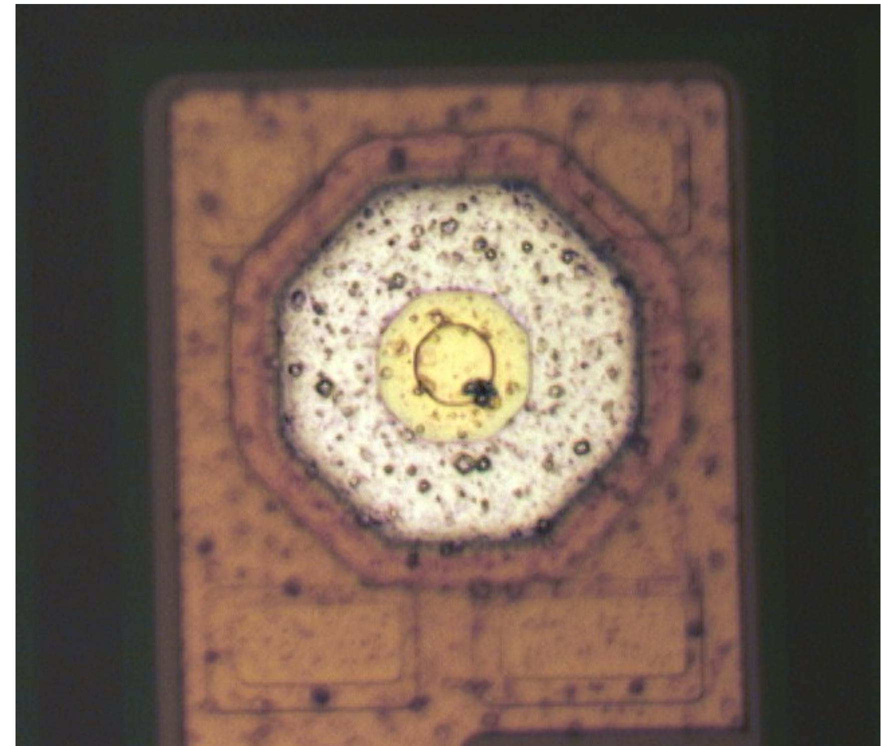


Indium Deposition

- Photolithographic process like UBM, but thicker (3.5 + 4.5 μm, LOR > 1.2 metal thickness)

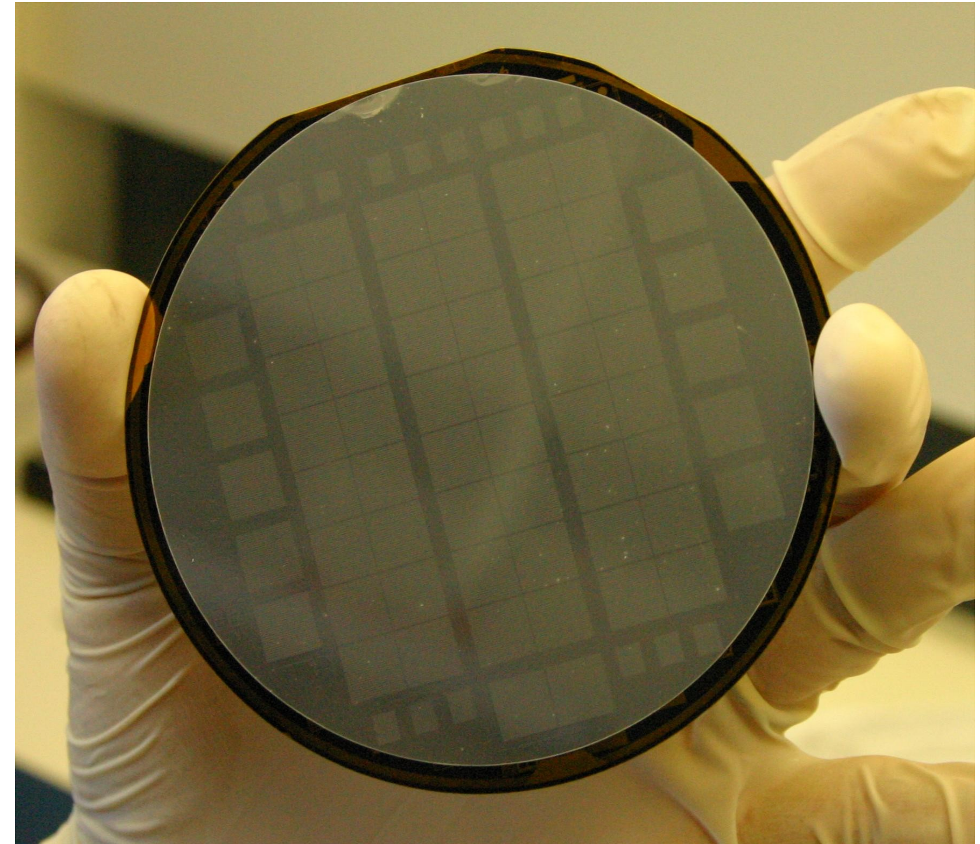


- Indium evaporation in apparatus designed and built at PSI
  - Vessel is water-cooled
  - Photoresist better removable
  - 1×200mm or 3×100mm wafer
  - Space for several boats (alloy's possible)
- Same lift-off process as for UBM



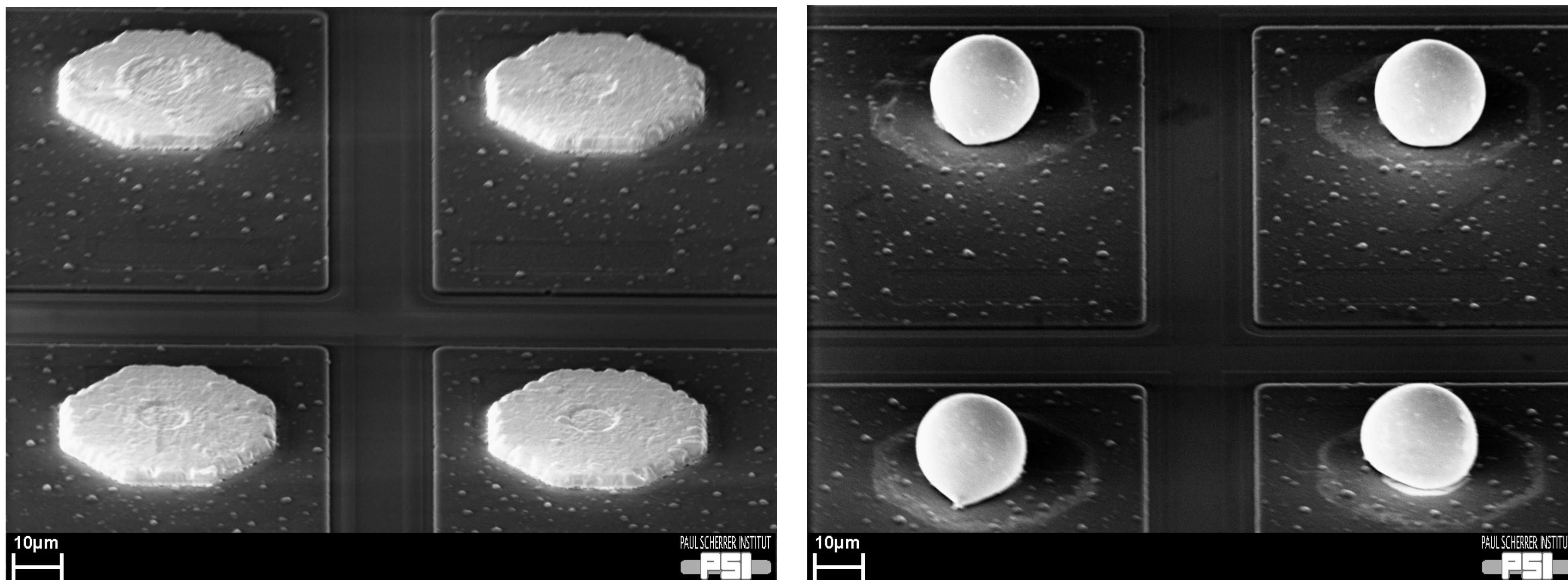
Indium Deposition (2)

In evaporation vessel



wafer after evaporation

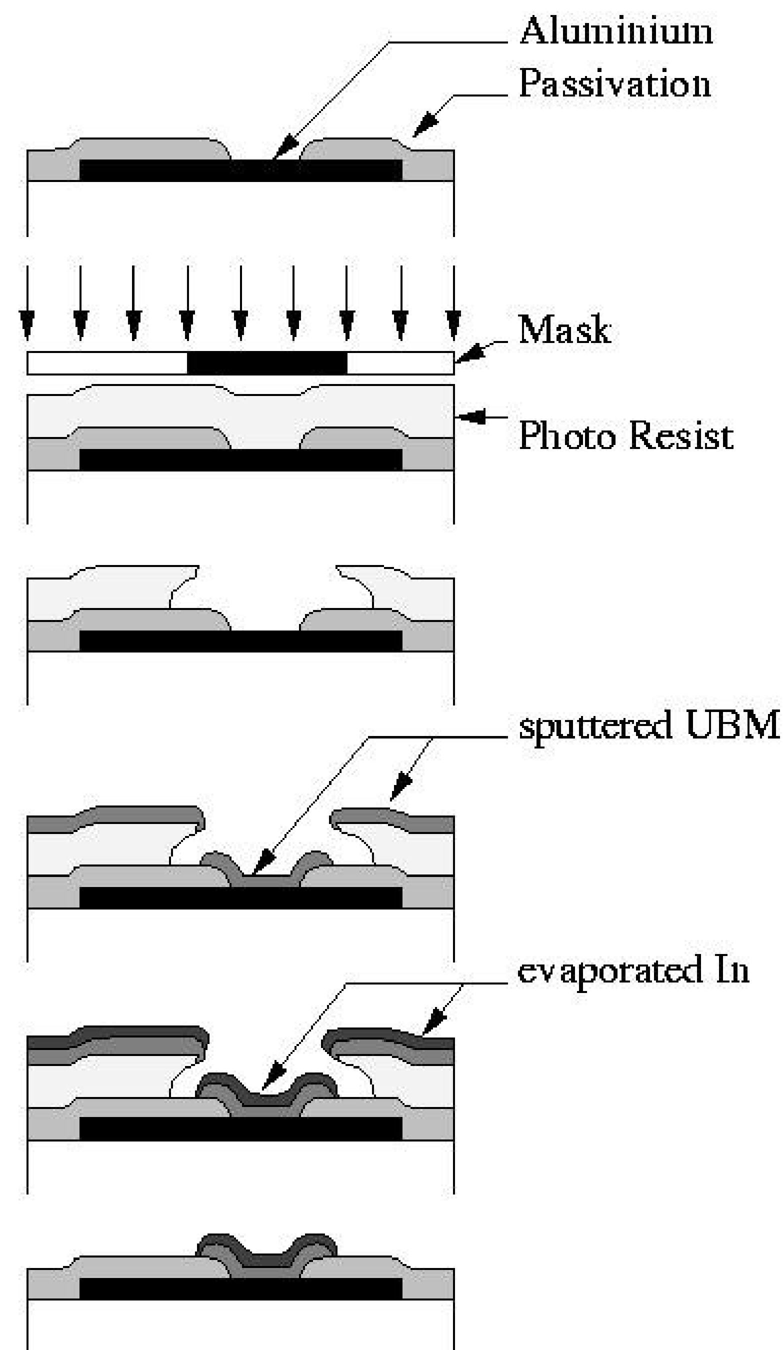
Reflow



- Short (~1min) heating to about 200°C
- Size of bumps
  - volume of evaporated Indium ~4000μm^3
  - diameter of wetable UBM pad 18 μm

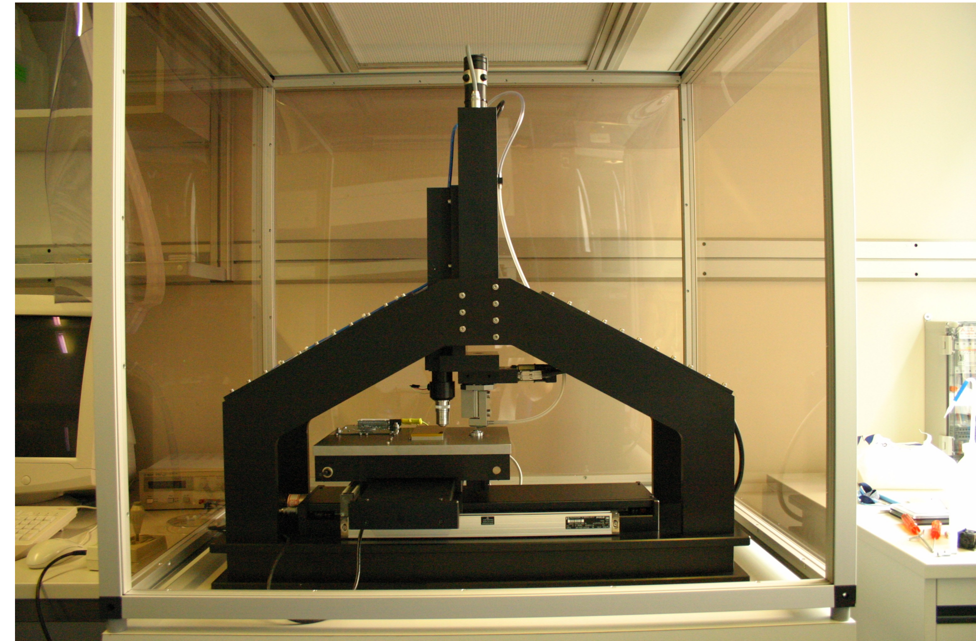
Metal Deposition on ROC

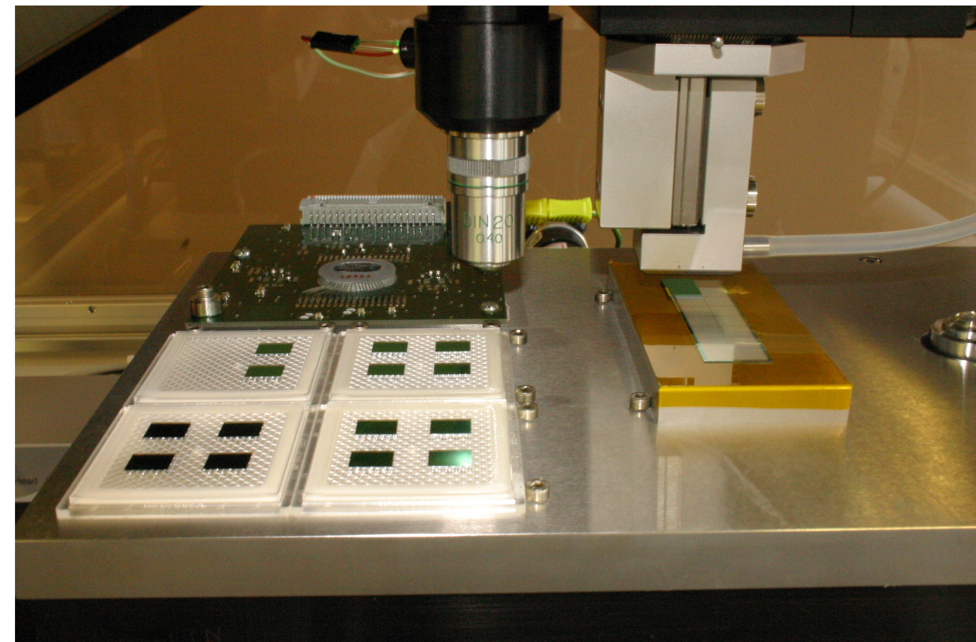
- On ROC only thin metal layers are deposited
  - UBM (same composition as on sensor)
  - Thin In-layer for better adhesion before reflow of joined samples
- Only one layer of photo-resist
  - easy, acetone used for lift-off
- Photolithography for 200mm wafers possible in-house



Automatic Chip Placement

- Machine designed and built in 2002-4
- Main challenges
  - calibration of stages
  - **software**
- ROCs are automatically taken, aligned with 2nd camera, and placed on the
  1. probe card (test functionality)
  2. sensor (and pressed down)
- Automatic operation since 2005
  - 50min/module (including chip test)
  - 15min for preparation and loading
  - no human interference necessary
- Now commercially available



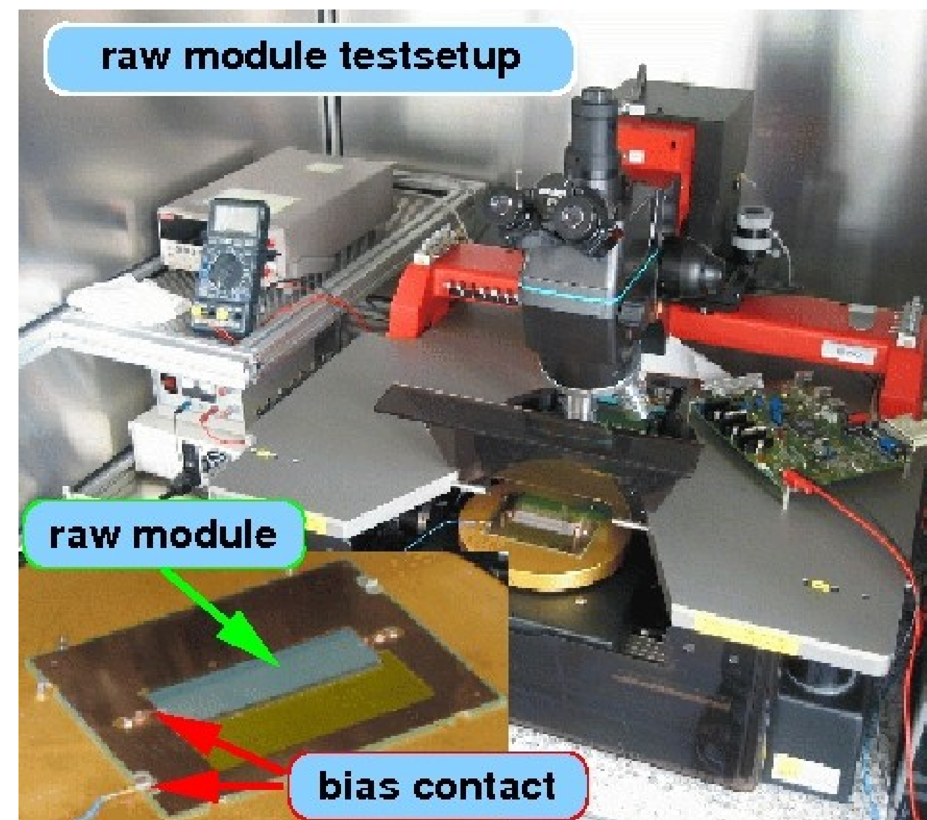


Reflow of Joined Module

- Mechanical strength
  - before reflow the modules are extremely fragile
  - transfer to furnace is critical
- Self alignment
  - misalignment of a few micrometers is corrected by surface tension
- Controlled and reproducible environment (time, pressure, temperature, ...) provided by electronically controlled set-up (designed and built at PSI).

Test of Raw Modules

- Probe card contacts 1 ROC
  - Test functionality of each ROC
  - Bump yield
  - Sensor IV (when 1 ROC is grounded)
- Bad ROCs are replaced (rework)
- If sensor is bad, module is rejected
- Overall raw module yield ~90% (after rework)

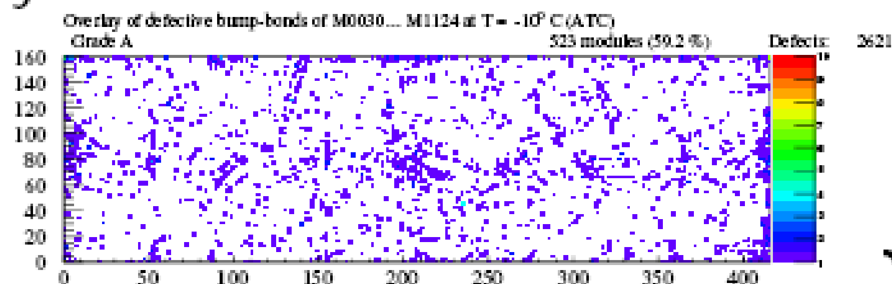


Picture provided by Stefan Koenig, PSI

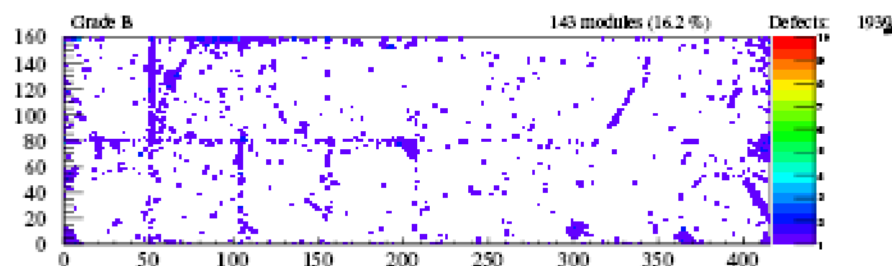
Bump Yield

Overlay of modules tested at T = -10° C (ATC)

Final Grade A
(523 modules)

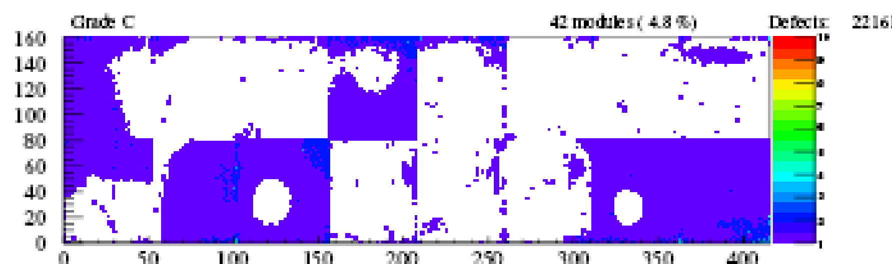


Final Grade B
(143 modules)



} 44.3 Mio. Pixel

Final Grade C
(42 modules)

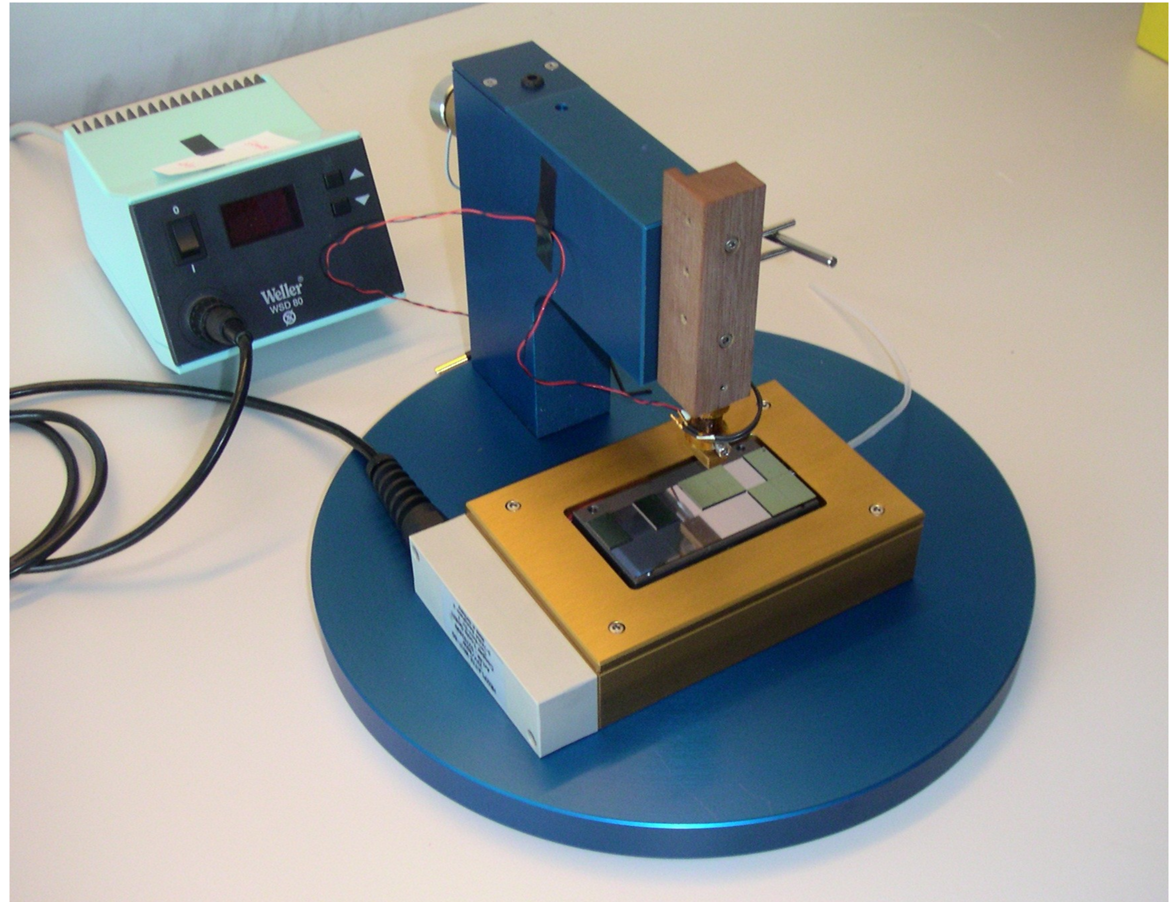


2.8 Mio. Pixel

From database of the ETH group (U. Langenegger et al.)

Rework

- Sometimes defective ROCs have to be replaced after test of bare module
- Little number of modules affected (low statistics)
- Introduction of dry mechanical cleaning step strongly reduced number of failures
- Working principle
  - module and ROC are heated
  - ROC is lifted with heated vacuum chuck
  - new ROC is placed
- Success rate seems high
- Bump yield of reworked ROC is lower (low statistics)

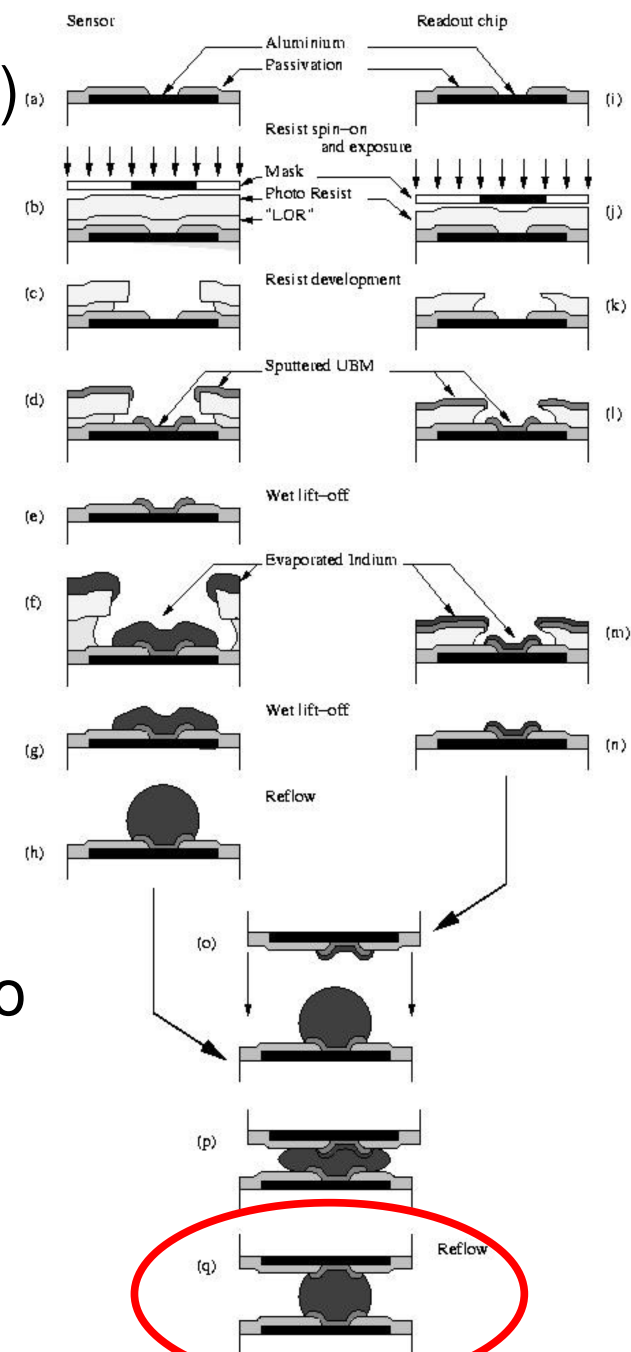


Practical Aspects

- Photolithography (Sensor)
  - Surfaces of ROCs, sensors ... quite different
  - Adhesion problems with sensors having a rough metallization (stray light)
  - Cured by introducing LOR (not light sensitive)
- ROCs
  - Corrosion of pads. Happens on few ROC wafers, especially if lift-off was done with high ultrasonic power. Not yet fully understood.
- Dead Chips
  - **One** failure mode are silicon pieces, which was strongly reduced by a dry mechanical cleaning step
  - Rework possible but painful (try to avoid)
- Logistics: Three Departments of PSI are involved
  - Lab. for Particle Phys. (TEM): Logistics, chip and sensor testing, Indium evaporation
  - Lab. for Micro and Nanotechnology (SYN): Clean room. All photolithographic steps
  - Lab for Development and Methods (NUM): Sputtering of UBM

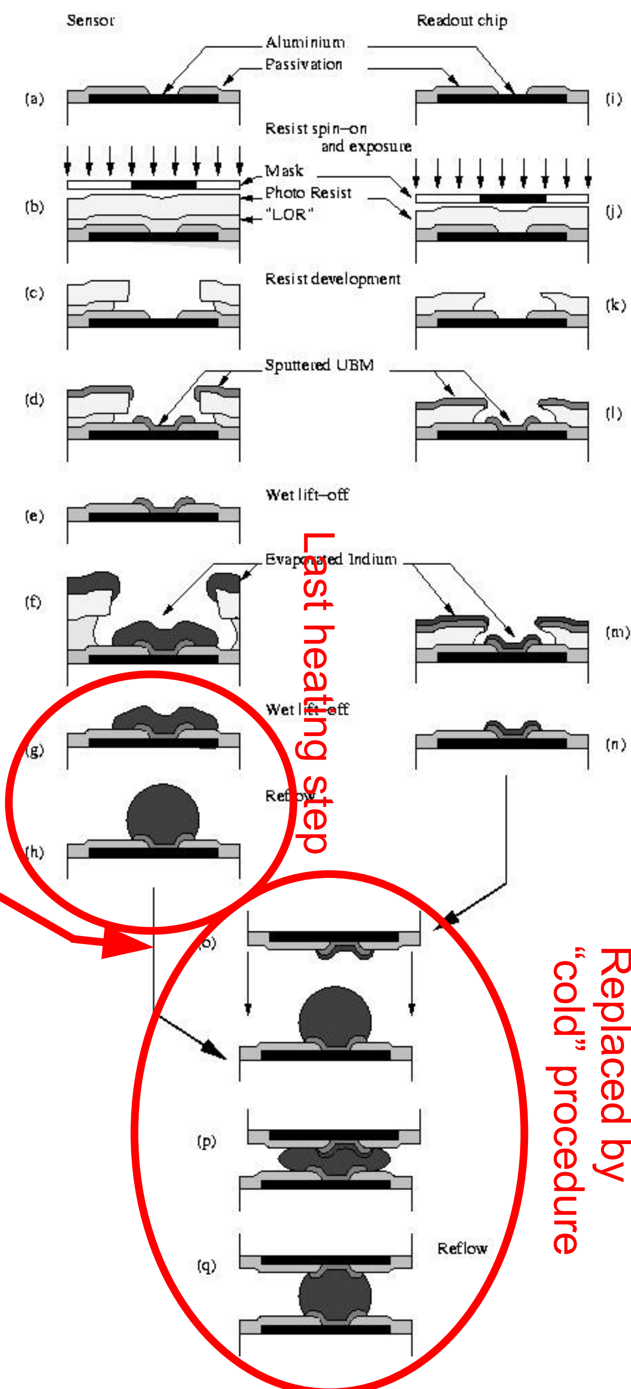
Samples for Irradiation

- A small sensor (size of 1 ROC, 1 cm x 1 cm) contains all features of the full module
- Last heating step is the reflow of the flip chipped sample
  - Self alignment
  - Mechanical strength
- Strongly advise to irradiate flip chipped and reflowed samples
- In case of diced samples photo lithography o single dies (in principle) possible
  - **Extremely labour intensive**
  - Presently a problem with resources at PSI

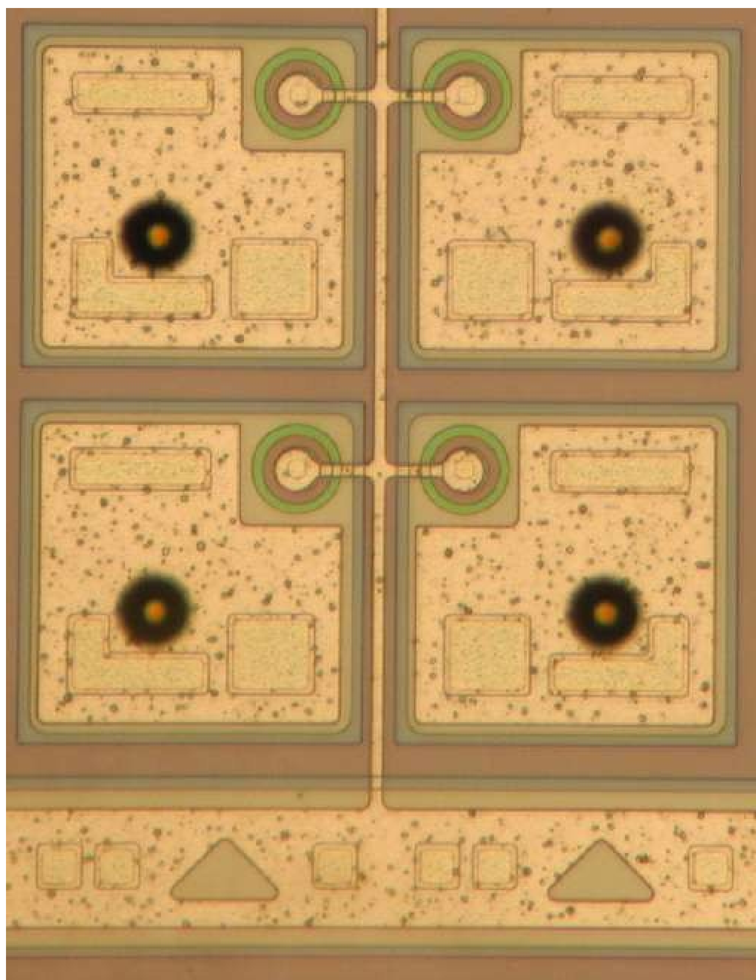


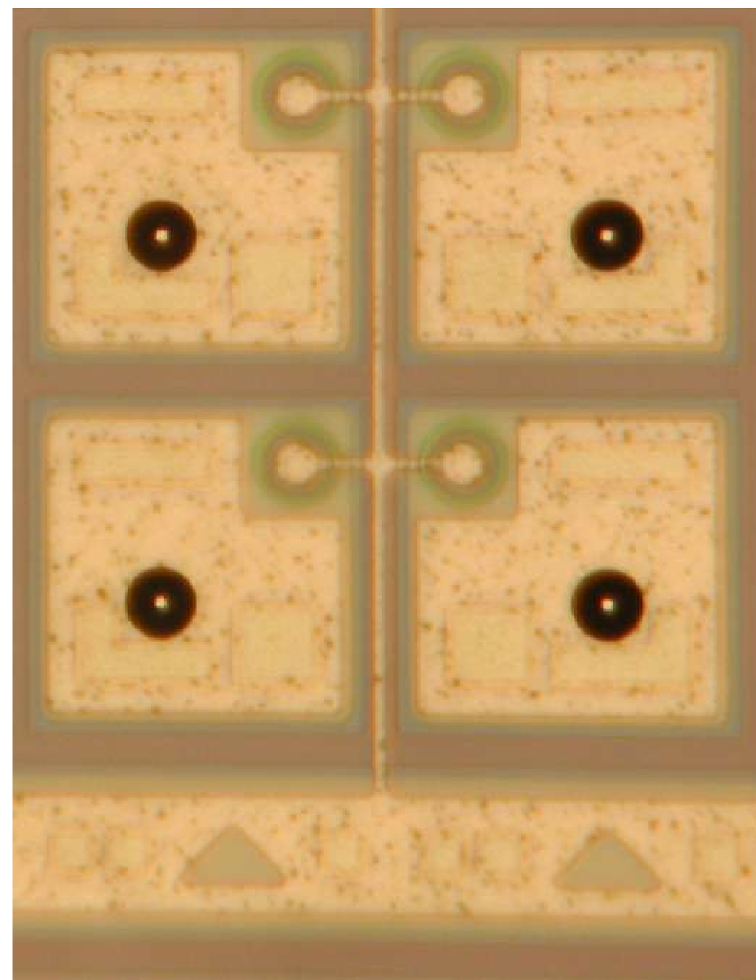
"Cold" flip chipping

- In 2002 – 04 no (really) radiation hard readout chip was available (we used for sensor characterisation an old Honeywell chip)
  - Sensor was irradiated after bump reflow
    - Handling becomes critical
  - Flip chip procedure was adapted
    - Extremely labour intensive (several hours per sample)
    - Yield ~ 70%
    - Bump yield low but acceptable for test beam campaigns (> 90%)



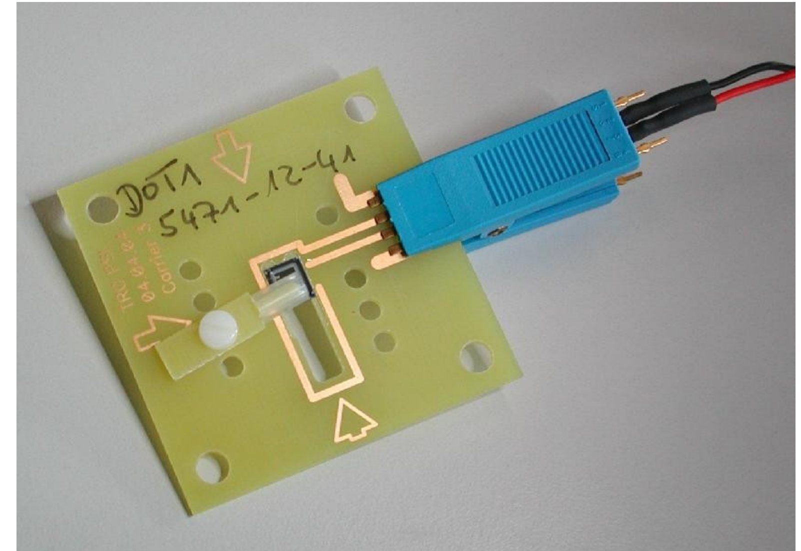
Reflowed Indium Bumps

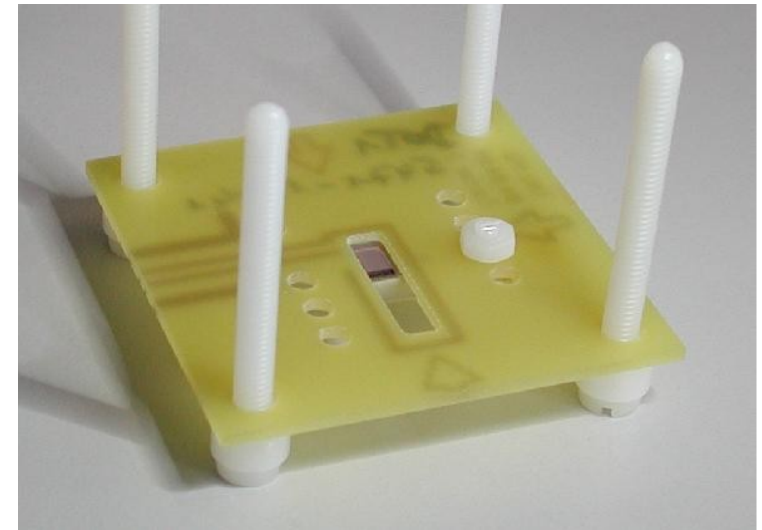




Support Frame

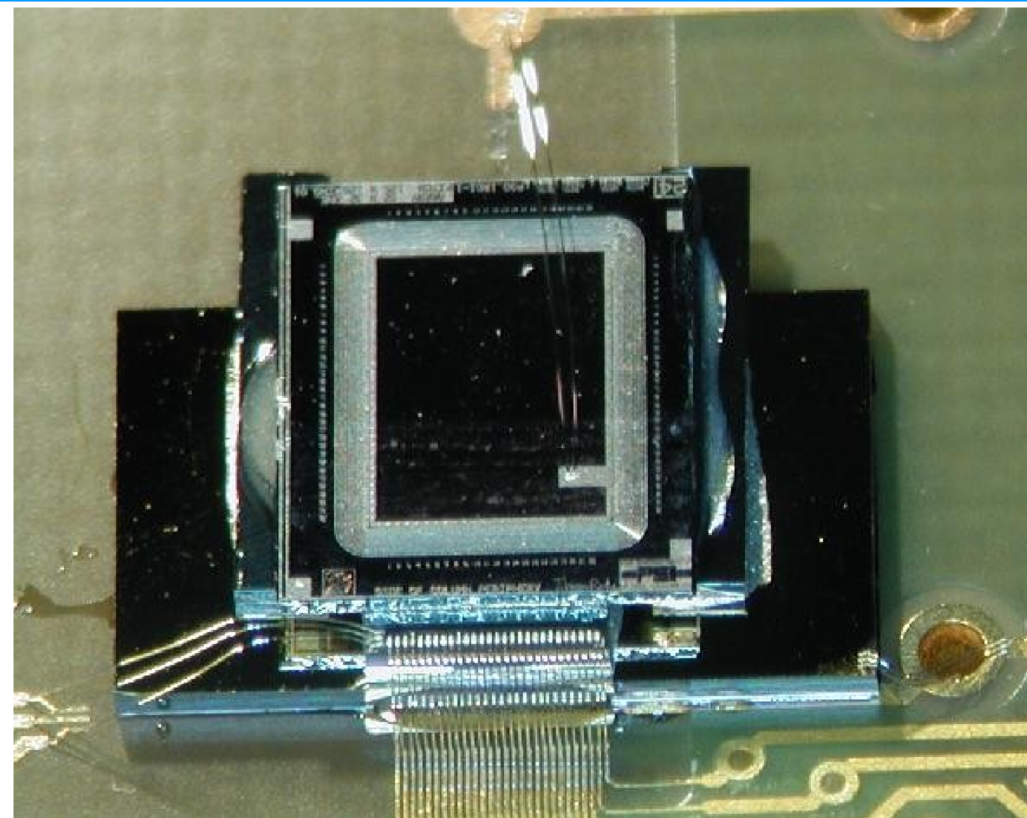
- During irradiation and transport bumps have to be protected
  - PCBs are large and heavy
    - Take much space in the shuttle
    - Activation of support frame is problematic
- Sensors are wire bonded to PCB
  - IV test is possible
- Sensor is clamped to the PCB and easily removable

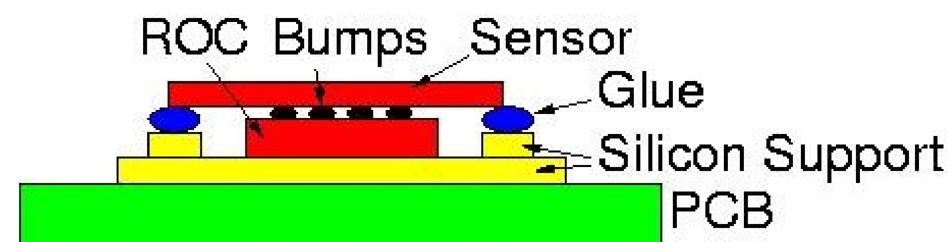


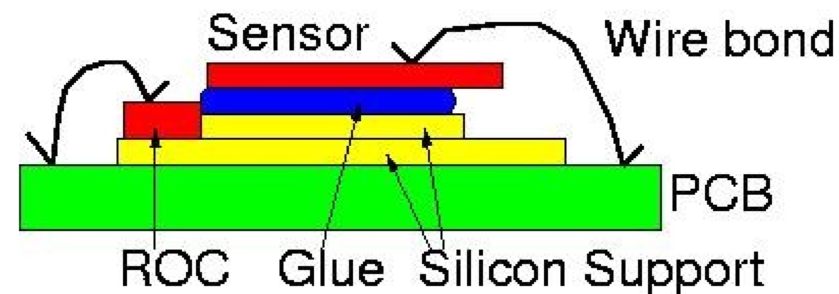


Flip Chip Procedure

- No self alignment
  - Samples have to be extremely flat during bump bonding
  - Placement has to be done more precisely (difficult with the "old" manual chip placer
  - ROC was glued to small silicon piece
- Bump bonds are mechanically weak
  - Sensor was placed into glue
  - Bump head has to stay on the sample until glue is hardened

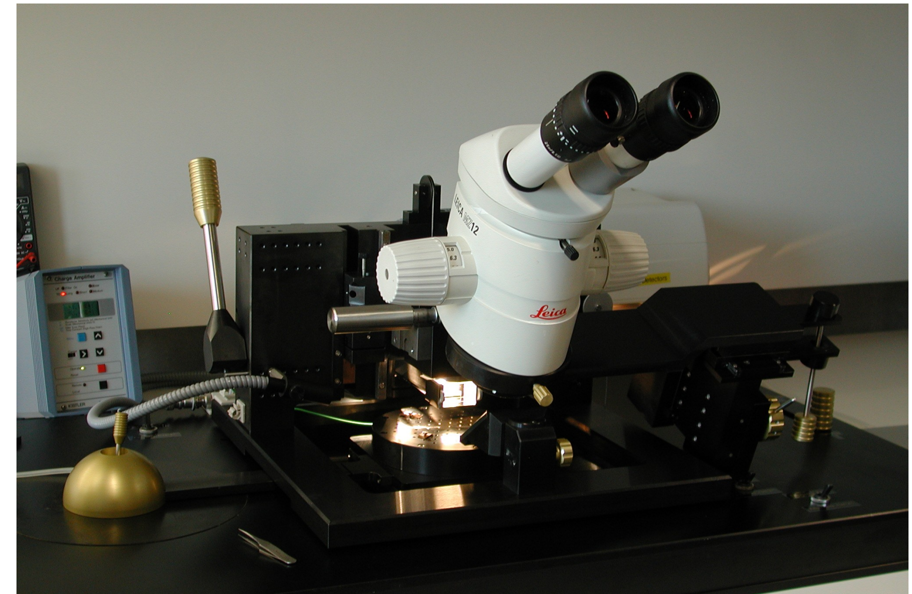


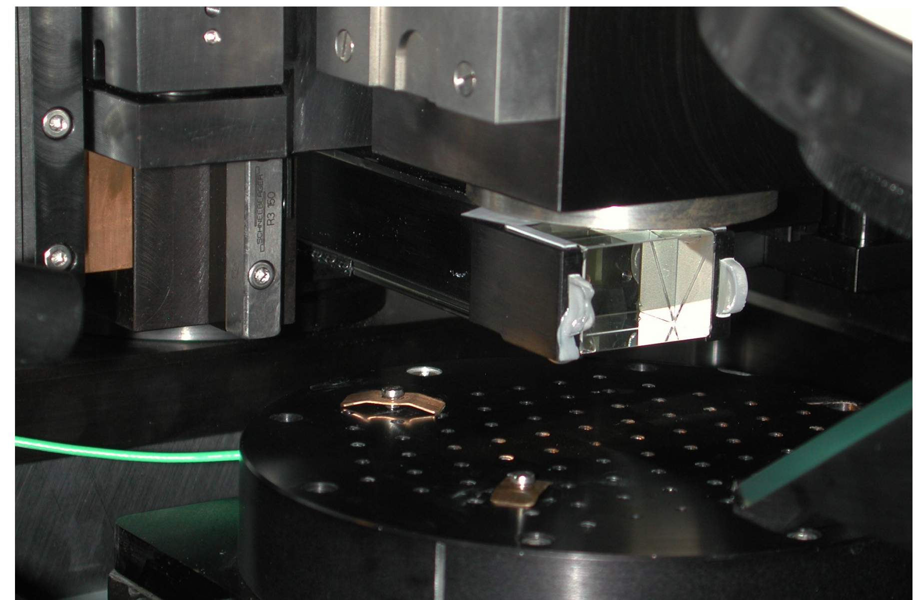




“Manual” Chip Placement

- Machine constructed and built in 1997
- ROC and sensor viewed at the same time through a prism
- Very flexible
- 3-4h per 16-chip module
- Operation “tedious” (practical limit: ~2-3 modules/week including inspections)
- Used so far for
  - ~50 multi-chip modules
  - many single chip sensors
  - ~1000 chips in total
- Was replaced by automatic machine for “large scale” production (~1000 modules)





Conclusions

- Bump bond process successfully developed
- Process features
  - UBM of Ti/Ni/Au on both sides
  - “Thick” Indium bumps on the sensor
  - “Thin” Indium layer on ROC
  - Reflow of In bumps and joined module
- Bump yield better than 99.9%
- Construction CMS pixel finished
- Bumping single dies is (in principle) possible
- “Cold” flip chip procedure for irradiated sensors was developed for a low number of samples
  - Make large efforts to avoid this in future !!!