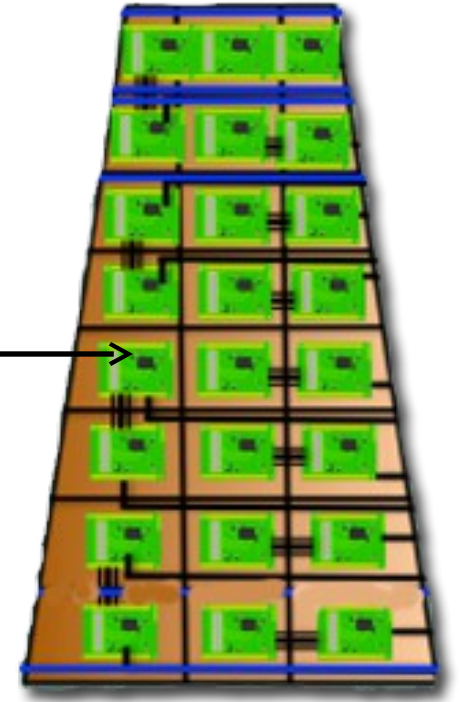
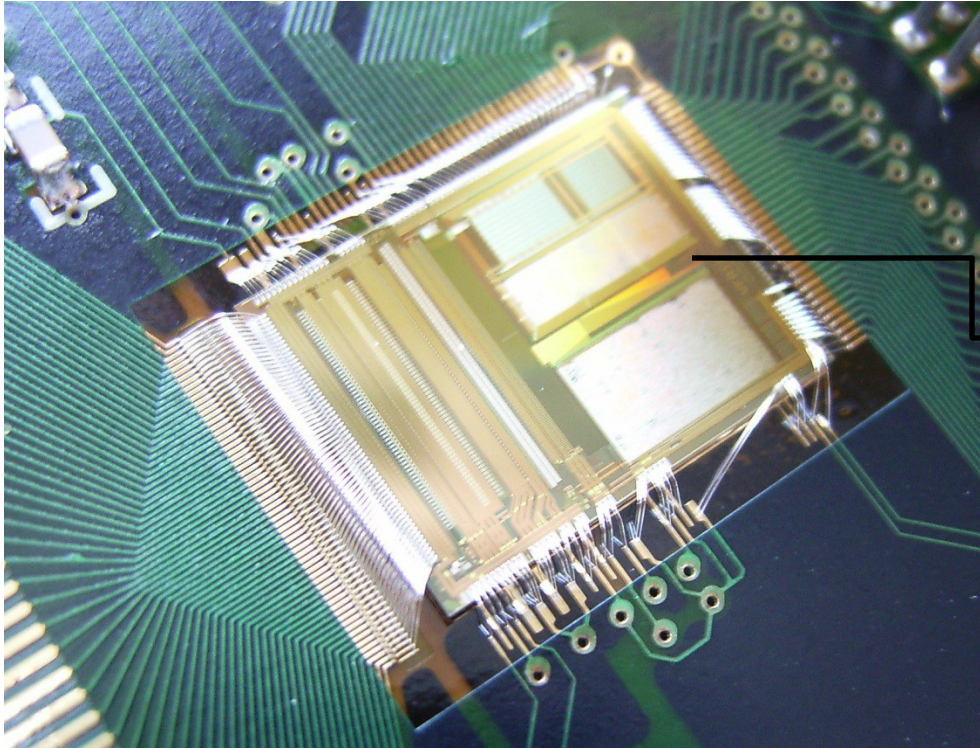

Extracting the VFAT2 data for SRS

Rehab Masod



VFAT2 (Trigger and Tracking)

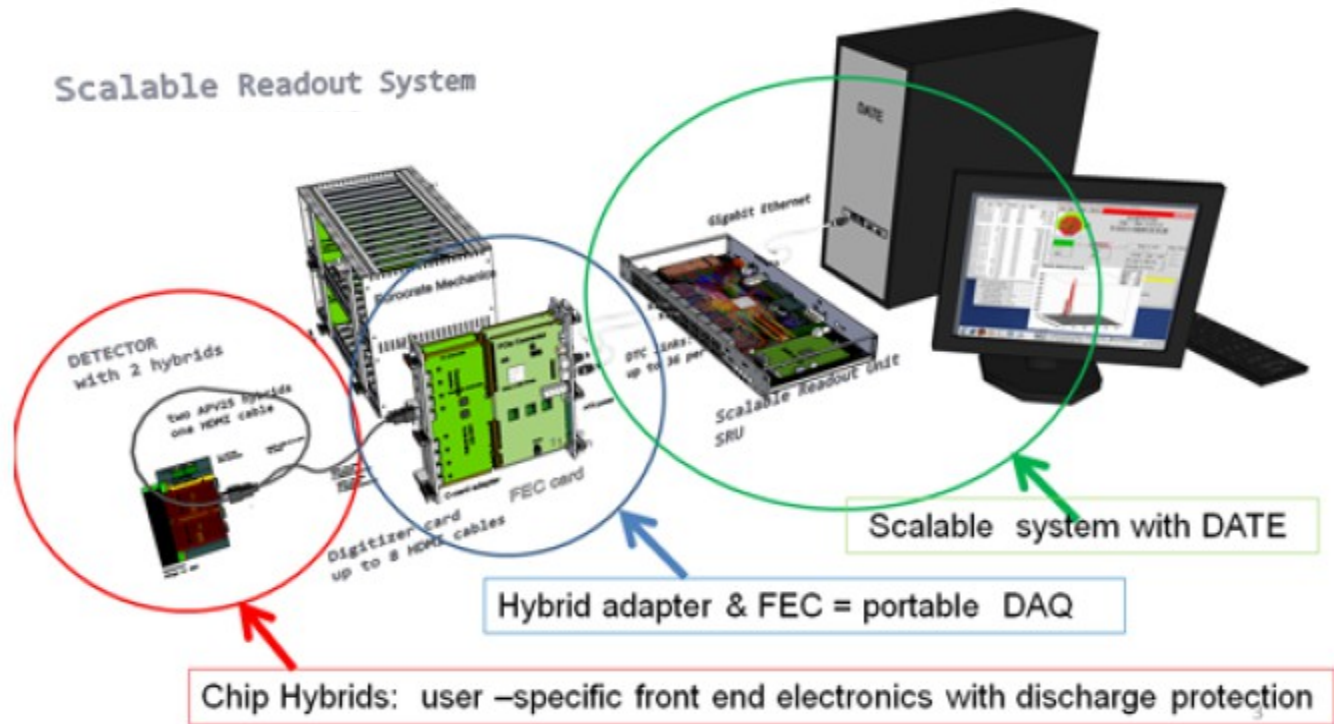


A front end “system on chip” providing fast trigger information and digitized data storage for the charge sensitive readout of multichannel silicon and gas particle detectors.

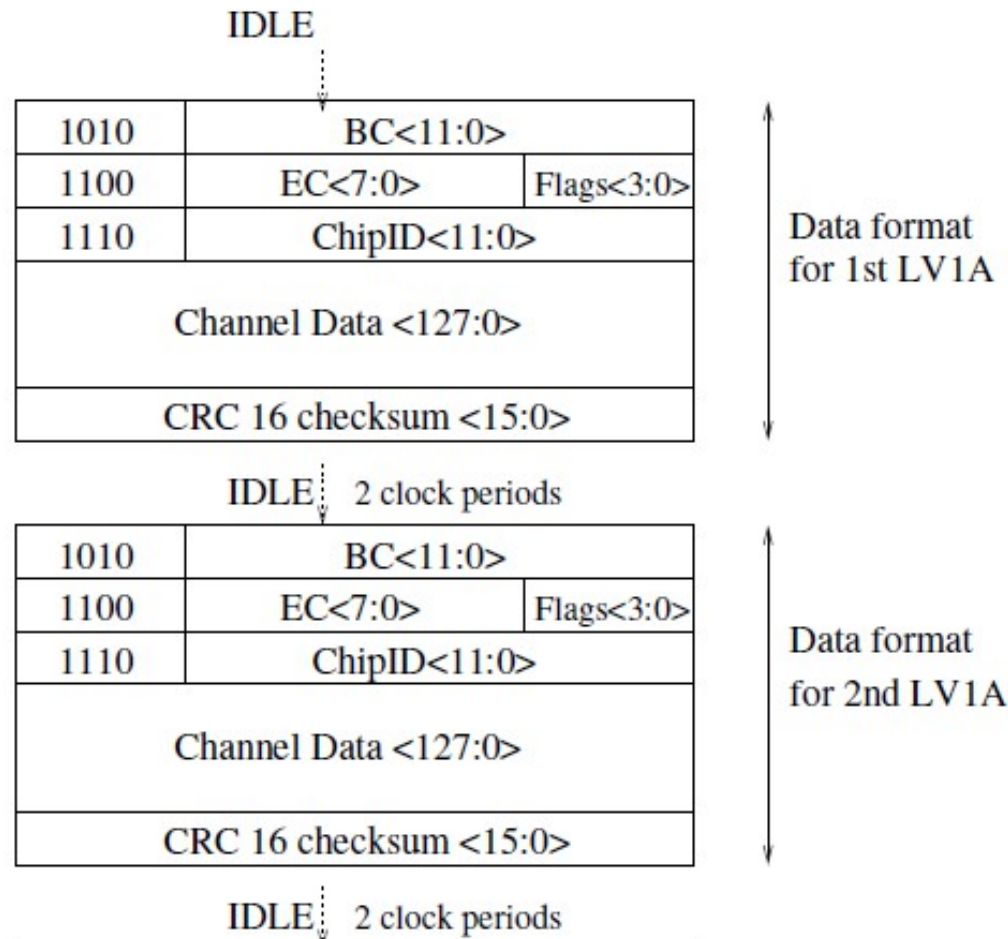


Scalable Readout System (SRS)

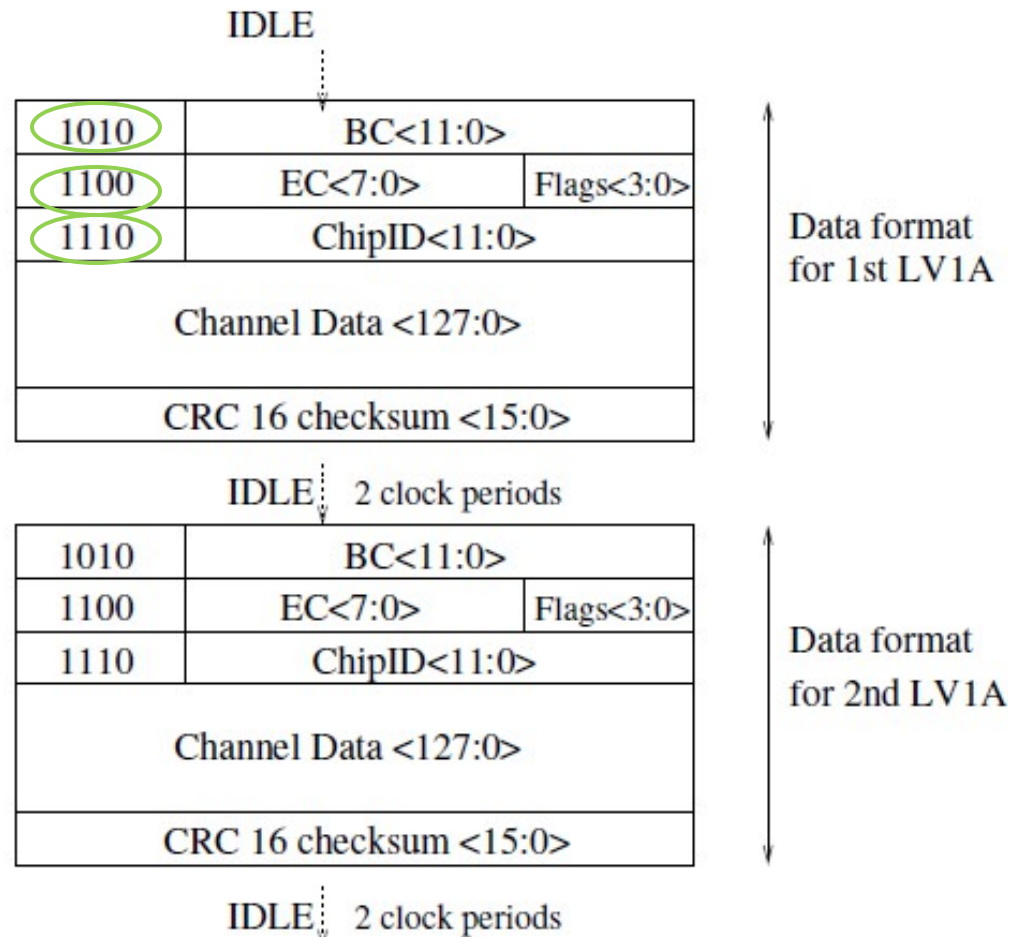
physical overview SRS of RD51



Data format



Data format



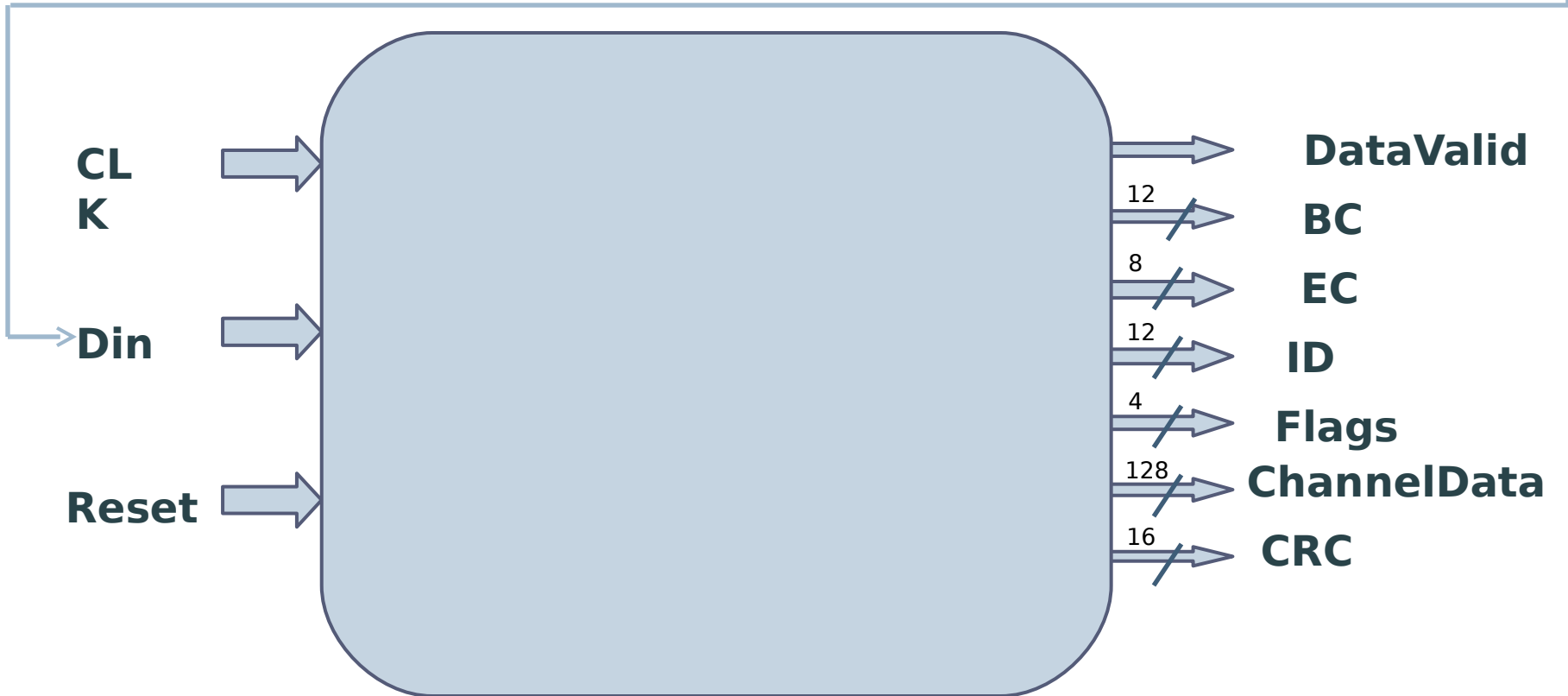
Entity of data out from VFAT2



Entity of data out from VFAT2

000	1010101010	11000	110	1100	11111	000	01010	0001
1	1		0	0	0	1		

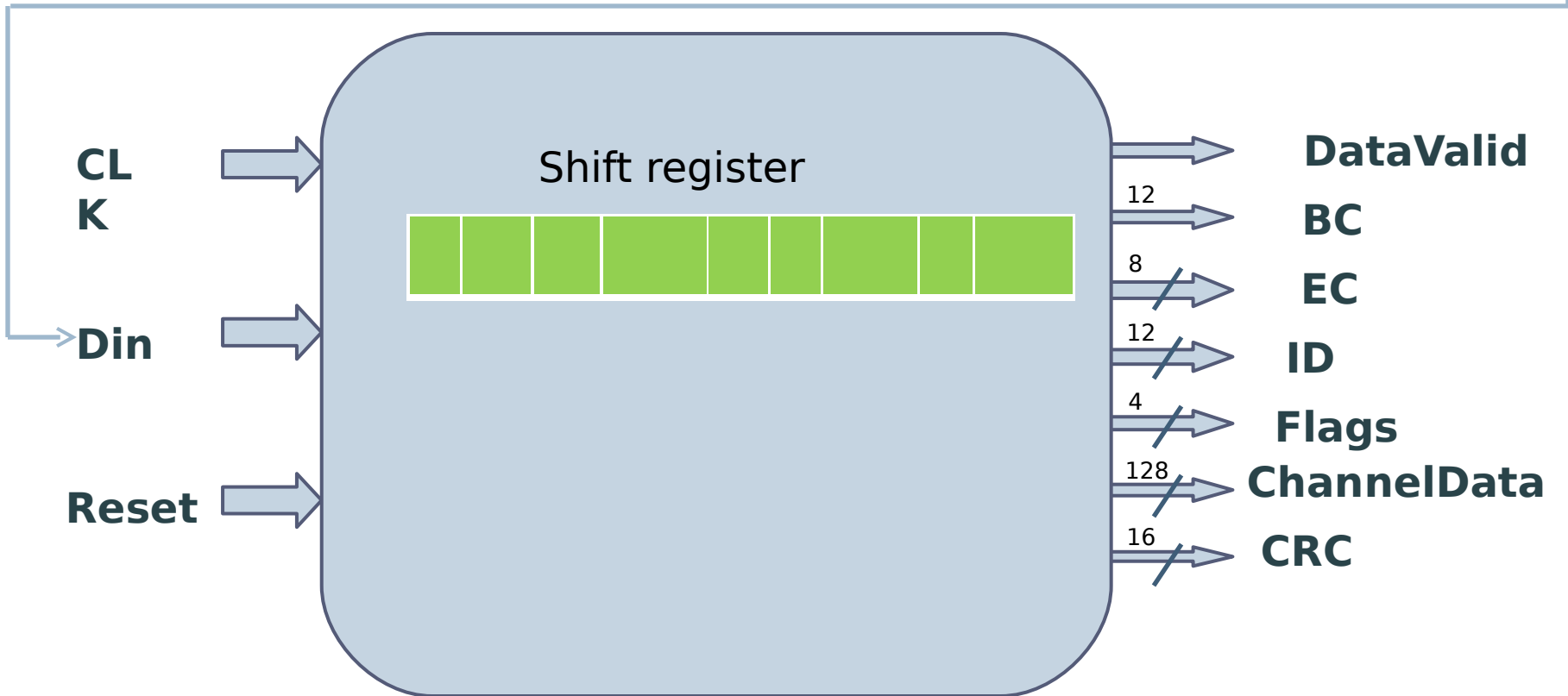
Data from VFAT2



Entity of data out from VFAT2

000	1010101010	11000	110	1100	11111	000	01010	0001
1	1		0	0	0	1		

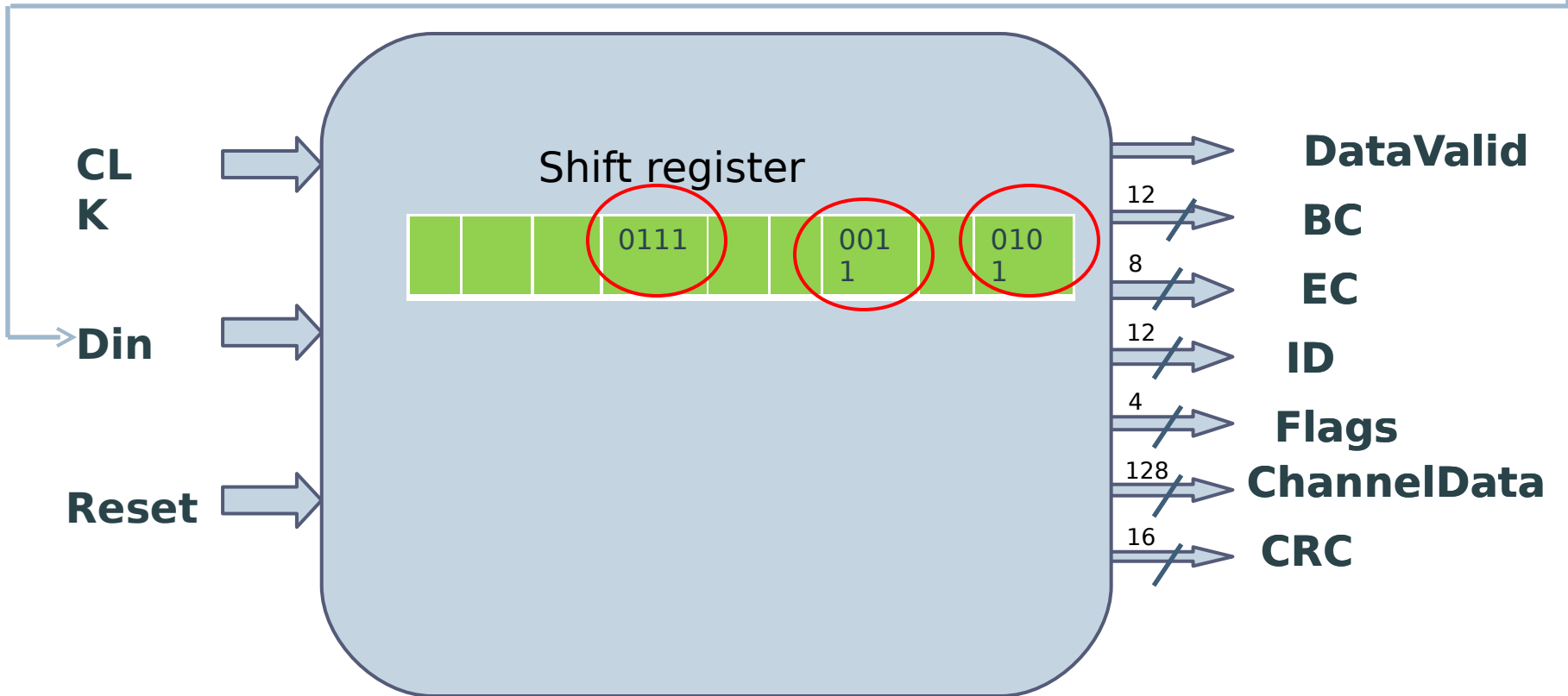
Data from VFAT2



Entity of data out from VFAT2

000	1010101010	11000	110	1100	11111	000	01010	0001
1	1		0	0	0	1		

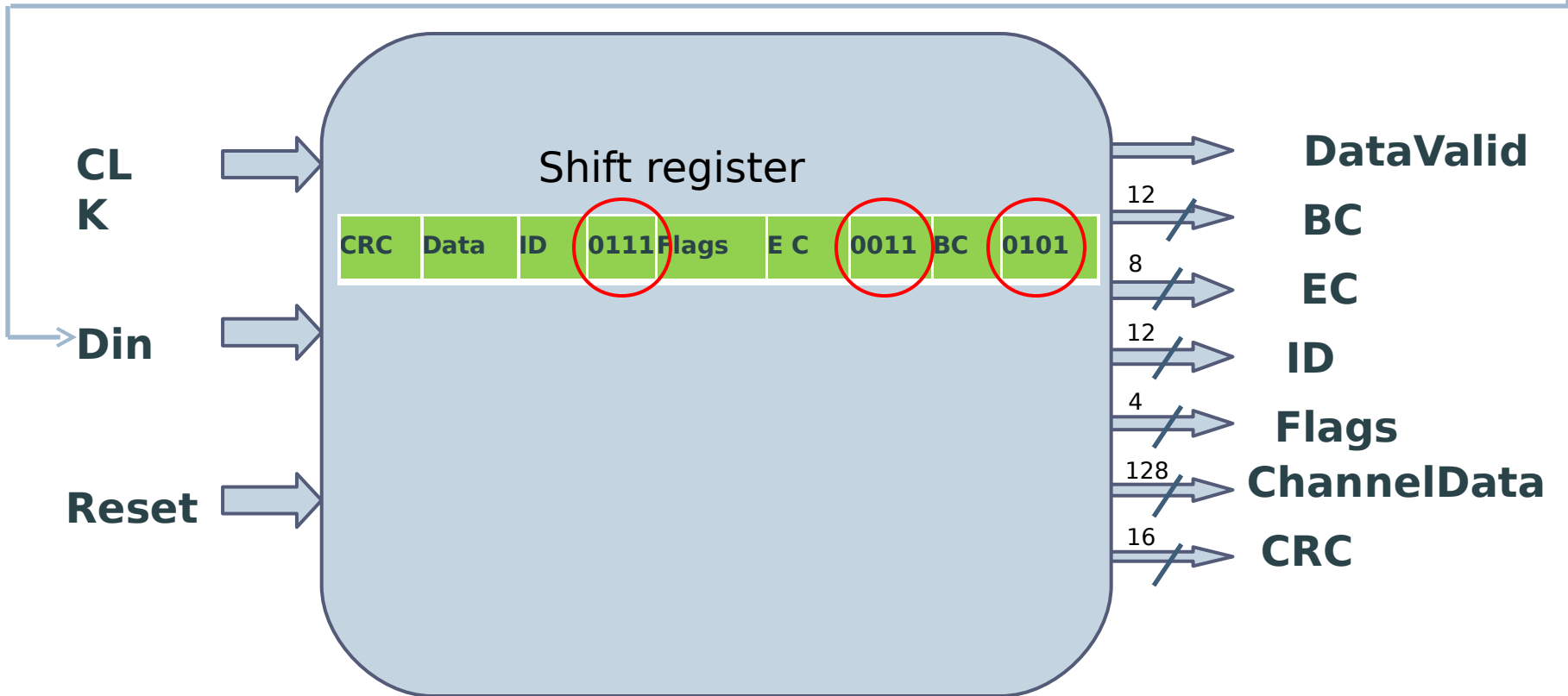
Data from VFAT2



Entity of data out from VFAT2

000	1010101010	11000	110	1100	11111	000	01010	0001
1	1		0	0	0	1		

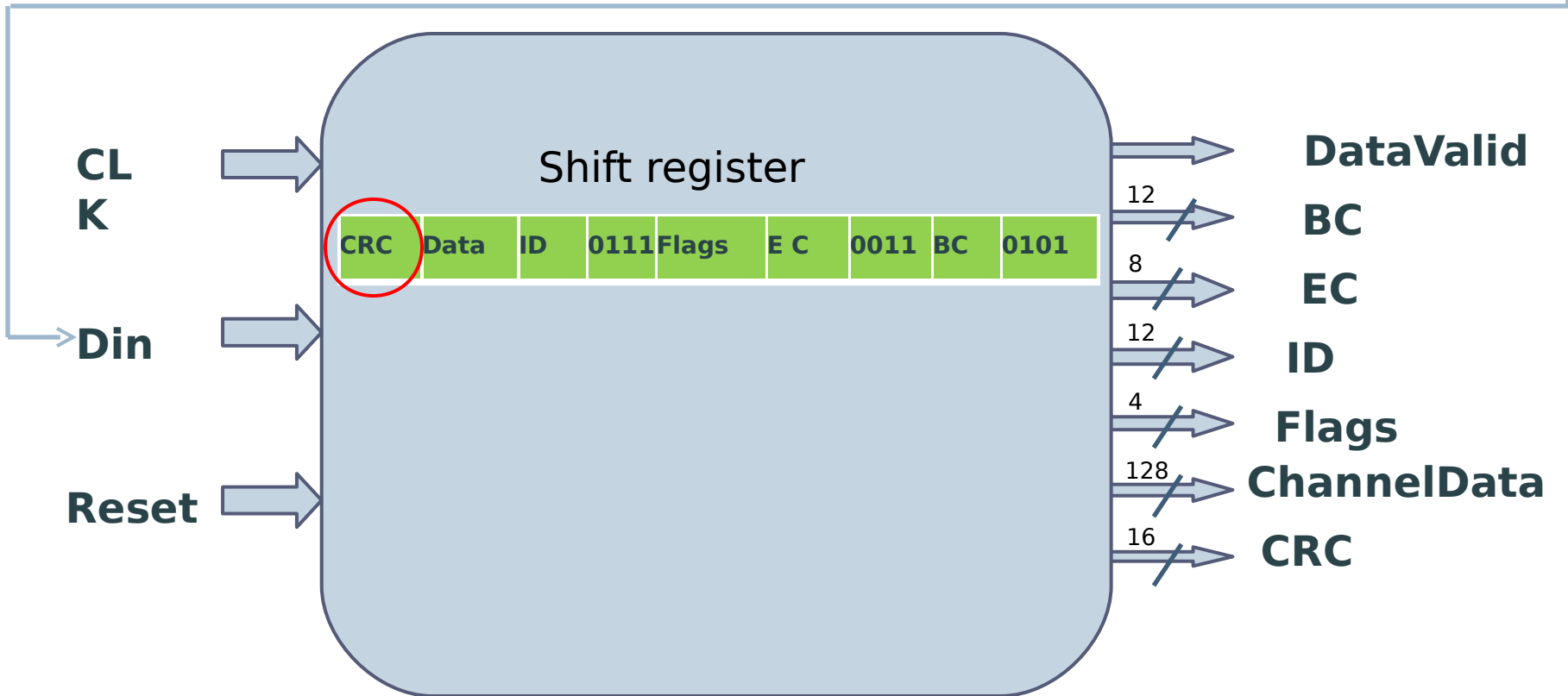
Data from VFAT2



Entity of data out from VFAT2

000	1010101010	11000	110	1100	11111	000	01010	0001
1	1		0	0	0	1		

Data from VFAT2



EDA tool

The screenshot displays the Xilinx ISE IDE interface. The main window shows the VHDL source code for an entity named 'DataOut'. The code includes library declarations for IEEE and UNISIM, followed by an entity declaration with a port list. The architecture is behavioral and defines several signals.

```
2 library IEEE;
3 use IEEE.STD_LOGIC_1164.ALL;
4 use IEEE.STD_LOGIC_ARITH.ALL;
5 use IEEE.STD_LOGIC_UNSIGNED.ALL;
6 --library UNISIM;
7 --use UNISIM.VComponents.all;
8 -----Entity
9 entity DataOut is
10 Port ( Clk      : in   STD_LOGIC;
11        Din       : in   STD_LOGIC;
12        Reset    : in   STD_LOGIC;
13        DataValid : out  STD_LOGIC;
14        Dout     : out  STD_LOGIC_VECTOR (127 downto 0);
15        BC       : out  STD_LOGIC_VECTOR (11 downto 0);
16        EC       : out  STD_LOGIC_VECTOR (7 downto 0);
17        Flags    : out  STD_LOGIC_VECTOR (3 downto 0);
18        IDVal    : out  STD_LOGIC_VECTOR (11 downto 0);
19        CRC      : out  STD_LOGIC_VECTOR (15 downto 0));
20 end DataOut;
21 -----architecture
22 architecture Behavioral of DataOut is
23 -----Signals
24 signal DataOut      : STD_LOGIC_VECTOR (127 downto 0) := (others => '0');
25 signal BCVal        : STD_LOGIC_VECTOR (11 downto 0) := (others => '0');
26 signal ECVal        : STD_LOGIC_VECTOR (7 downto 0)  := (others => '0');
27 signal FlagsVal     : STD_LOGIC_VECTOR (3 downto 0)  := (others => '0');
28 signal IDVal        : STD_LOGIC_VECTOR (11 downto 0) := (others => '0');
29 signal CRCVal       : STD_LOGIC_VECTOR (15 downto 0) := (others => '0');
```

The interface includes a 'Sources' pane on the left showing the project hierarchy, a 'Processes' pane with simulation options, and a 'Transcript' pane at the bottom with tabs for Console, Errors, Warnings, Tcl Shell, and Find in Files. The status bar at the bottom right shows 'CAPS NUM SCRL Ln 17 Col 56 VHDL'.

Simulation

The screenshot displays the ISim (O.87xd) simulation environment. The main window shows a waveform plot with a time scale of 1.00us. The waveform displays several signals: clk, din, reset, datavalid, channeldat, bc[11:0], ec[7:0], flags[3:0], id[11:0], crc_chek[15:0], data_t[0:19], and clk_period. The data_t[0:19] signal shows a hexadecimal value of a934c885e1351234567891234567891234567891234544fb. The waveform is zoomed in to 5 ps per division (X1: 5 ps).

The Objects panel shows the simulation objects for data_out_tb. The Object Name and Value columns are as follows:

Object Name	Value
clk	1
din	1
reset	0
datavalid	0
channeldat...	0000000000000000
bc[11:0]	000000000000
ec[7:0]	10001000
flags[3:0]	0000
id[11:0]	000000000000
crc_chek[15...	0100010011111011
data_t[0:19]	1010100100110100
clk_period	25000 ps

The Console window shows the following output:

```
# run 1.00us
# run 1.00us
# run 1.00us
```

The bottom status bar indicates the simulation time: Sim Time: 8,000,000 p

Simulation

The screenshot displays the ISim (O.87xd) simulation environment. The main window is titled "ISim (O.87xd) - [Default.wcfg*]". The interface includes a menu bar (File, Edit, View, Simulation, Window, Layout, Help), a toolbar, and several panels.

Instances and Processes: Shows the instance and process name "data_out_tb".

Objects: Lists simulation objects for "data_out_tb".

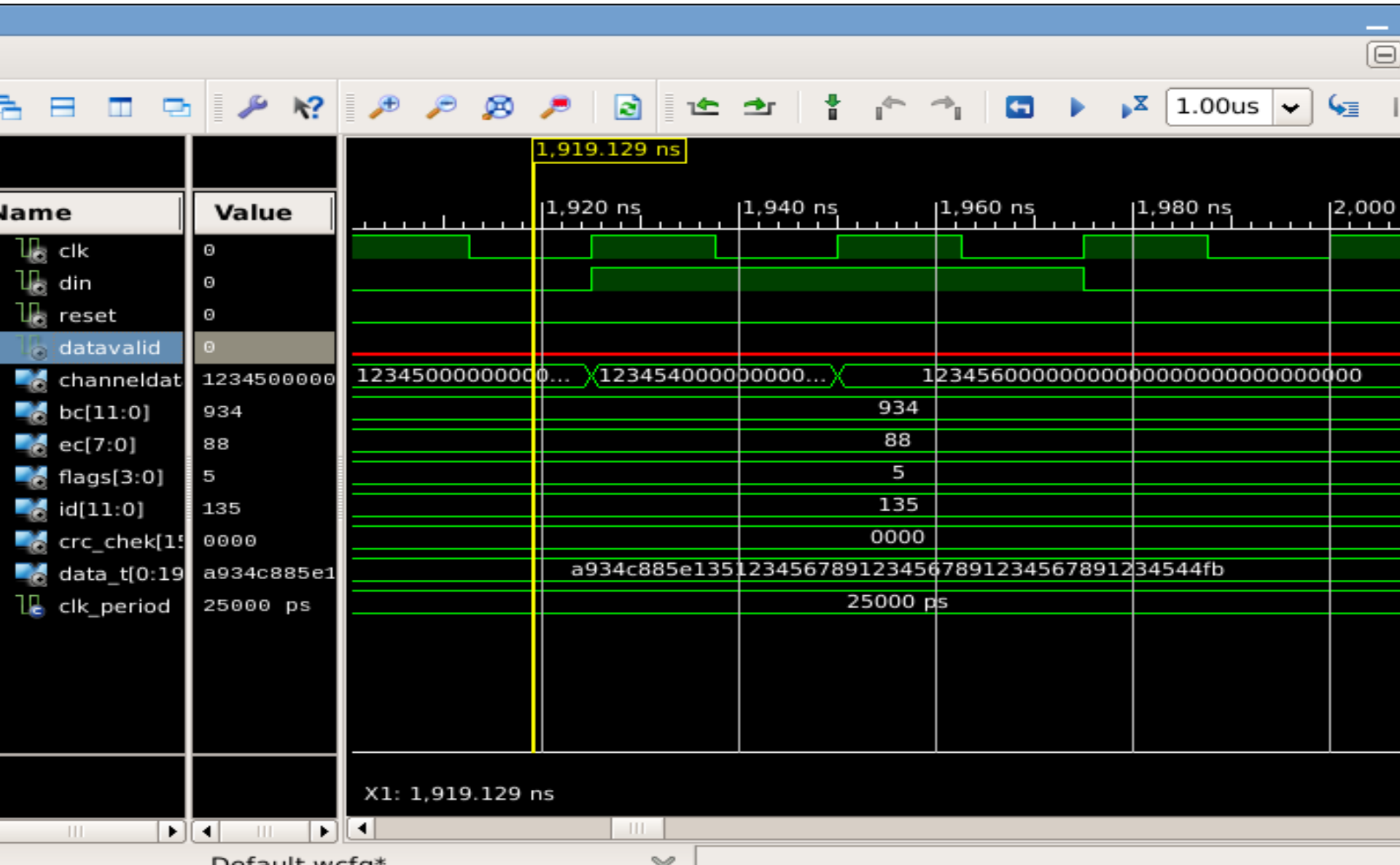
Object Name	Value
clk	1
din	1
reset	0
datavalid	0
channeldat...	0000000000000000
bc[11:0]	000000000000
ec[7:0]	10001000
flags[3:0]	0000
id[11:0]	000000000000
crc_chek[15...	0100010011111011
data_t[0:19]	1010100100110100
clk_period	25000 ps

Timing Diagram: Shows a waveform with a time scale of 1.00us. A vertical yellow line marks a time point of 1,383.129 ns. The waveform displays signals for clk, din, reset, datavalid, channeldat, bc[11:0], ec[7:0], flags[3:0], id[11:0], crc_chek[15...], data_t[0:19], and clk_period. The data_t[0:19] signal shows a hexadecimal value of a934c885e1351234567891234567891234567891234544fb.

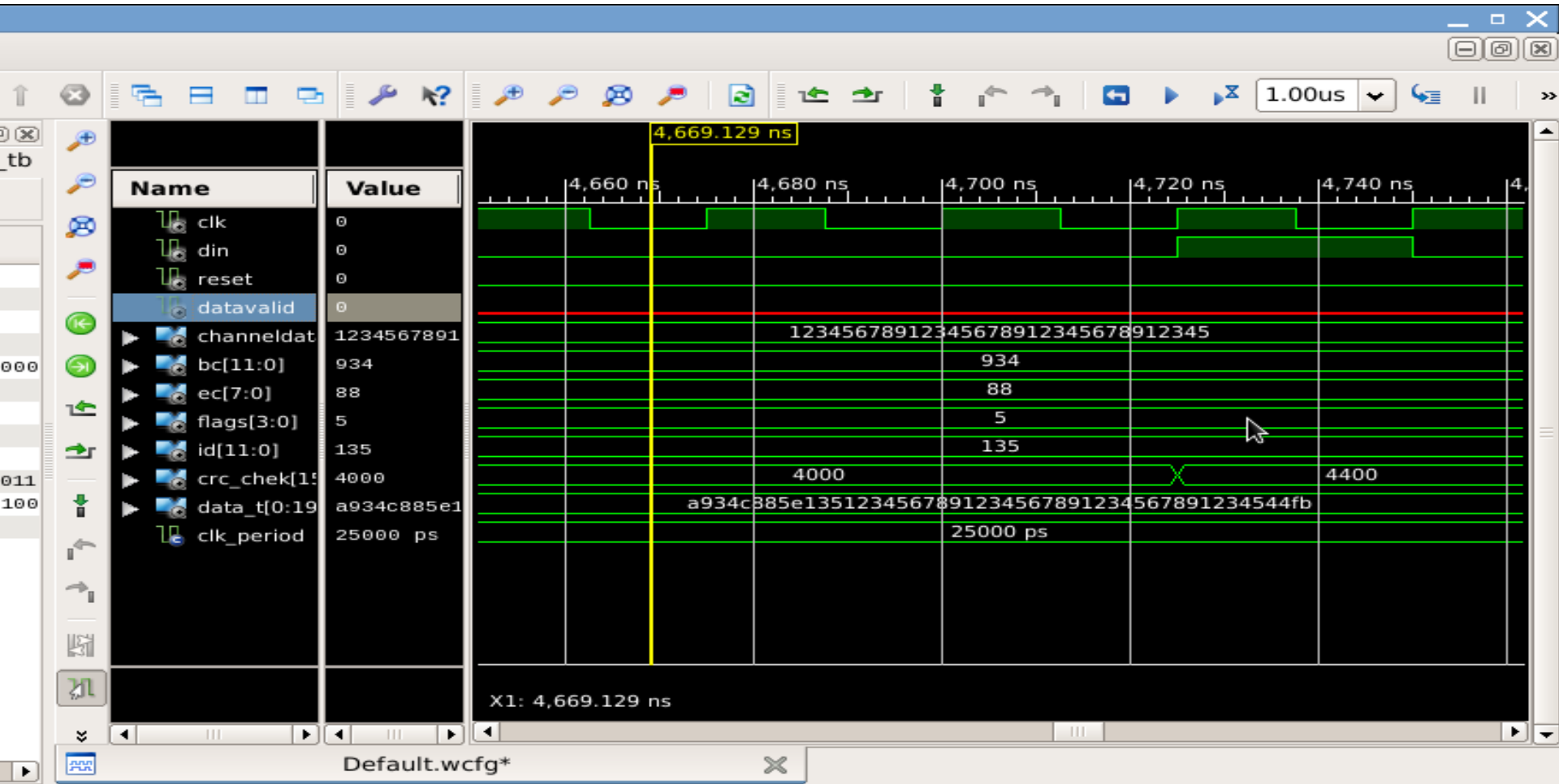
Console: Shows the command "# run 1.00us" repeated three times.

Bottom Panel: Includes tabs for Console, Compilation Log, Breakpoints, Find in Files Results, and Search Results. The status bar indicates "Sim Time: 8,000,000 ps".

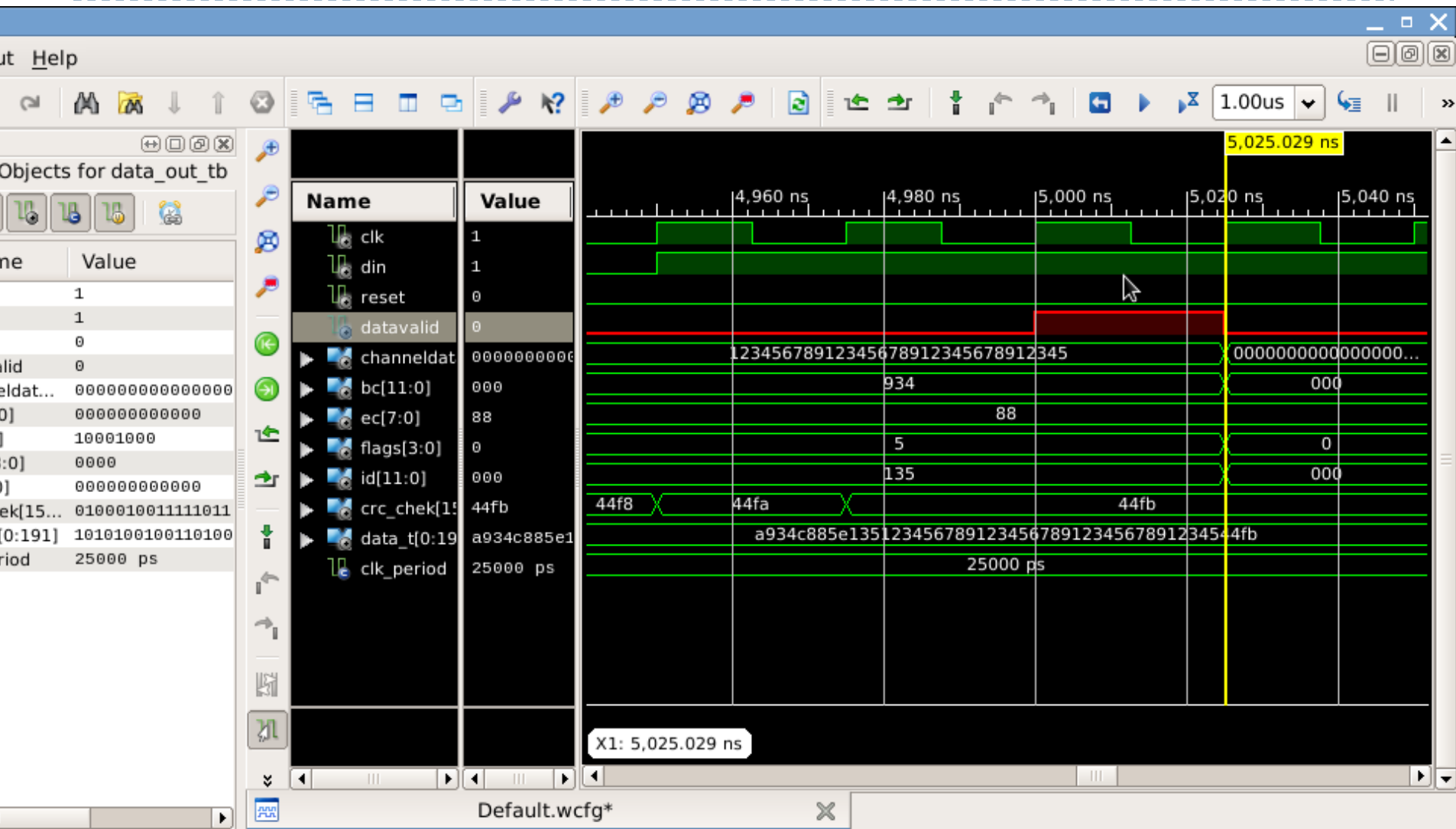
Simulation



Simulation



Simulation



Thank you

