LHC-LARP WP4 Feedback Project

-*System Hardware Development Progress and Plans* -

J. Dusatko

November 15, 2013

Contributors / Collaborators

SLAC:

J. Fox, J. Cesaratto, C. Rivetta, O. Turgut, K. Pollock, J. Olsen, C. Yee, J. Dusatko

CERN:

W. Hofle, U. Wherle, G. Kotzian, H. Bartosik, D. Valuch

Outline

1) Introduction
2) Feedback Demo System Progress
3) 8GSa/s Architecture Upgrade
4) CERN Collaboration
5) PLL/Delay Controller Progress
6) Amplifier Testing Progress
7) Development Roadmap

Introduction

- As part of the High-Lumi Larp Feedback Project, a 4GSa/s general-purpose signal processing prototype demonstrator system was developed for proof-of-concept intrabunch transverse instability control studies for the SPS.

- This system was designed and developed in less than a year at SLAC; and builds on the components developed for the Excitation system. It provides a proof-of-concept test bed for feedback technologies and techniques.

- The system was developed to initially control a single bunch within the SPS; however, this is expandable
  - Utilizes FPGA technology, allowing for reconfigurability.

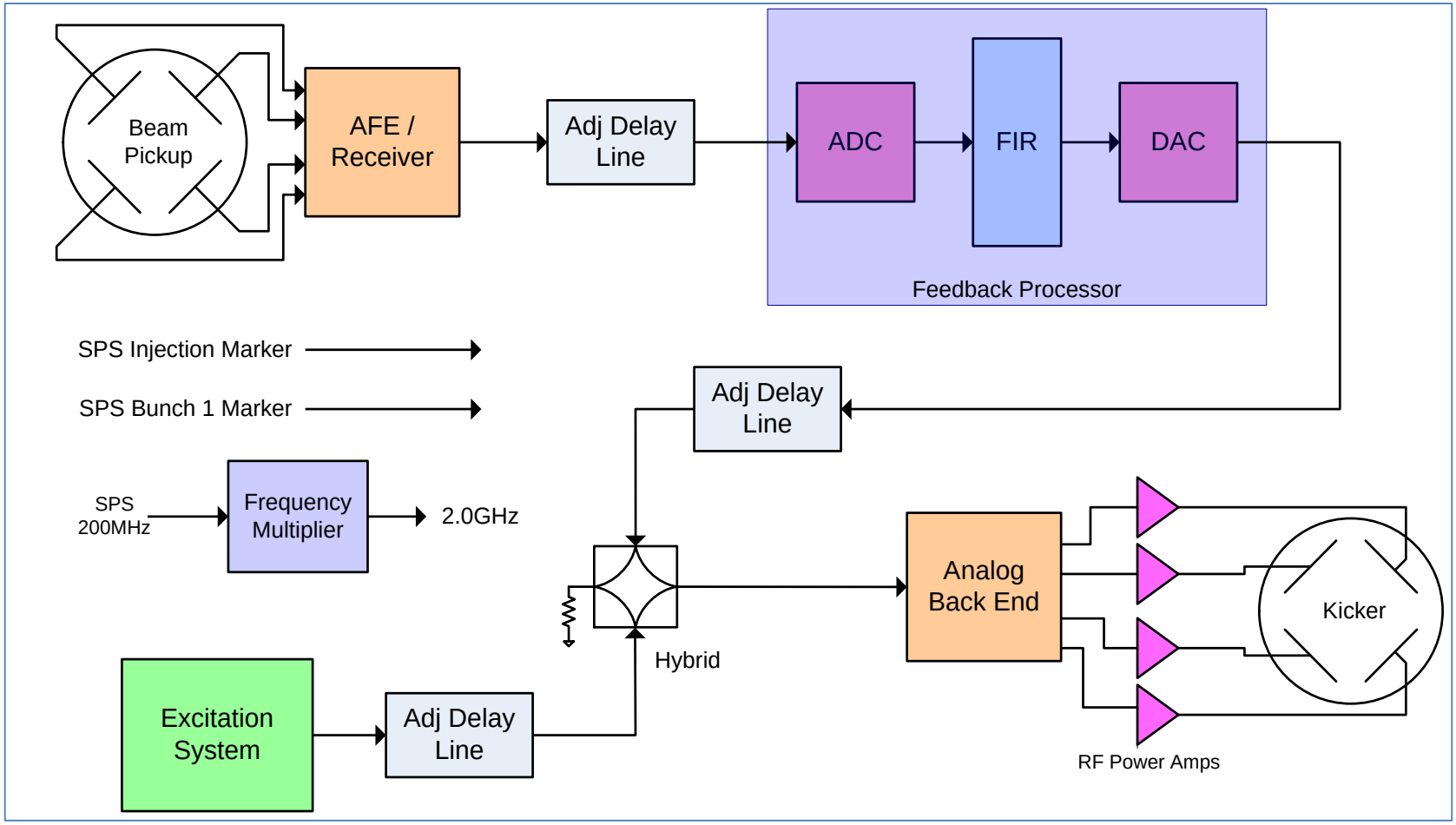
- Was used in MD studies from November 2012 to February 2013
  - A wealth of useful data was collected and is being analyzed
  - Preliminary results show that closed loop control of mode 0 was achieved

- The next step is to expand the demonstrator system to develop functionality, technologies and techniques for the final full-feature system prototype.

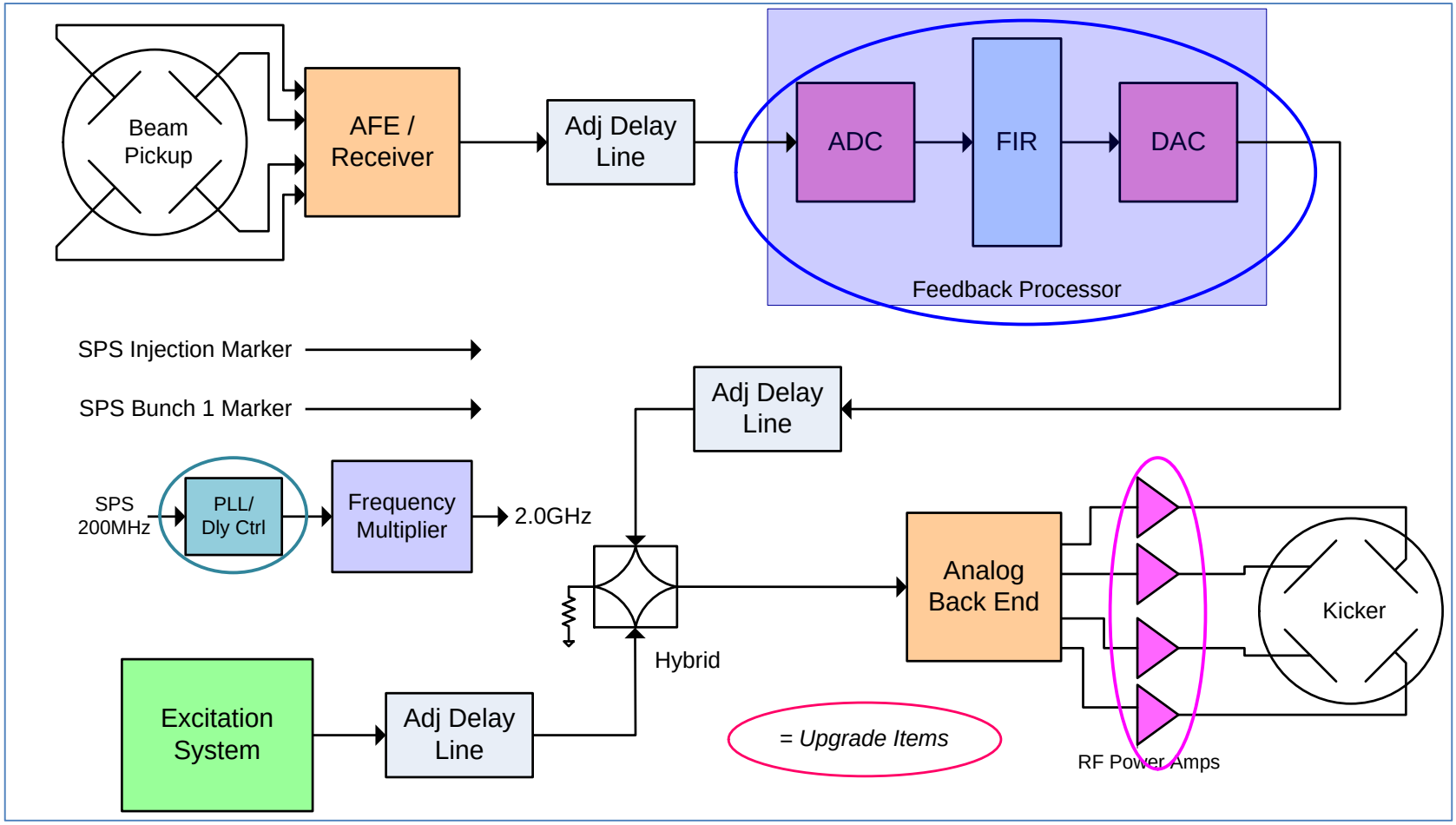
→ NOTE: The current "box" is a prototype intended to be an test bed for the final full-featured prototype, which will be a different design (it will be custom-tailored to fit into the CERN SPS systems).

- Other HW upgrade work going on:
  - Development of a PLL/Delay Controller (Sync DAC/Adj. delays automatically following SPS ramp)
  - Evaluation/Characterization of new RF power amplifiers

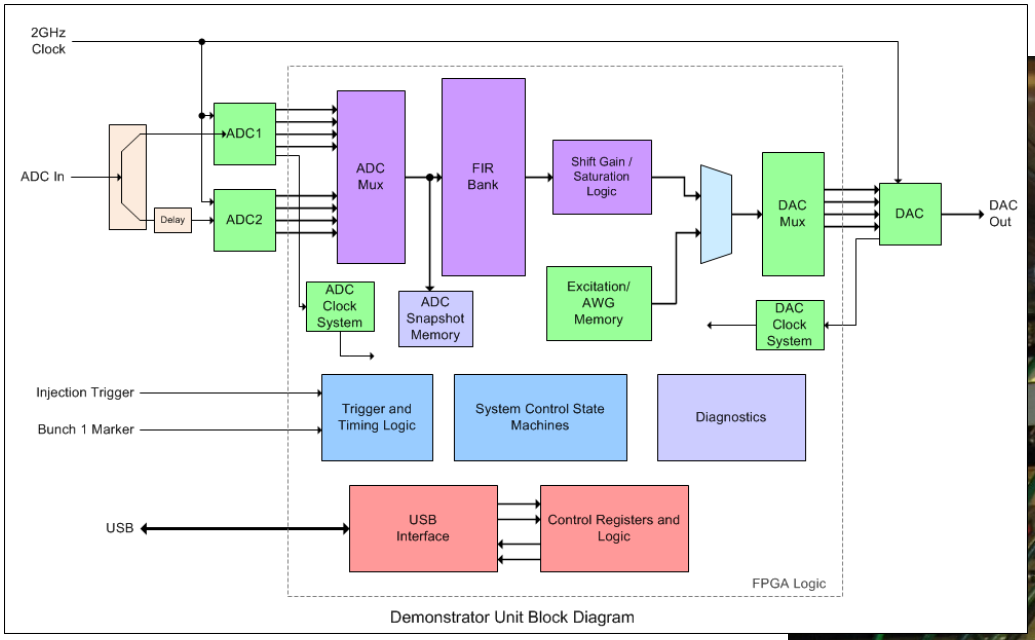
Overall System Block Diagram



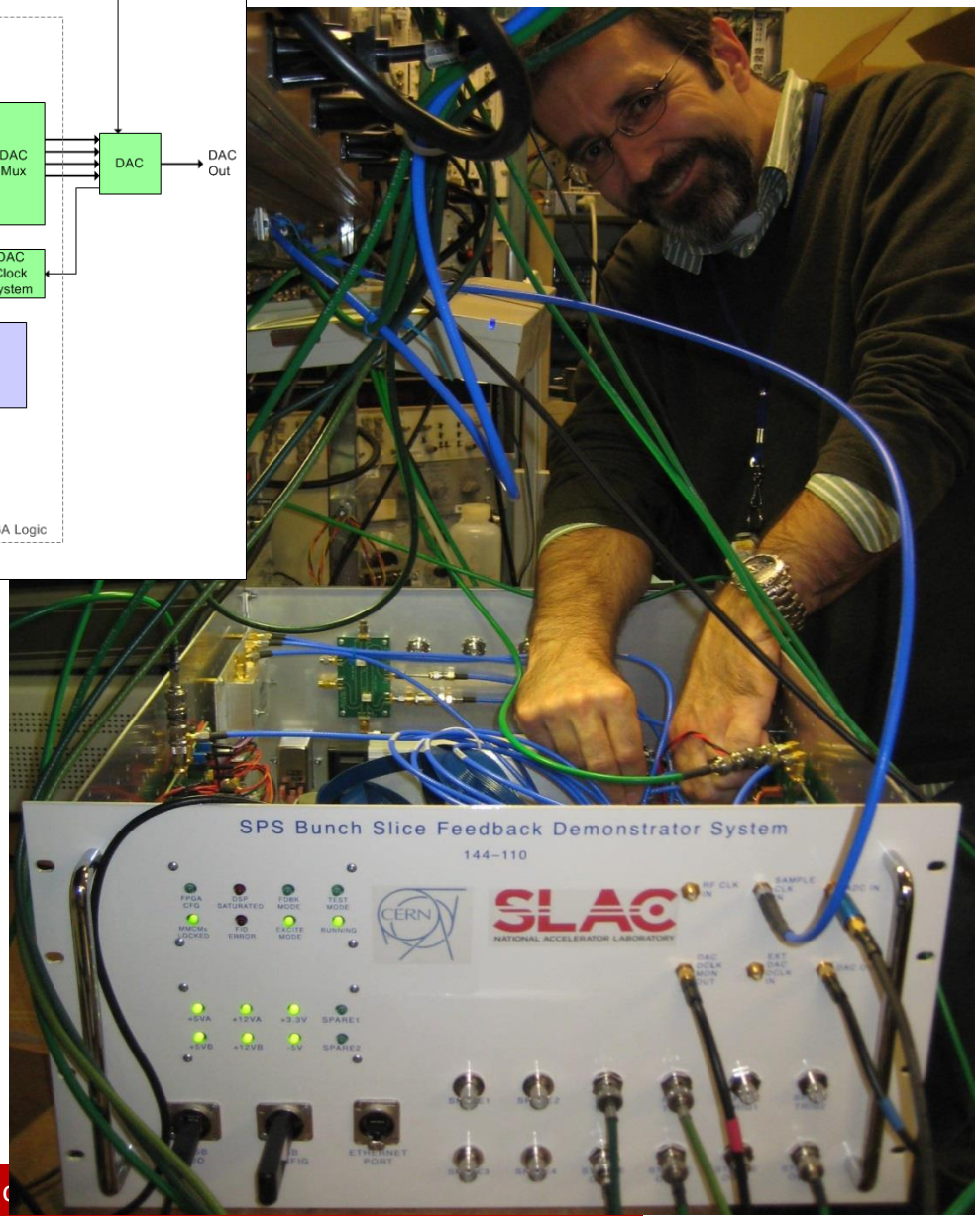
Overall System Block Diagram - Upgrades



The Feedback Processor



Demonstrator Unit Block Diagram



Features:

- Maxim MAX19693 12-bit 4 GSa/s DAC
- Two Maxim MAX109 2GSa/s 8-bit ADCs interleaved to get 4 GSa/s
- Xilinx Virtex-6 FPGA for all digital signal processing
- Multi-mode operation: Feedback channel -or- Excitation/AWG
- Timing and Trigger processing
- Diagnostics include:
  - ADC Snapshot memory
  - Trigger rate and missing trigger
  - DSP Saturation Indicator
- USB 2.0 Interface to host
- Suite of Visual Basic & Matlab SW

Feedback Hardware Upgrade Plans

- With the success of the single-bunch demonstrator, we plan on adding the following enhancements:
  - **Multi-Bunch Control**: Preliminary design studies suggest that the demonstrator platform can be expanded to serve at least one SPS batch (48 bunches) / Can handle scrubbing bunch directly at full rate (estimated 24 bunchlets), or a greater number at lower sampling rates (e.g. 48 bunchlets at 2GSa/s) / Ultimate limitation is FPGA internal resources (FPGA + SW work)
  - **Orbit Offset Rejection**: Bunch-by-bunch orbit offset rejection via use of common mode range of ADC. Adds two bits of dynamic range to the front end / Will implement only for single-bunch initially (small amount of HW + FPGA + SW work)
  - **Excite/Record Mode**: Add the ability to record into Snapshot memory while playing out an excitation sequence (FPGA + SW work)
  - **DAC Clock Synchronization**: The DAC device has no reset, so its four input samples can't lock to a consistent sample clock phase / PLL being developed to fix this (HW work)
  - **Deeper Snapshot Memory**: On-board RAM enables up 100K+ turns to be stored (FPGA + SW work)

  → These items are our initial plan, but can add additional features/changes to enhance usefulness

  → We plan on adding these functions for the upcoming 2014 run

Feedback ADC Noise Mitigation

The Problem:

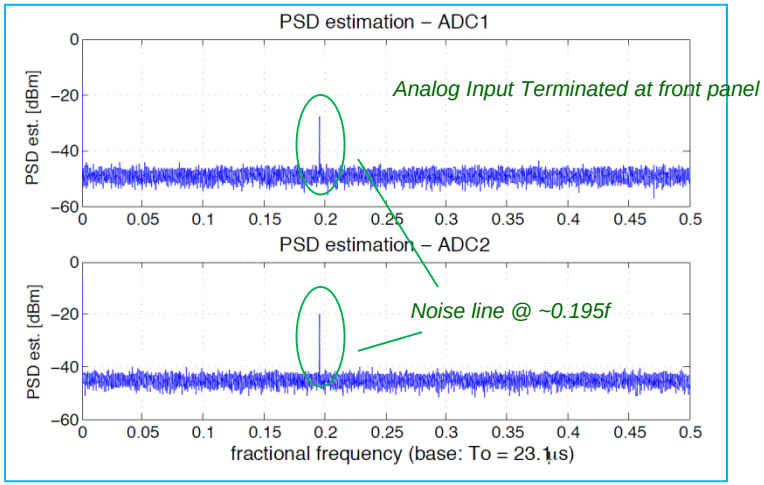
- In analyzing the data taken during the Machine Development runs, a spectral line was discovered in the FFTs of the ADC snapshot data.
- This noise line was present even without any input signal to the ADCs (i.e. the analog input was terminated into 50 ohms at the chassis front panel).
- The noise is at a frequency quite close to the SPS betatron tune frequency and interferes with our measurements.

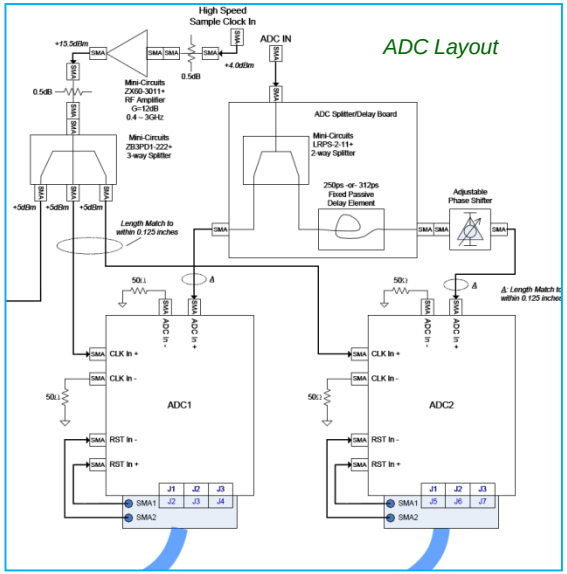
The Cause:

- Subsequent investigation revealed that the signal and power grounding system of ADCs and the chassis was not optimal and created high-impedance paths, allowing currents to flow in the ground system.
- The ADCs are actually separate circuit boards (evaluation boards purchased from the ADC manufacturer)
  - This approach was taken in order to develop the prototype rapidly

The Fix:

- The fix will involve creating a low-impedance ground system between both ADC boards and the chassis ground (essentially mount boards on a copper plate with distributed, low impedance grounds)
- The work will start soon
- The <u>ultimate</u> fix is to design a proper ADC daughterboard – this should be done for the full-featured prototype





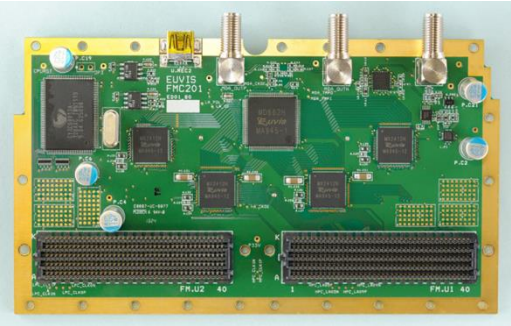
Towards an 8GSa/s Architecture

- Currently, the 4GSa/s architecture allows us to take 16 samples across an SPS bunch

- Increasing the sampling rate to 8GSa/s allows us even greater flexibility:
  - Increased sampling resolution (32 samples across a single bunch)
  - Single ultra-fast 8GSa/s feedback channel
  - Dual 4 GSa/s channels for two sets of pickups and kickers
  - Enhanced diagnostics

- To accomplish this, we need faster ADCs and DACs:

  - **DAC**: Have identified a high speed DAC (Euvis, Inc. MD662H DAC device: 8GSa/s, 12-bits) / Purchasing a demo board from the company and will begin evaluating



  - **ADC**: Investigating High speed ADCs: most single ADCs are still limited to ~2GSa/s, so we must resort to interleaving techniques (some ADC makers are interleaving multiple ADCs on the same silicon die (e.g. Texas Instruments LM97600 4-channel 5GSa/s (interleaved), 8-bit ADC) / Note we already interleave two 2GSa/s ADCs in the current demo system

CERN Collaboration

- In order to ensure knowledge transfer and enhance our working relationship, we are pursing a deeper collaboration with CERN in the development of the Feedback System Hardware:

- CERN personnel visit to SLAC:
  - D. Valuch to visit SLAC for several weeks in late spring/early summer 2014
    - Provides the opportunity to learn about the Feedback hardware
    - Participate in development process
    - Perform measurements with the demo system
  - This will ensure a smooth transition in the handing off of the full-featured prototype to CERN

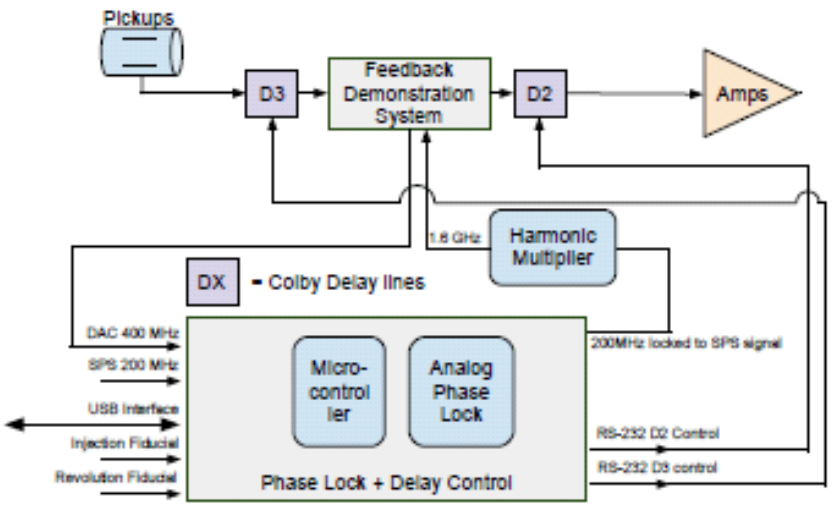
- Developing documentation for the system:
  - User Manual
  - SW Programming Guide
  - FPGA Gateware Description (in progress)

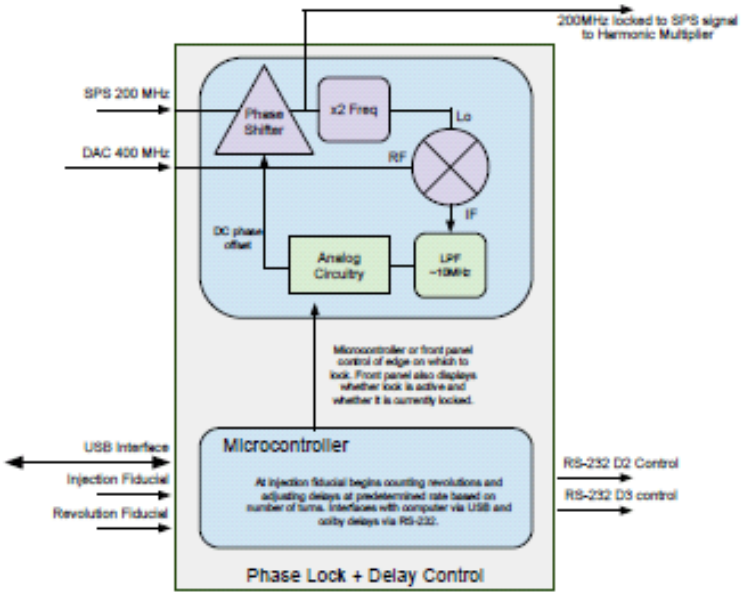
- Additional Collaboration:
  - Started a collaboration with J. Molendijk at CERN in the use of the CERN-developed Cheburashka tool and the use of the FPGA Wishbone bus protocol. The goal is to eventually implement the wishbone bus in the feedback system FPGA.

→ Collaboration will be crucial in the development and delivery of the "Productionized" Full-Featured Prototype to CERN

PLL/Delay Controller Development

- A system clock phase locked loop and automatic delay controller has been under development (*work done by K. Pollock*)
- The PLL will lock to the SPS 200MHz RF Clock and provide a deterministic clock phase for the DAC
- The Delay control will automatically adjust the passive delay lines as the SPS ramps / development is in its preliminary stages
- **Status**: PLL board is completed, undergoing testing and the chassis is being assembled



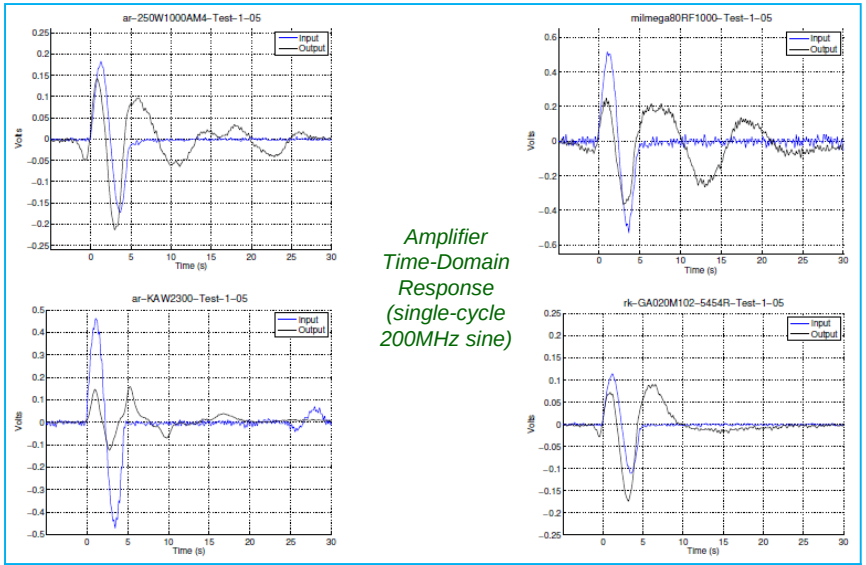


RF Power Amplifier Evaluation

RF Amplifier Evaluation and Characterization:
(*work performed by K. Pollock*)

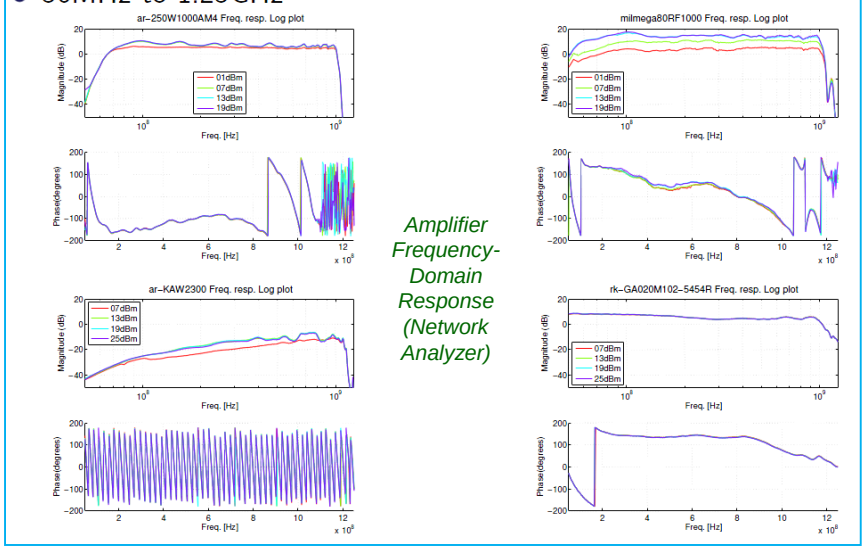
- The current RF power amplifiers exhibit non-optimal time-domain behaviour / differ widely in power response on a unit-to-unit basis / were forced to de-rate below specified maximum output power (100W → 80W)
- The challenge: most amplifier manufacturers design (and only test in this space) for CW operation, we required pulsed operation at wide bandwidth and high power
- Decided to find and evaluate a variety of amplifiers to determine their characteristics and see if they meet our requirements:
  - 20-1000MHz or 0-1000MHz / 100W power / Instantaneous BW / 100% ampl mod / Linear phase across the band
  - Developed a set of standard tests , tools and procedures for amplifier characterization
  - Tests were done in the time and frequency domains
- We performed these tests (plots on the right) on four different amplifier units (loaned to us for evaluation by the amplifier manufacturers):
  - MilMega 80RF1000-250
  - Amplifier Research KAW-2300 (modified)
  - R&K GA020M102-5454R
  - Amplifier Research 250W1000AM4

→ Results suggest the R&K amplifier performs closest to our requirements (lower right-hand plot in both time & frequency results to right)



Amplifier Time-Domain Response (single-cycle 200MHz sine)

- 50MHz to 1.25GHz



Amplifier Frequency-Domain Response (Network Analyzer)

Feedback Hardware Development Roadmap