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LHCb

LHCb Calorimeter Upgrade Electronics Review

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Universitat de Barcelona and La Salle

Calorimeter Upgrade Review – 14th June 2013 – CERN

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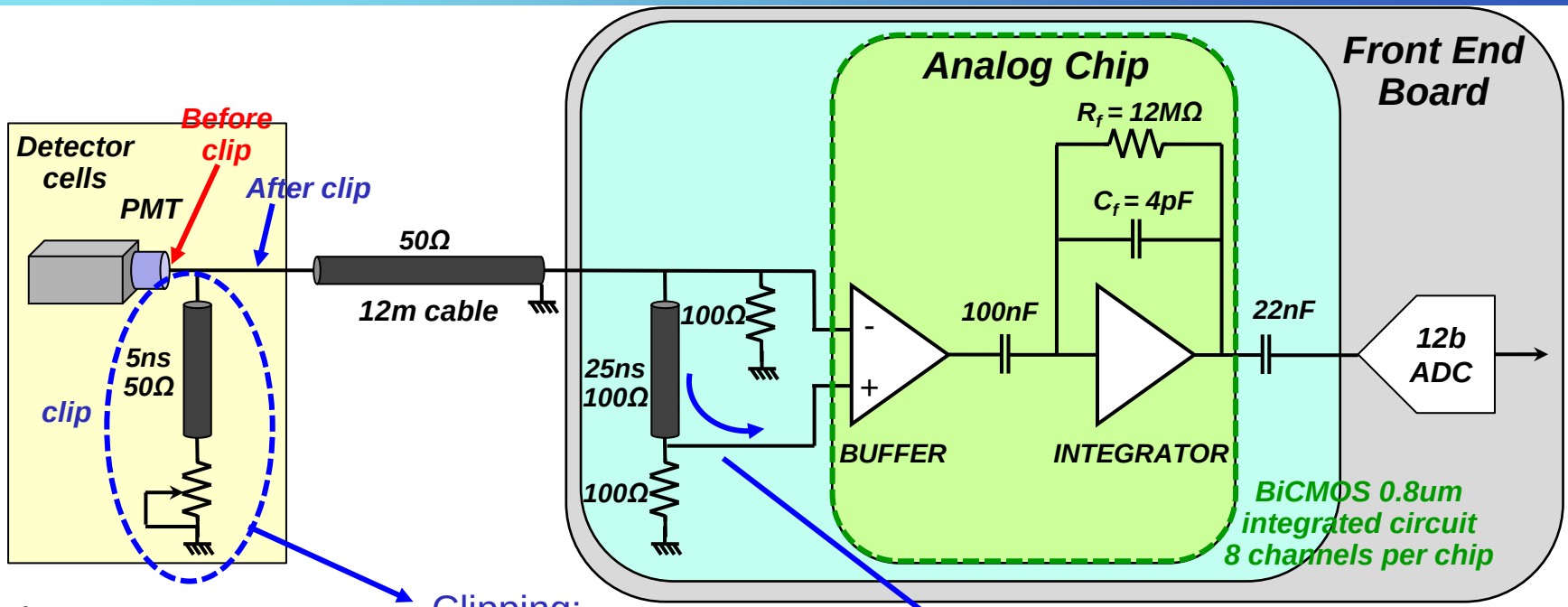
- Introduction
- Integrated Implementation
- COTS
- Test Beam
- Delay line
- Slow control

Current Analog Signal Processing



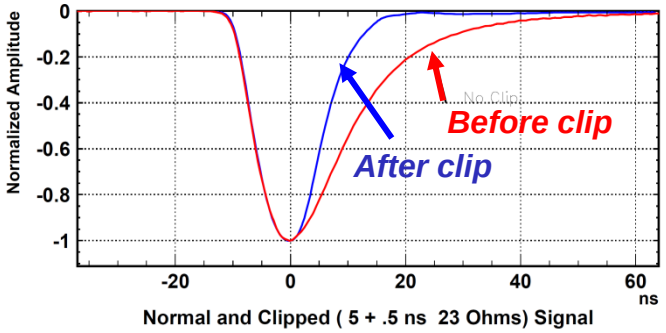
Specifications:

- Pulse shaping in 25ns
- Spill over < 1% after 25ns
- Integrator plateau: 4ns
- Linearity < 1%
- Rise time ~ 5 ns

Clipping:

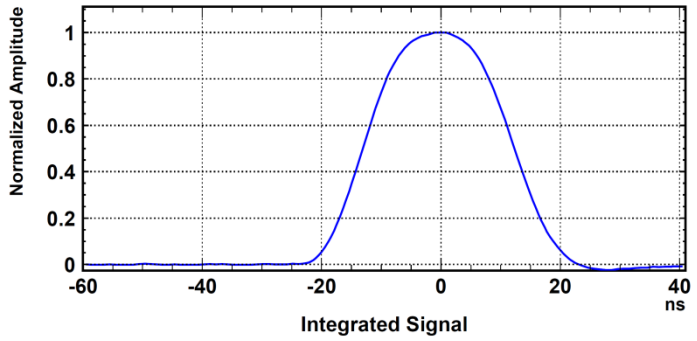
⇒ Reduce signal tail

⇒ Reduce spill over

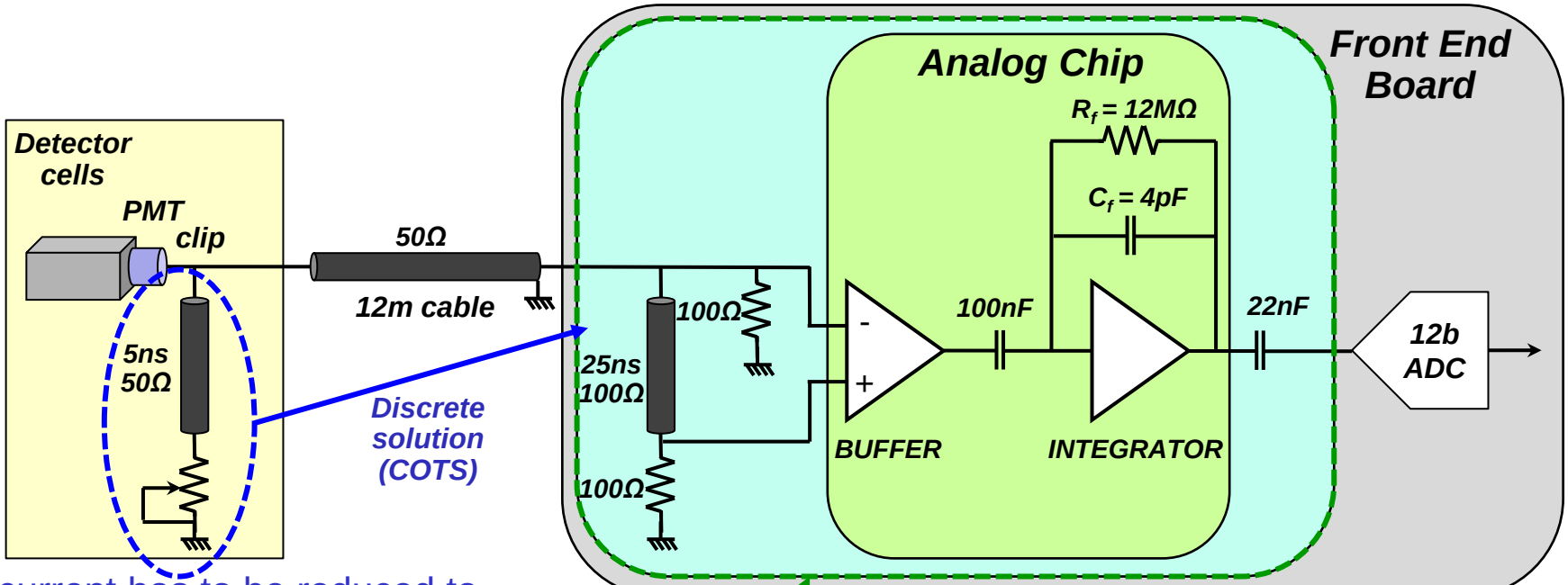


Integrator discharge:

Clipped signal + delayed negative clipped signal



Analog Electronics Upgrade Motivation



PMT current has to be reduced to increase lifetime

⇒ FE electronics gain has to be increased correspondingly

– BUT FE noise should not be increased in the operation!

Noise < 1 ADC Count

– For 12 bit DR, input referred noise <1nV/sqrt(Hz)

⇒ Termination resistor at input generates too much noise

Solutions:

– New ASIC
  - ✓ Increased gain
  - ✓ Active cooled termination

– Discrete solution: Components Out-of-The-Shelf (COTS)
  - ✓ 2/3 of the signal are lost by clipping
  - ✓ Remove clipping at the PM base (detector)
  - ✓ Perform clipping after amplification in FE using delay lines

Radiation tolerance:

– Dose 15 krad per fb^{-1}

✓ Radiation qualification tests

✓ Design techniques on ASIC

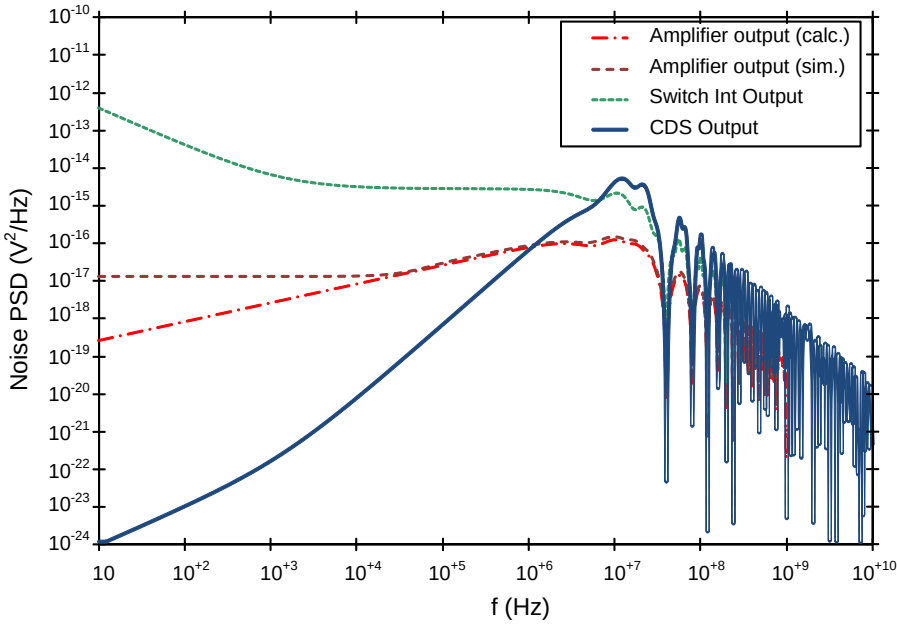
→ Enclosed transistors with guard rings

Analog Signal Processing

Energy range	0-10 GeV/c (ECAL) Transverse energy
Calibration	4 fC /2.5 MeV / LSB
Dynamic range	4096-256=3840 :12 bit
Noise	<≈1 LSB or ENC < 4 fC
Termination	50 ± 5 Ω
Shaping	25 ns (99 % of the charge)
Spill-over noise	< LSB
AC coupling	5-20 μs
Baseline shift Prevention	Dynamic pedestal subtraction (CDS) Pedestal is the smallest of 2 prev. samples
Max. peak current	4-5 mA (clipped)
Spill-over correction	Clipping
Linearity	< 1%
Crosstalk	< 0.5 %
Timing	Individual (per channel)

- **Signal processing elements (analog):**
  - **Amplification**
  - **Integration / shaping**
- **Dynamic pedestal subtraction (CDS):**
  - **Needed to correct baseline shift**
  - **And to filter LF noise (pick-up)**
    - **Has proven to be crucial in LHCb**
  - **Noise Power Spectral Density (PSD) in signal increases by ~ sqrt(2)**

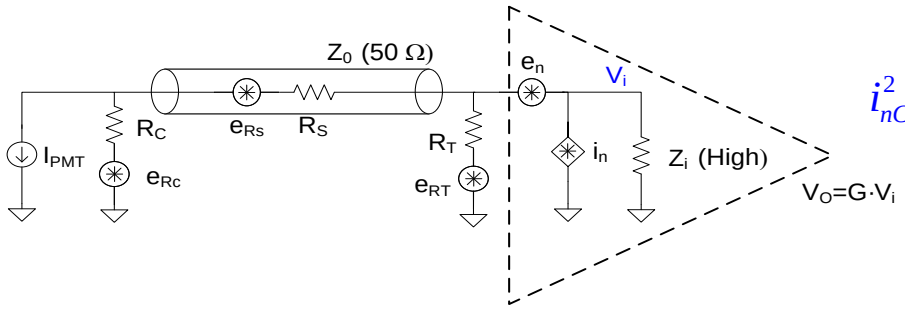
Noise PSD at different stages of the signal processing



Analog Signal Processing

- Noise contributions of

(1) Std high Zin amplifier

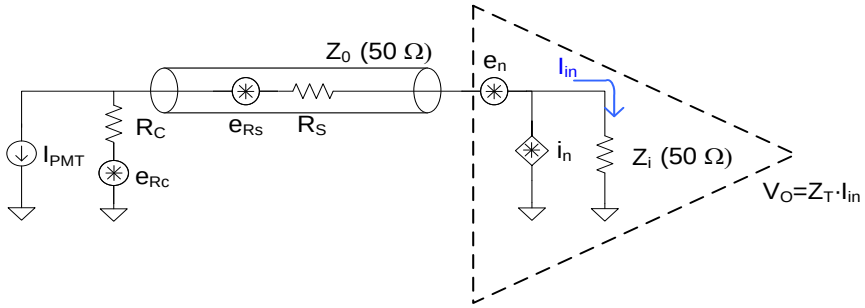


Referred to the clipped PMT current i_{nCLIP}

$$i_{nCLIP}^2 = \frac{e_n^2}{|Z_0|^2} + i_n^2 \left|\frac{1}{2}\right|^2 + \frac{4KT}{R_T}\left|\frac{1}{2}\right|^2 + \frac{4KT}{R_C}\left|\frac{R_C}{Z_0+R_C}\right|^2 + \frac{4KTR_S}{|R_S+Z_0|^2}$$

Typically dominant contributions

(2) Electronically cooled amplifier (0T)



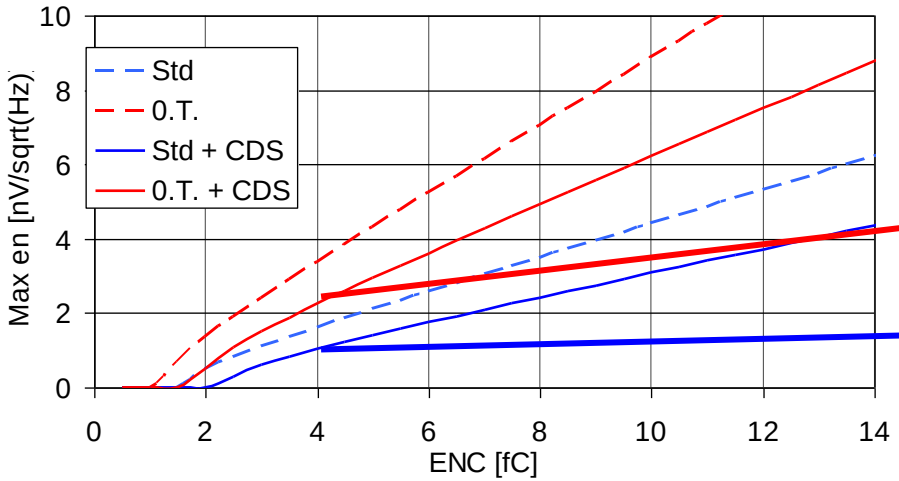
$$i_{nCLIP}^2 = \frac{e_n^2}{|2Z_0|^2} + i_n^2 \left|\frac{1}{2}\right|^2 + \frac{4KT}{R_C}\left|\frac{R_C}{Z_0+R_C}\right|^2 + \frac{4KTR_S}{|R_S+Z_0|^2}$$

Analog Signal Processing

- ENC: amplifier + integrator (time T) + CDS:
  - White noise $ENC^2_{A+I} \approx \frac{1}{2} i^2_{CLIP} T$
    - Resistive source imp.
  - Amp BW >> 1/T $ENC^2_{A+I+CDS} \approx i^2_{CLIP} T$

- Assumptions:
  - Cable modelled as lumped element*
  - Cable seen as Z_0 at HF from amp. side*
  - $R_T=Z_0$ (V amp) and $Z_i=Z_0$ (I amp)
  - Uncorrelated noise for CDS

Total input referred series noise requirement



- R_C=21 Ω
- R_S=18 Ω
- i_n neglected

.* R.L. Chase, C. de La Taille et alt., NIM A330, 1993

- OT with e_n< 2 nV/sqrt(Hz) fulfils requirements,
- Whereas std amp should have e_n< 1 nV/sqrt(Hz) !

Integrated Solution

Very difficult to integrate inside an ASIC
HQ analog delay lines

↓

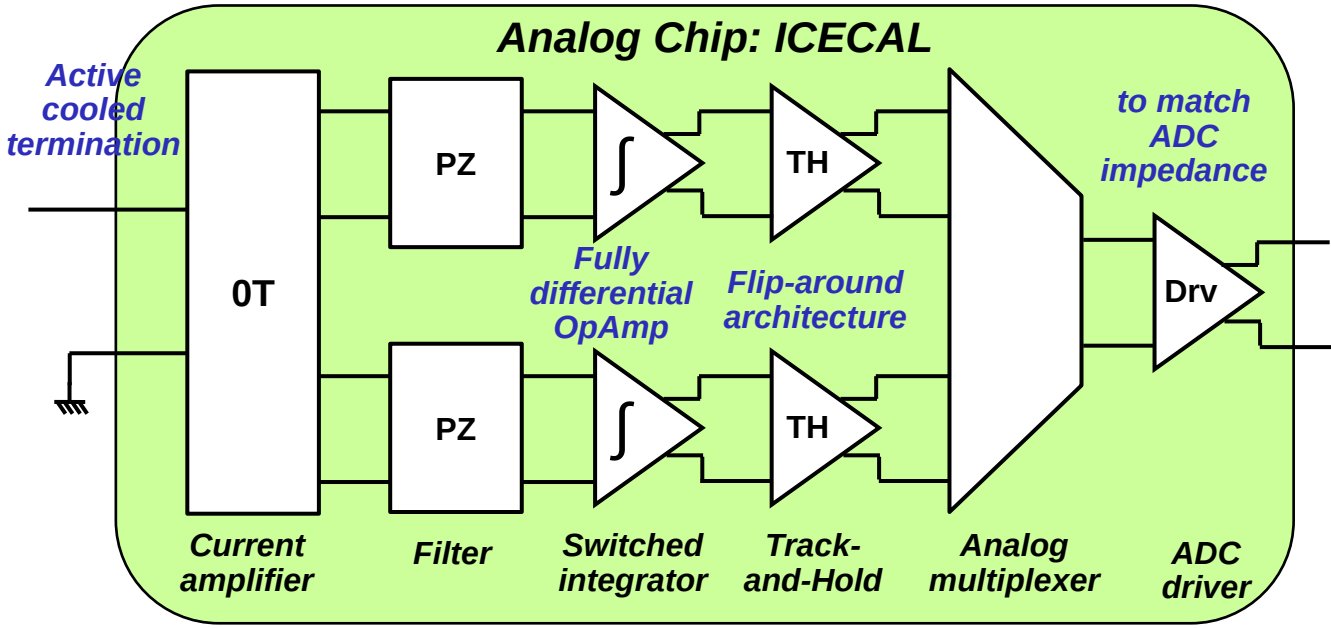
2 switched alternated paths (like in PS/SPD)

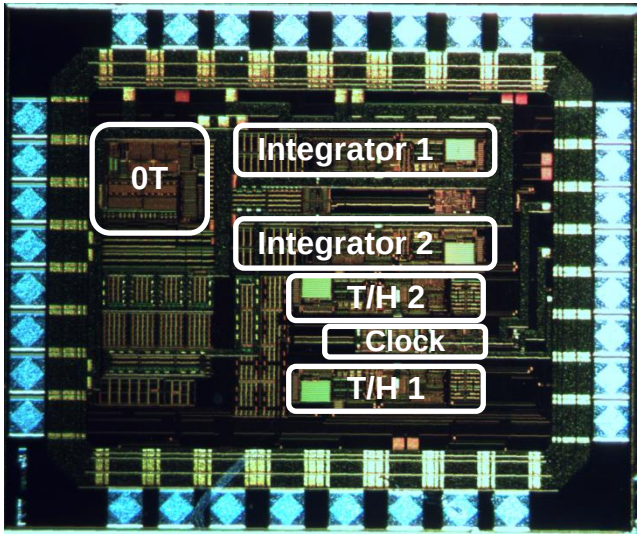
↓

Switching noise!

↓

Fully diferential ASAP





Two prototypes already designed and tested:

- Preamp + integrator
- Preamp + integrator + TH

Technology:

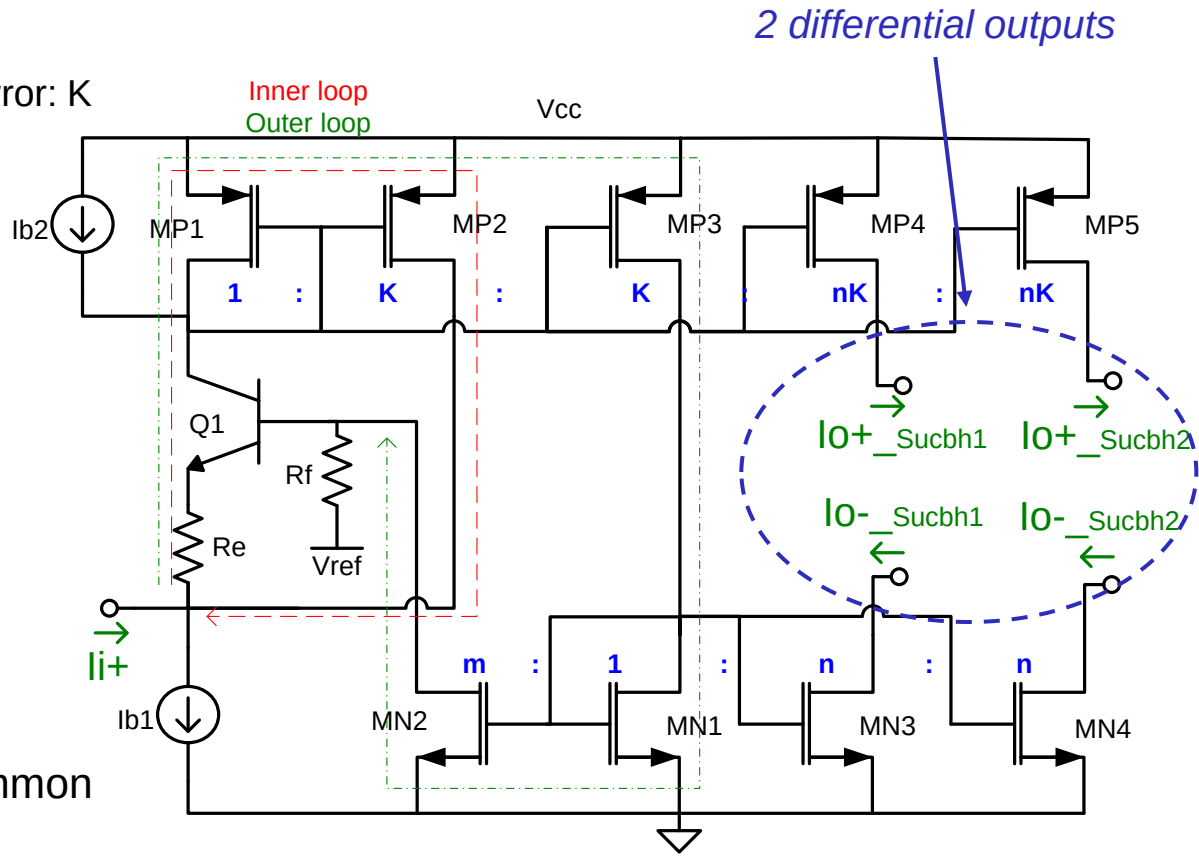
- SiGe BiCMOS 0.35um AMS

Channel Architecture: Current Amplifier Input Stage

- Current mode feedback:
  - Inner loop: lower Z_{in}
    - Current feedback (gain): mirror: K
  - Outer loop: control Z_{in}
    - Current feedback: mirror: m
    - Current gain: m
- Electronically cooled input impedance

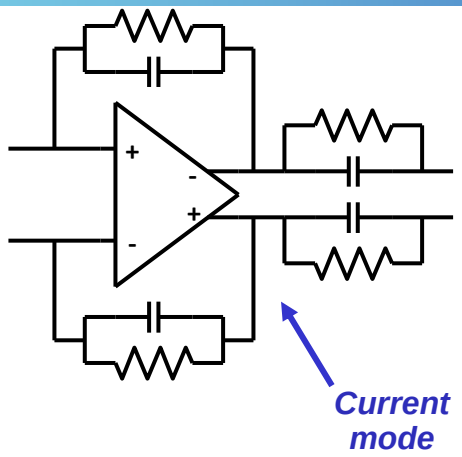
$$Z_i \approx \frac{1/g_{m1} + R_e}{1+K} + \frac{K}{1+K} mR_f$$

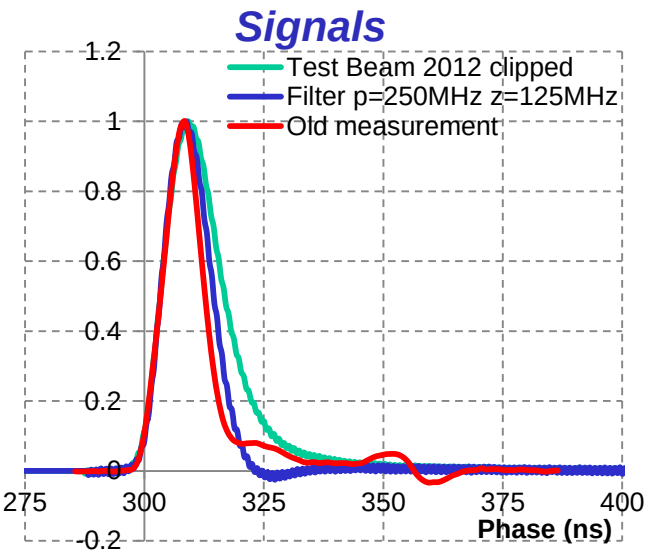
- Current mode feedback used
  - Optical comunications
  - SiPMreadout
- Low voltage
  - Only 1 Vbe for the super common base input stage
- Better in terms of electrostatic discharge (ESD):
  - No input pad connected to any transistor gate or base

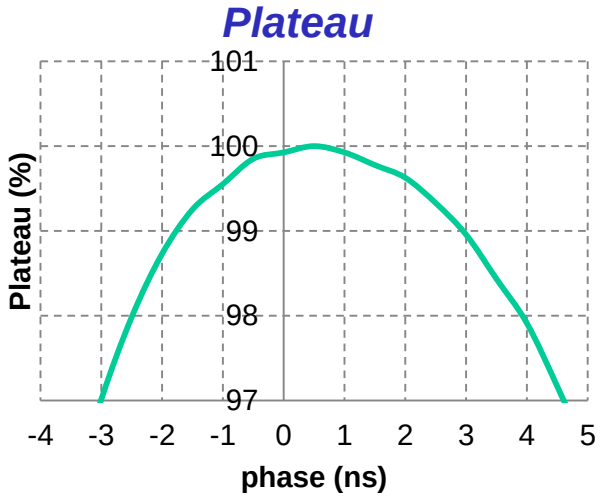


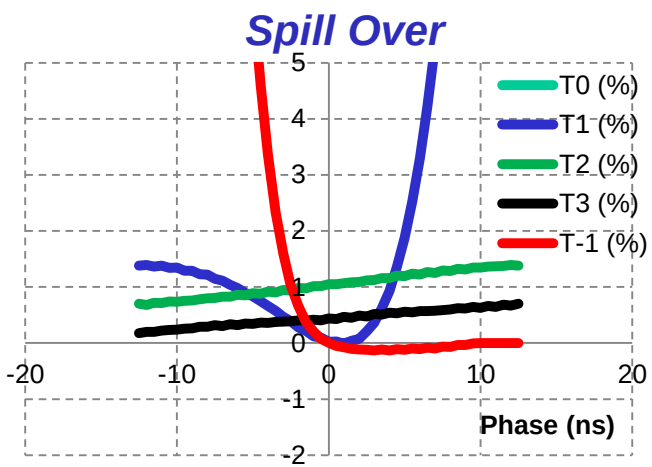
Channel Architecture: Pole-Zero Filter

- Problem :
  - Test beam signal is wider than expected
- Solution: fast pole-zero filter
  - Pole at 250 MHz
  - Zero at 125 MHz
- To reduce signal LF component:
  - Better plateau
  - Reduce spill over
- Noise impact:
  - Transient noise simulation
  - 500 iterations
  - 10% noise increase



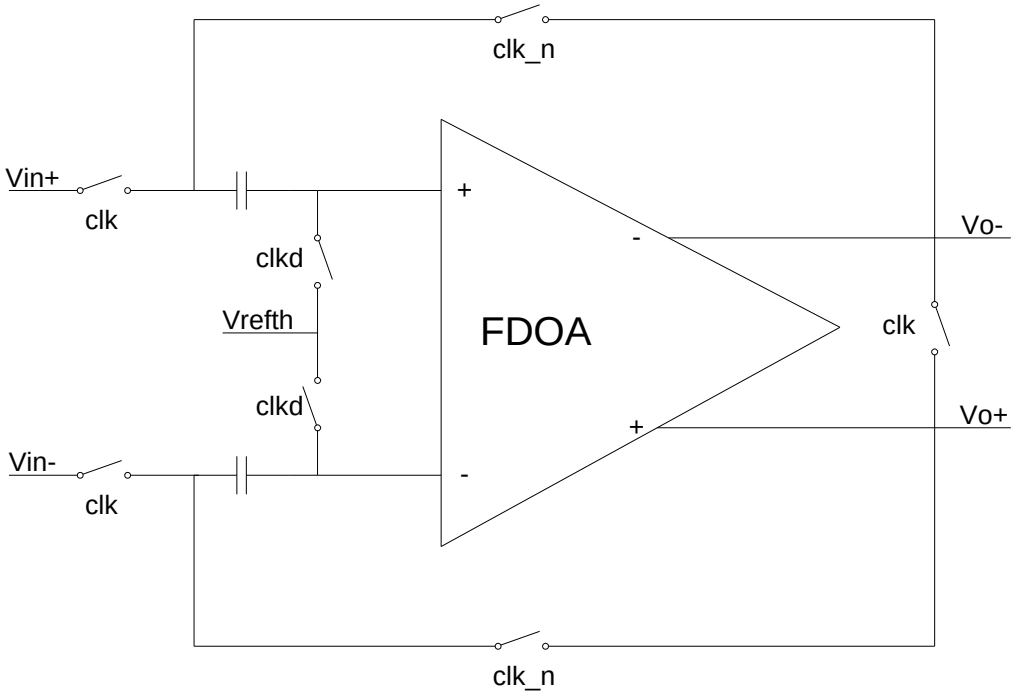


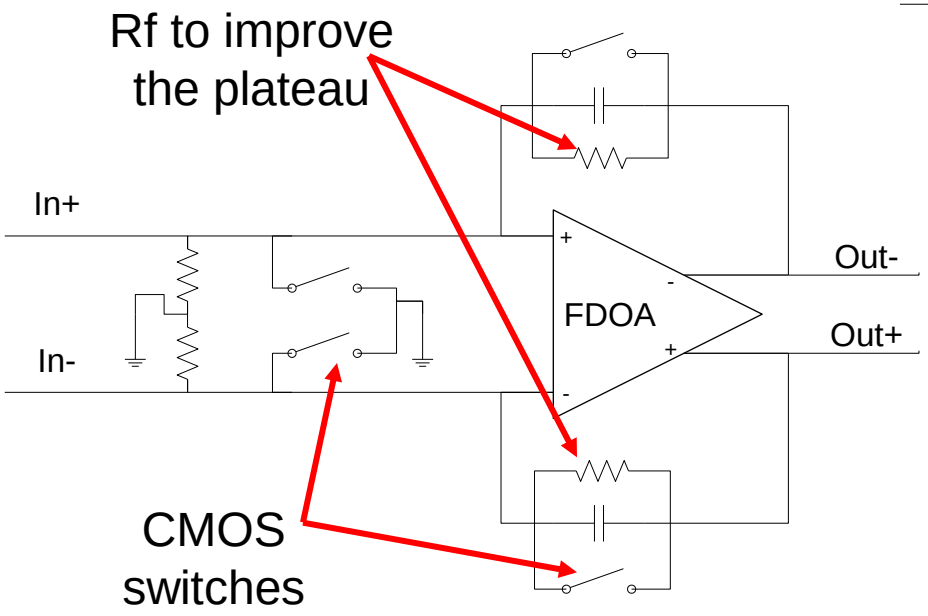




Channel Architecture: Switched Integrator / Track-and-Hold

- Switched integrator
  - Integrator plateau : 4 ns
  - Linearity < 1%
  - Residue < 1% after 25 ns
  - Reset time < 5 ns



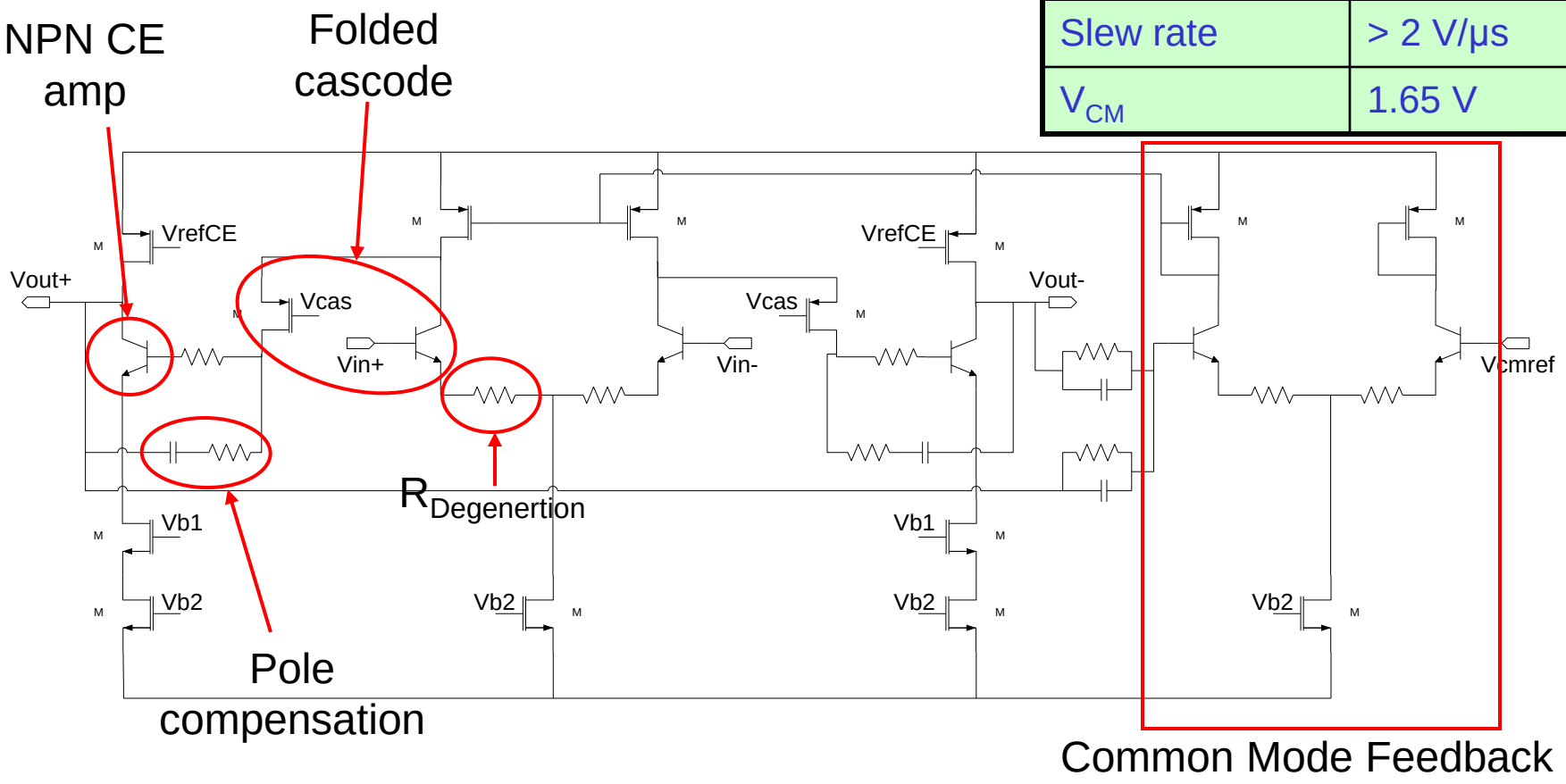


- Track-And-Hold:
  - 12 bit: flip-around architecture

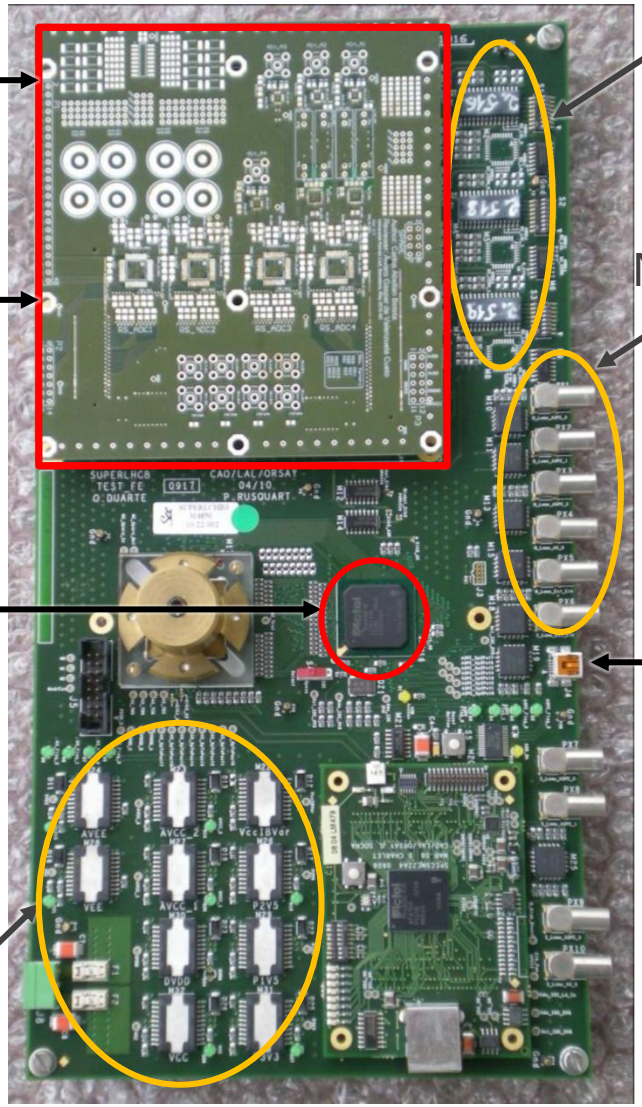
Channel Architecture: Fully Differential Op Amp

- Fully differential Op Amp:
  - Folded cascode + Miller stage with CMFB

FDOA specifications	
Parameter	**Value**
Gain bandwidth	500 MHz
Phase margin	> 65º
Slew rate	> 2 V/µs
V_{CM}	1.65 V



Front End Board Prototype Tests



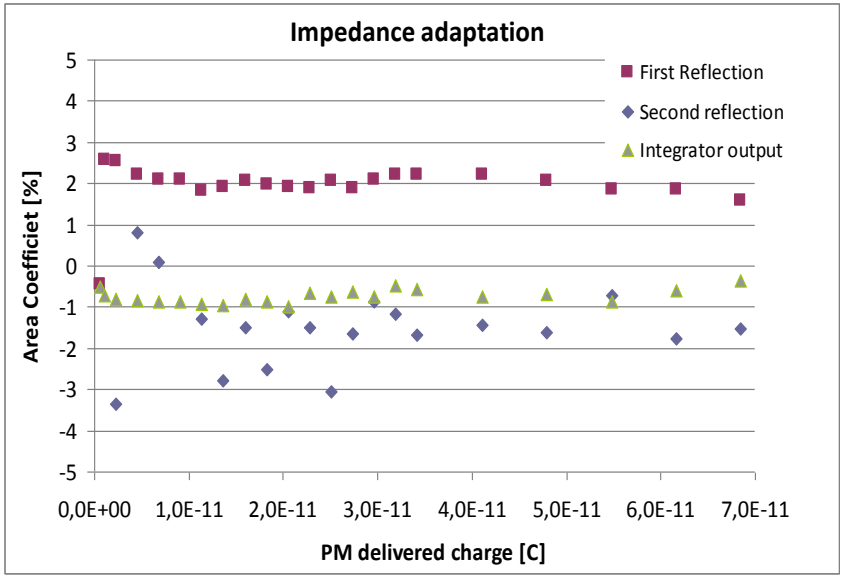
Verilog blocks:

- USB and control board
- General functionality
- DAQ

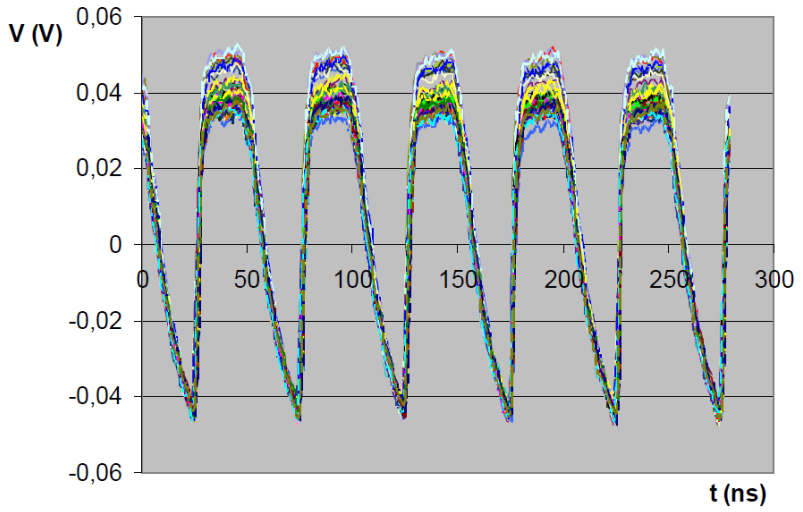
- Tests:
  - Linearity
  - Noise
  - Integral plateau
  - Spill over

ICECAL lab measurements

- Z_{in}:
  - Z_{in} fine tunable with R in parallel (~390Ω)
  - Study stability of Z_{in} as a function of frequency from reflections as seen at:
    - Input of the chip
    - Waveform generator output
  - Dynamic variation of input impedance << 1% for full dynamic (50 pC)
  - Low Refl. Coef. dispersion < 0.5%

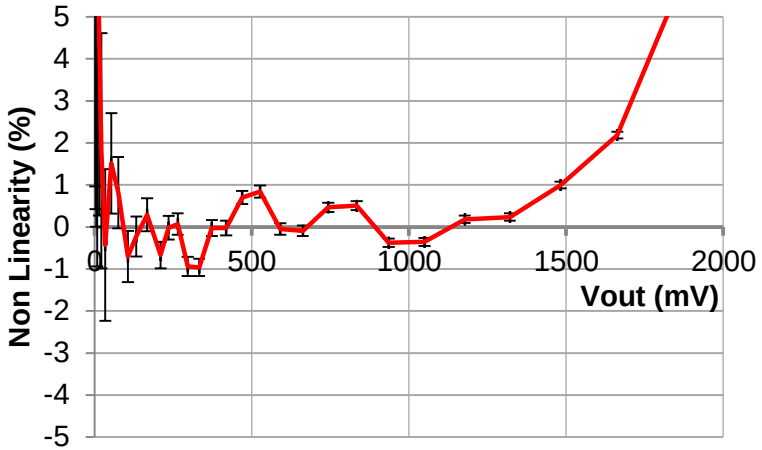


- Noise:
  - Spec: noise ~< 1 ADC count
  - Measurements with all setup:
    - ~1,6 ADC counts
    - ~1,7 ADC counts (dynamic pedestal subtraction)
  - Measurements without cable:
    - ~1,0 ADC counts
    - ~1,25 ADC counts (dynamic pedestal subtraction)

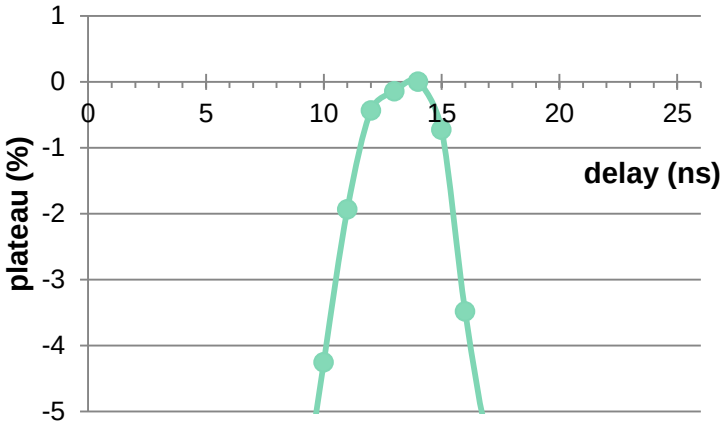


ICECAL lab measurements

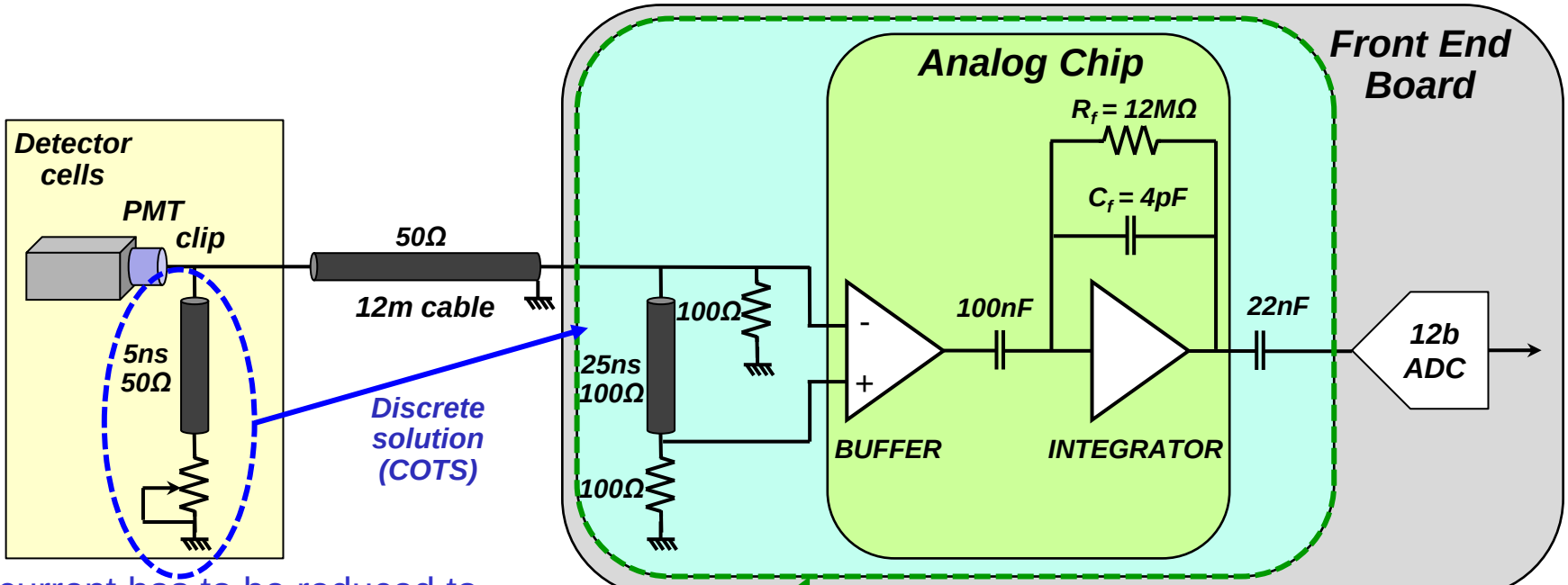
- Linearity:
  - Simulations show that the linearity is lost at ~1,8V
  - Cause: single-ended limit to maximum Vout of FDOA at the NMOS stage
  - Solution: apply different offset to each pos/neg signal to reduce overall signal excursion



- Integrator output plateau:
  - Spec: 4ns <1% variation
  - Cope with different particle time arrival
  - Initially OK, but signal used was not correct; pulse width underestimated (due to cable and clipping effects)
  - Solution: fast pole-zero filter to reduce low frequency components



Analog Electronics Upgrade Motivation



PMT current has to be reduced to increase lifetime

⇒ FE electronics gain has to be increased correspondingly

– BUT FE noise should not be increased in the operation!

Noise < 1 ADC Count

– For 12 bit DR, input referred noise <1nV/sqrt(Hz)

⇒ Termination resistor at input generates too much noise

Solutions:

– New ASIC
  - ✓ Increased gain
  - ✓ Active cooled termination

– Discrete solution: Components Out-of-The-Shelf (COTS)
  - ✓ 2/3 of the signal are lost by clipping
  - ✓ Remove clipping at the PM base (detector)
  - ✓ Perform clipping after amplification in FE using delay lines

Radiation tolerance:

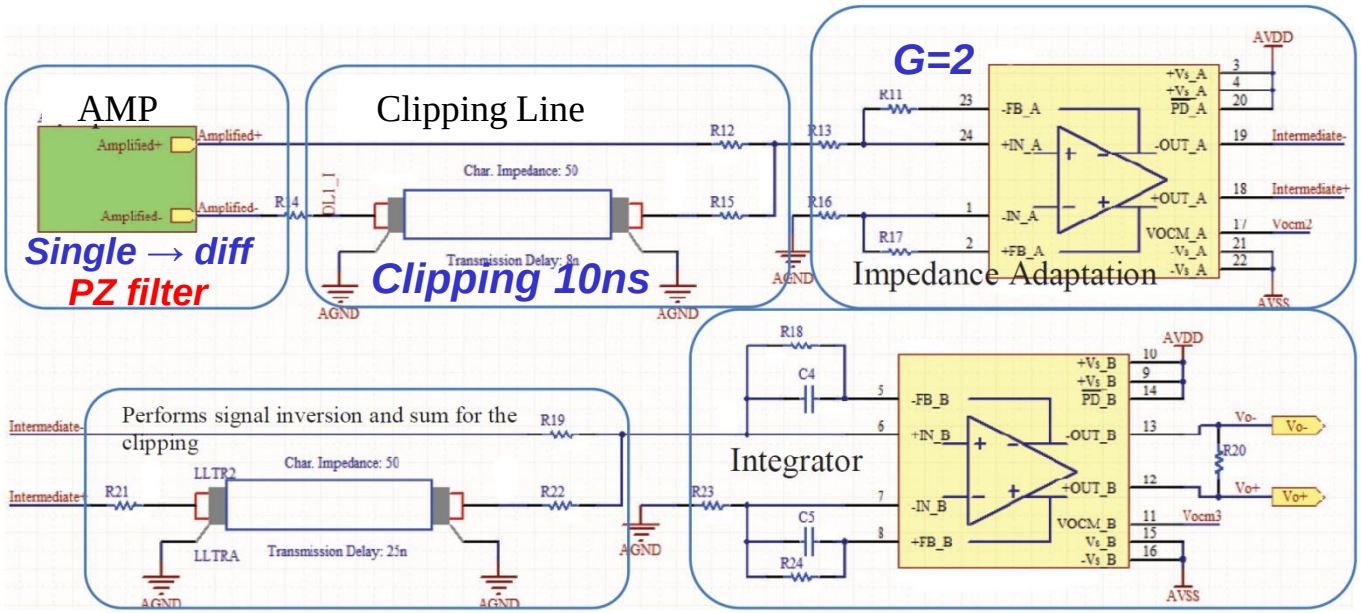
– Dose 15 krad per fb^{-1}

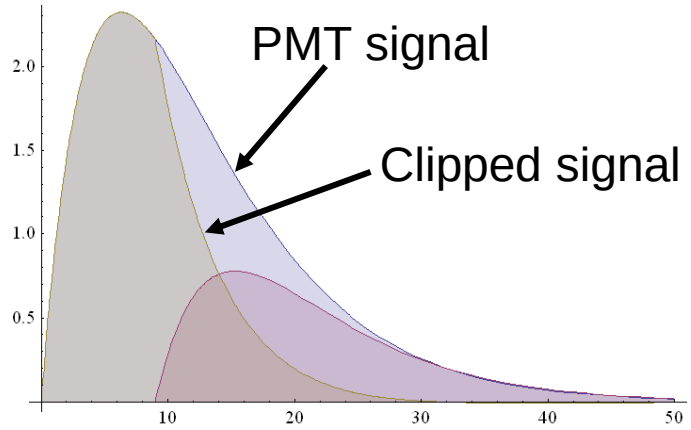
✓ Radiation qualification tests

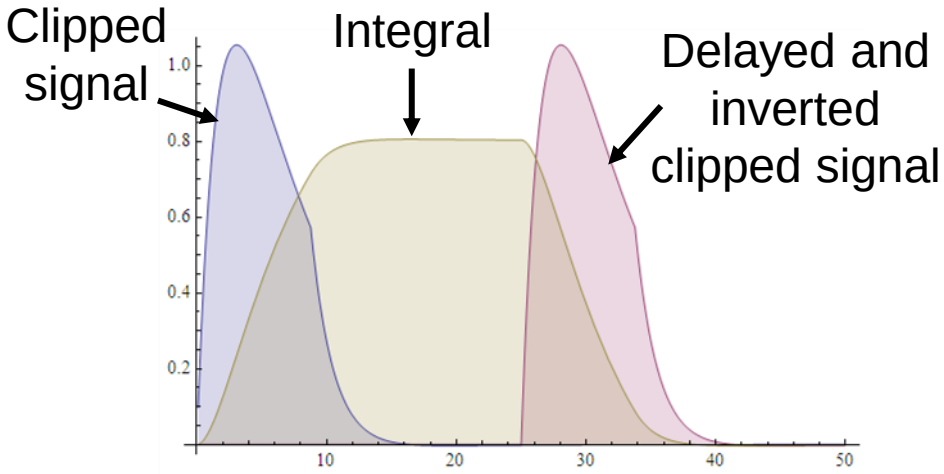
✓ Design techniques on ASIC

→ Enclosed transistors with guard rings

COTS Channel Architecture

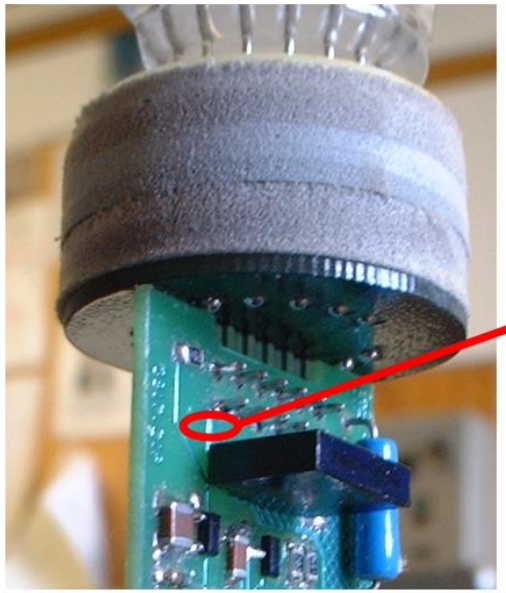


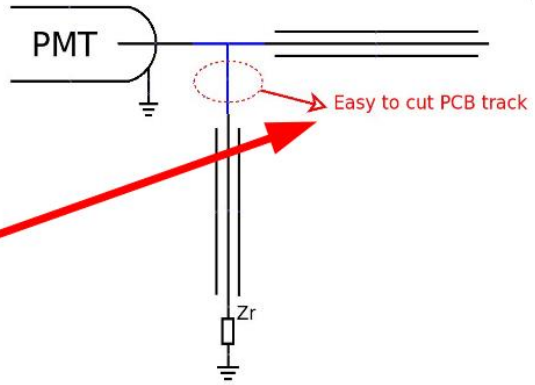




COTS: clipping

- Clipping is done in the FEB, not in the PMT base:

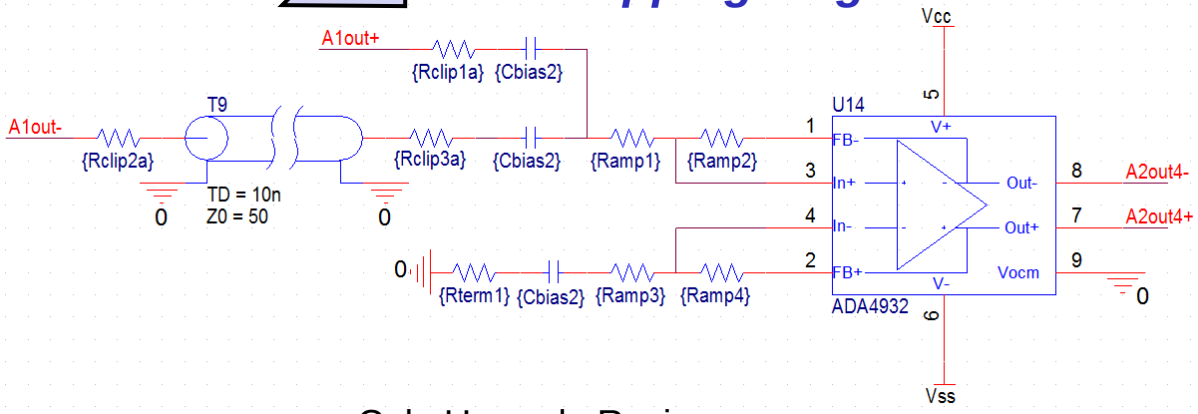




- 2/3 of the signal are lost by clipping
- Remove clipping at the PM base (detector)
- Perform clipping after amplification in FE using delay lines

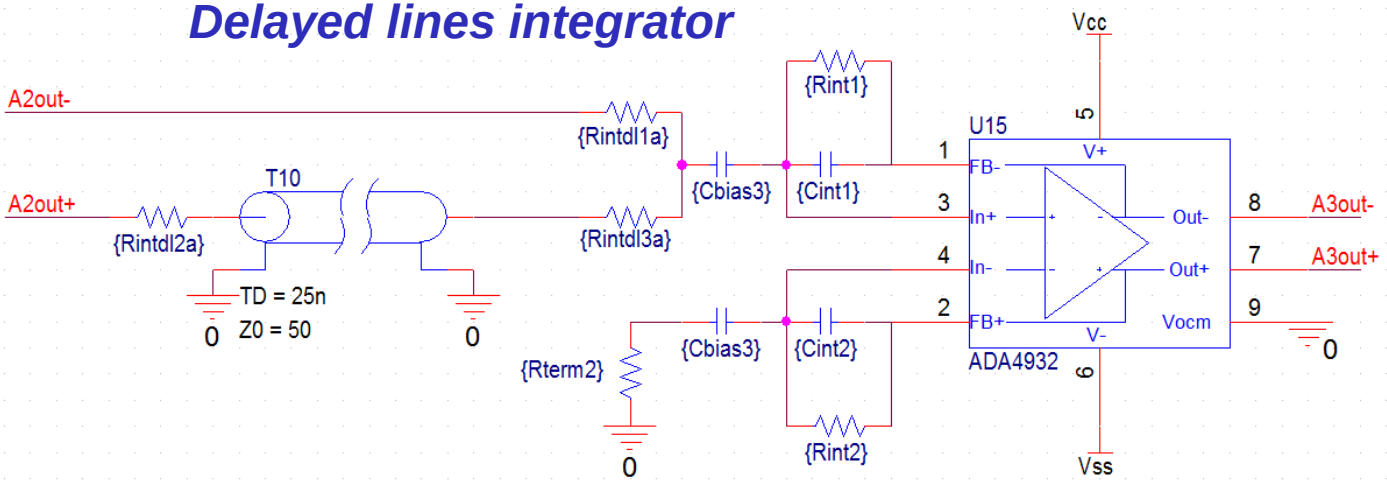
⇒ Greater signal/noise ratio

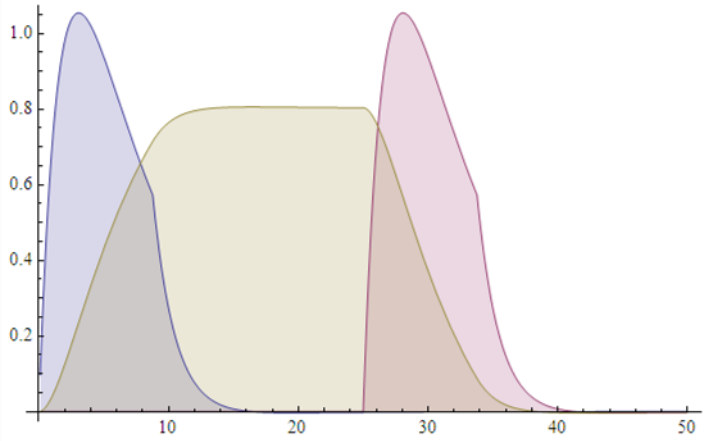
Clipping stage

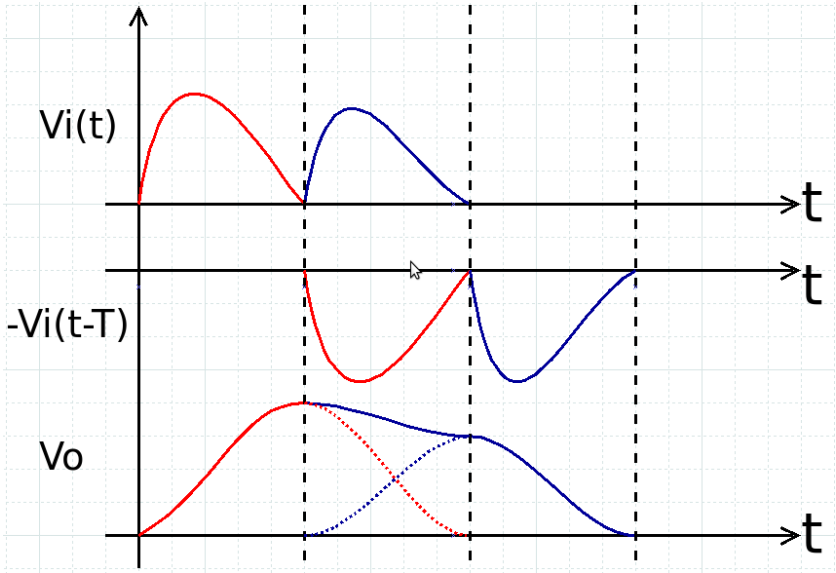


COTS: integration

Delayed lines integrator

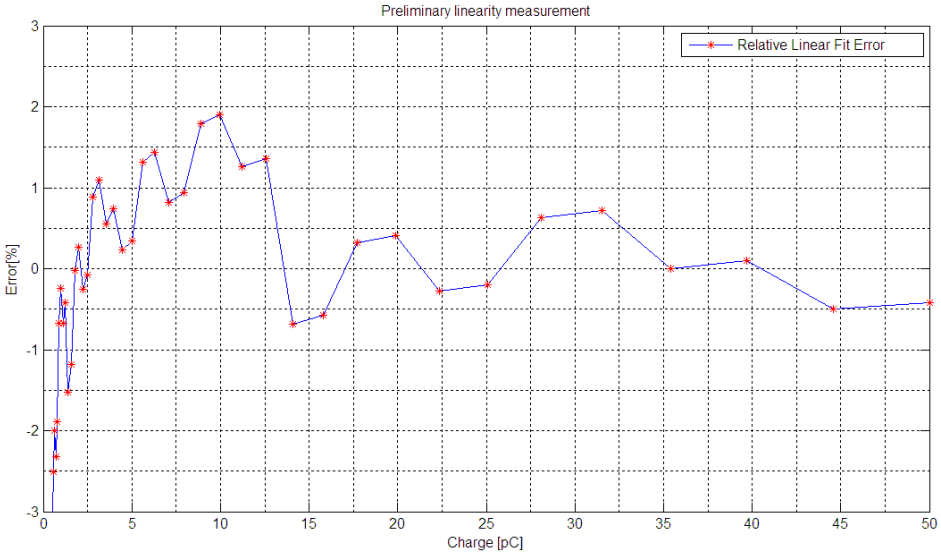




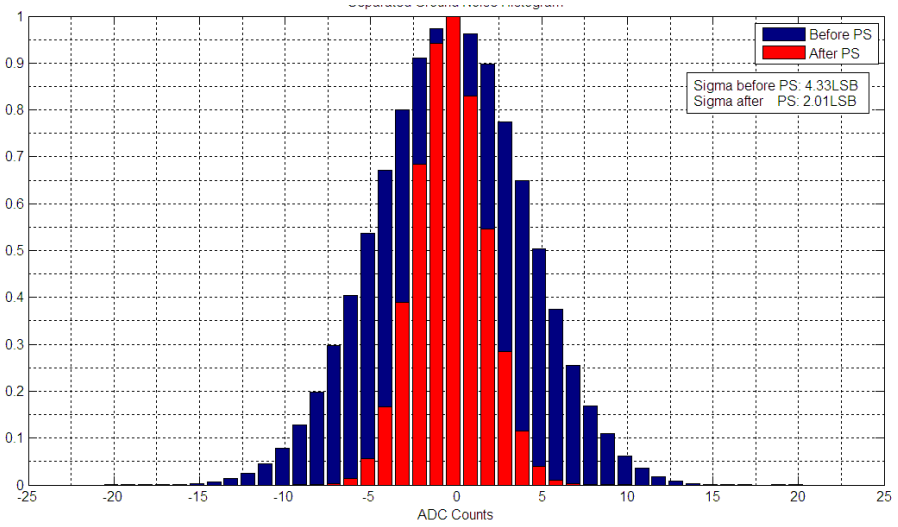


COTS: lab measurements

- Linearity:
  - Low voltage measurements present high relative errors
  - Systematics due to the attenuator



- Noise:
  - Spec: noise ~< 1 ADC count
  - Measurements with joint ground planes:
    - ~4,23 ADC counts
    - ~2,31 ADC counts (dynamic pedestal subtraction)
  - Measurements with separated gnd planes:
    - ~4,14 ADC counts
    - ~1,99 ADC counts (dynamic pedestal subtraction)



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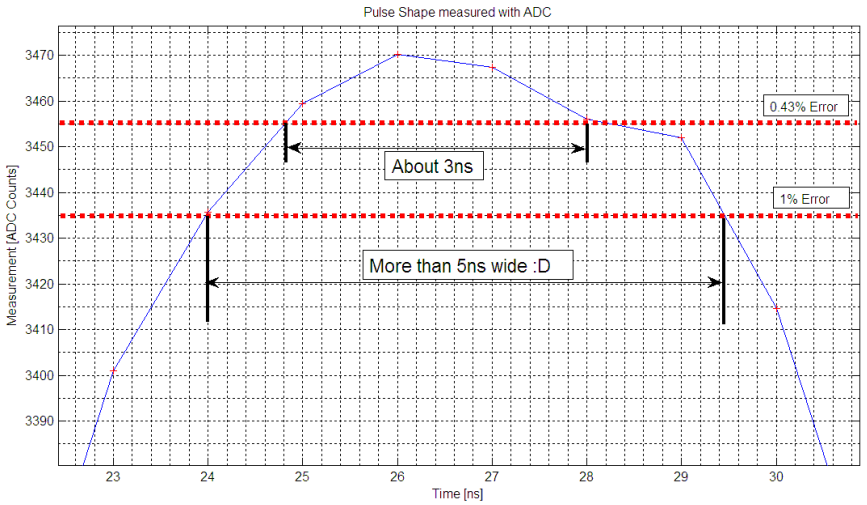
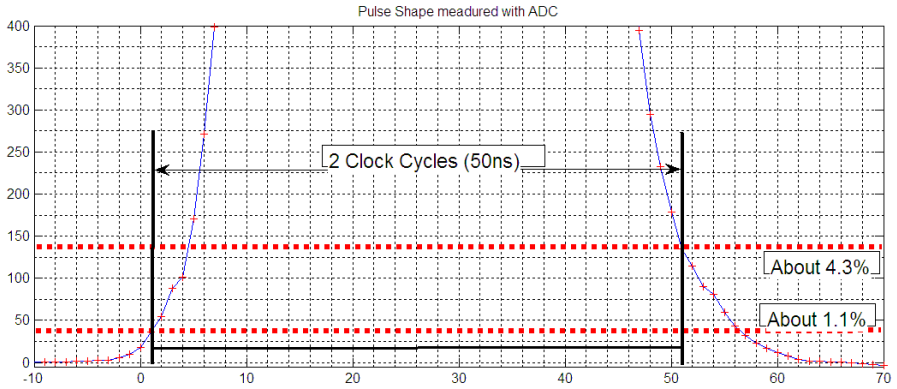
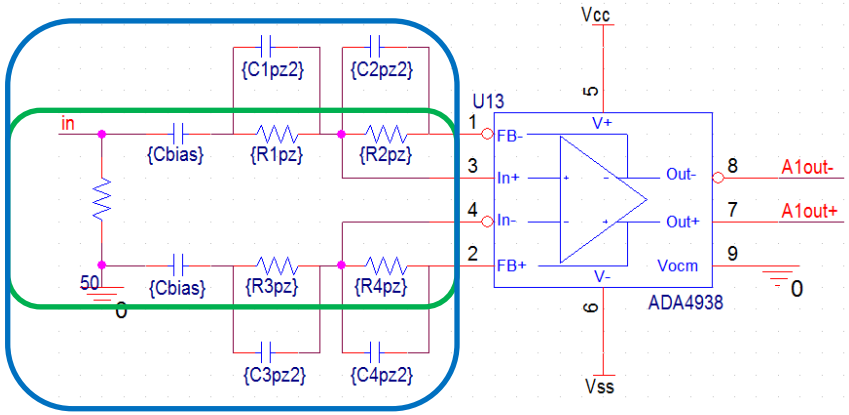


- Spill over:
  - Spec: <1% in the following cycles respect to the signal
  - Not met.
  - Solution: fast pole-zero filter to reduce low frequency components

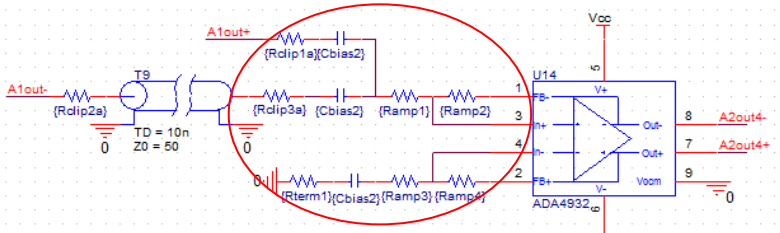


COTS: Post Test Beam 2012

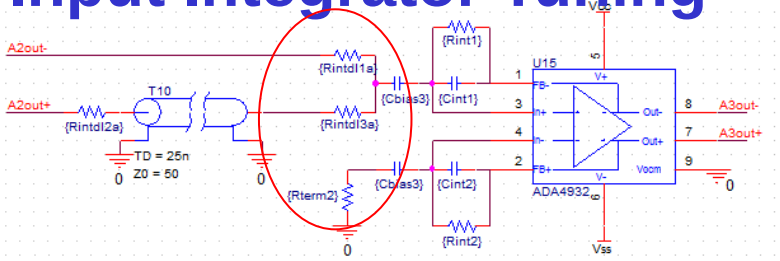
- COTS modifications after TB 2012
  - Signal measured at Test Beam is more expanded than the one used for original design
  - Need to equalize the cable effect
    - Pole-zero due (under study)
  - Pole-zero on pre amplifier of the first stage proposed
    - Problems:
      - G=10 → BW≤100Mhz → pole & zero freq > AMP BW
      - Capacitor values < 1p → values comparable to parasitic capacities
      - Zin ≠ cte 50



Clipping Tuning

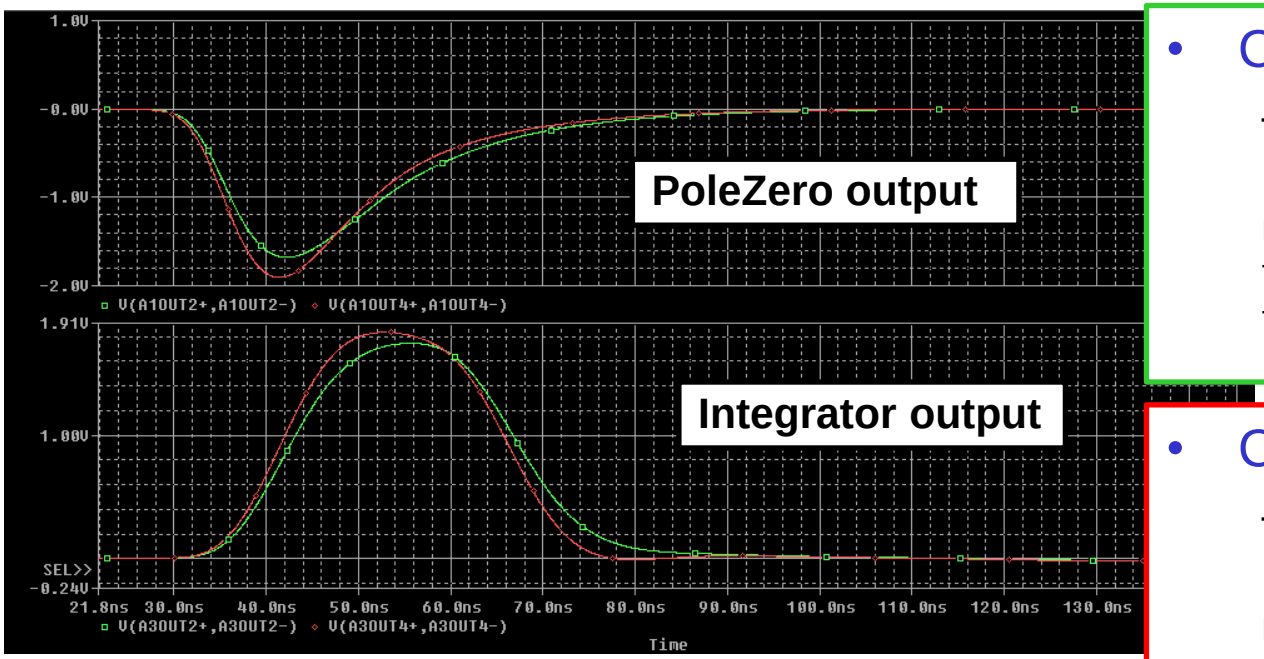


Input Integrator Tuning



Pre Amp → PZ modification

COTS mezz 5 simulations



- COTS TB input signal
  - Without pole-zero filter

Plateau = 4.55793 ns
T(1% - 100%) - = -29.35551 ns
T(100% - 1%) = 59.23128 ns

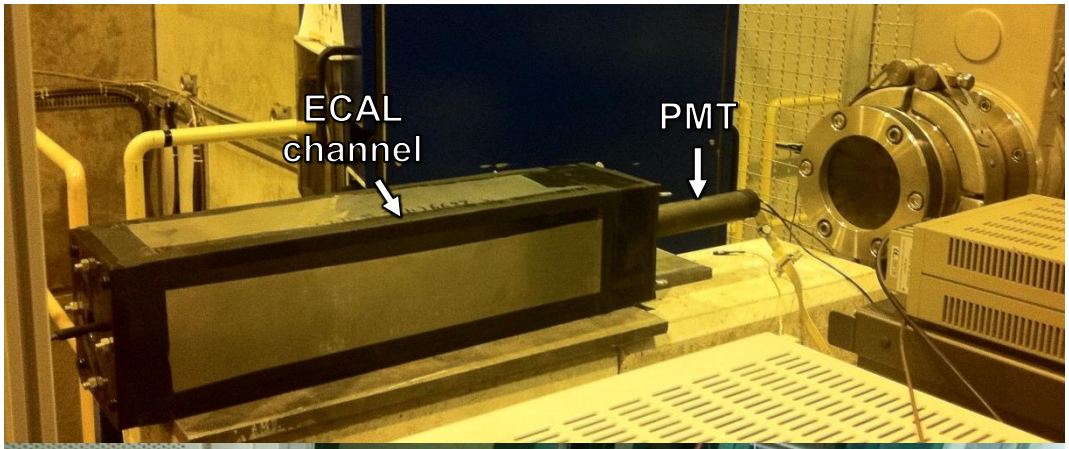
- COTS TB input signal
  - With pole-zero filter

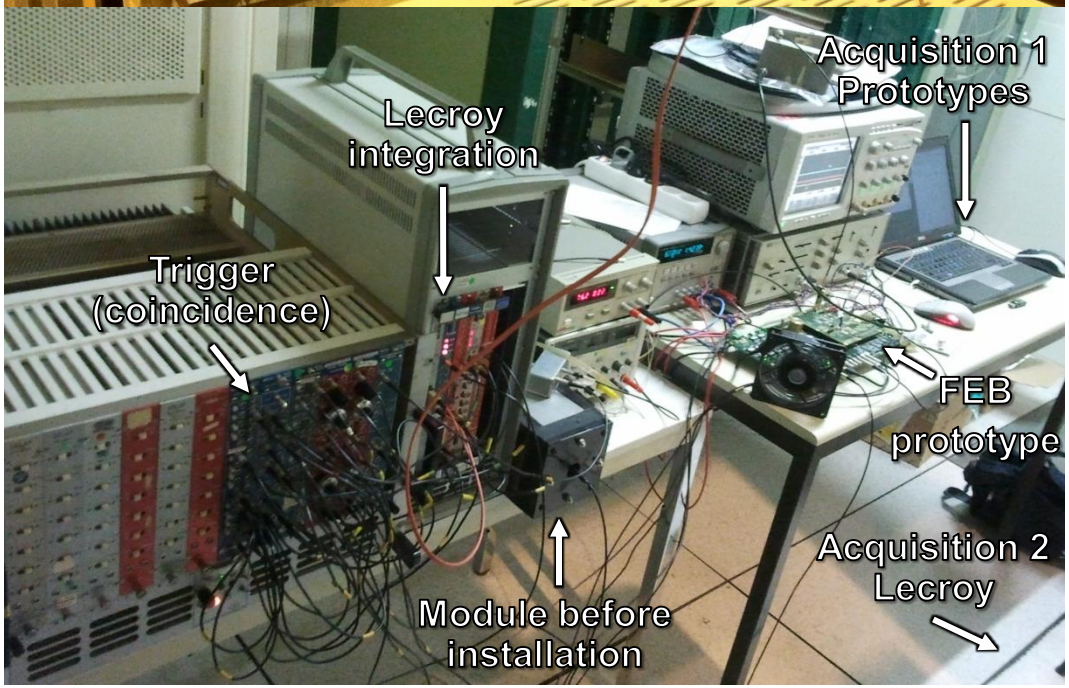
Plateau = 4.35421 ns
T(1% - 100%) = 24.84842 ns
T(100% - 1%) = 24.75773 ns

- Tuning:

- Circuit tuning done in both results to optimize results:
  - Spillover → minimize
  - Plateau → maximize
  - Undershoot → minimize

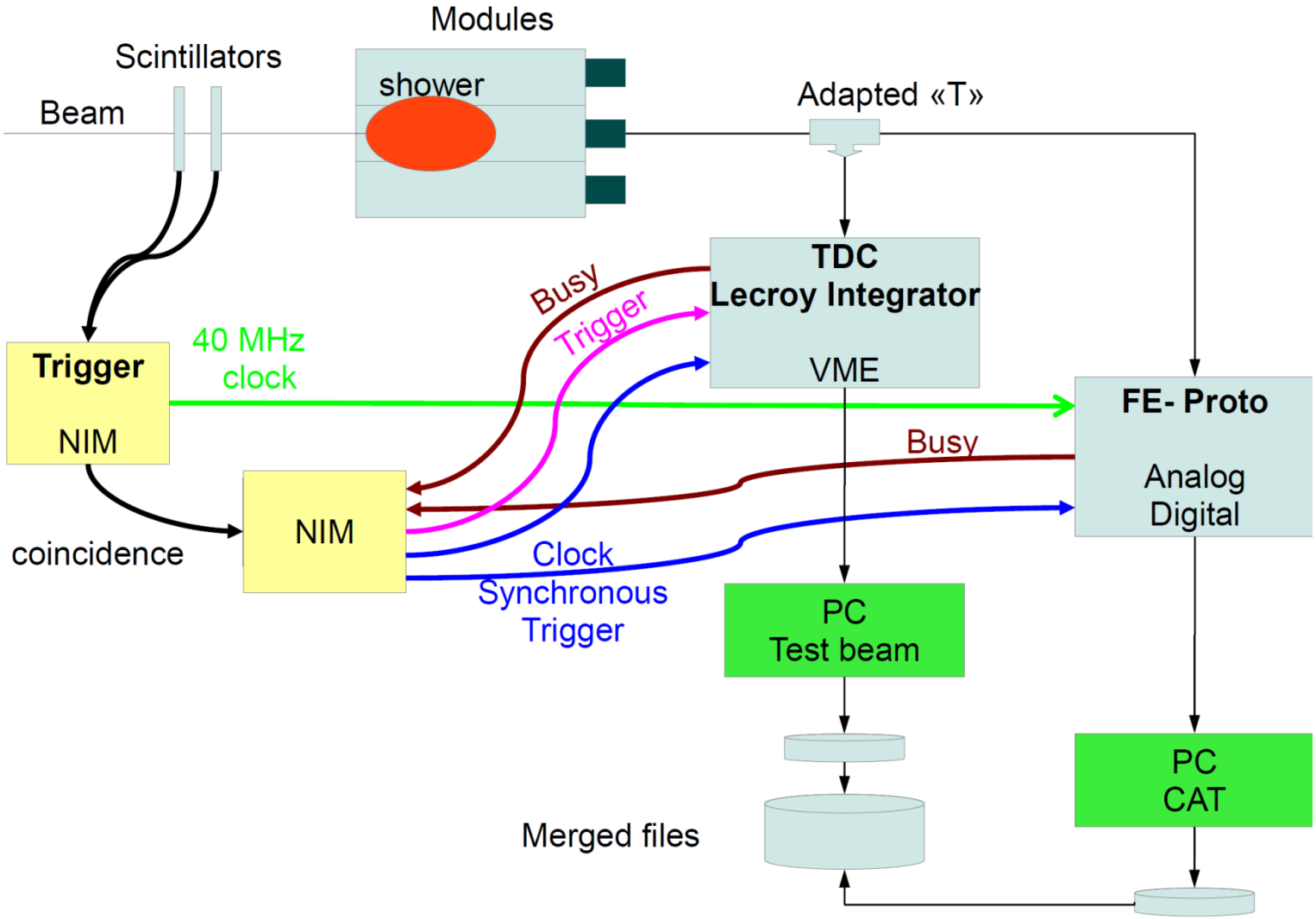
Test Beam Measurements





- November 2012
- Beam line T4-H8 at CERN
- Used e- of 50 to 125GeV
- Setup:
  - ECAL channel
  - PMT
  - 12m cable
  - FEB prototype
  - Lecroy integrator
  - Time-to-Digital Converter (TDC)

Test Beam Measurements

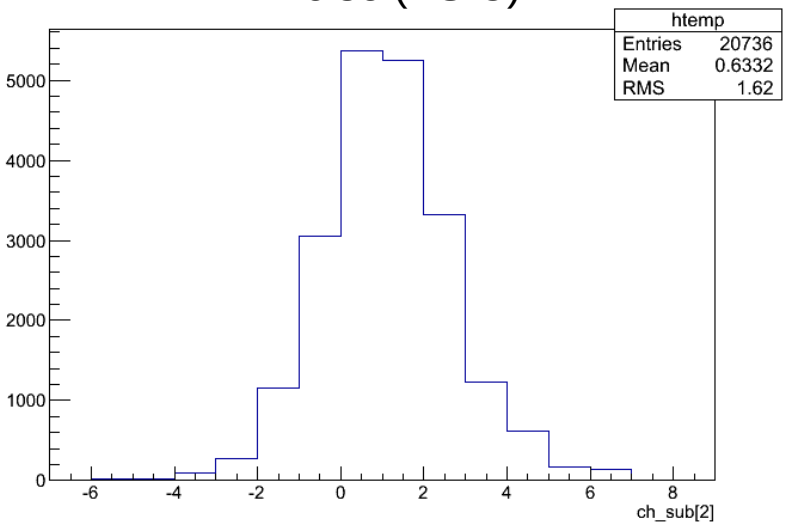


Test Beam Measurements

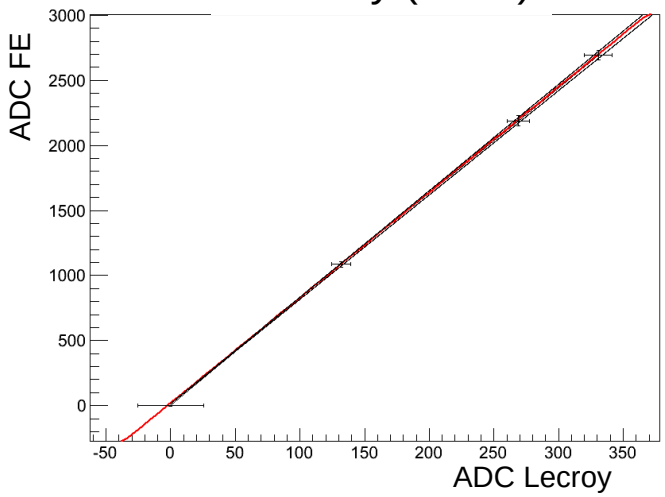
- Noise:
  - Noise after pedestal subtraction:
    ~1.6 ADC (ASIC)
    ~2.6 ADC (COTS)

  → Contribution of 10-15% due to the use of a “T” to distribute the signal:
    ~1.4 ADC (ASIC)
    ~2.3 ADC (COTS)
- Linearity:
  - Linearity better than 1%

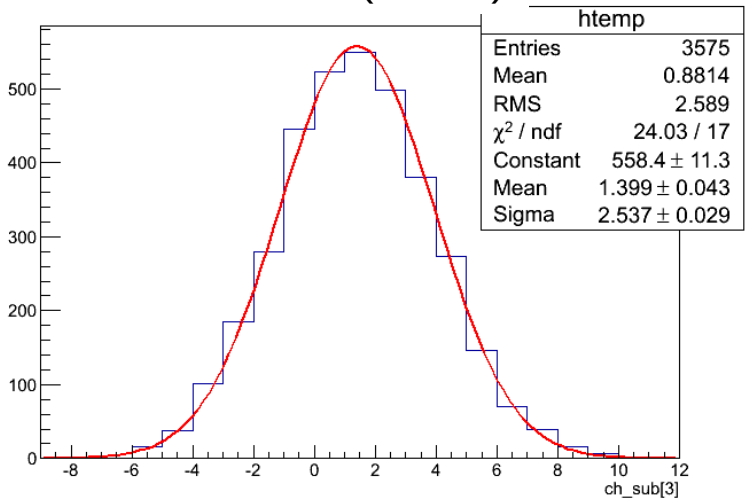
Noise (ASIC)



Linearity (ASIC)



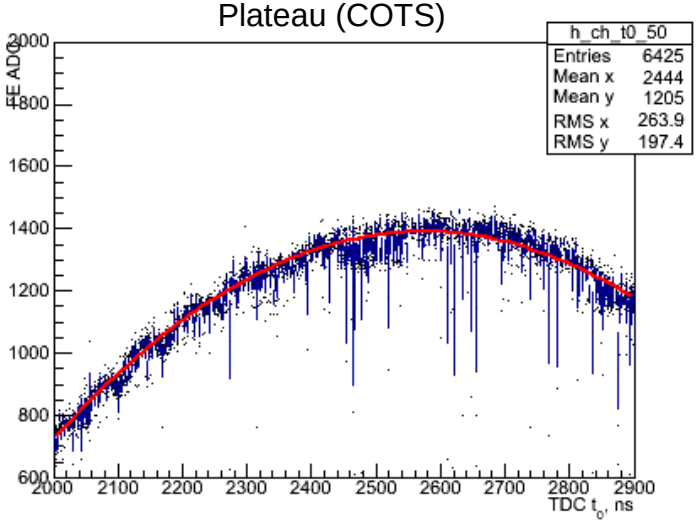
Noise (COTS)



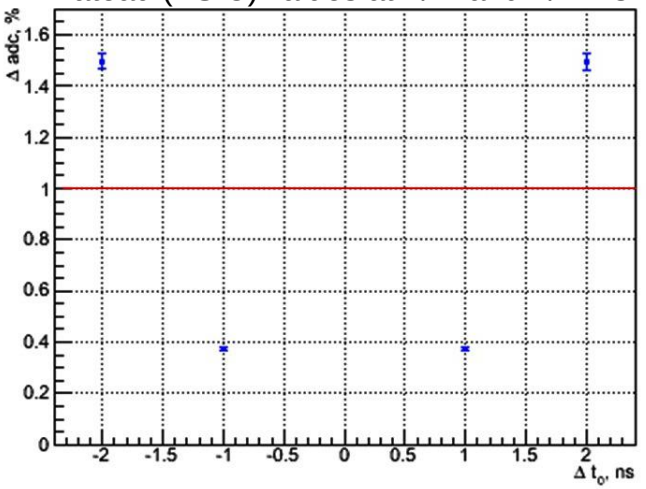
Test Beam Measurements

- Plateau:
  - Integral plateau ~1.6% at ±2ns (ASIC) and <1% (COTS)
- Spill over:
  - Spill over of ~8% in following sample (ASIC)
- Pulse width underestimated (due to cable and clipping effects):
  - Affects plateau and spill over
  - ⇒ Pole-zero filter proposed for final version of ASIC/COTS

Plateau (COTS)



Plateau (ASIC) values at +/-1 and +/-2 ns



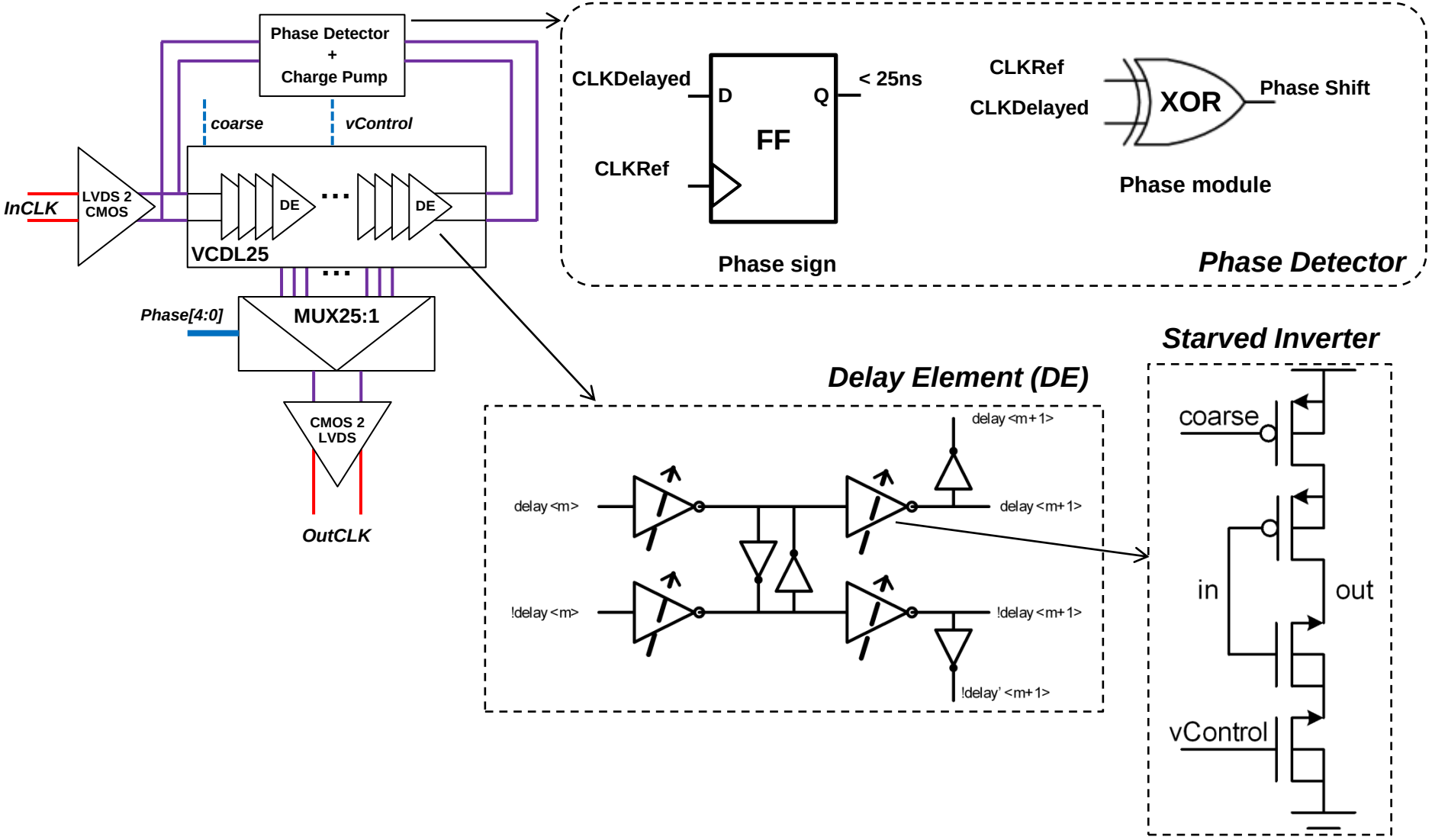
Complete results can be found at the presentations by Olga Kochebina at Calorimeter Upgrade meetings 19/12/2012 and 12/04/2013

Delay Line

- We need delay lines:
  - To synchronise ICECAL integrator, track & hold and the external ADC.
  - To adjust the ADC clock phase in COTS solution.

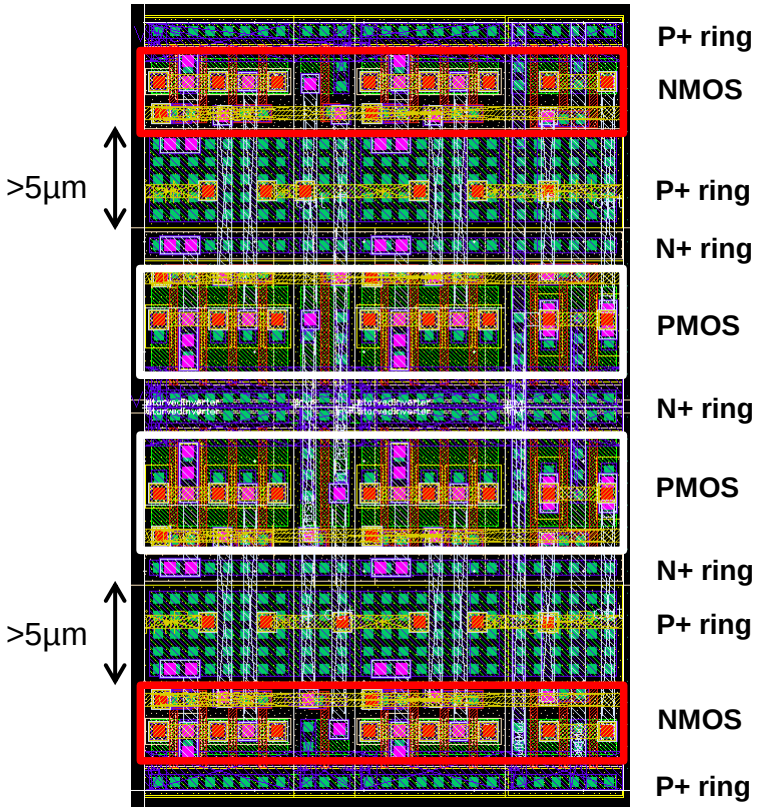
- Challenges:
  - Radiation hardness:
    - SEU → TMR (triple voting).
    - SET → glitch suppressors.
    - SEL → guard rings (full custom digital design).
  - Delay line variability:
    - Process variations → **external** adjust (coarse).
    - Environmental variations → **internal** locked loop adjust (vControl).
  - Noise:
    - Stringent noise requirements of the ASIC analog components (ICECALv3) → differential design, guard rings..

Delay Line: design overview



Delay Line features

- 4 DLL Channels (4x3 = 12 independent sub-channels):
  - 25 configurable clock phases (1-ns step).
  - Peak-to-peak Jitter: 3 ps.
  - Differential Non Linearity (DNL): 18 ps.
  - Delay Range: 17.45 ~ 39.88 ns.
  - DLL Locking time: 2.5 ~ 10 µs.
  - DLL peak-to-peak ripple voltage ~ 1 mV.
  - ~280 mW of power consumption.
  - Technology: AMS 0.35 CMOS.
- Reset:
  - Glitch supressor (≤ 8ns) ensures that SETs do not accidentally reset the chip.
- Reliability (SEL avoidance):
  - Extra design rules:
    - ≥ 5µm between N-DIFF layer and NWELL.
    - Guard rings between PMOS and NMOS.



Example: Delay Element

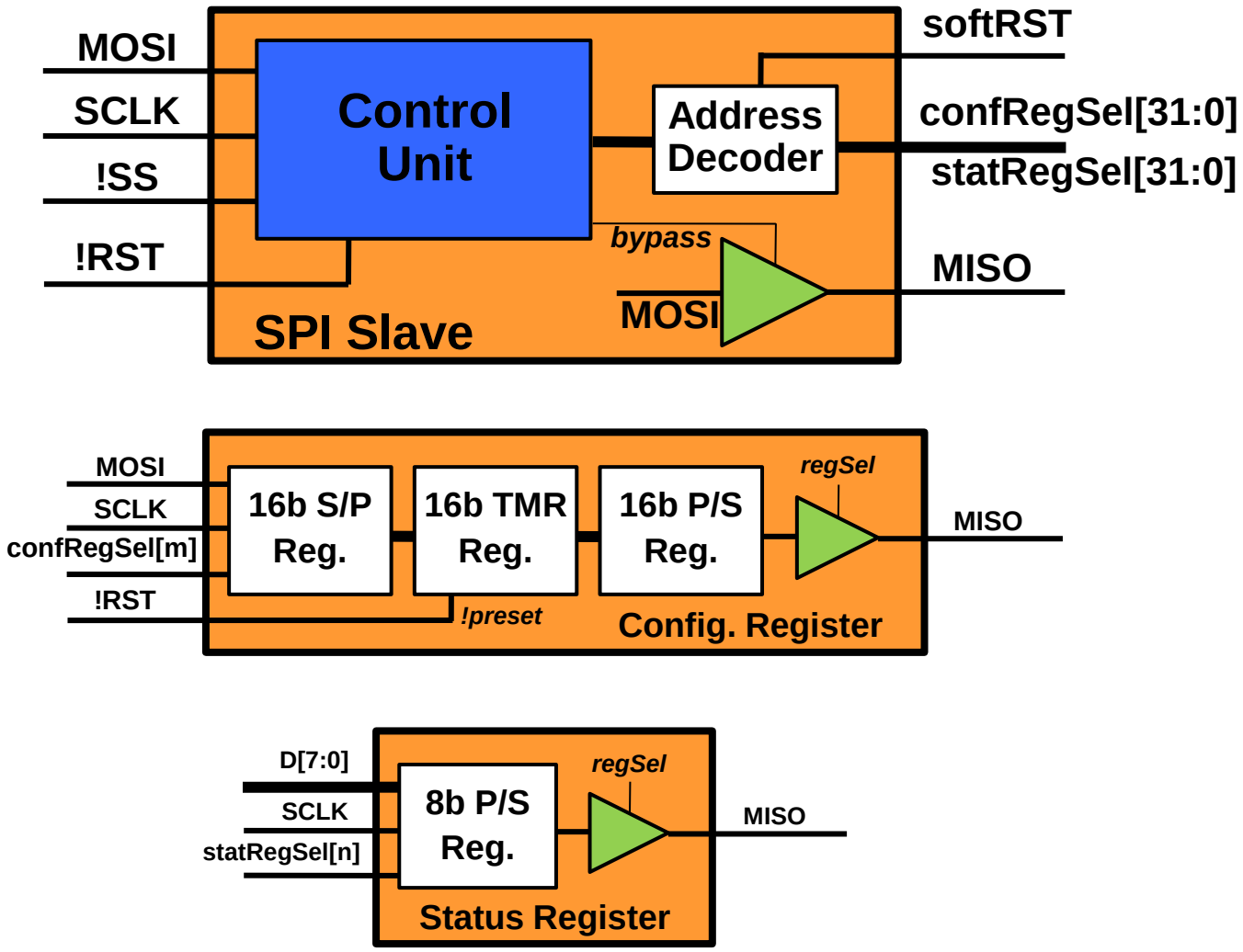
Slow control

- We need slow control:
  - To configure and check the status of delay lines.
  - To configure ICECALv3 Analog blocks.

- Challenges:
  - Radiation hardness:
    - SEU → TMR (triple voting).
    - SEL → guard rings (full custom digital design).

- Features:
  - SPI slave:
    - Works fine @ 20 Mbps.
    - Up to 32 configuration registers and 32 status registers.
    - Also implements a software reset pulse (to reset DLL charge pumps).
  - Serial registers:
    - 16 bits R/W TMR registers (configuration).
    - 8 bits RO (status). No memory.

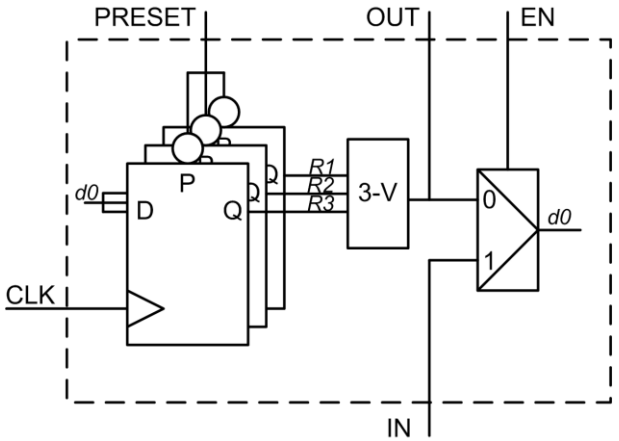
Slow control: design overview



Slow control implementation

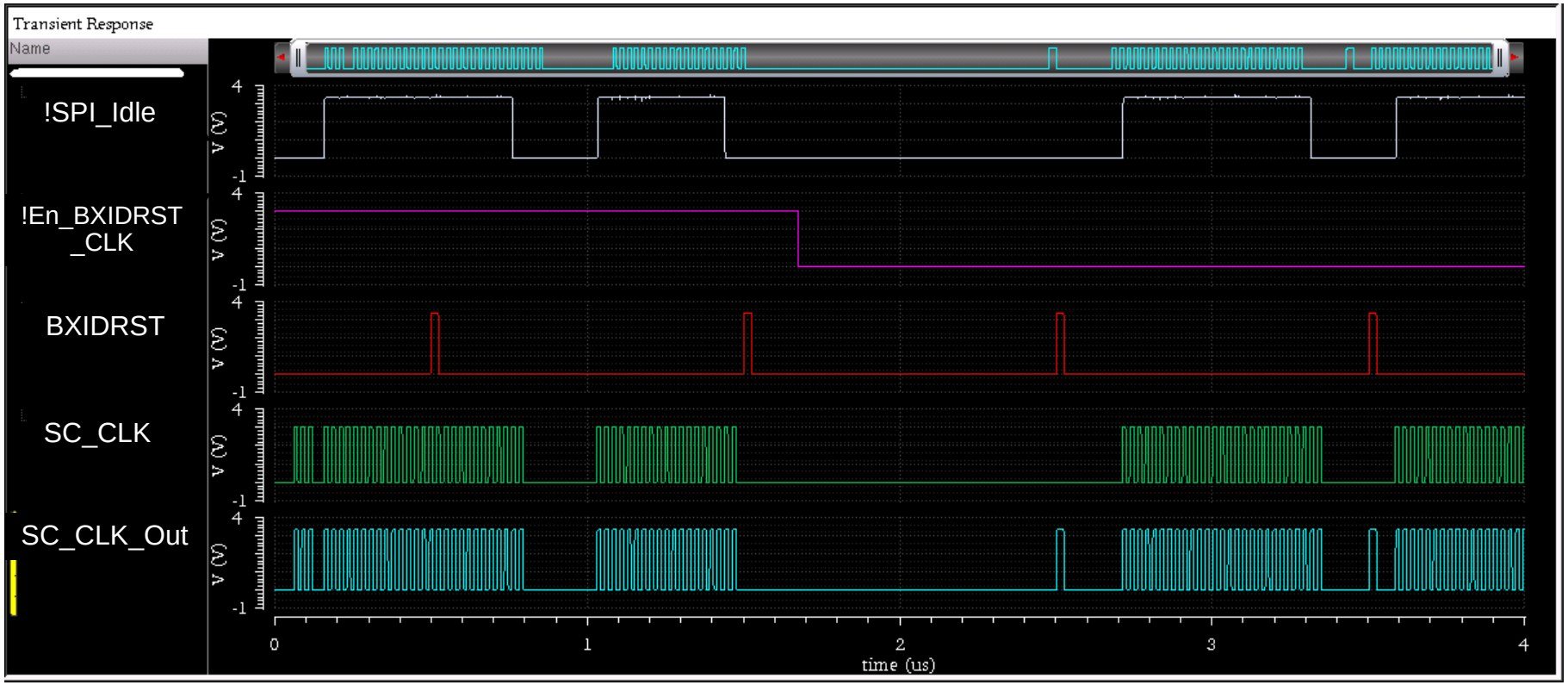
- SPI Slave control unit FSM:
  - SEU tolerant.
    - Number of states = 4.
    - Necessary bits to encode the states: **2 bits**.
    - Used bits to encode the states: **3 bits**.
    - Hamming distance between idle state and critical states > 1:
      - If SEU occurs, the FSM is automatically recovered after the next clock rising edge.
      - **Problem: not corrected until the next frame arrives (slow control clock is inactive during idle periods).**

- 16 bits TMR register:
  - Each bit is stored in 3 flip-flops.
  - A combinational block computes the majority.
  - If SEU occurs, the faulty bit is automatically corrected in the next clock rising edge.
    - **Problem: the register is protected as long as SC CLK is active.**



Improved SPI slave (ICECALv3)

- Use the BXIDRst as auxiliary clock:
  - Only when SPI slave is idle (white).
  - This capability can be enabled/disabled via SPI (purple).
  - TMR registers and SPI FSM will be refreshed every 3564 BXs (red).



Summary

- Analog shaping electronics: two solutions
  - ASIC:
    - cooled input termination for reduced noise
    - 2 interleaved channels and switched integrators: no deadtime
    - Full 4 channel ASIC to be sent in November 2013
  - Discrete elements (COTS):
    - Clipping removed from PMT base and installed in the FEB: increase in signal
    - Definitive version scheduled for the end of 2013
  - Final decision beginning 2014
  - Prototypes tested both at lab and at a test beam:
    - Specifications met except for integrator plateau and spill over
    - Simulations show a pole–zero filter would fix it.
- A delay chip has been designed for the clock distribution
  - It will be integrated in the ASIC (Nov 2013)
  - Can be used standalone for COTS
  - Standalone prototype tests ongoing
- The slow control of the ASIC(s) is based on SPI protocol
- Radiation qualification tests foreseen

Backup…

Choice of Technology

- SiGe BiCMOS is preferred:
  - SiGe HBTs have higher gm/Ibias than MOS: less noise, less Zi variation
  - SiGe HBTs have higher ft (>50 GHz): easier to design high GBW amplifiers
- Several technologies available:
  - IBM
  - IHP
  - AMS BiCMOS 0.35 um

	IBM	IHP	AMS
HBT ft	> 100 GHz	190 GHz	60 GHz
CMOS	0.13 um	0.13 um	0.35 um
Proto Cost [€ /mm^2]	> 3 K	> 3 K	1 K

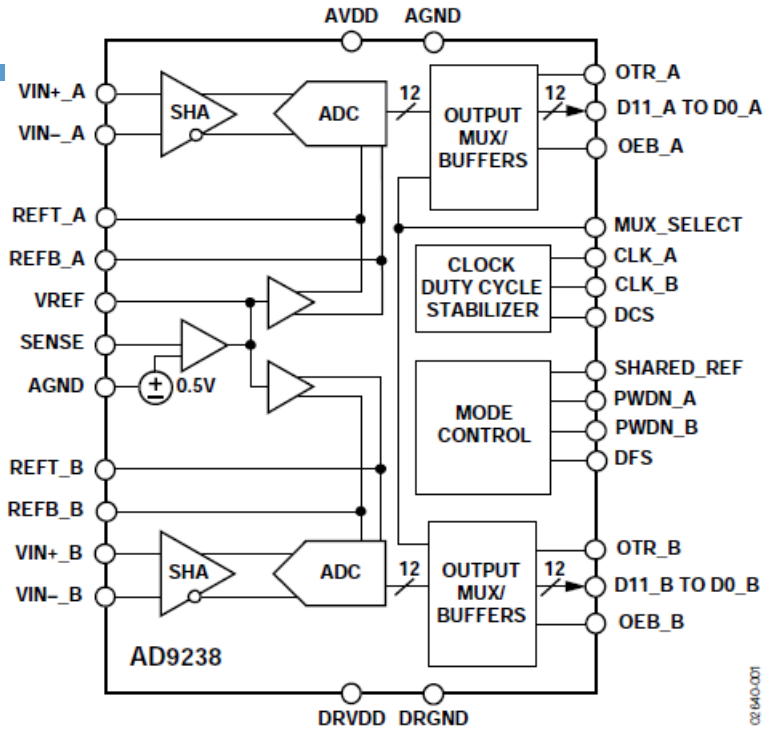
- AMS is preferred
  - Factor 2 or 3 cheaper
  - Too deep submicron CMOS not required / not wanted:
    - Few channels per chip (4 ?)
    - Smaller supply voltage
    - Worst matching
  - Radiation hardness seems to be high enough
    - 30 Krad seems to be OK (checked by other Upgrade projects)

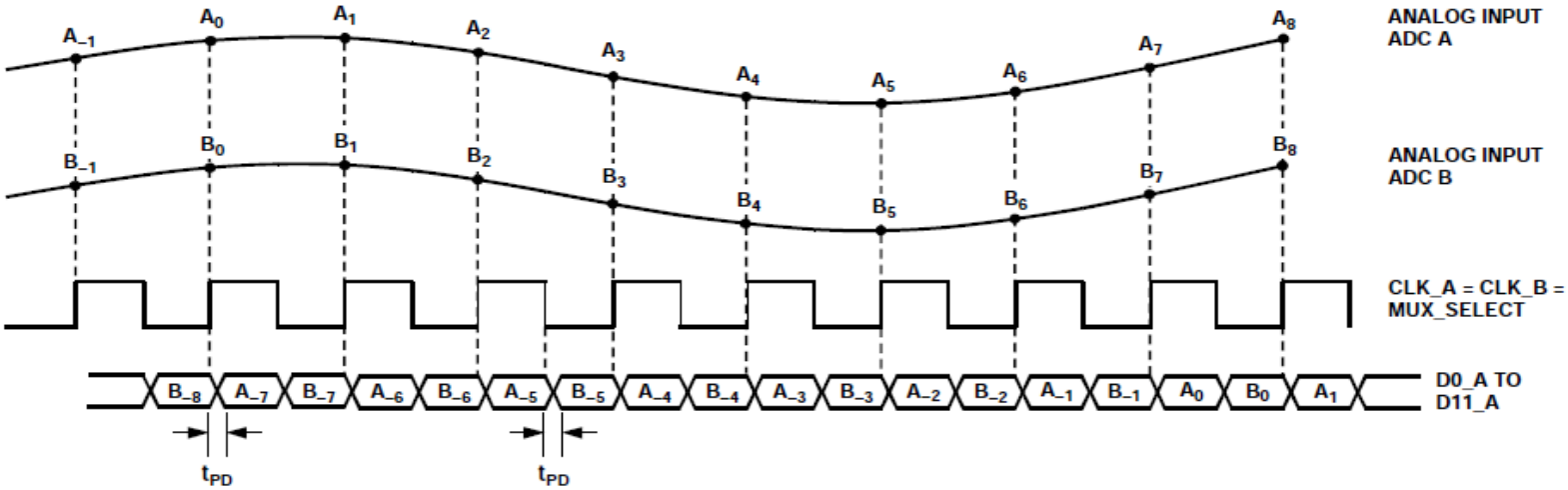
Choice of ADC

- In order to make the proper interface between the analogical part and the ADC it is necessary to have it previously selected.
- Our ADC needed 12 bits resolution, at least 40MHz conversion frequency and it was also desirable a small package due to space restrictions.
- The more suitable components for our application where:
  - Texas Instruments ADS6122
    - 1 ADC/Chip but 5x5mm only, LVDS, DDR!
  - Texas Instruments ADS6222
    - 2 ADC/Chip, LVDS, DDR!
  - Analog Devices AD9238
    - 2 ADC/Chip, LVTTL.

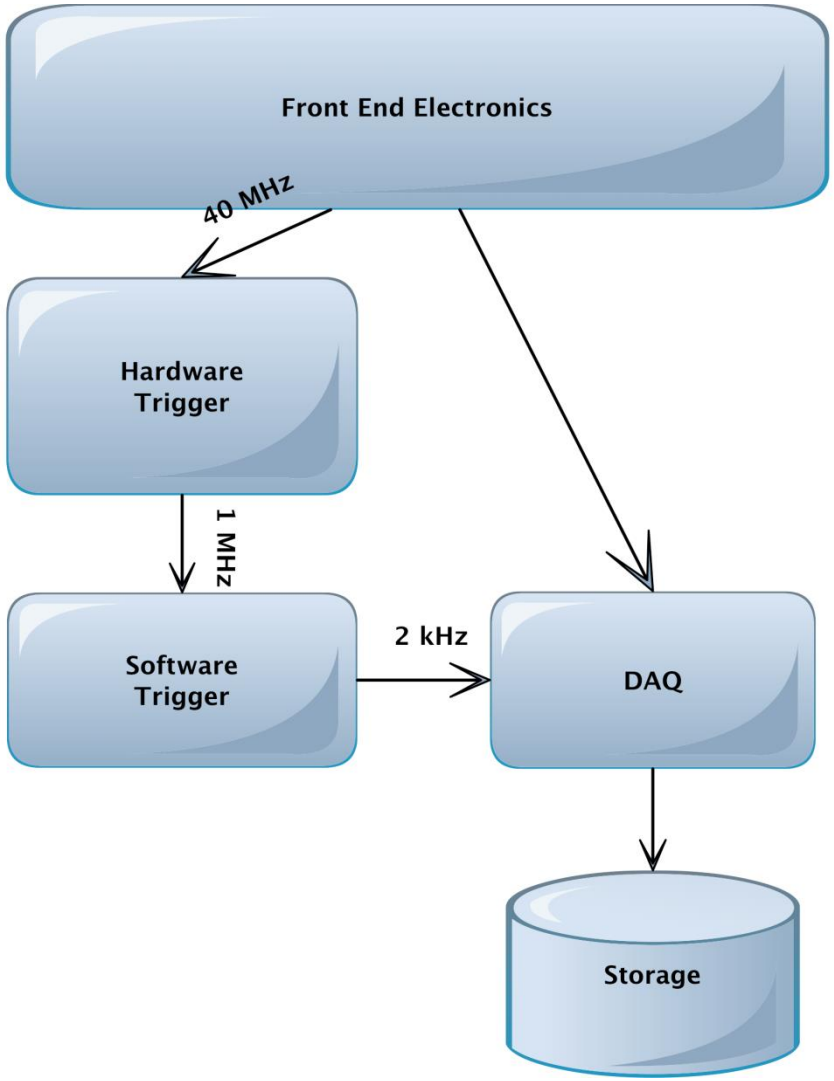
Choice of ADC

- Analog Devices AD9238
  - One sampling clock per channel
  - Optional multiplexing
  - No RAM configuration



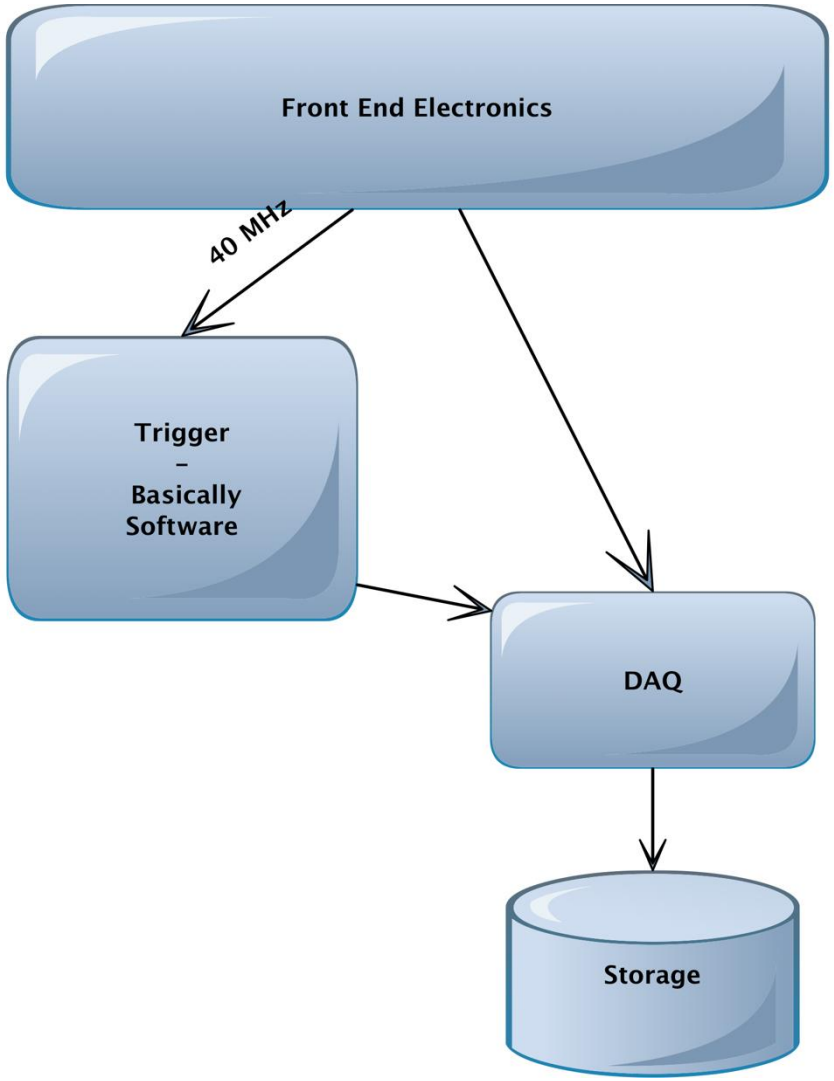


General Requirements



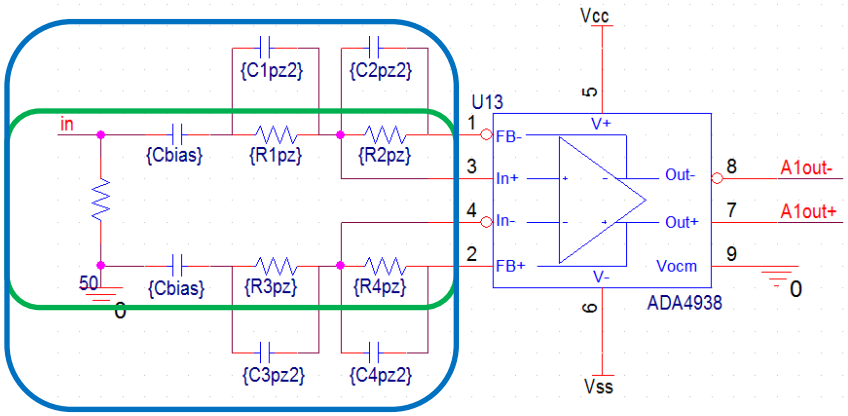
- 40 MHz frequency
- Front End Electronics Resolution must meet detector requirements
  - Precision
  - Noise
- Radiation tolerance conditions (SEU-SEL)
- ECAL : 6000 Channels
- HCAL : 1500 Channels
- Detector side
  - PMT + base
- Front End Electronics
  - Analog processing
  - Digital processing
  - Control Scheme

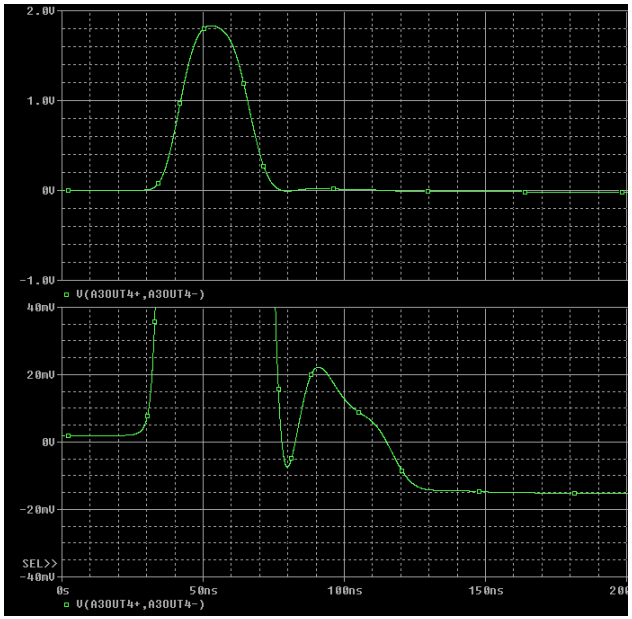
The need for an upgrade



- 2018 : luminosity increase
  - Keep same detector
  - Lower PMT gain to protect against aging
  - Lower signal
  - Increase Electronics gain
  - Keep precision
- Change in the trigger structure
- Change in the control structure
  - Requires changes in digital FE part

COTS: stage 1





- Original COTS design
  - Rin=50
  - Amplifier ADA4938 G=10
  - Single to differential
- COTS modifications after TB 2012
  - Signal measured at Test Beam more expanded than the one used for design
  - Added a filter to equalize the cable
    - Pole-zero (under study)
- Adjusting
  - Fixed values: BW
  - Variables adjustable: Gain, pole, zero

Slow control implementation

- SPI Slave control unit FSM:
  - SEU tolerant.
  - Hamming distance between states > 1.

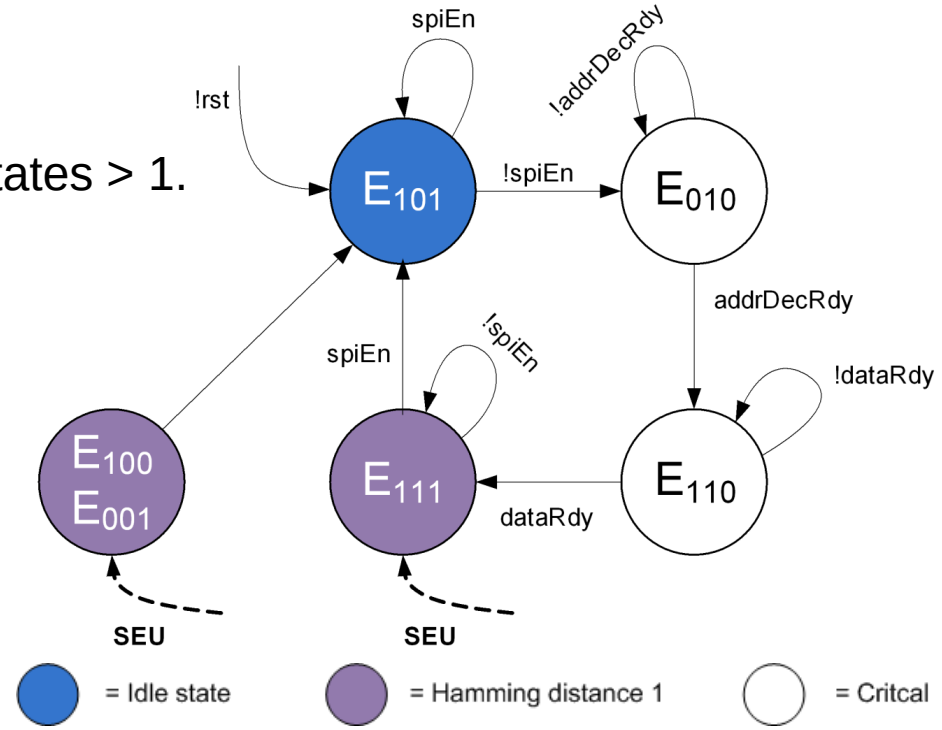
Idle state (E_{101}) → spiEn = '1'

If 1-bit SEU occurs:

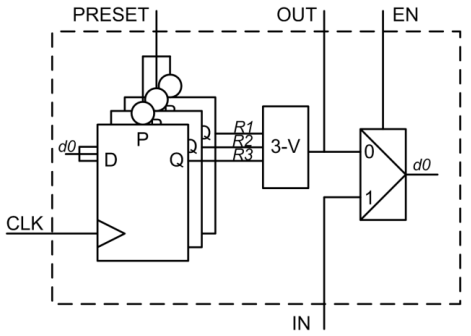
E_{100}, E_{100}, E_{111} → E_{101}

... After the next clock cycle.

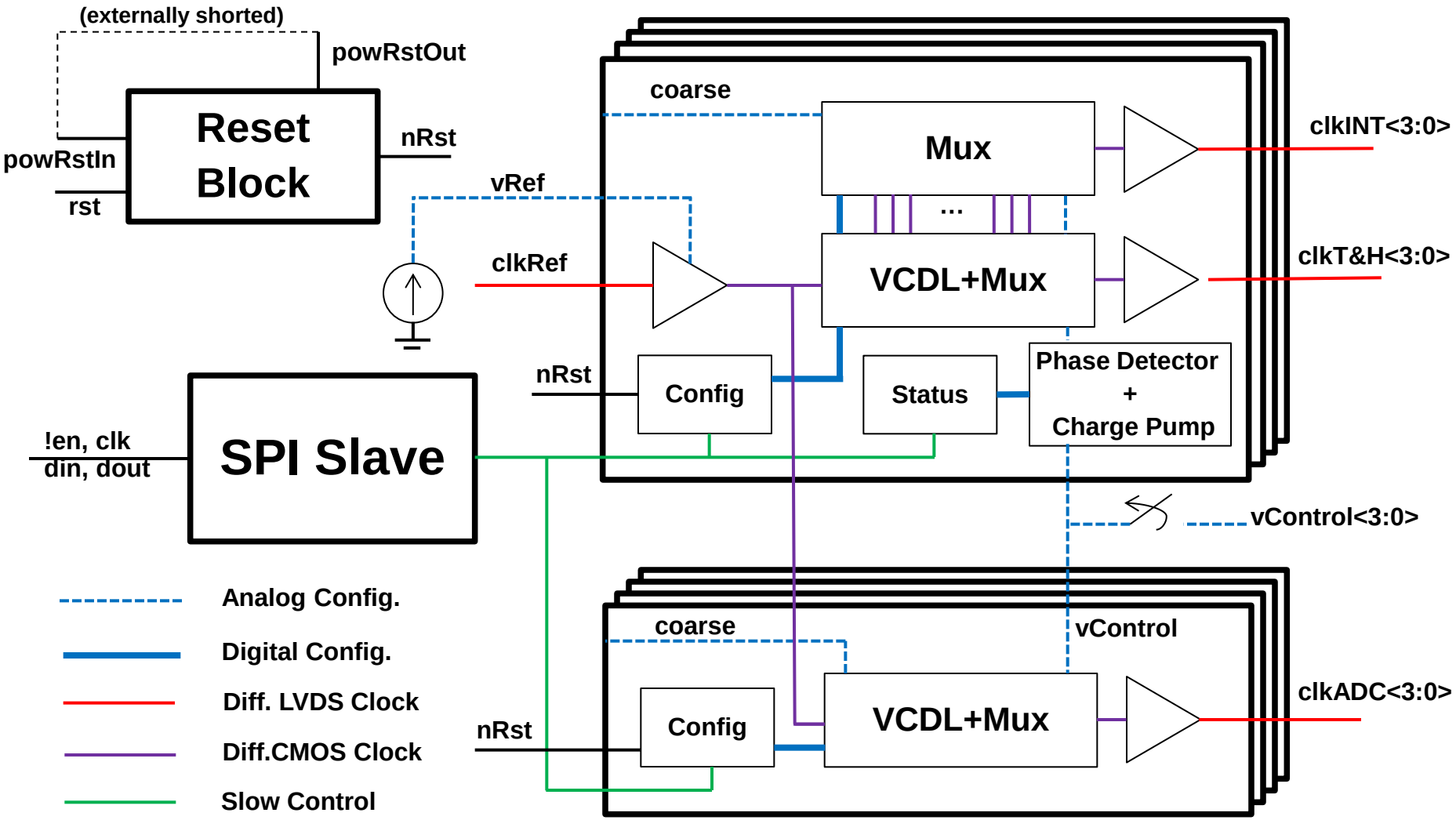
Problem: not corrected until the next frame arrives.



- 16 bits TMR register:
  - Each bit is stored in 3 flip-flops.
  - A combinational block computes the majority.
  - If SEU occurs, the faulty bit is automatically corrected in the next clock rising edge.
    - Problem: the register is protected as long as SC CLK is active.

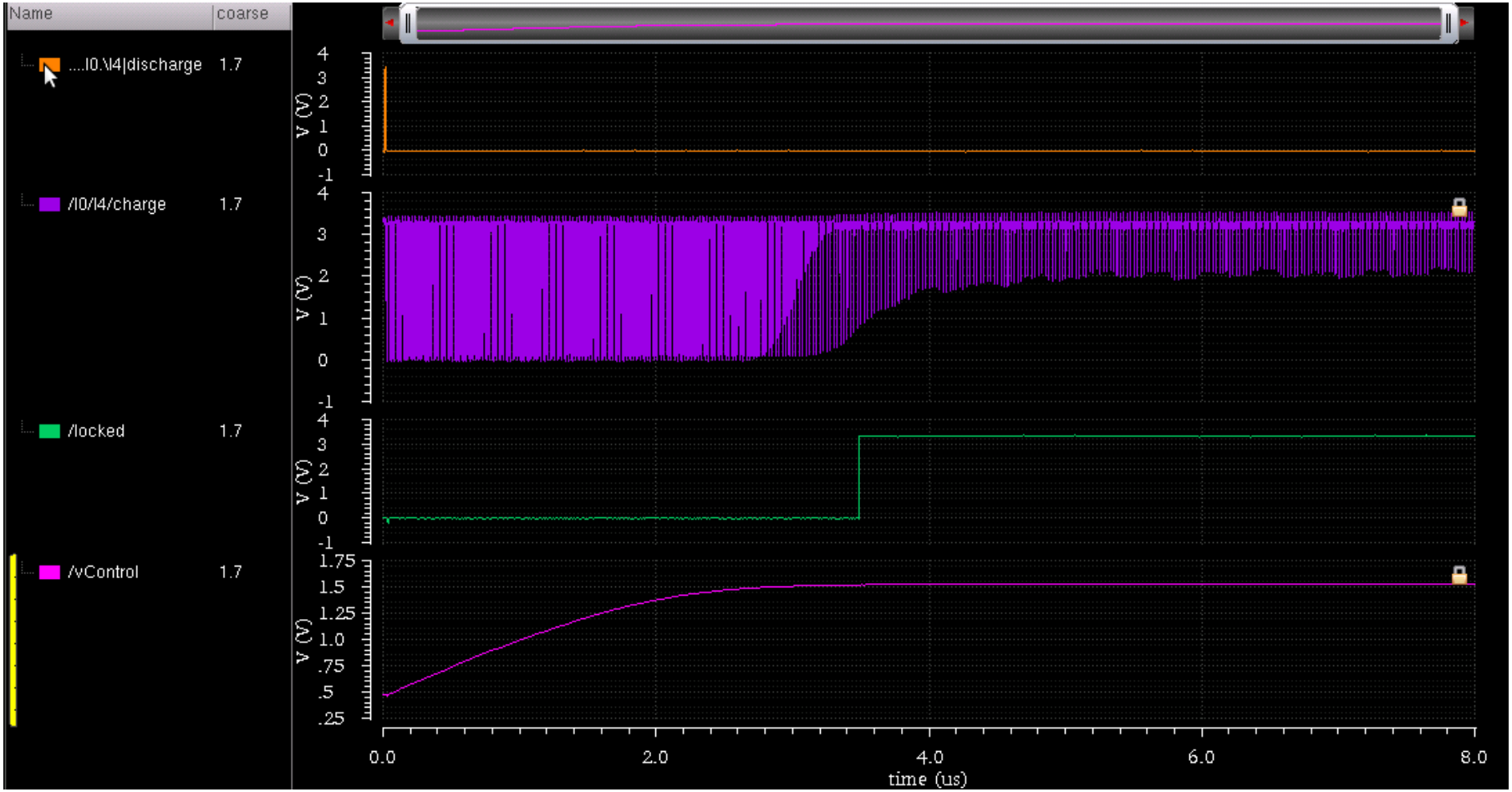


Delay Line: design overview



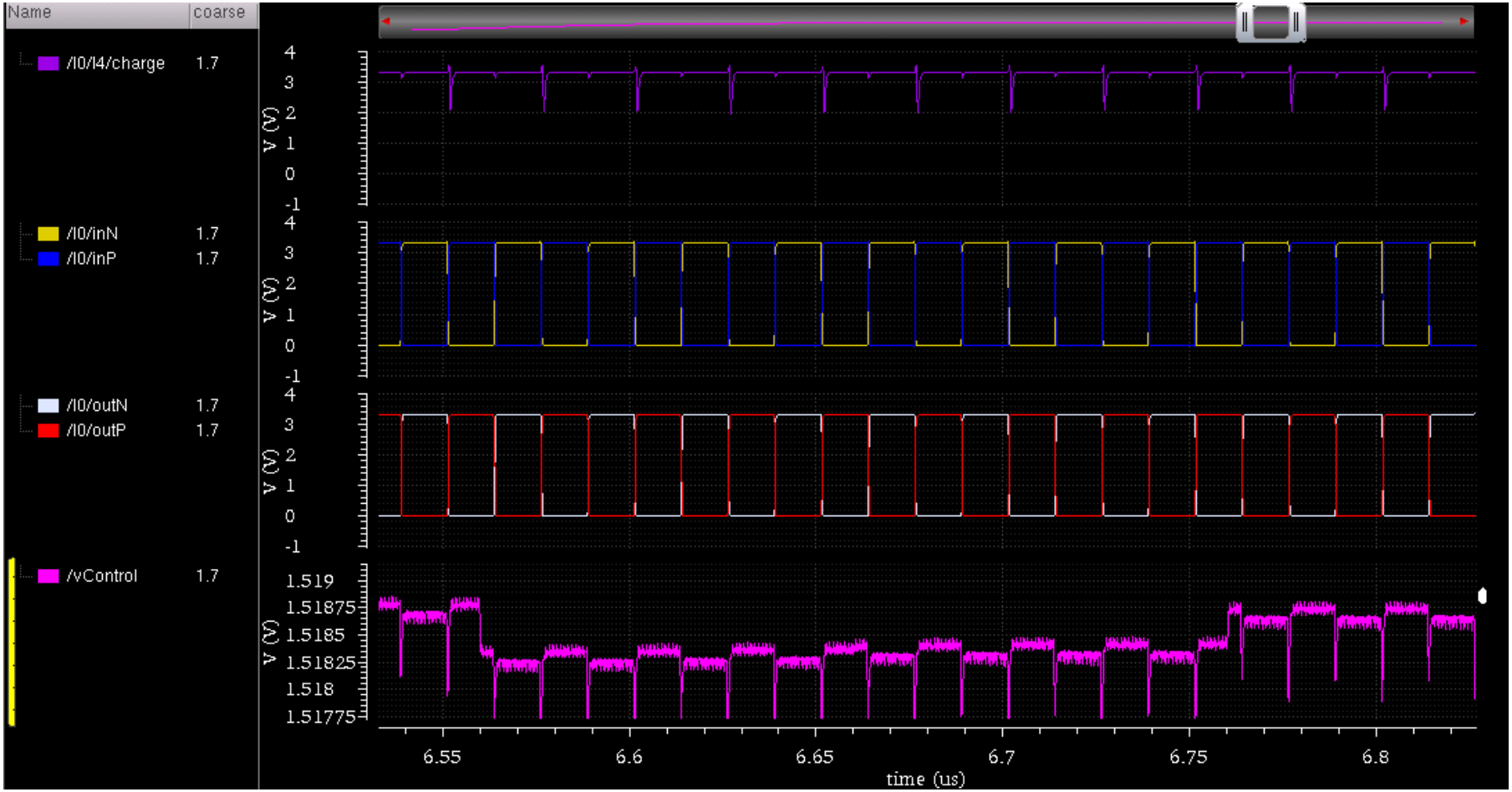
Delay Line implementation

- Simulation results: Charge pump.



Delay Line implementation

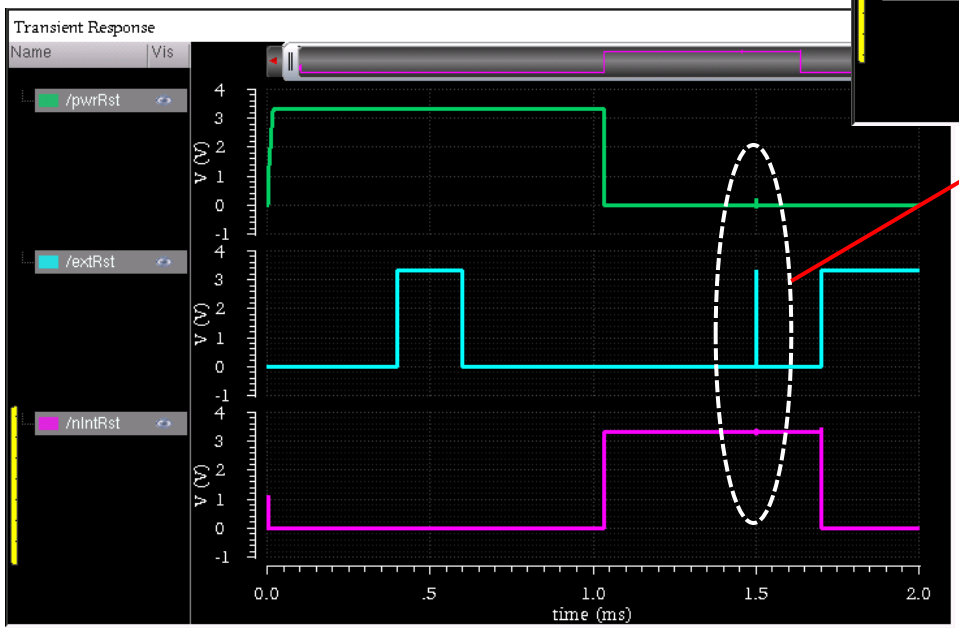
- Simulation results: Phase detector (locked).

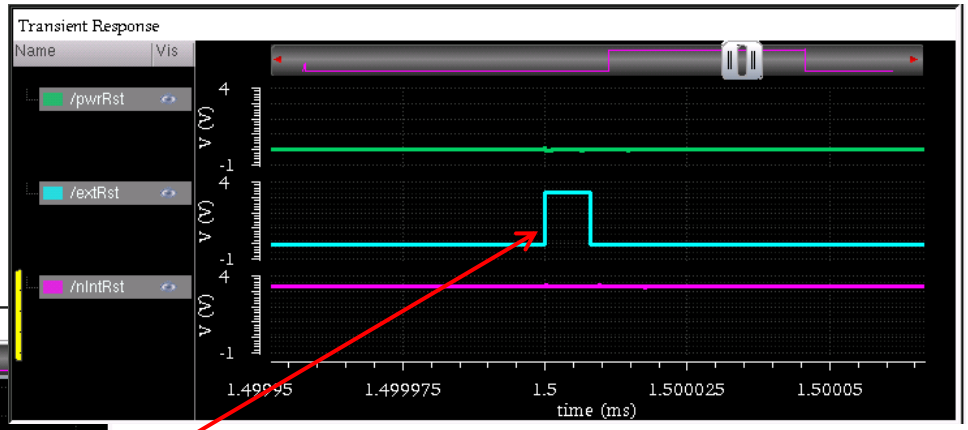


Delay Line implementation

Simulation results:

Power RST + glitch supressor





- **Top: Power RST. 1-ms-wide.**
- **Mid: External RST.**
- **Bottom: glitch-free Internal !RST.**

SPI Slave Addressing Scheme

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
R/!W	Pump Rst	Status/!Conf	$RSEL_4$	$RSEL_3$	$RSEL_2$	$RSEL_1$	$RSEL_0$

ADDR	ICECAL Ch	Width (bits)	Description
0x00	0	16	Integrator / Track&Hold Clock Configuration Register.
0x01	0	16	ADC Clock Configuration Register.
0x02	1	16	Integrator / Track&Hold Clock Configuration Register.
0x03	1	16	ADC Clock Configuration Register.
…			
0x10	2	16	Integrator / Track&Hold Clock Configuration Register.
0x11	2	16	ADC Clock Configuration Register.
0x12	3	16	Integrator / Track&Hold Clock Configuration Register.
0x13	3	16	ADC Clock Configuration Register.
…			
0x40	Any	-	Software Reset of the Charge Pumps.
…			
0xA0	0	8	Status Register.
0xA1	1	8	Status Register.
0xB0	2	8	Status Register.
0xB1	3	8	Status Register.
…			
0xFF	-	-	SDI / SDO Bypass. For testing purposes.