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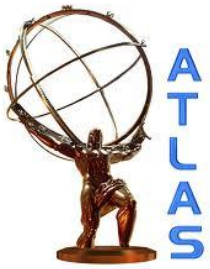

Upgrading the ATLAS Tile Calorimeter electronics

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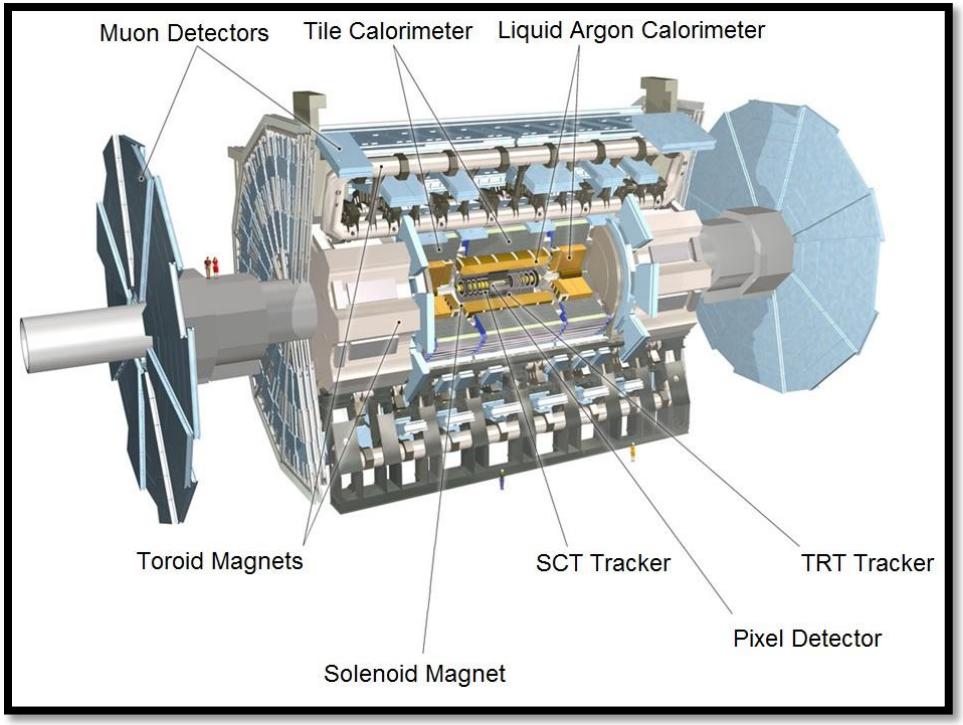
On behalf of the ATLAS Tile Calorimeter System

Outline

- Introduction
- Detector Concept
- Why Upgrade?
- Current Versus New Architecture
- Demonstrator Project
  - Overview
- Tile Muon Project
- Summary

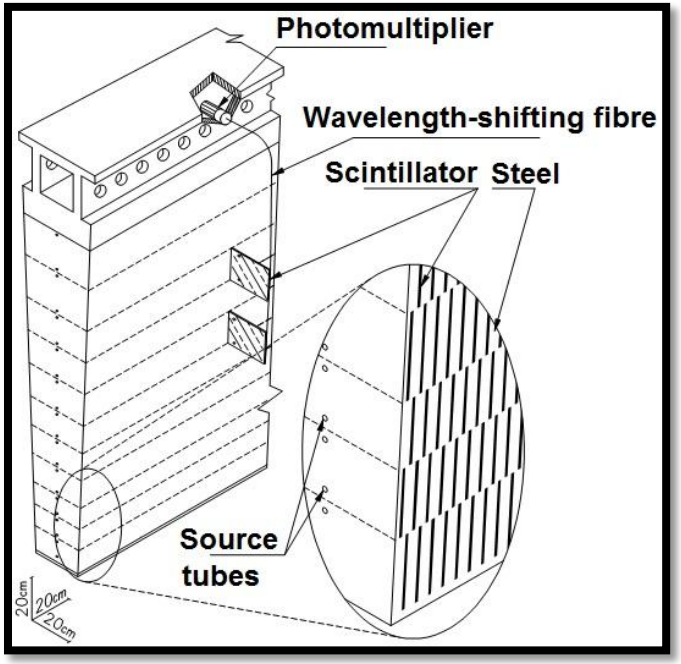


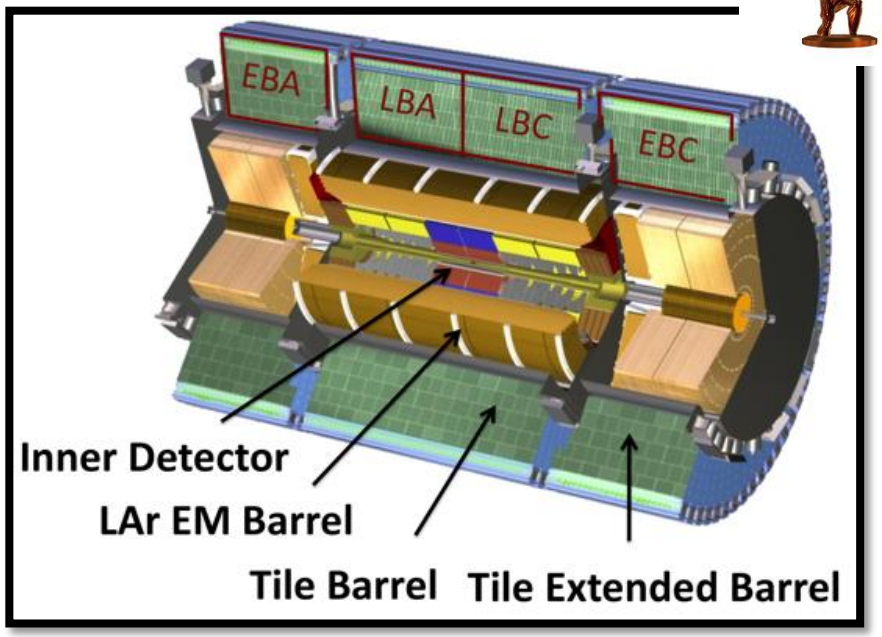
ATLAS detector - Features

- Weight : 7000 t
- Length : 46 m
- Diameter : 25 m
- Around 100 million electronic channels
- Around 3 000 km of cables

The ATLAS Tile Calorimeter (*TileCal*)

- Hollow cylinder, mechanically divided into three partitions, positioned in the most central region of ATLAS
  - at the read-out point of view there are four partitions: EBA, LBA, LBC and EBC
  - weighs 2,900 tons
- Based on steel plates as absorber material and plastic scintillating tiles for sampling the energy



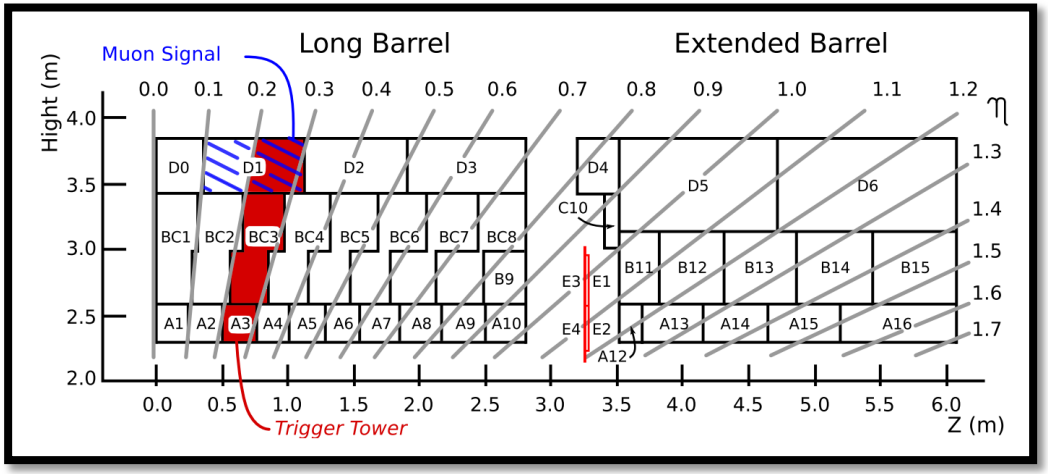


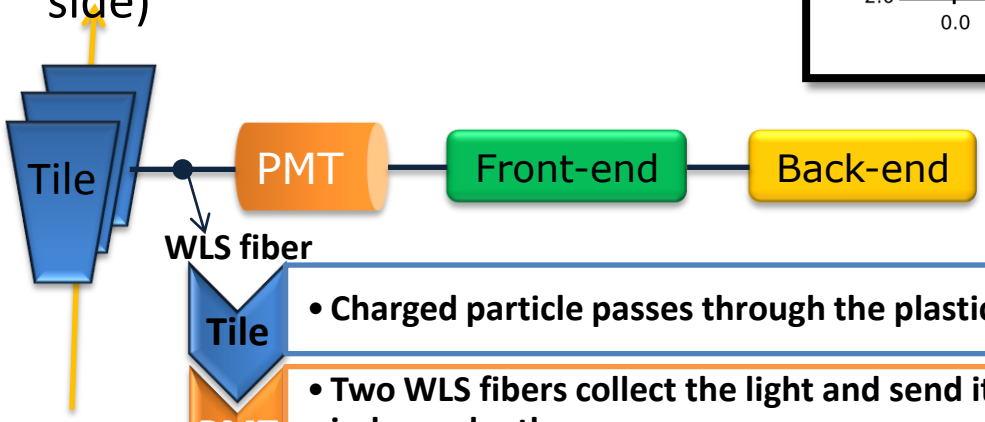
- Each partition is divided in 64 modules with a trapezoidal shape
- The front-end electronics is located in the outermost region of each module (in what we call a "super-drawer")
  - Wavelength shifting (WLS) fibers transmits the light to the photo-multiplier tubes (PMT)
  - The PMT is the first step in the *TileCal* signal chain
- In total, *TileCal* has 9852 PMTs

Detector Concept

- Based on a simple concept
- The *TileCal* modules are divided into cells, which consist of a certain number of steel plates and plastic scintillators.
- Each cell is read-out by different two PMT's (one per side)

ATLAS Tile Calorimeter Cells Layout





Tile • Charged particle passes through the plastic scintillating tile and produces some light

PMT • Two WLS fibers collect the light and send it to two different PMTs that are read out independently

FE • The signal is integrated, sampled and stored in a pipeline memories in front-end electronics

BE • Stored data is transferred to back-end electronics

Upgrade - Motivation

- ATLAS (Tile Calorimeter) performance during the first years of LHC in operation has been outstanding , **but new conditions (challenges) are expected for the next years**

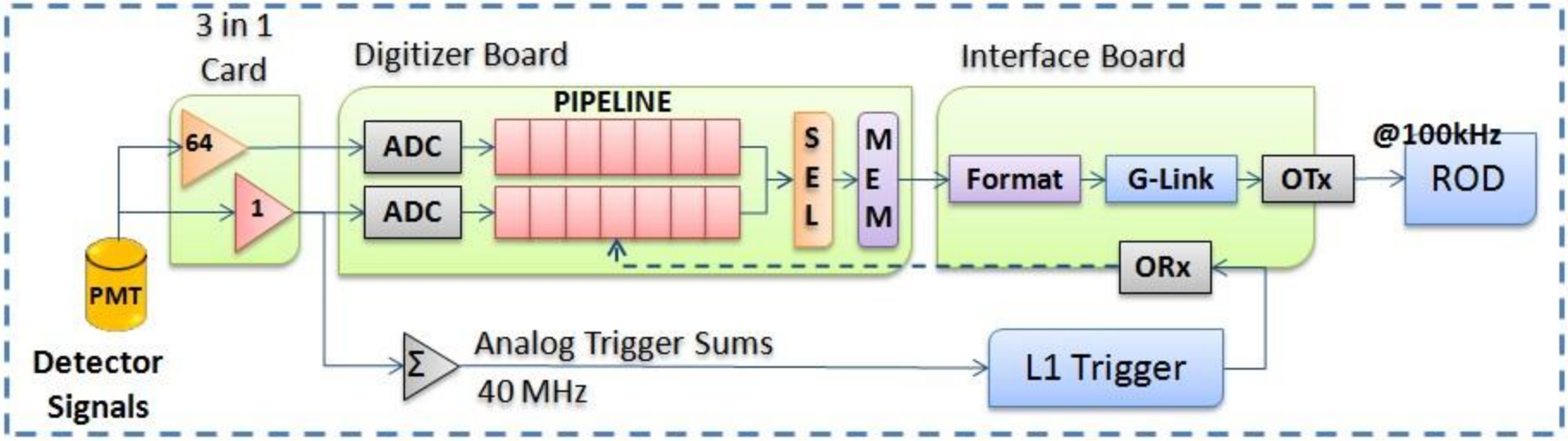
1. **Increasing the instantaneous luminosity with a factor of 5 by 2023**
   - More events accepted with current criteria, but level 1 rate must stay at 100kHz – L2 capacity increased, but also event sizes
     - Introduce Level 0 trigger to reduce Level 1 input rate to limit
   - Higher data rate for communication between front-end and back-end electronics
     - On every bunch crossing, all data should be sent from the on-detector electronics to the off-detector
     - No analog trigger; all signals (digital) sent via fast fiber
   - Increased occupancy - ~200 minimum bias events/BC pile up
2. **Adapt to changing physics requirements**
   - Usage of D-cells to contribute to the Level 1 muon trigger

Upgrade - Motivation

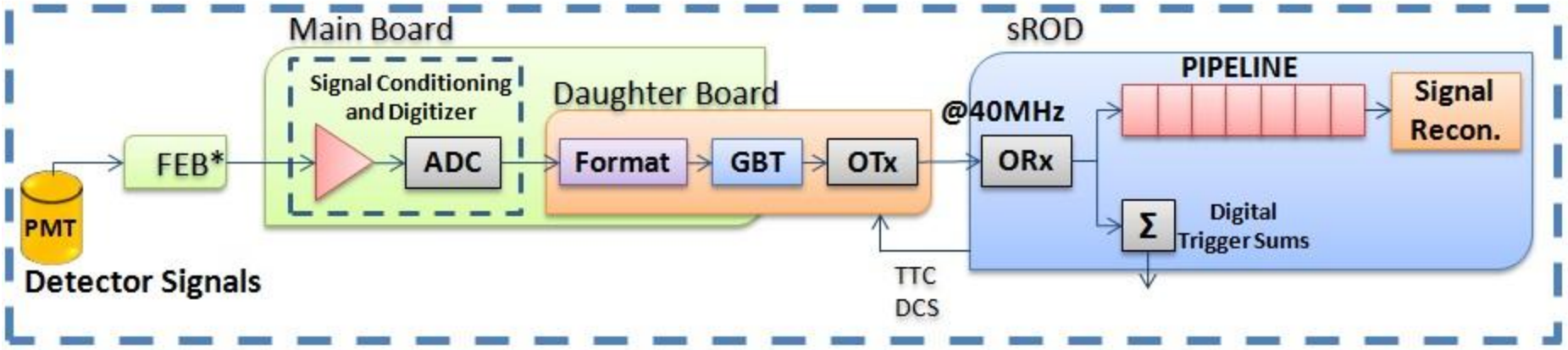
3. **Replacement of on –detector electronics due to old age and radiation**
   - Designed for 10 years
   - Higher levels of radiation, requires higher levels of radiation tolerance by the electronics installed in the cavern
4. **Reduce single point failures of electronics (reliability and robustness)**
   - Full redundant in the read-out path from cells to the data links in the back-end
   - Increase modularity in front-end to limit consequences of failures
     - Reduce the smallest independent on-detector electronics module, from 45 to 6 channels,
   - Redundancy low voltage power supplies
     - Challenge to route more fibers and LV cables inside *TileCal* Drawer

Phase II – Current Versus New Architecture

- Current Architecture



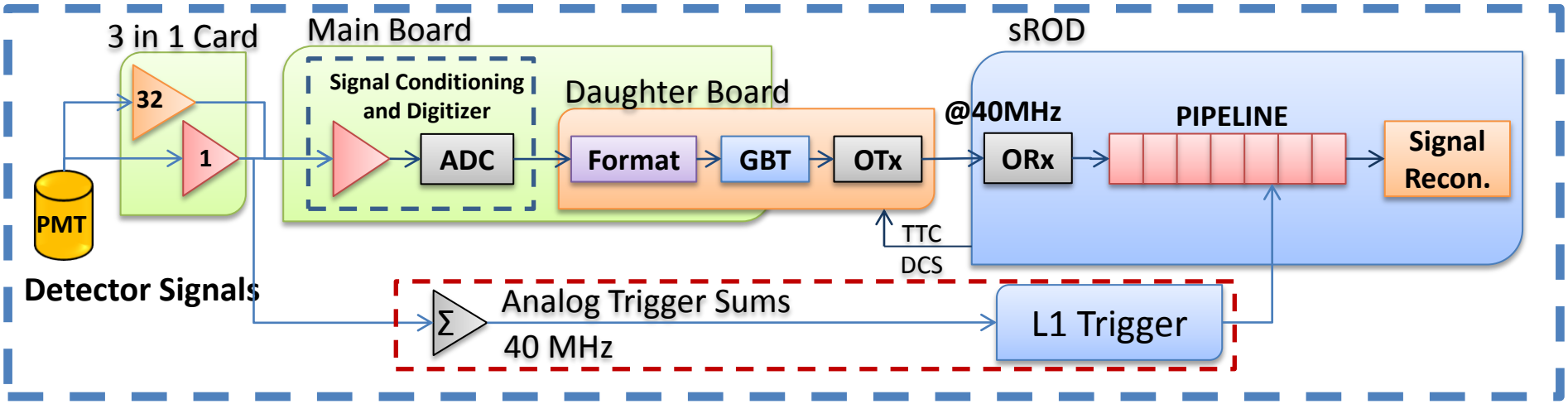
- Proposed New Architecture



*will be evaluated in test beams

Tile Demonstrator Drawer

- Such an extensive redesign needs testing
  - Long Shutdown 1 (LS1) in LHC (2013-2014)
  - Possibility of evaluating and qualifying the proposed technology
- Installation of one hybrid drawer, combining a version that fulfill all upgrade requirements while also being compatible with the present system
  - Still using analog trigger
  - The sROD system will interpret the Trigger Timing Control (TTC) and the Detector Control System (DCS) commands and translate new detector data into a form acceptable by the present ROD

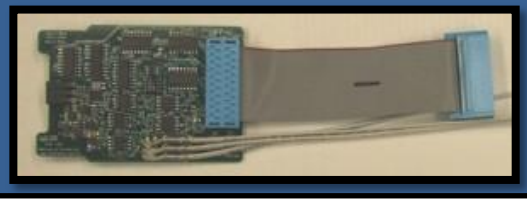


Front-end Electronic Options

Demonstrator

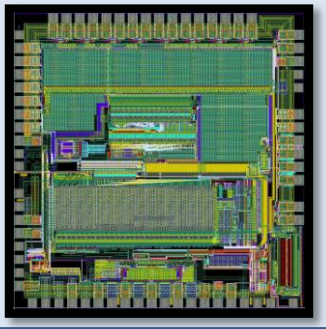
Modified 3-in-1 Card

- Based on current 3-in-1 cards
  - But with better linearity and lower noise
- Two different analog outputs, with different gains
  - Can provide analog trigger in demonstrator
- Calibration capabilities
- Integrator read-out for dedicated and in-physics calibration data
- Approved in radiation tests



QIE ASIC

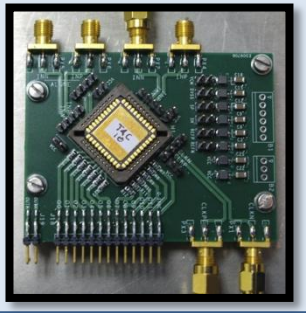
- Based on QIE chip from *Fermilab*
- Four different gains, but without shaping
- Data Output : 10 bits encodes a 17-bit dynamic range
- Clean measurement every 25 ns
  - Useful for pile-up



FATALIC

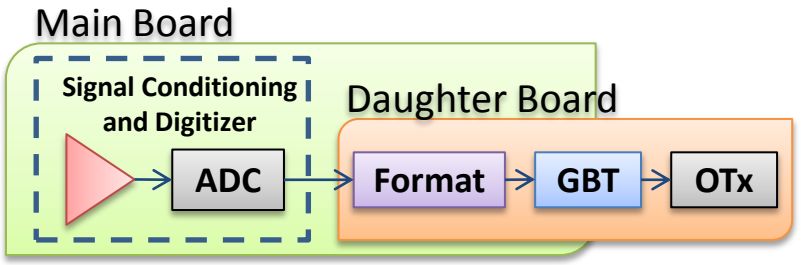
- Combines "Front-end for Atlas TileCal Integrated Circuit" (FATALIC) with "Twelve bits AdC for s-atlas Tilecal Integrated Circuit" (TACTIC) in a ASIC solution
- FATALIC
  - 3 gain ranges (1, 8 and 64), with shaping stage
- TACTIC
  - 12-bit pipelined ADC
  - 40 MHz

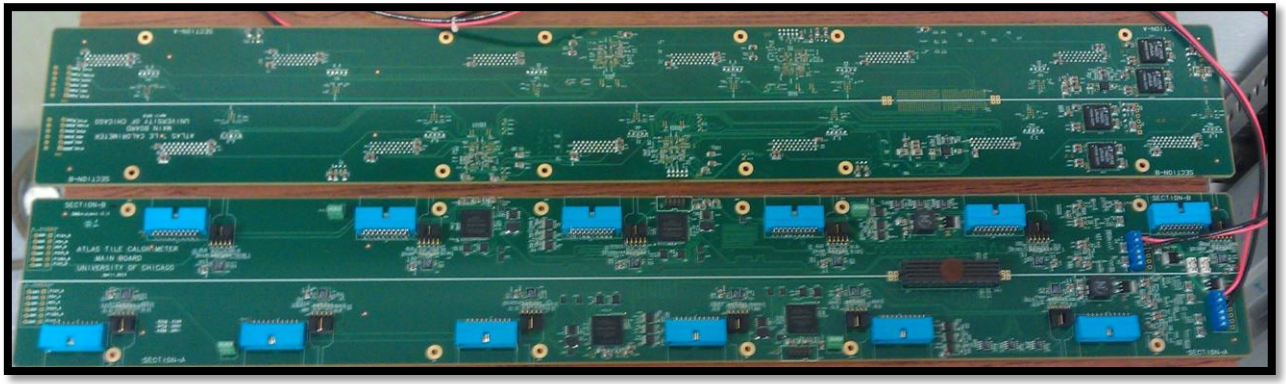
TACTIC ADC



Demonstrator Overview

- **Main Board**
  - Designed to receive and digitize signals coming from the modified 3 in 1 card
    - 12 inputs (from the 3 in 1) per board
  - 4 Altera FPGAs used for digital control of front-end boards
  - Power distribution divided into two halves (redundancy)
  - Digitized data is sent to daughter board (FMC connector)

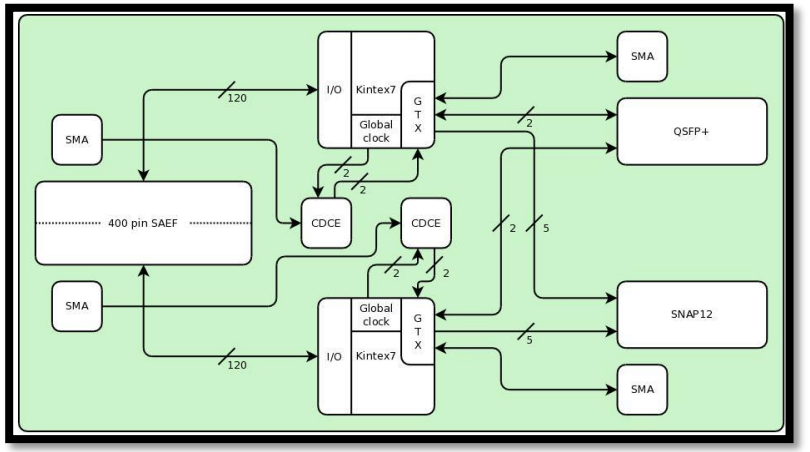


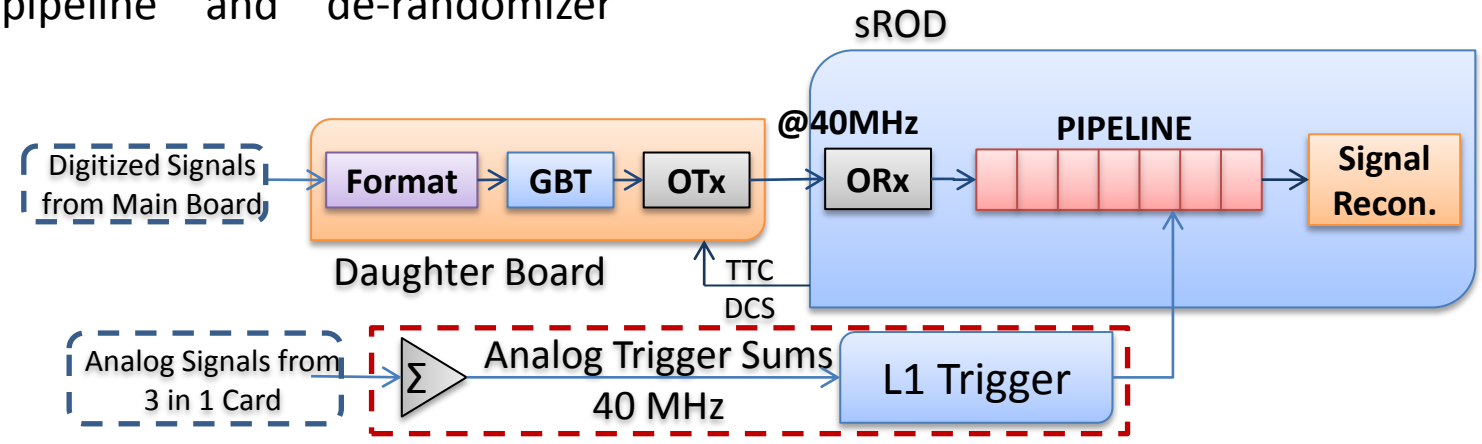


Demonstrator Overview

- **Daughter Board**
  - High speed data interface with back-end electronics
  - Implements a redundant system
    - 2 FPGAs, 2 QSFP modules and GBT x chips
- **sROD**
  - Interface between front-end electronics and trigger system
  - Takes care of the initial trigger processing while temporarily storing the main data flow in pipeline and de-randomizer memories.

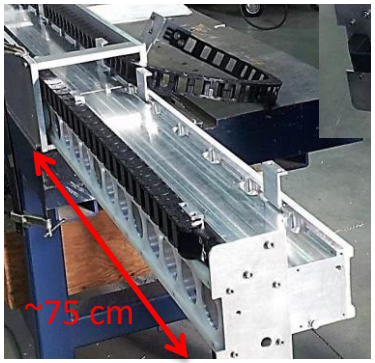
Conceptual design of daughter-board (second prototype)



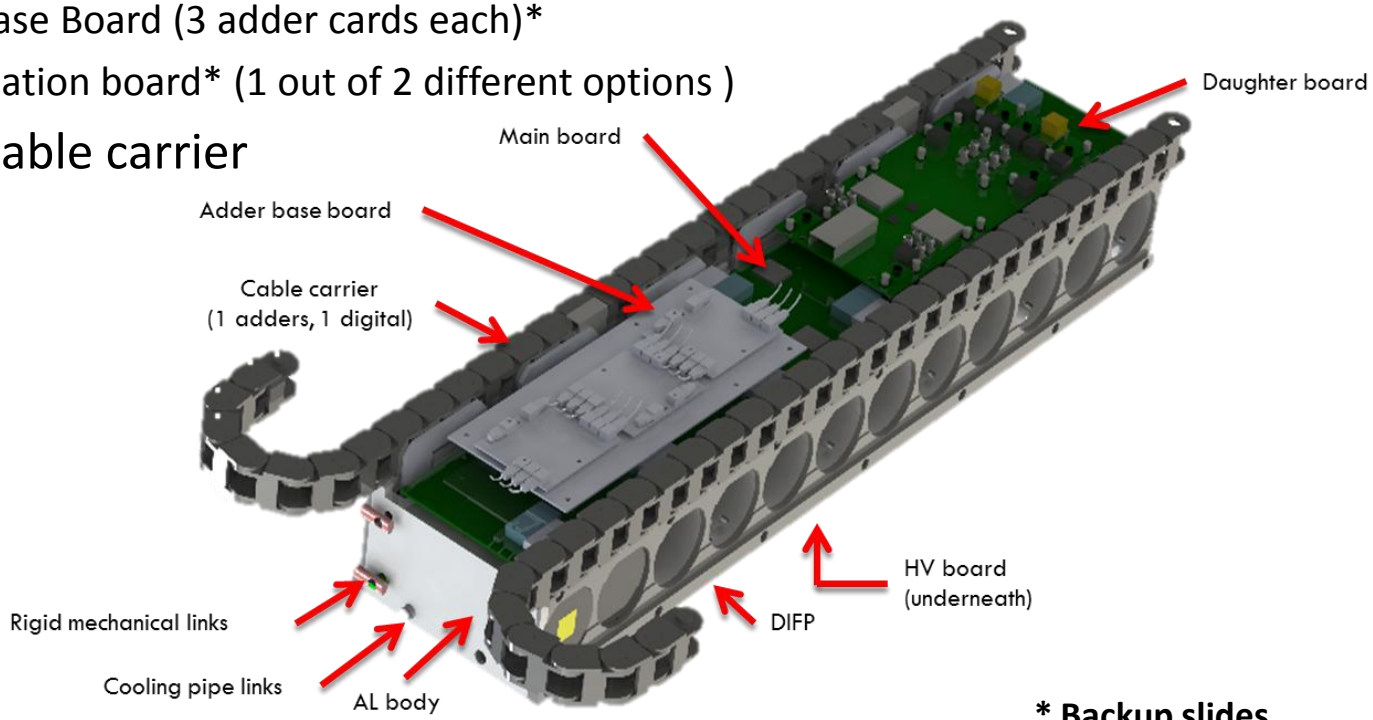


Mechanics/MiniDrawers

- New mechanical design in the *TileCal Drawer* for the upgrade
- Composed of 4 mini-drawers
  - Each mini-drawer has
    - 12 Front-end boards
    - 1 Main Board
    - 1 Daughter board
    - 1 Adder Base Board (3 adder cards each)*
    - 1 HV regulation board* (1 out of 2 different options)
- Equipped with cable carrier



Mini-drawer with cable carriers



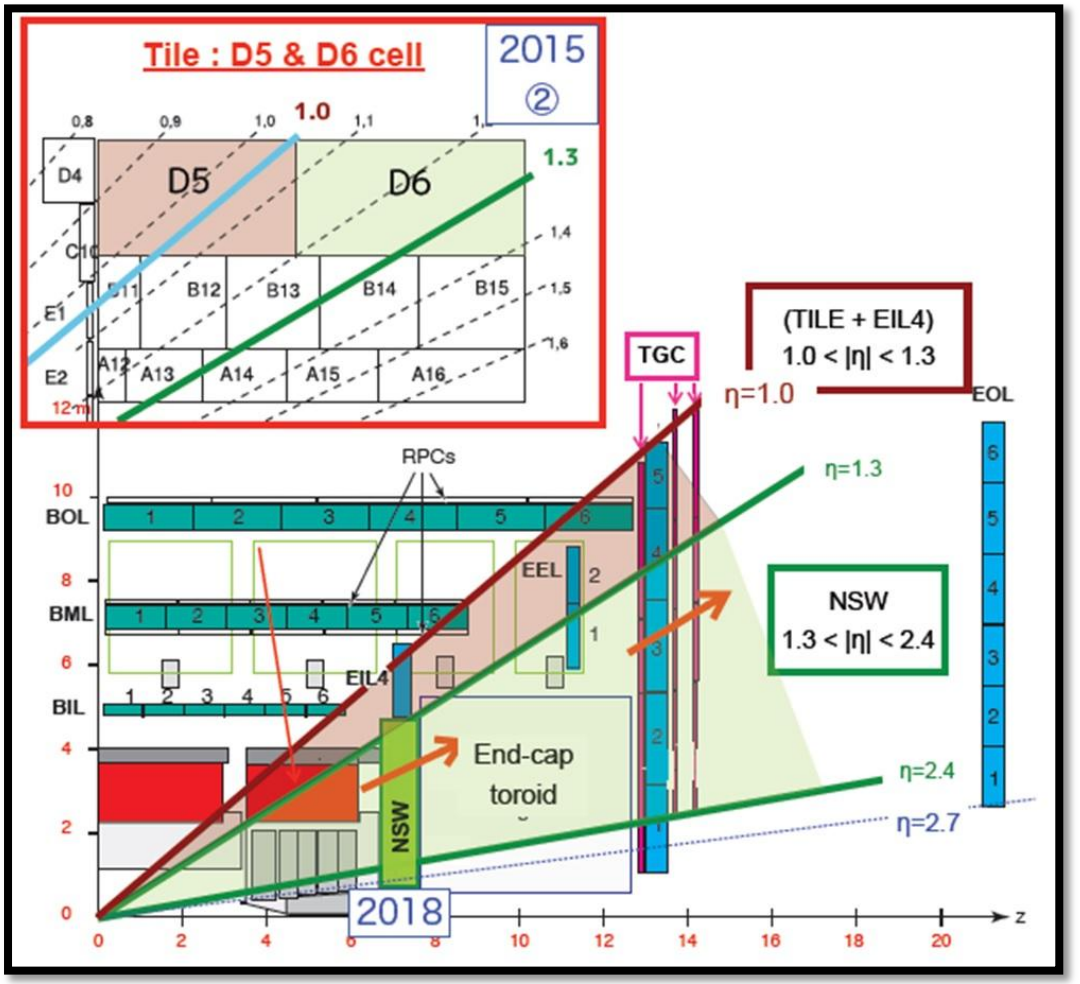
*** Backup slides**

Upgrade Status

- **Front-end Boards**
  - **Modified 3 in 1**
    - Prototype tested
      - Passed radiation tests
  - **QIE**
    - Scheduled to receive 40 more chips (20 already in hands)
    - Promising results in radiation tests
      - Already approved in noise, dynamic response and TDC tests
  - **FATALIC**
    - Good results with first and second prototypes – ongoing tests on third version
    - Designing TACTIC second version
- **Main Board**
  - First version is under tests now
    - Promising results
- **Daughter Board**
  - First prototype tested in 2011
  - Second prototype manufactured in 2012 managed to provide continuous data stream to back-end
  - Third prototype already designed and under tests now
- **sROD**
  - First prototype already produced (on assembling manufacture)
  - Firmware developments already started

Tile Muon Project

- L1 μ trigger in the End-cap region is polluted due to slow charged particles (protons)
- For the region covered by 1.0<|η|<1.3, it can be cleaned-up by taking coincidence with TGC (Thin Gap Chambers) inner station chambers and Tile D5 and D6



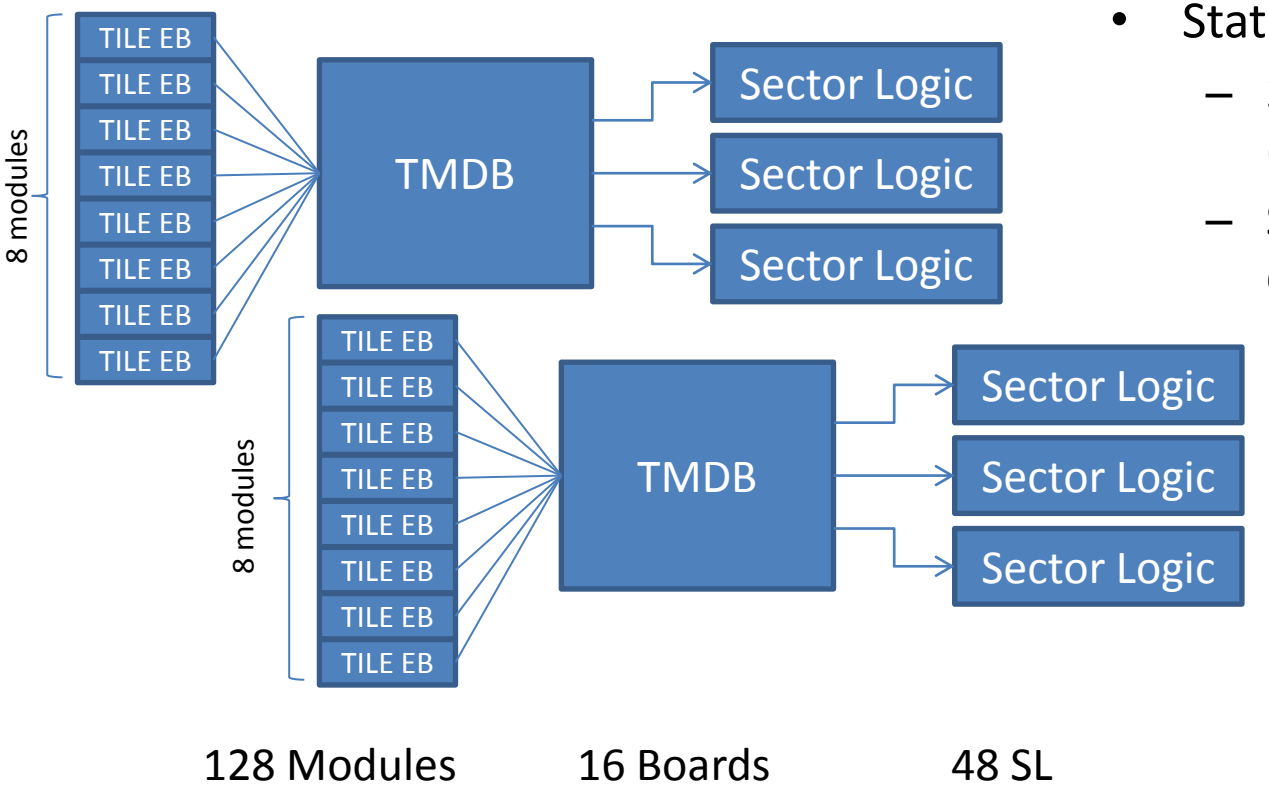
Summary

- For the next years, new conditions are expected in LHC
  - Increase the instantaneous luminosity
    - Complete redesign of the front-end and back-end electronics for Phase II Upgrade
  - Several ongoing projects on the ATLAS Tile Calorimeter related to electronics upgrade and replacement
    - Implement redundancy in all front-end elements
    - Some choices pending on the test beam performance in 2015
- During LS1, possibility of installing a hybrid demonstrator for testing some features of the future architecture
  - Early prototype of the electronics planned to be installed before 2015
- Usage of D-Layer cells to contribute to the Level 1 muon trigger
  - Scheduled installation for next year

BACK UP

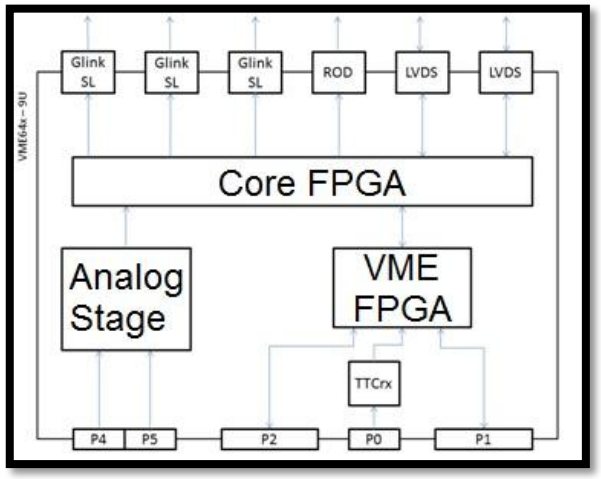
Tile Muon Digitizer Board

- Biggest challenge for ATLAS Tile Calorimeter upgrade is the read-out of the D-Layer cells to contribute to the Level 1 muon trigger
- New Tile Muon Digitizer Board will read-out 512 outputs (that were never used before) from 128 different modules to improve the efficiency of trigger for muons



- Status
  - 3 prototypes already produced (on assembling manufacture)
  - Starting firmware developments

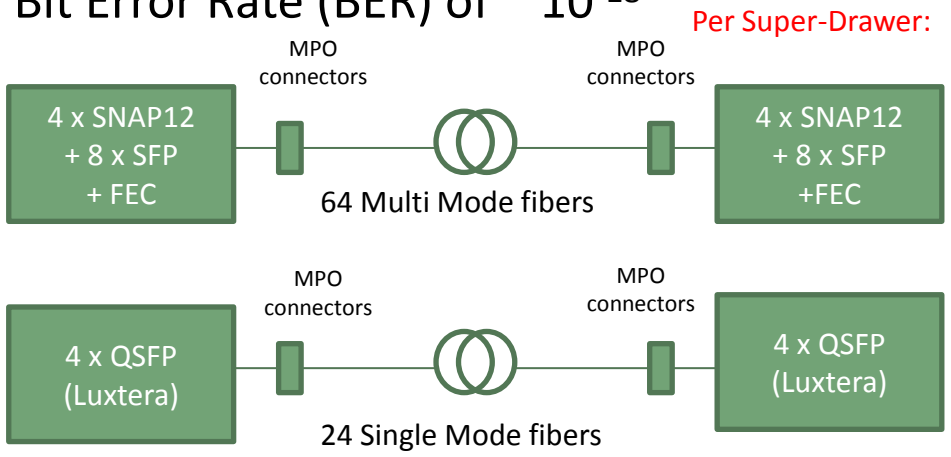
TMDB



Optical Links

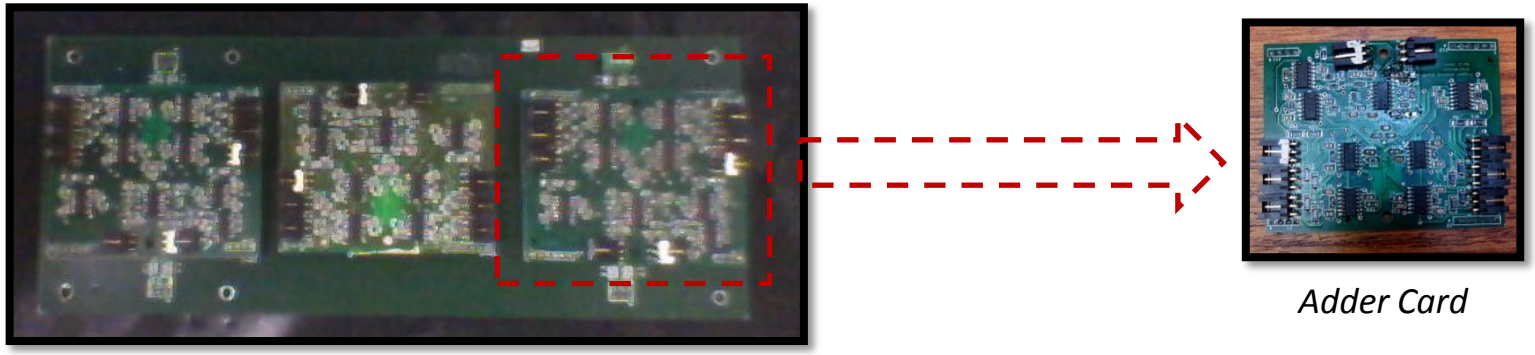
1. Vertical-Cavity Surface-Emitting Lasers (VCSEL)
   - Qualified at 10 Gbps, with Bit Error Rate (BER) of ~ 10^{-12}
   - Increasing bandwidth increases problems
   - Requires Multi Mode fibers
2. QSFP+ transceivers based on modulators
   - A commercial off-the-shelf solution exists that uses single mode fibers at high transfer rates from Molex using Silicon Photonics technology developed by Luxtera (QSFP Active Optical Cable)
   - Operates above 40 Gbps, with Bit Error Rate (BER) of ~ 10^{-18}
   - Radiation hard proved

- **QSFPs are the preferred option for the demonstrator**



Base Board for Adder Cards

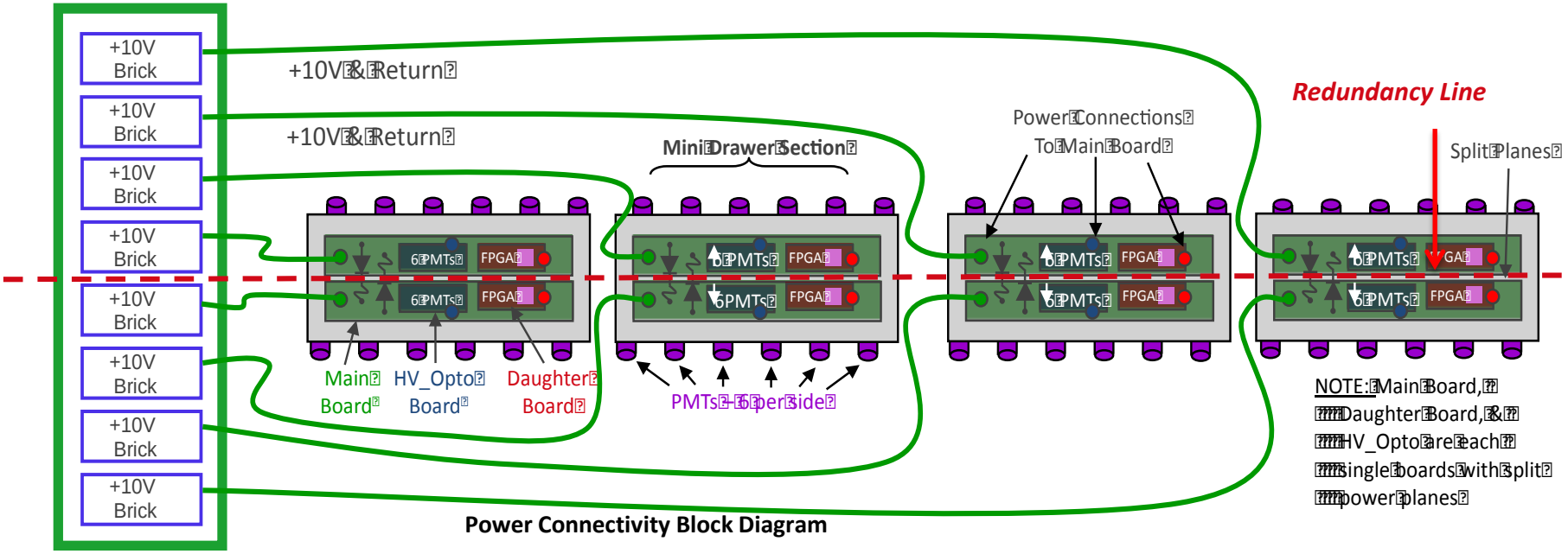
- In the present architecture, the analog signal sent to the ATLAS Level 1 trigger is obtained by the analog sum of pulses coming from different cells
- For the Demonstrator Drawer the analog trigger path should be preserved (as similar as possible to the current system)
- Passive board that should be connected to the Main Boards was designed to carry the adder board



Second prototype of Base Board for Adder Card

Adder Card

Power Distribution



- One of the goals of the ATLAS Tile Calorimeter upgrade is to maximize the redundancy and so minimize the coverage damage in case of failure
- Point-to-point connection from brick to Main Boards

Demonstrator
High Voltage Power Distribution

- A high voltage system is required in TileCal to provide power to the photo-multipliers
- Regulation made by HV Opto (based on current design)
  - Controlled by Daughter Board
  - Communication with the Detector Control System via the sROD
- Status
  - First HV Opto has been produced
    - Radiation testing in March 2014

First prototype of HV_Opto board

CAD Diagram of Mini-Drawer