State of the Art in Microelectronics Miniaturization and Integration

Microelectronics for Particle Detectors

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Overview

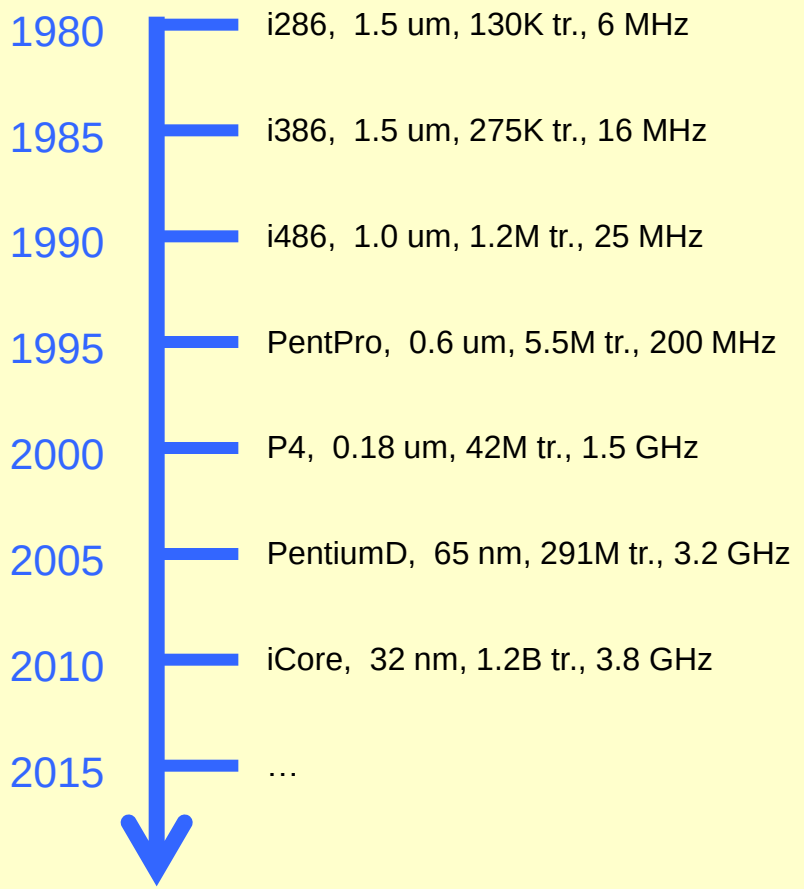
- Motivations: i.e. the talk's message:
  - Experiments require systems, not chips
- Brief intro on technology perspectives
  - History
  - Technologies for SoC
  - Advanced Devices for Billion transistor chips
- Opportunities:
  - SoCs for gas detectors
  - SoCs for trackers
- Conclusions

MOTIVATIONS

- History of μElectronics for HEP vs Commercial
- Areas with potential for growth

Microelectronics in HEP

- 1985 to 1995 - Generation 0 :
  - 2u down to 1.0 u
  - Proofs of concept
  - First dedicated ASICs for strip detectors
    - » Low-noise charge amplifiers
  - First simple digital chips
- 1995 to 2005 – Generation 1:
  - 0.8um down to 130nm
  - Front-end ASICs with analog/digital pipelines
    - » First complex pixel chips
  - Radiation issues (a very hard problem!)
  - First monolithics (MAPS etc.)
- 2005 onwards:
  - 130 nm and below
  - Complex SoC
  - Intelligent detectors
    - » Capable of performing significant local processing
    - » But the brain is in the electronics, sorry…
  - System optimized for (integration) cost
  - High density interconnect
    - » Stacks of chips or hybrid chip-detectors



Intel Processors Timeline

Microelectronics in HEP

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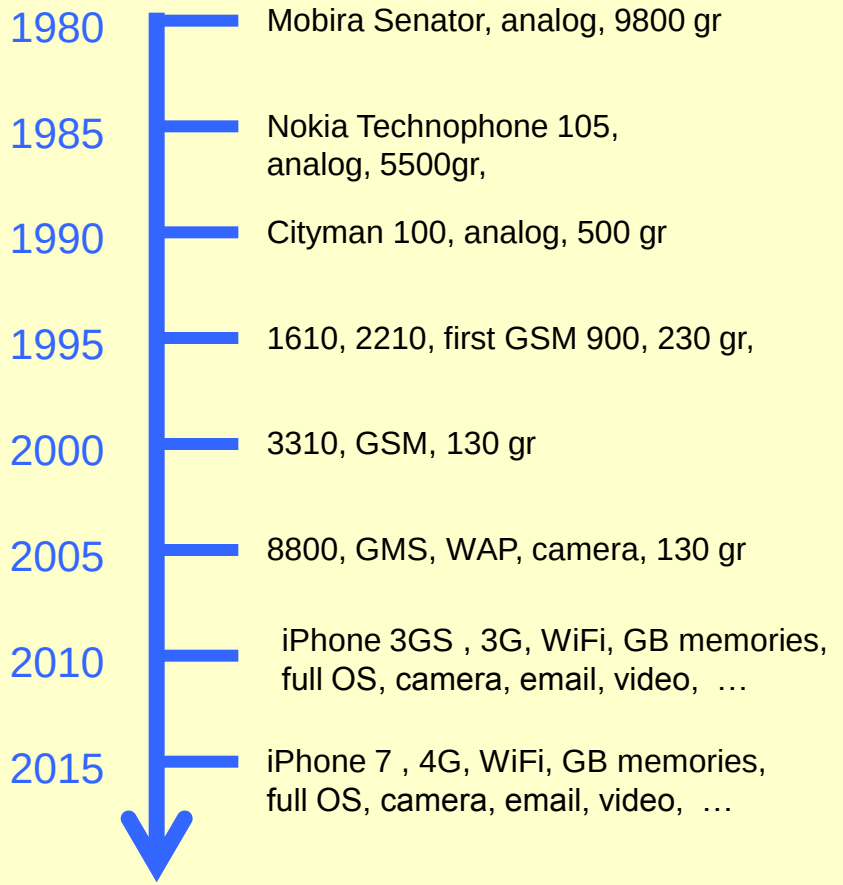
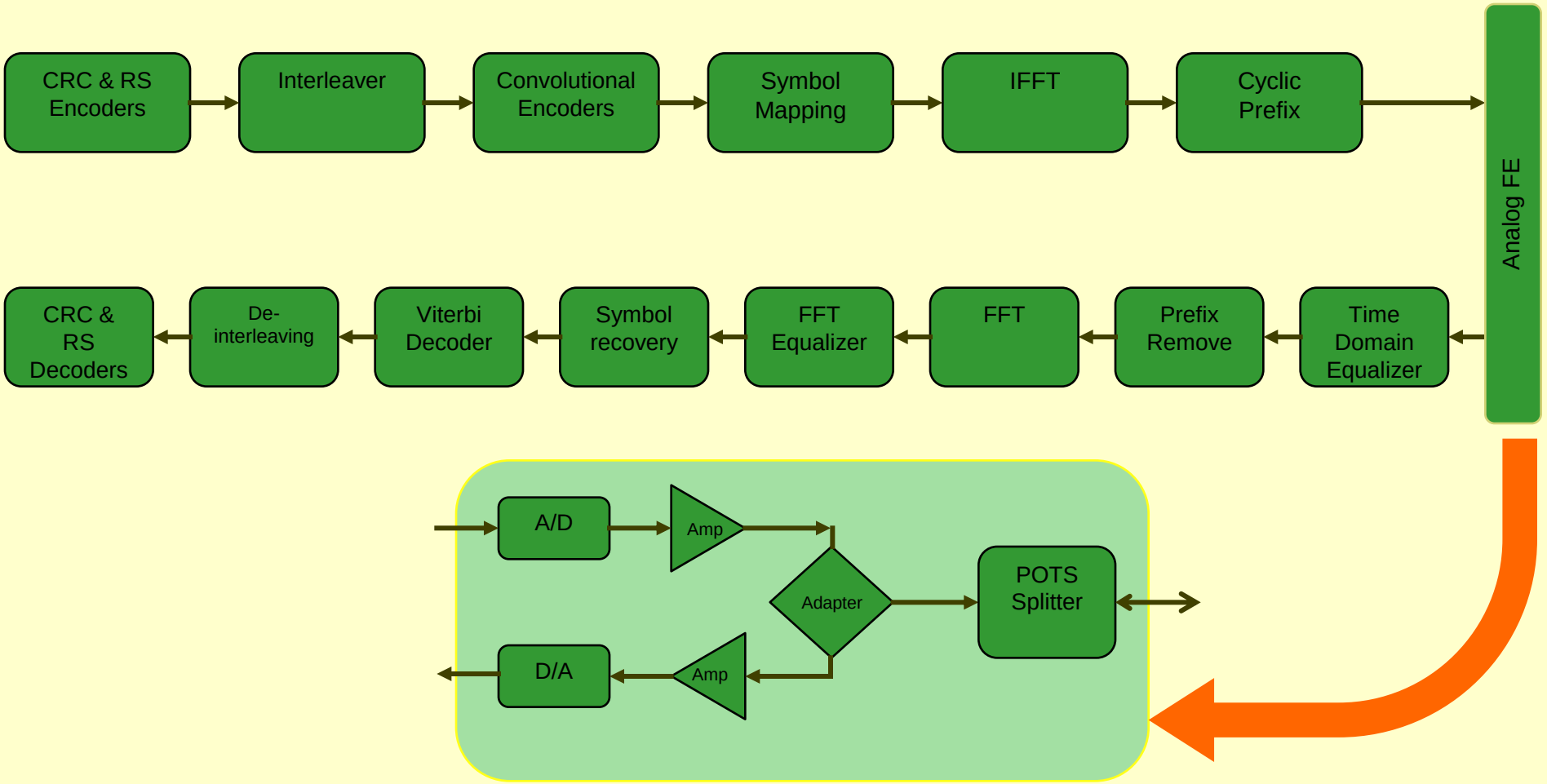


Phones Timeline

System Complexity – ADSL Example



Why do you need microelectronics?

- Functionality
  - Requirements for new (large) detectors can only be fulfilled by Application Specific Ics
    - » Example: no way to buy a ready-made Tracker
- RH
  - No choice other than advanced or modified tech ASICs
  - COTS not easily qualified for usage
- Cost:
  - HEP instrumentation has not made the transition to "commodity" detectors, everything is hand-made, design is for performance and not (really) for cost, systems are not conceived for manufacturability, just for function or/and performance

Potential for improvements

- FE: Low
  - » intrinsic speed or resolution of detectors is not expected to improve dramatically
  - » FE circuits close to intrinsic noise margins
  - » CMOS tech evolution is not going to improve analog (actually probably worse, see later)
  - » Only 3D integration can change the game
- A/D Conversion: Medium to Hih
  - » conversion energy is still being improved, new architectures introduced, digital helps. Caveat: many companies make ADC IPs, do not design ADC, buy them!
- Digital signal processing: High to very high
  - » Little or no "signal processing" is done today in HEP (shaper is analog)
  - » Some laudable attempt in the "Altro" project (pedestal correction, tail cancelation etc.)
  - » Much more to be done
- Data Processing (i.e. Feature Extraction): Huge
  - » Little intelligence in chips: lots of raw (and meaningless!) data shipped out at the cost embedded BW, power and of expensive links
  - » Trigger (i.e. pattern recognition) opportunities
  - » Feature extraction could easily be done now

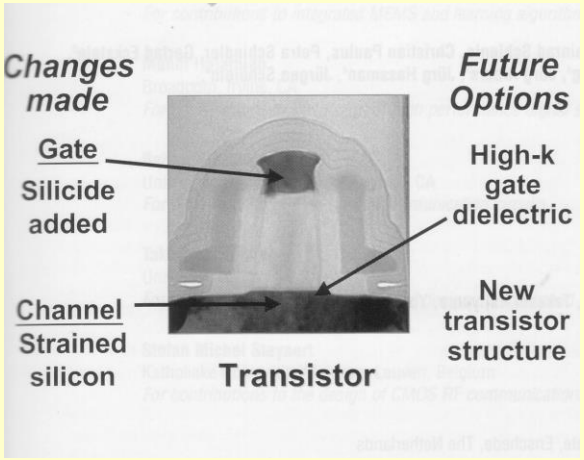
WHAT TO EXPECT FROM ADVANCES IN TECHNOLOGY

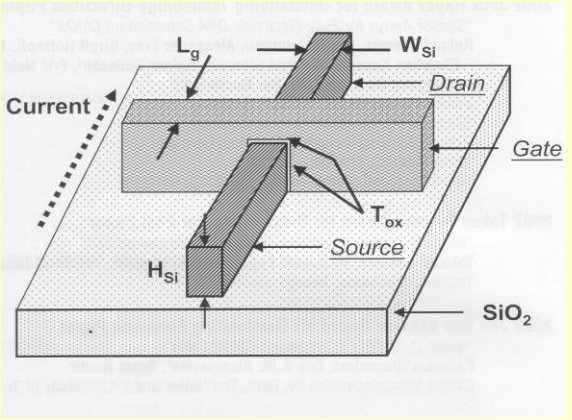
- Advanced CMOS
- A flavor of the problems for making nano-transistors

How many more generations?

- "The end of the planar FET is close, but perhaps one or two generations can be added if newer transistors can be made, for example the 'FINFET' "

G. Moore, 2003





CMOS Technology Roadmap

From ITRS 2011

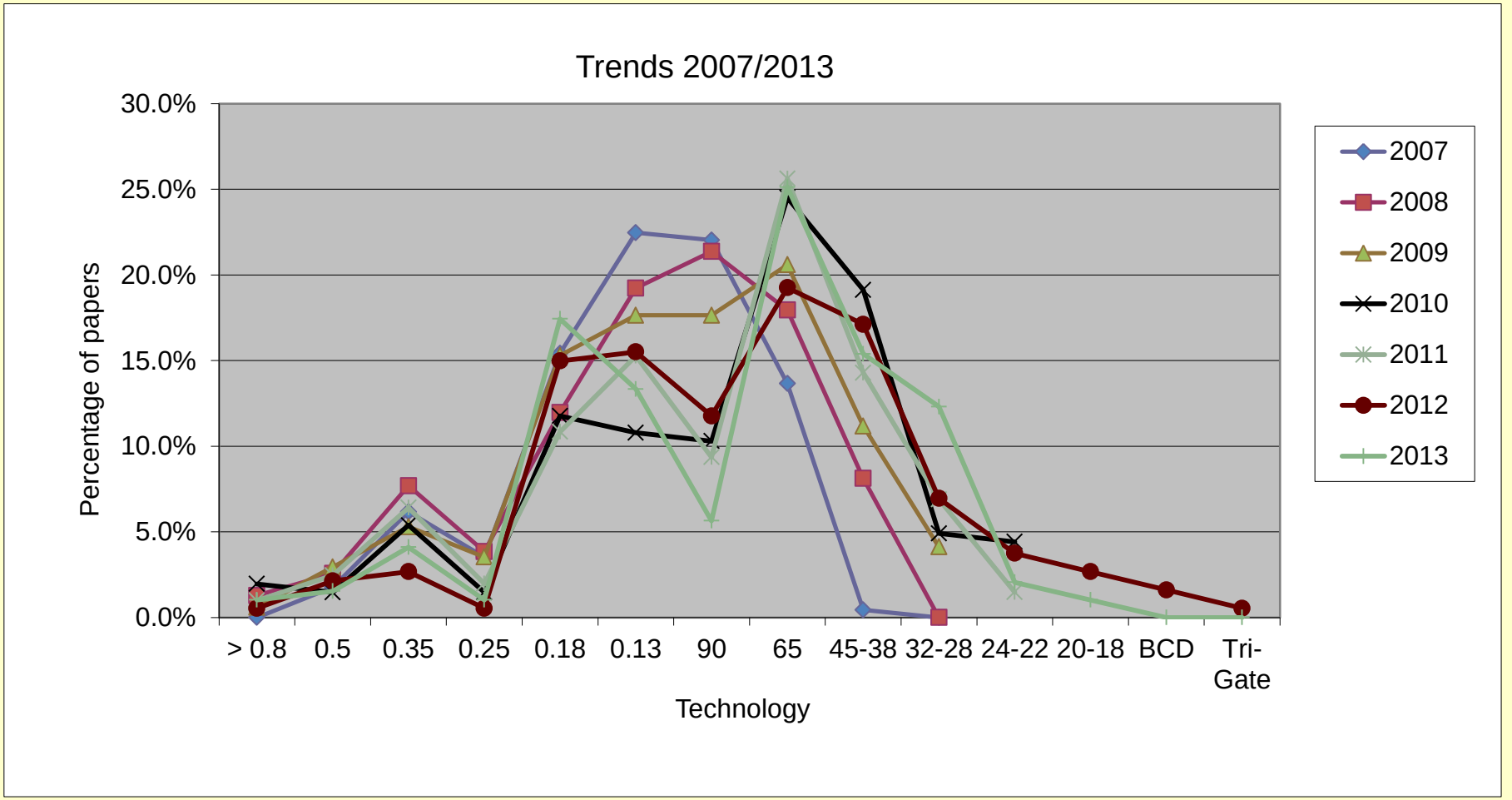
Table B *ITRS Table Structure—Key Lithography-related Characteristics by Product*

Near-term Years

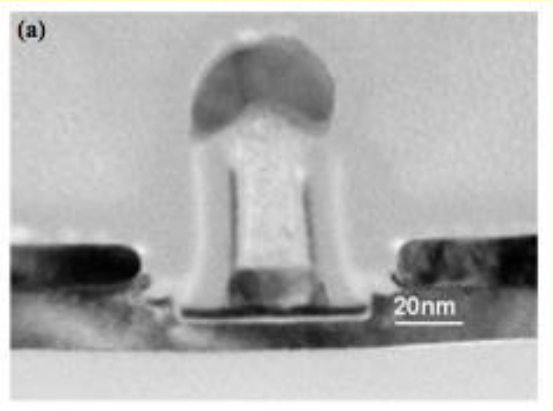
Year of Production	2011	2012	2013	2014	2015	2016	2017	2018
Flash ½ Pitch (nm) (un-contacted Poly)(f)[2]	22	20	18	17	15	14.2	13.0	11.9
DRAM ½ Pitch (nm) (contacted)[1,2]	36	32	28	25	23	20.0	17.9	15.9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)[1,2]	38	32	27	24	21	18.9	16.9	15.0
MPU High-Performance Printed Gate Length (GLpr) (nm) ††[1]	35	31	28	25	22	19.8	17.7	15.7
MPU High-Performance Physical Gate Length (GLph) (nm)[1]	24	22	20	18	17	15.3	14.0	12.8
ASIC/Low Operating Power Printed Gate Length (nm) ††[1]	41	35	31	25	22	19.8	17.7	15.7
ASIC/Low Operating Power Physical Gate Length (nm)[1]	26	24	21	19.4	17.6	16.0	14.5	13.1
ASIC/Low Standby Power Physical Gate Length (nm)[1]	30	27	24	22	20	17.5	15.7	14.1
MPU High-Performance Etch Ratio GLpr/GLph [1]	1.4589	1.4239	1.3898	1.3564	1.3239	1.2921	1.2611	1.2309
MPU Low Operating Power Etch Ratio GLpr/GLph [1]	1.5599	1.4972	1.4706	1.2869	1.2640	1.2416	1.2196	1.1979

There is no doubt that industry ~~will be~~ **is** well ahead of the requirements from the HEP community, including HL-LHC, ILC etc.

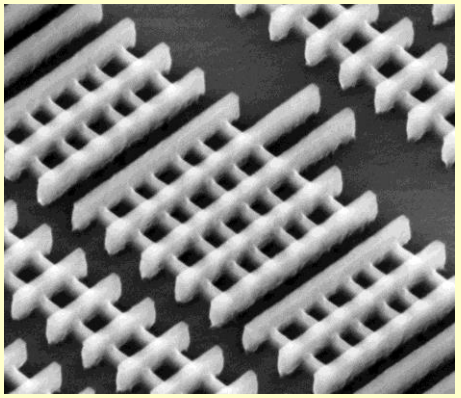
Technologies used in ISSCC papers



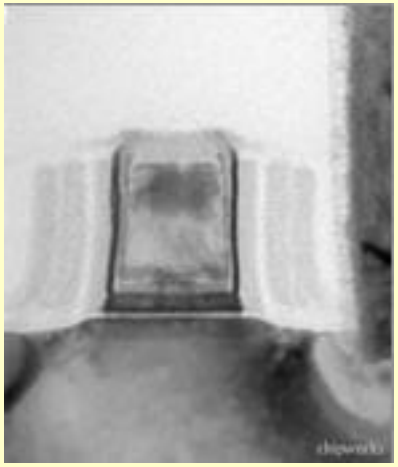
Some advanced devices



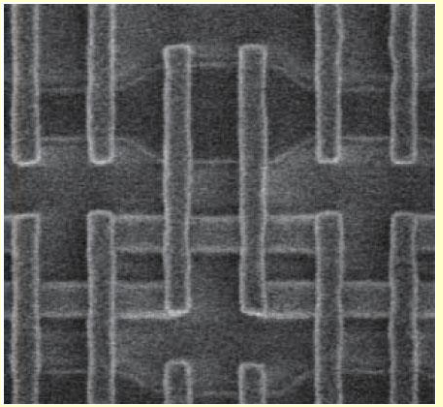
20 nm FDSOI from ST



22 nm TriGate from Intel



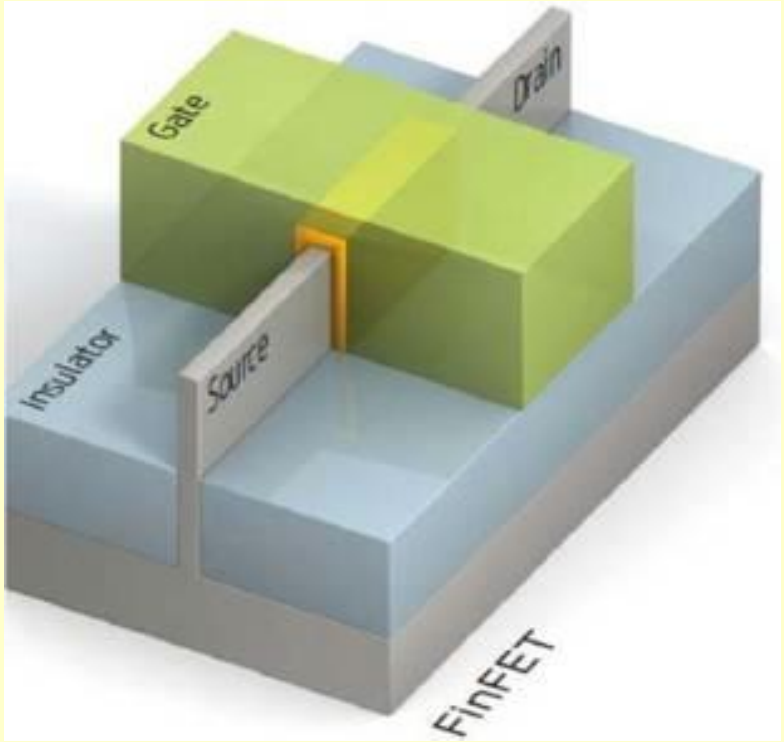
28 nm planar from TSMC



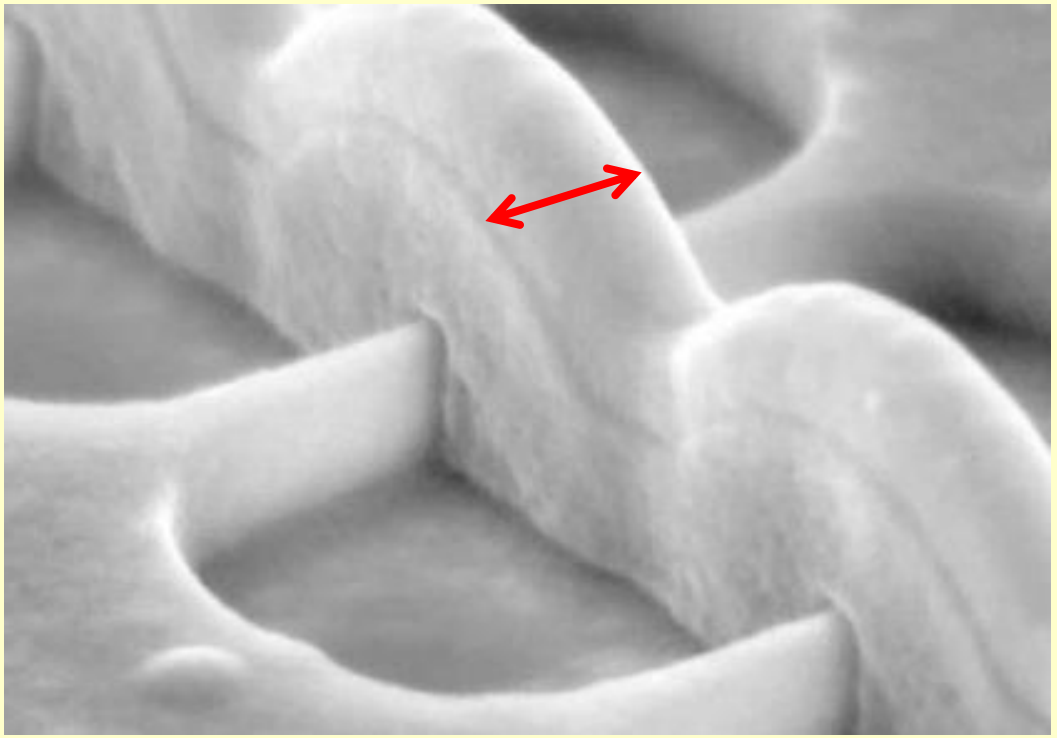
32 nm SOI from IBM

Various sources

16 nm FINFET

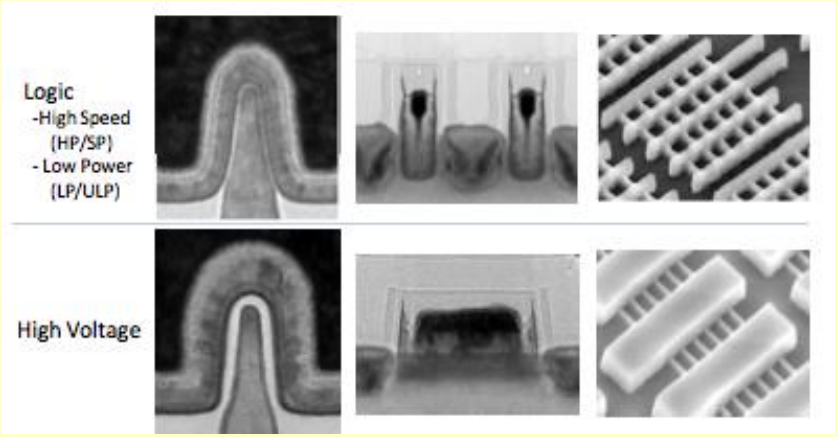


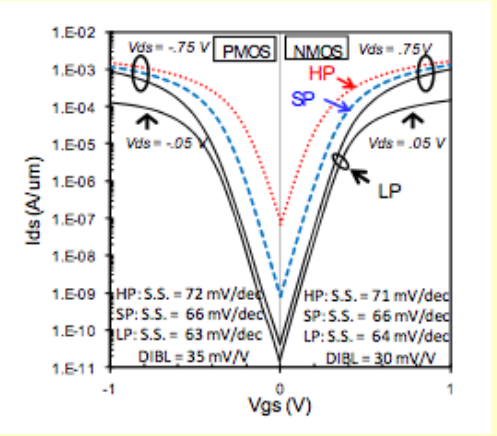
16 nm

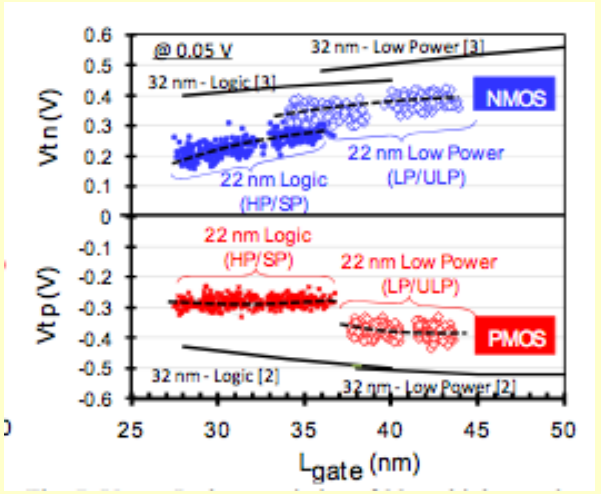


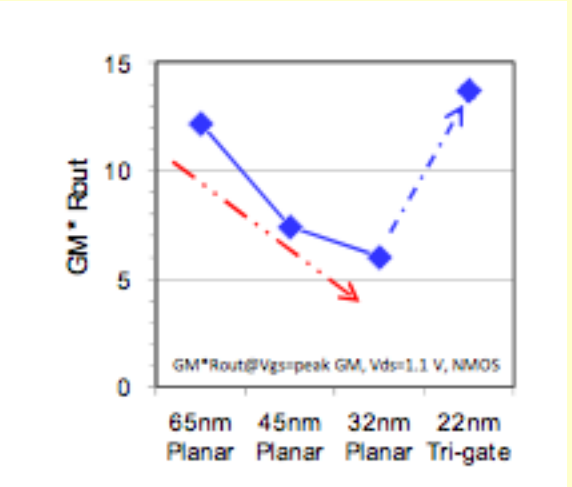
Source: TSMC

… and still, devices behave very well



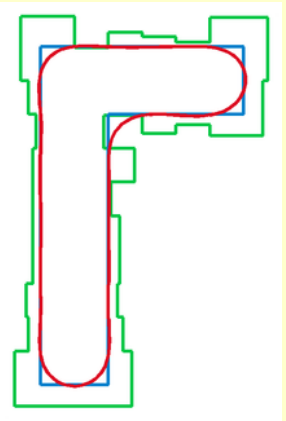


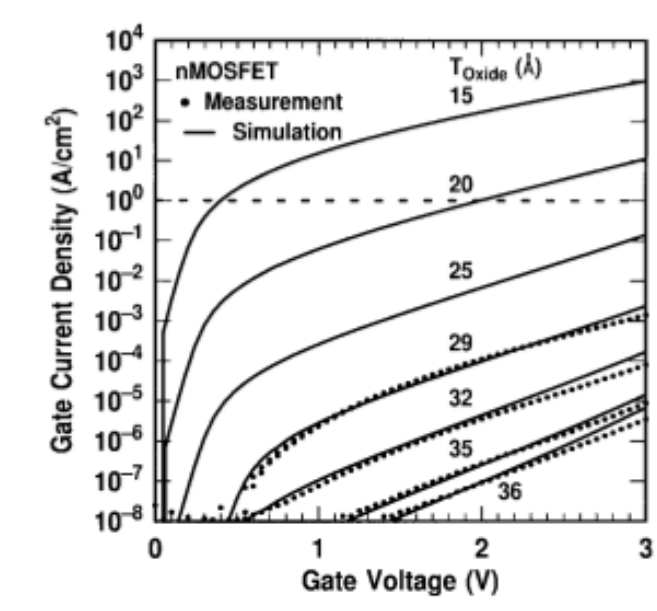




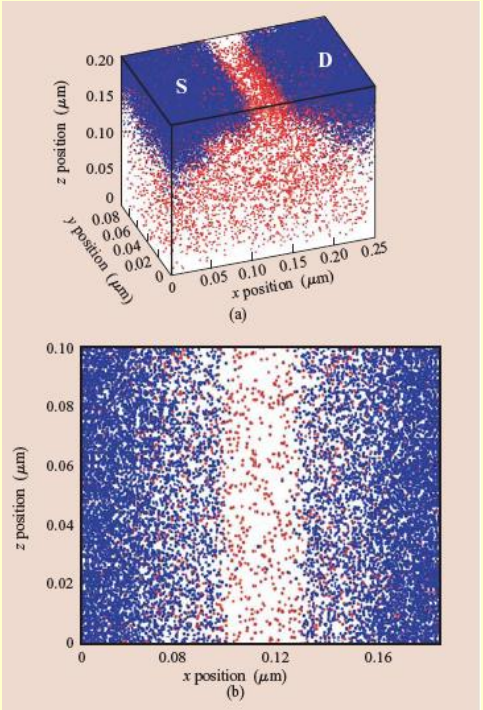
Technology enablers

- Lithography
  - Solution: turn the problem to work to your advantage!
  - OPC
    - » Correct mask and process distortions by synthesizing masks and not by introducing shorter wavelength
  - Double and multiple patterning
    - » Build images by superimposing patterns
- New materials
  - SOI wafers (reduce parasitic capacitances)
  - Si-Ge and channel stress (enhance mobility)
  - Gate oxide materials (need to avoid leakage currents)
  - Metal gates (avoid problem of poly depletion), lower R



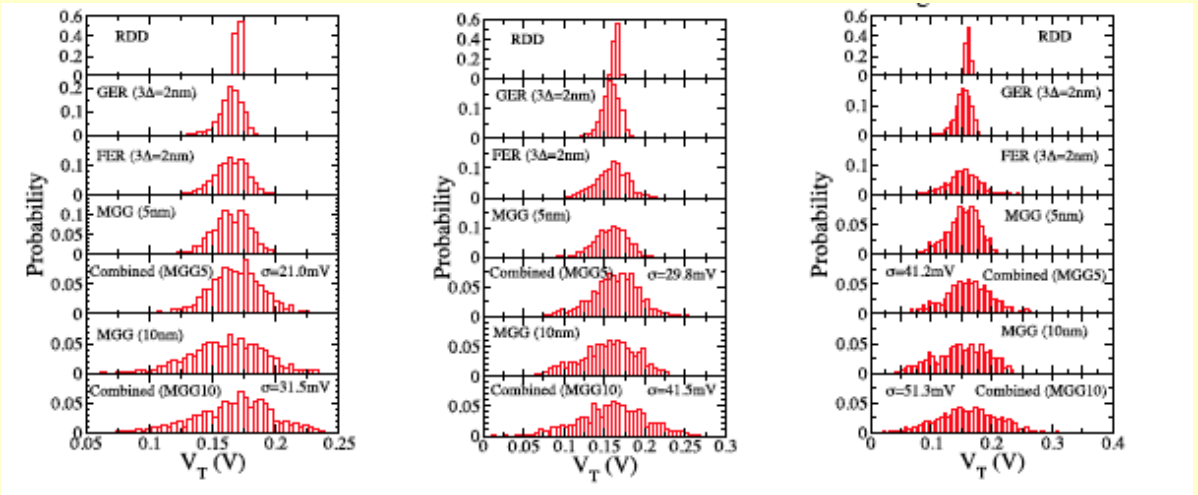


Atomic Scale Variability



Atomistic view of dopants in 50nm transistor

from K. Bernstein et al.,
IBM J. Res. & Dev. Vol. 50 No. 4/5, 2006



Distribution of Vt on three generations of FinFETS, 20nm, 14nm, 10nm

from X. Wang et al.,
IEDM 2011,

Some looming difficulties

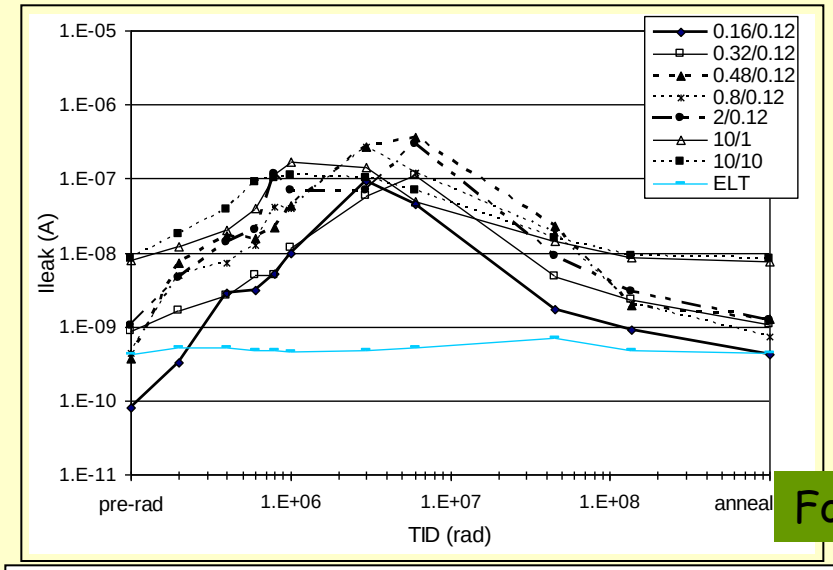
- Device v
  - transis … n
    "count … thick
- Slow lith
  - short … to make
- Cost of
  - Sub-2
- Design c
  - numbe … lly and
    physic
  - variab

IMPORTANT BENEFITS FROM NEW TECHNOLOGIES

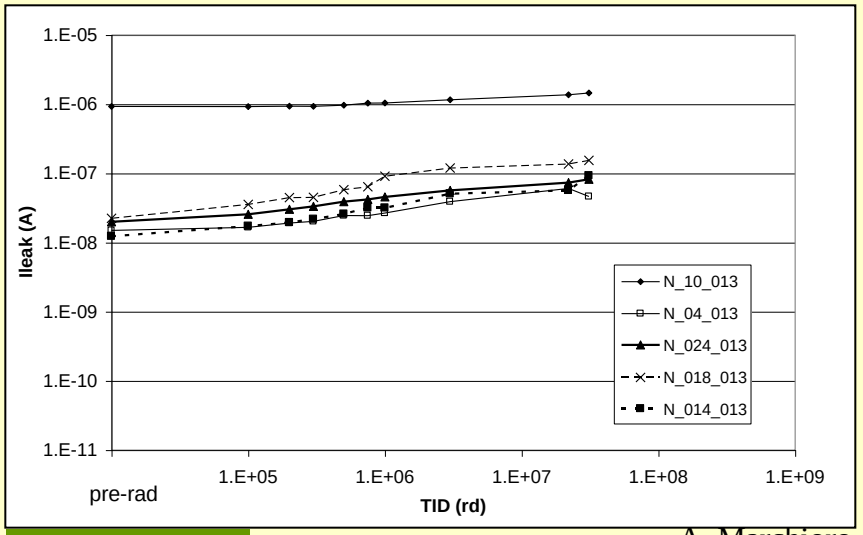
130 and 65 nm and Radiation hardness

Core 130nm NMOS transistors, normal layout

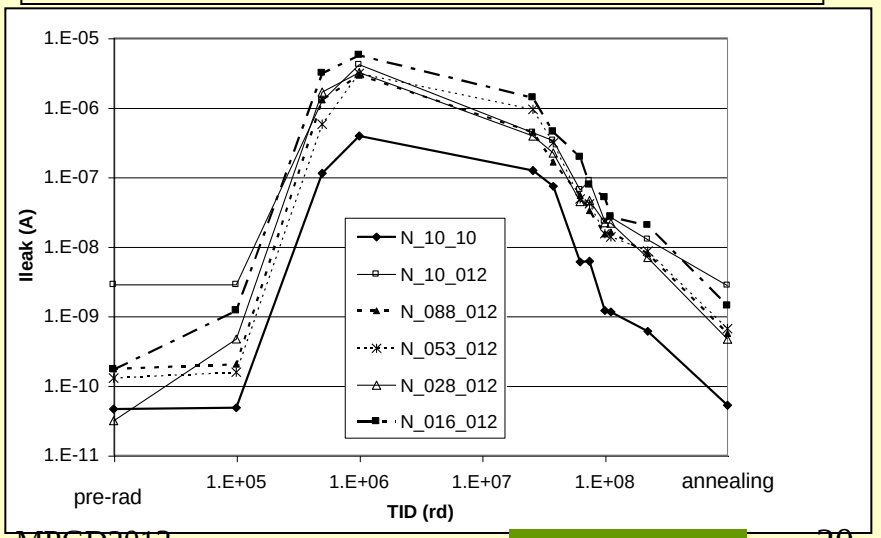
- Effect on the **leakage current**
  - Peak in leakage @ TID of 1-5Mrad
  - Good recovery, strong indications that ELT is not needed for regular digital



Foundry B

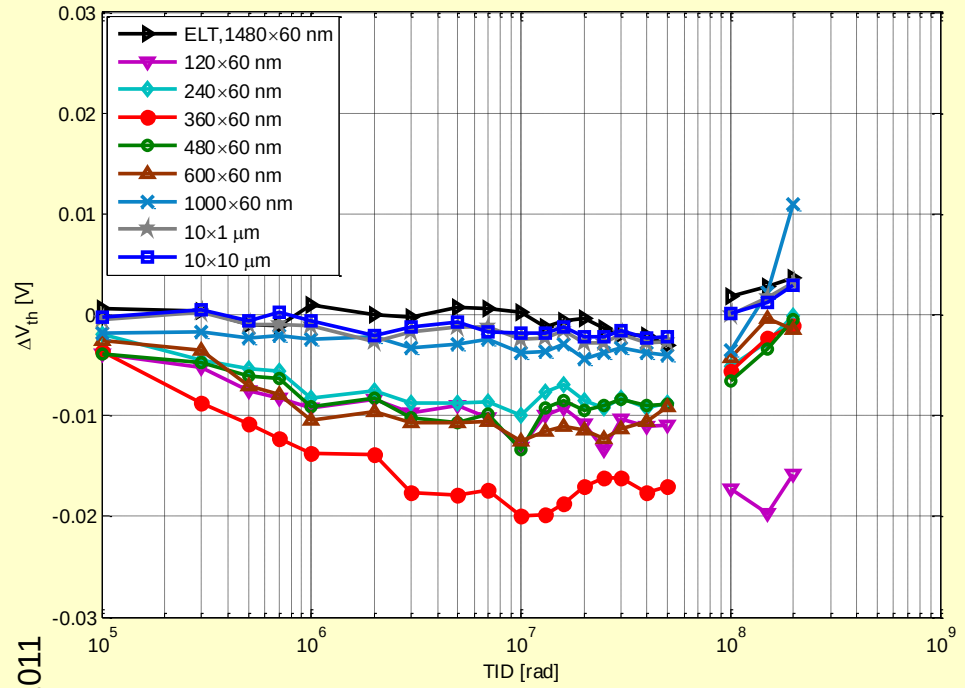


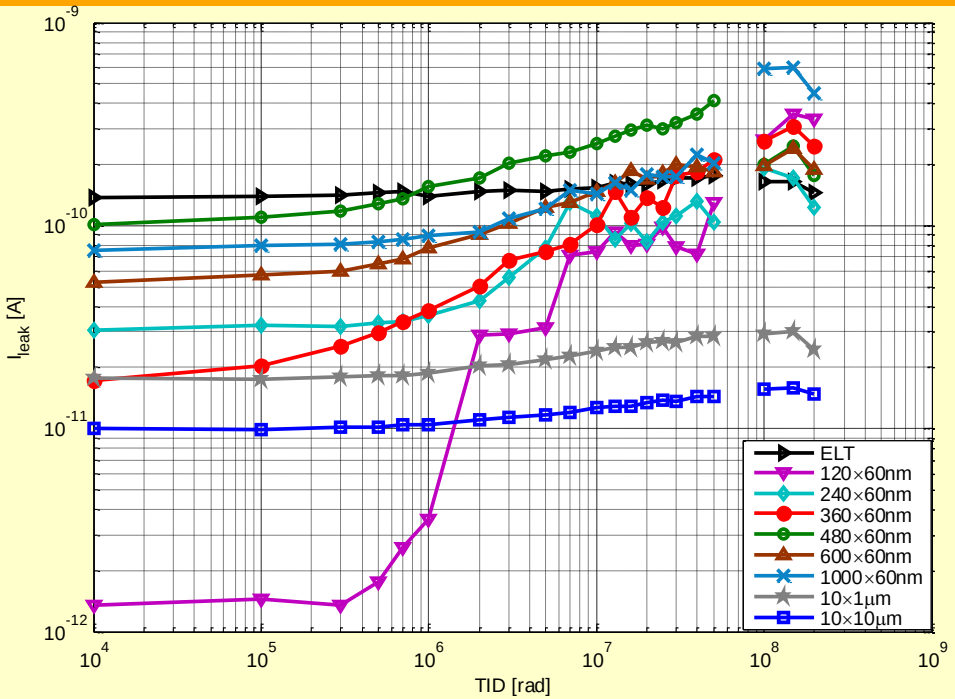
Foundry A



Foundry C

Core devices in 65nm, normal layout





- Up to ~20mV shift for 200 Mrad
  - Some rebound effect visible for narrow devices
  - in 130nm: was 150mV
- At high doses V_{th} shift is positive for wide devices, negative for narrow devices
  - STI edge oxide traps considerable charge (RINCE)
- Subtreshold slope does not change significantly

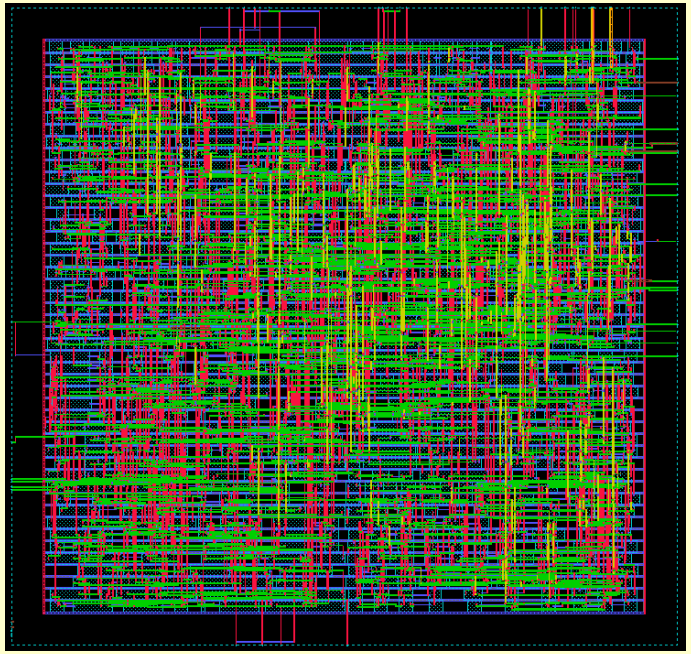
- Less than 10× increase in leakage for wide devices (W > 360nm)
- Narrow devices have up to 2.5 orders of magnitude increase

From S. Bonacini et al, TWEPP 2011

OTHER BENEFITS FROM NEW TECHNOLOGIES

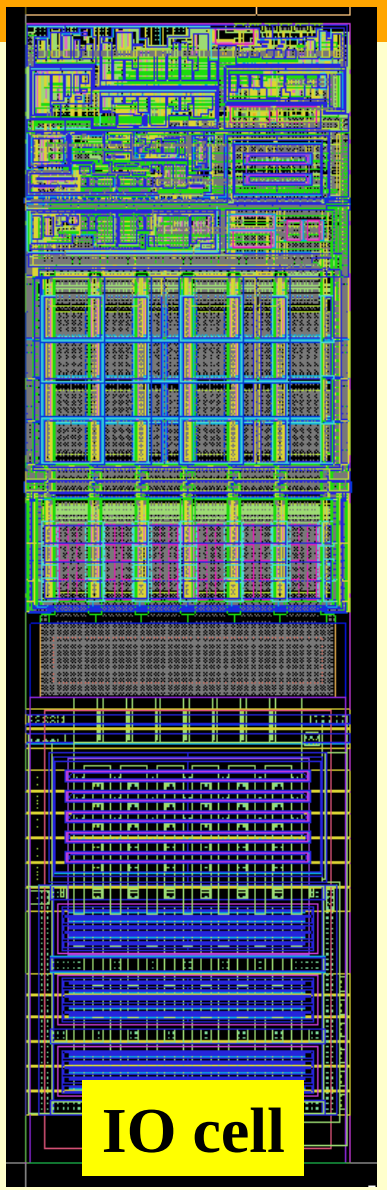
Size, functionality and features

Example of 130 nm density potential



12 bit PIC® compatible microprocessor core

Same scale



Any idea for embedded FE processing?

Facts and Figures

Characteristic	Unit	130nm (G)	90nm (G)	65nm (LP)
Die Area*	sq.mm	0.15	0.07	0.04
Fmax (worst case)	MHz	250	350	400
Dynamic Power**	mW/MHz	0.07	0.02	0.01
Static Power	mW	0.46	0.99	0.02
CPU Power at Fmax**	mW	17.96	7.99	4.02
AA Battery CPU runtime at Fmax	days	2.8	6.3	12.5
		in silicon	**in design**	**projection**

* CPU Die Area excludes Cache RAMs
** Power figures include 8KB I-Cache & D-Cache RAMs

Comparison of ARM® compatible processor from University of Edinburgh, see: http://groups.inf.ed.ac.uk/pasta/hw_encore.html

Interfacing to the “standard” world

- USB 2.0 OTG
  - ~ 20-60K Gates [1]
- Ethernet 10-100-1000 MAC
  - 20,560 gates [2]
- Notice that:
  - 1 mm^2 in 130 nm contains ~ 200K gates
  - 1 mm^2 in 65 nm contains ~ 800K gates
- …and
  - Production cost of 1 mm^2 in 130nm < 0.1 $
  - Production cost of 1 mm^2 in 65 nm < 0.15 $

[1] http://www.faraday-tech.com/techDocument/FOTG200_ProdBrief_v1.2.pdf
[2] http://opencores.org/project,ethernet_tri_mode

Further advantages at 130 nm and below

- More process options useful for detector integration
  - More metal levels:
    - » shielding, power distribution (pixel chips are often accessible on one side only), routability i.e. density
  - More device types
    - » Many optimized V_t MOSFETs, higher capacitor density, inductors, varicap, resistor types, fuses
  - More substrate options
    - » NMOS p-well is almost universally available
    - » substrate isolation for good noise isolation properties

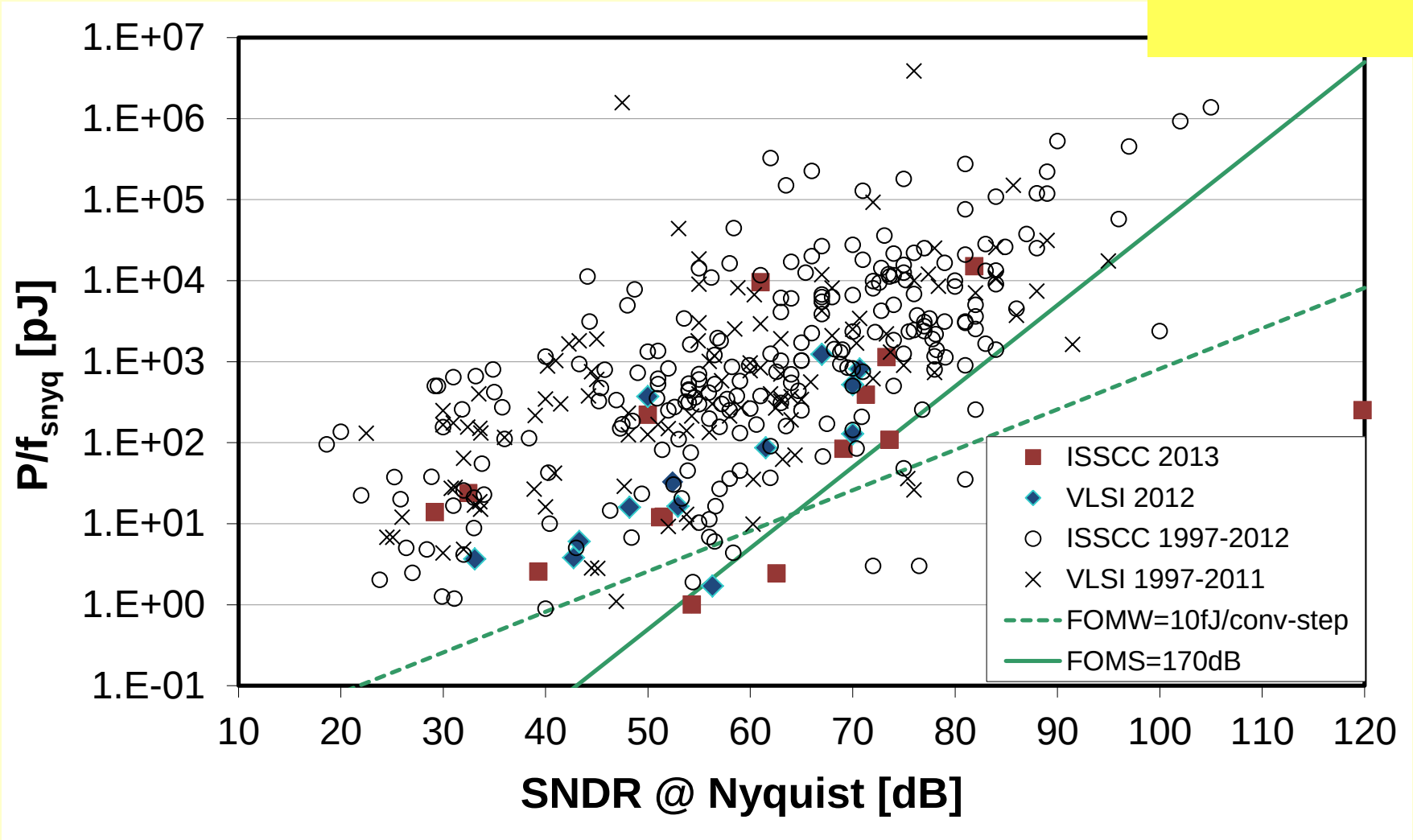
65nm

- Analog features:
  - Device intrinsic gain (= g_m * r_0): worse than 130nm
  - Device max frequency: ~ 2x better than 130nm
  - Matching: better than 130nm
  - Intrinsic noise: about same as 130 nm or slightly better
- Digital features:
  - density:
    - » 4 x 130nm (even with RT devices)
  - speed:
    - » ~ 2x 130 nm (depending on flavor)
  - power:
    - » ½ to ¼ than 130 nm

Advances in ADCs

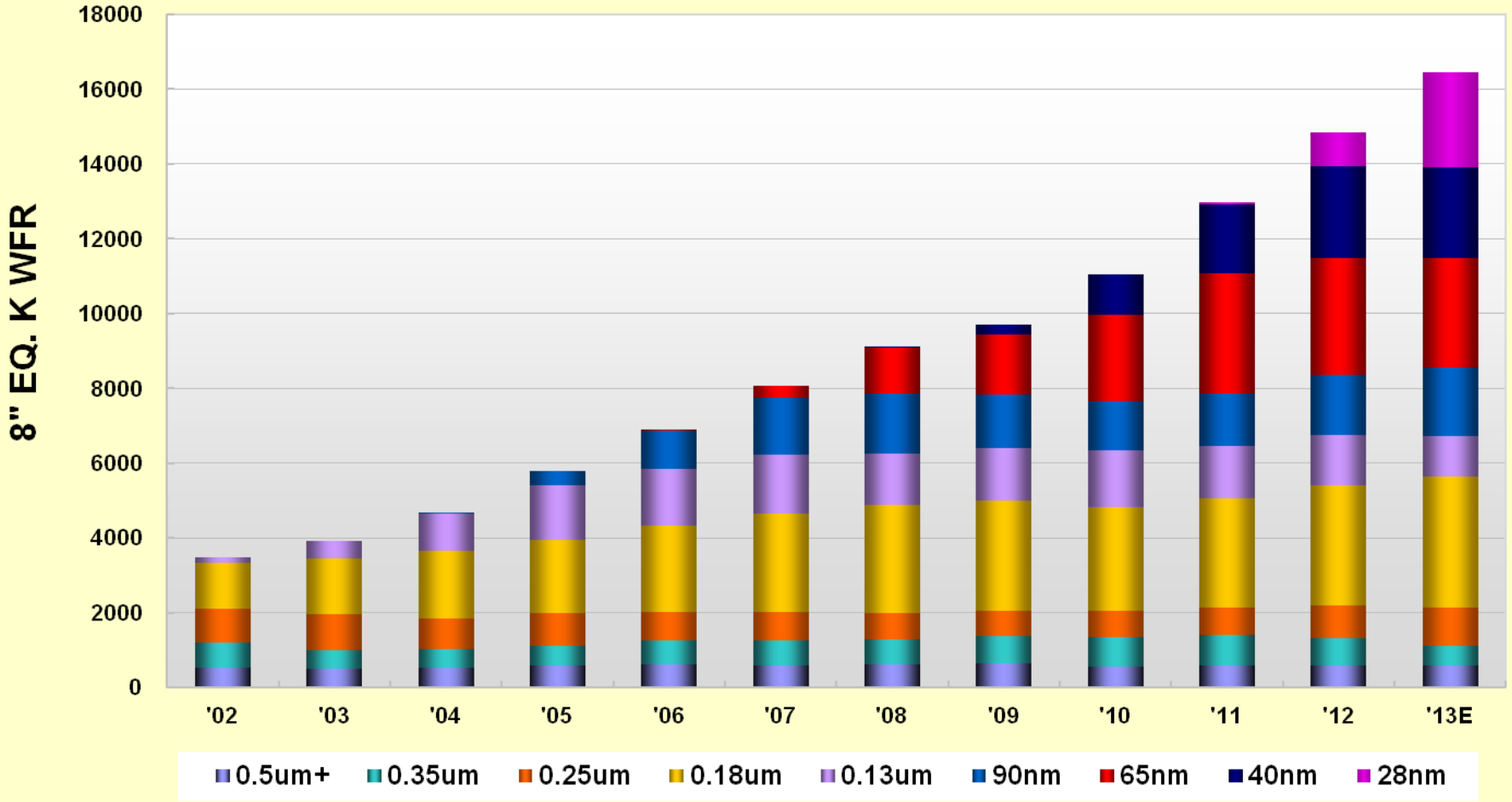
$$FM = \frac{Power}{Freq * 2 \wedge ENOB}$$

$$ENOB = \frac{(SNDR - 1.76)}{6.02}$$



Courtesy of Prof. B. Murmann, Stanford University

Obsolescence?



Source: TSMC financial report

OPPORTUNITIES:

- Chips for gas detectors
- Chips for trackers

Chips for gas detectors

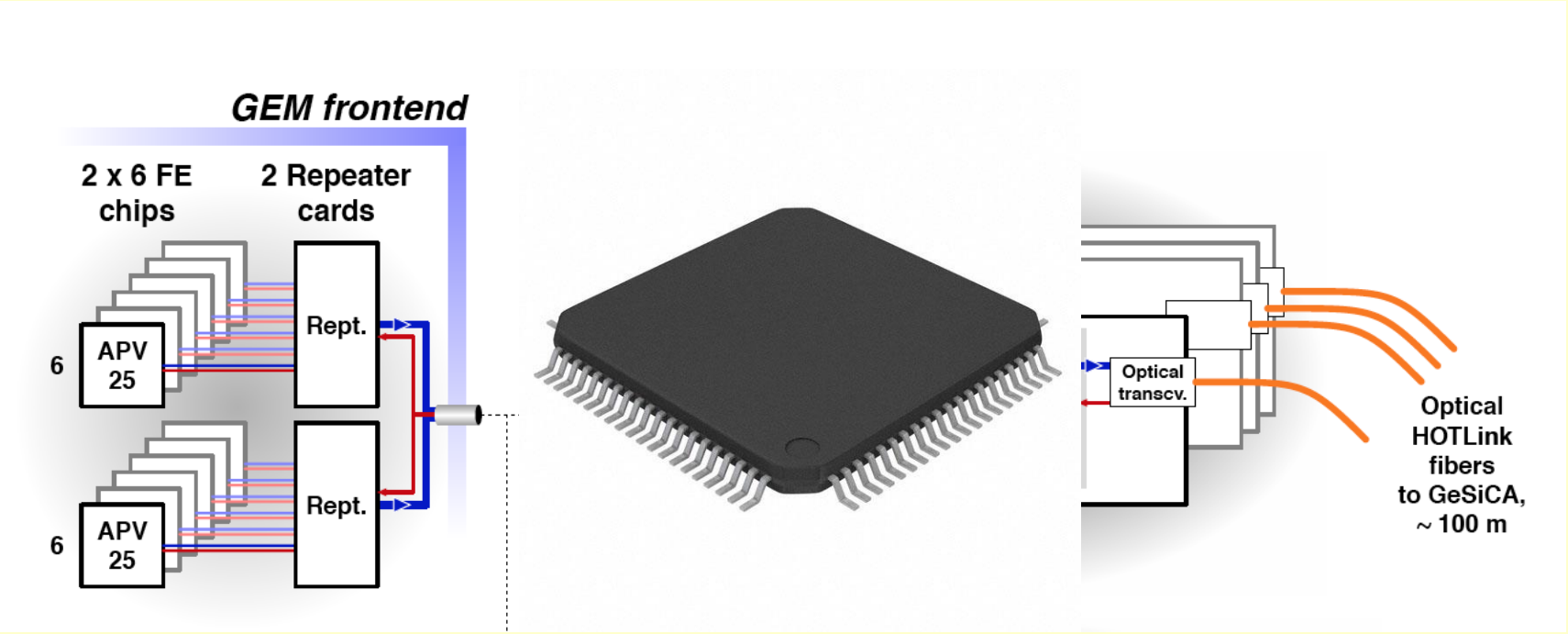


Figure 5.1 in B. Grube's Thesis "The Trigger Control System and the Common GEM and Silicon Readout for the COMPASS Experiment"

First complex chip: the “Altro”

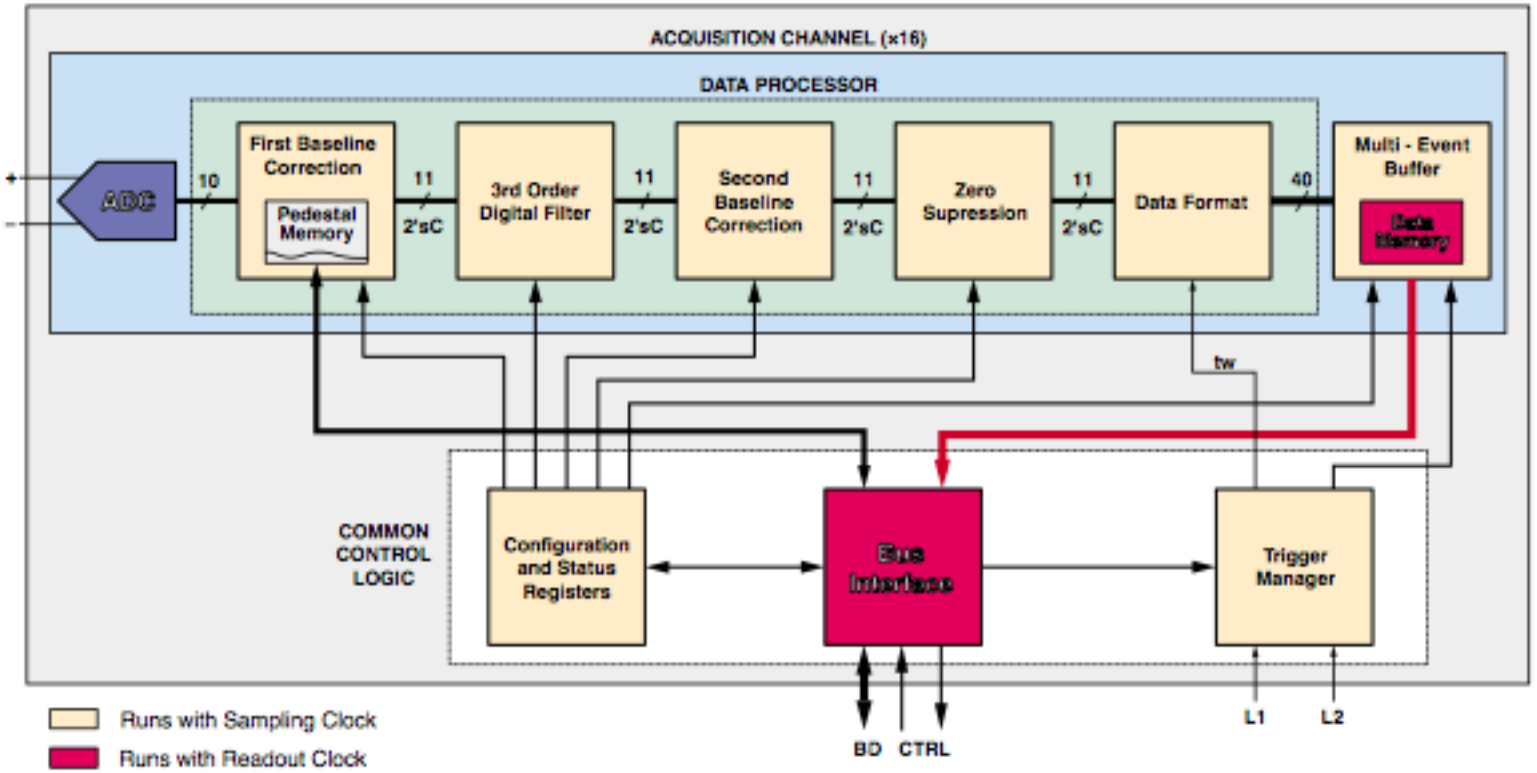
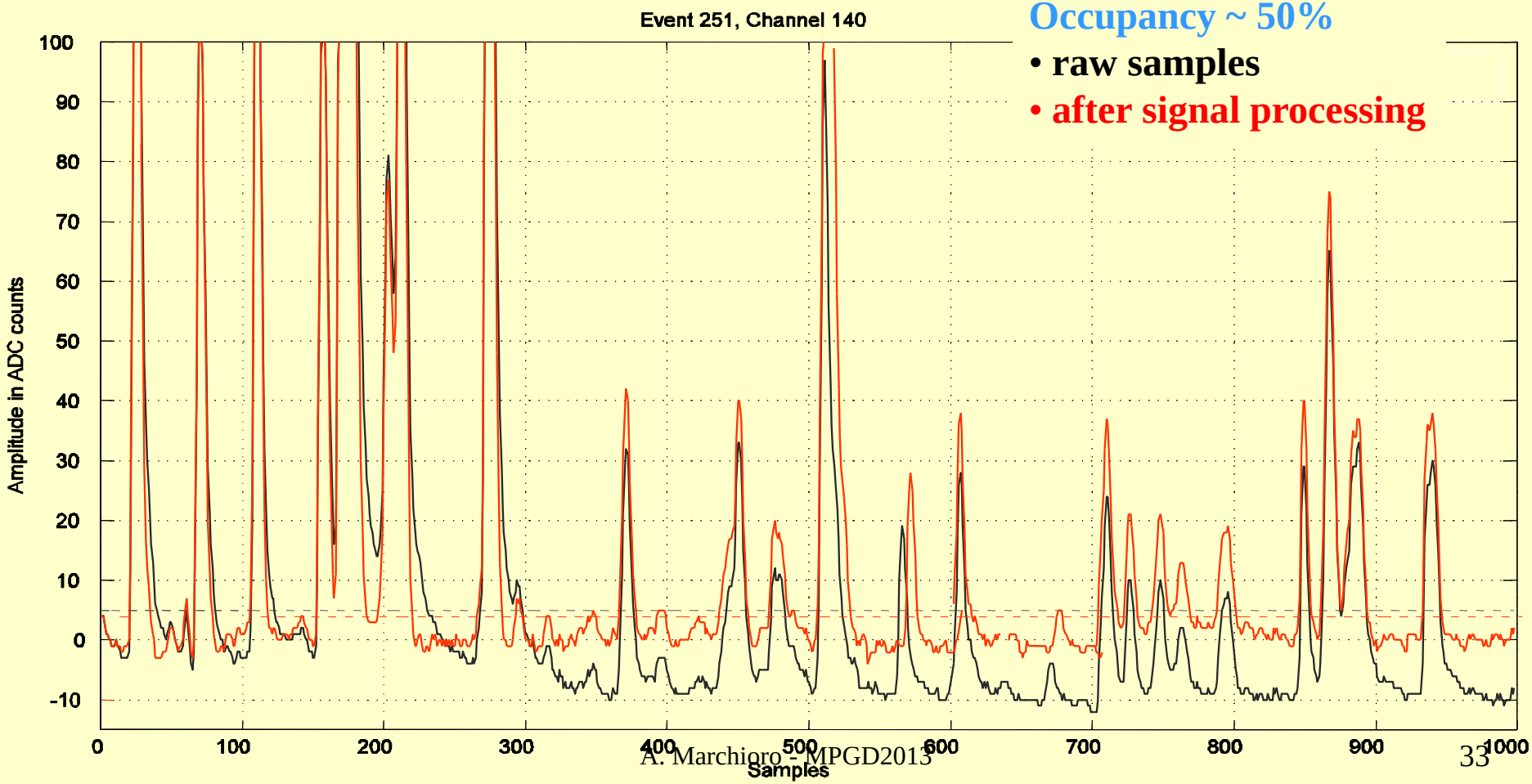


Figure 1.1. ALTRO Processing Chain

Source L. Musa, CERN-PH

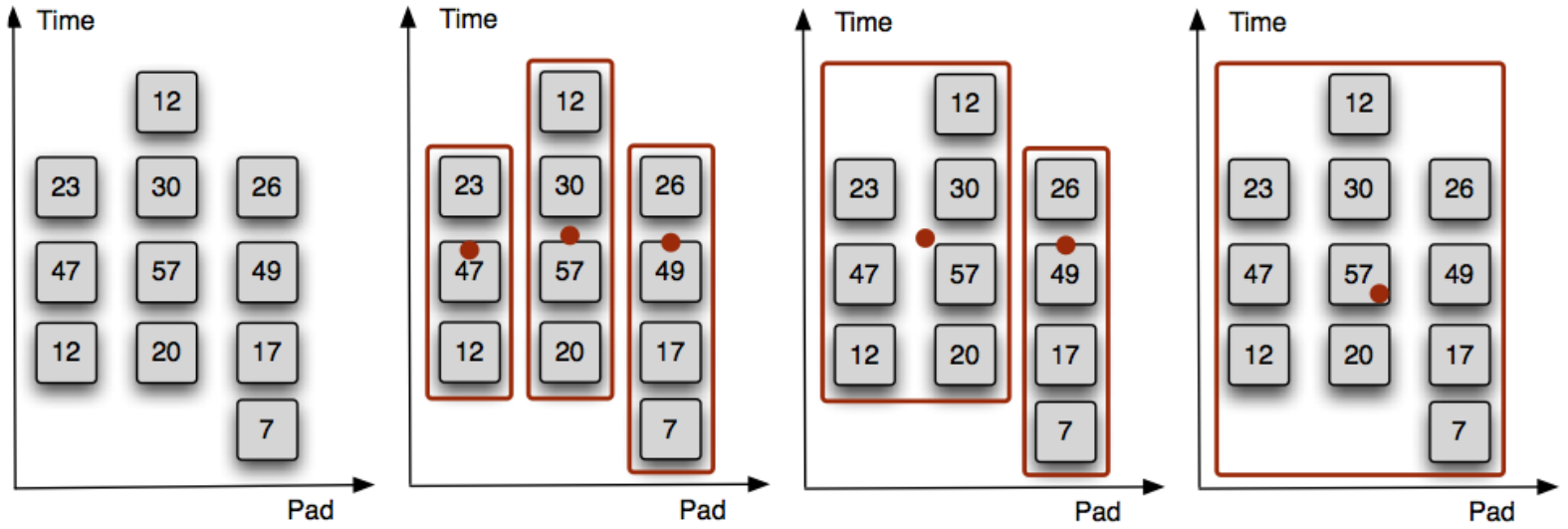
Signal Processing in Altro

HIGH MULTIPLICITY COSMIC RAYS



More cluster signal processing

- Induced charge is spread over several pads in order to increase the spatial resolution
  => To get the exact position the Center of Gravity of the charge cloud is calculated



1. channel extractor
- raw data decoding
- time information
- channel information
- charge sequence

2. channel processor
- processes one pad at a time
- applies gain correction
- calculates the CoGs for the charge sequences in time direction

3. channel merger
- compare neighbouring pads
- merge sequences
- deconvolution in pad direction

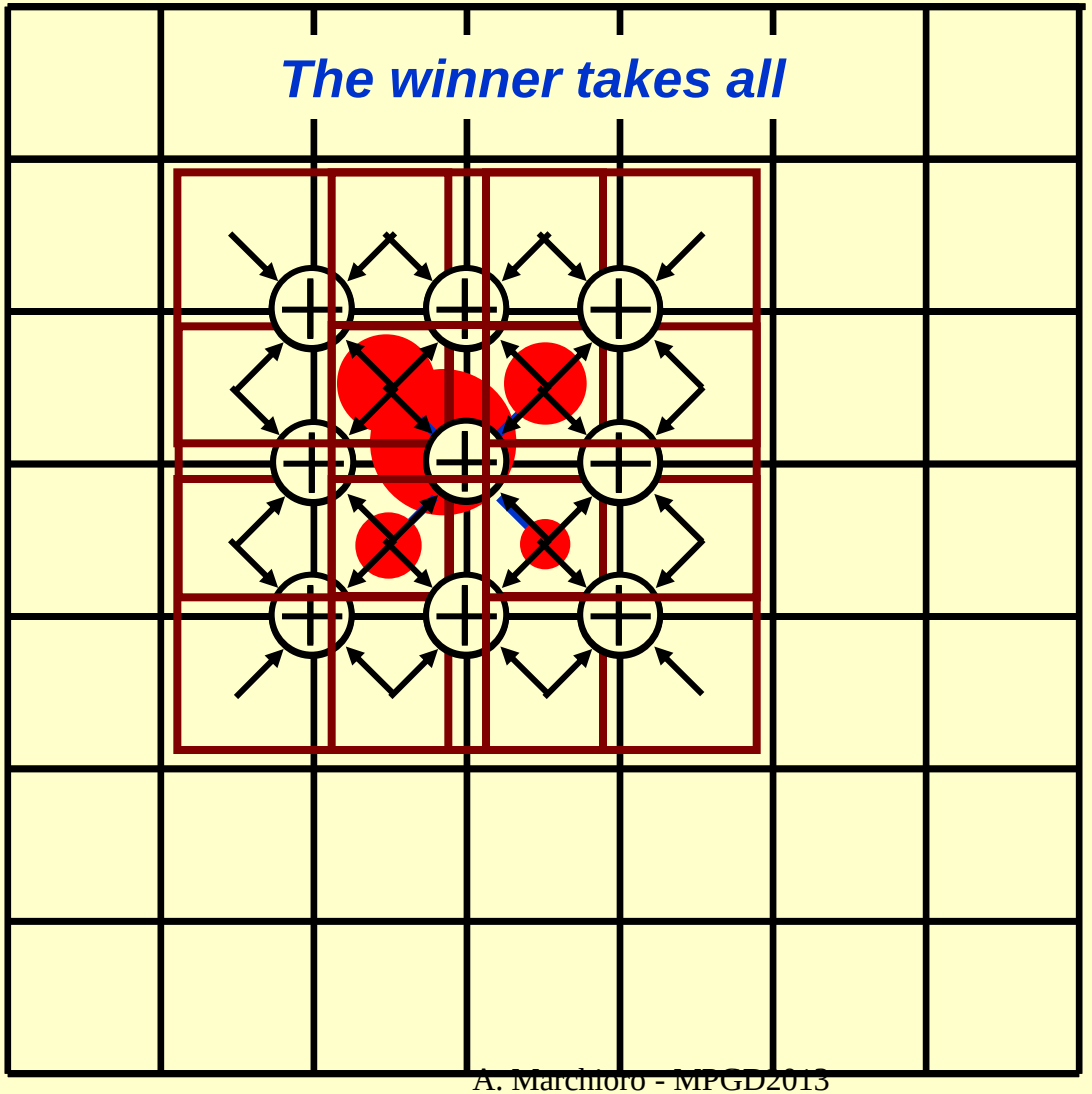
4. division unit
- calculate the position of the cluster and convert the results to a 32bit float

Source T. Alt, L. Musa, CERN-PH

“Image” processing on chip

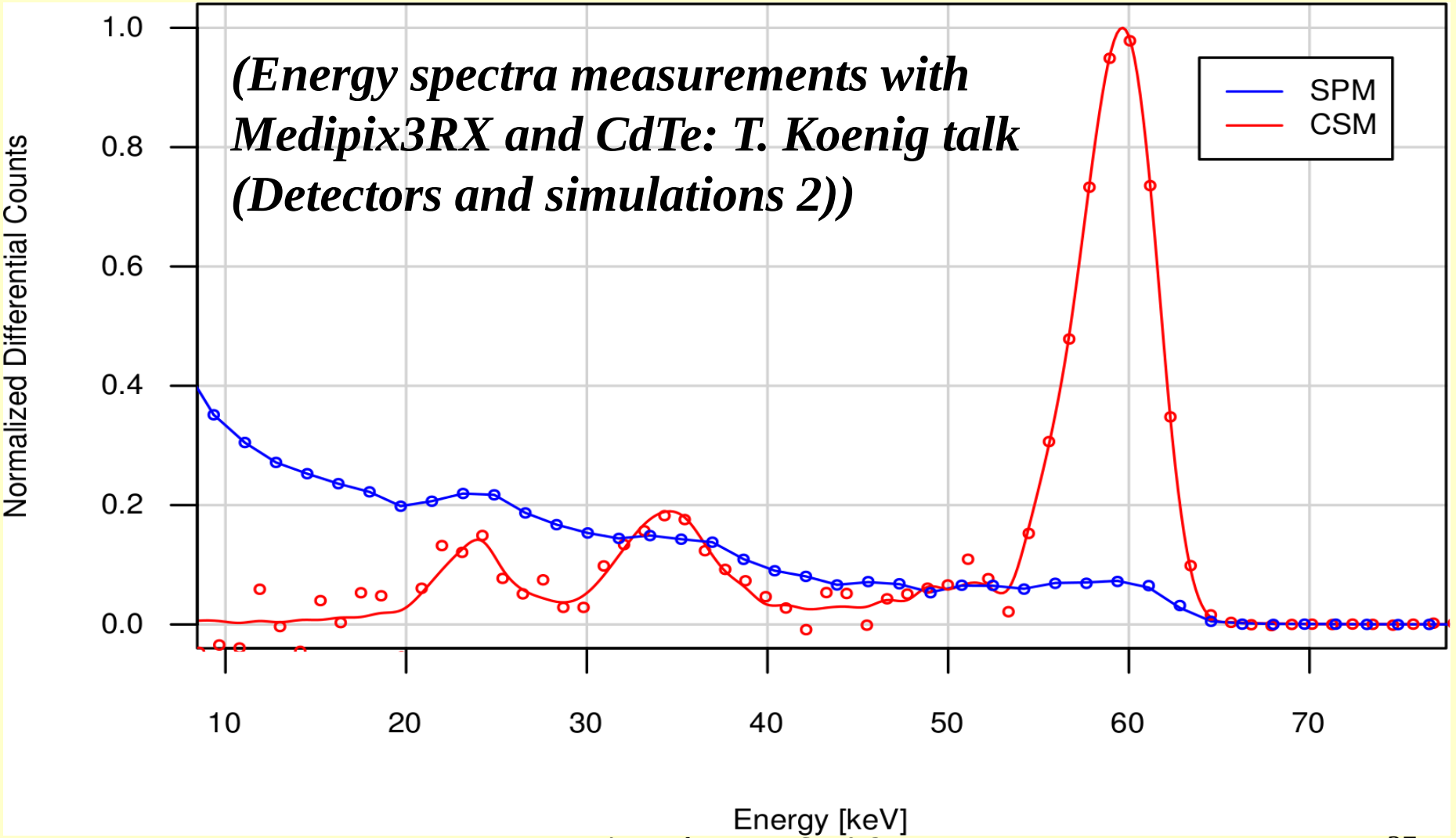
- “Image” processing well possible with current technologies
  - Cluster reduction on FE chips
  - Intelligent “zero suppression”
    - » Always collect “halos” around channels above threshold
  - Charge summing for adjacent pixels
    - » See Medipix3 approach!

Charge summing in Medipix3

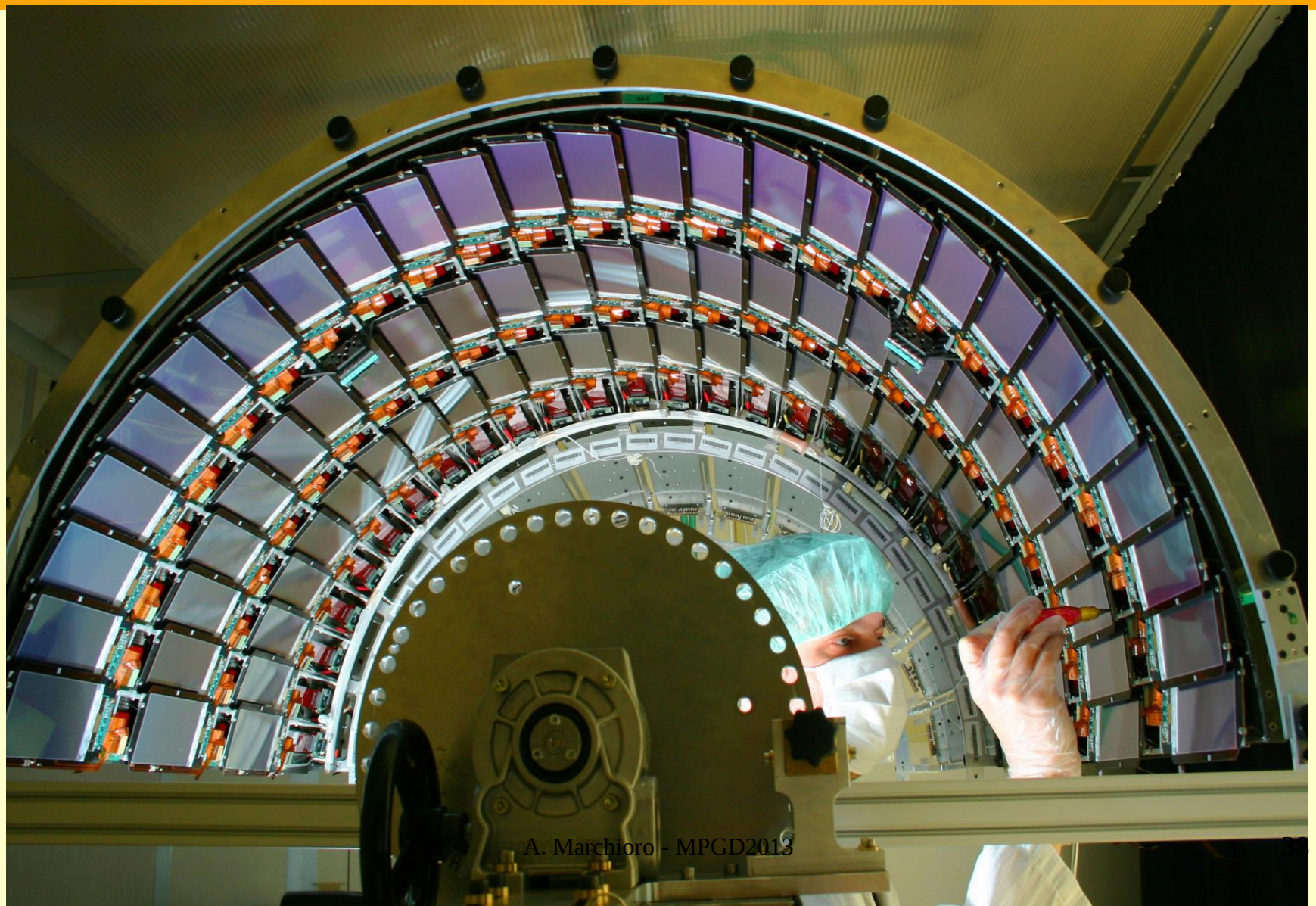


- Charge is summed in every 4 pixel cluster on an event-by-event basis
- Full charge is assigned to single hit

Measurements (60keV, 110μm pitch, 2mm CdTe)

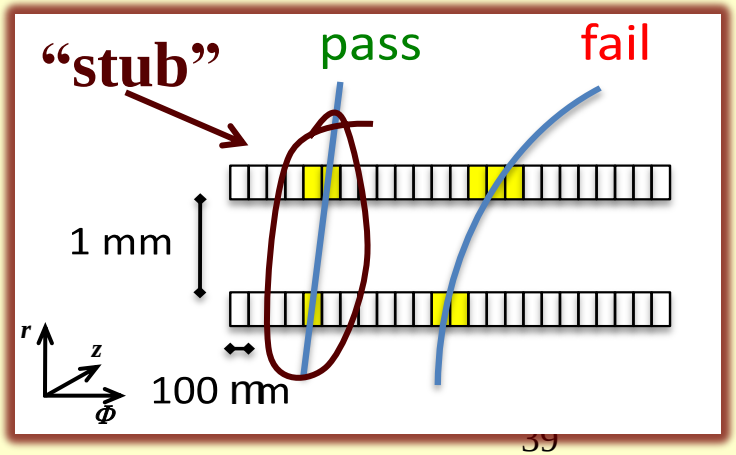


Chips for Trackers

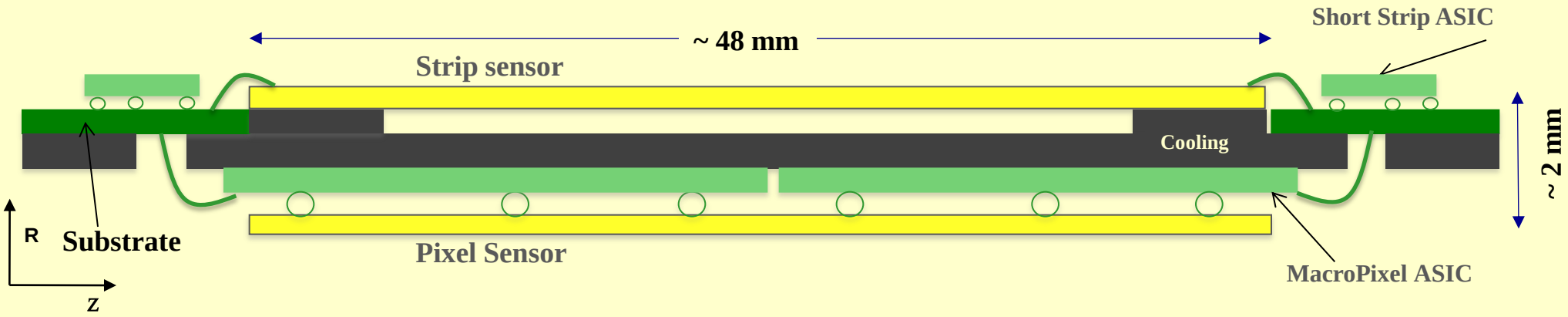


Local feature extraction for trackers

- Level-1 data require local rejection of low-p_T tracks
  - To reduce the data volume, and simplify track finding @ Level-1
    - » Threshold of ~ 1÷2 GeV ®data reduction of about one order of magnitude
- Design modules with p_T discrimination ("p_T modules")
  - Correlate signals in two closely-spaced sensors
    - » Exploit the strong magnetic field of CMS
- Level-1 "stubs" are processed in the back-end
  - Form Level-1 tracks, p_T > 2÷2.5 GeV
    - » To be used to improve different trigger channels

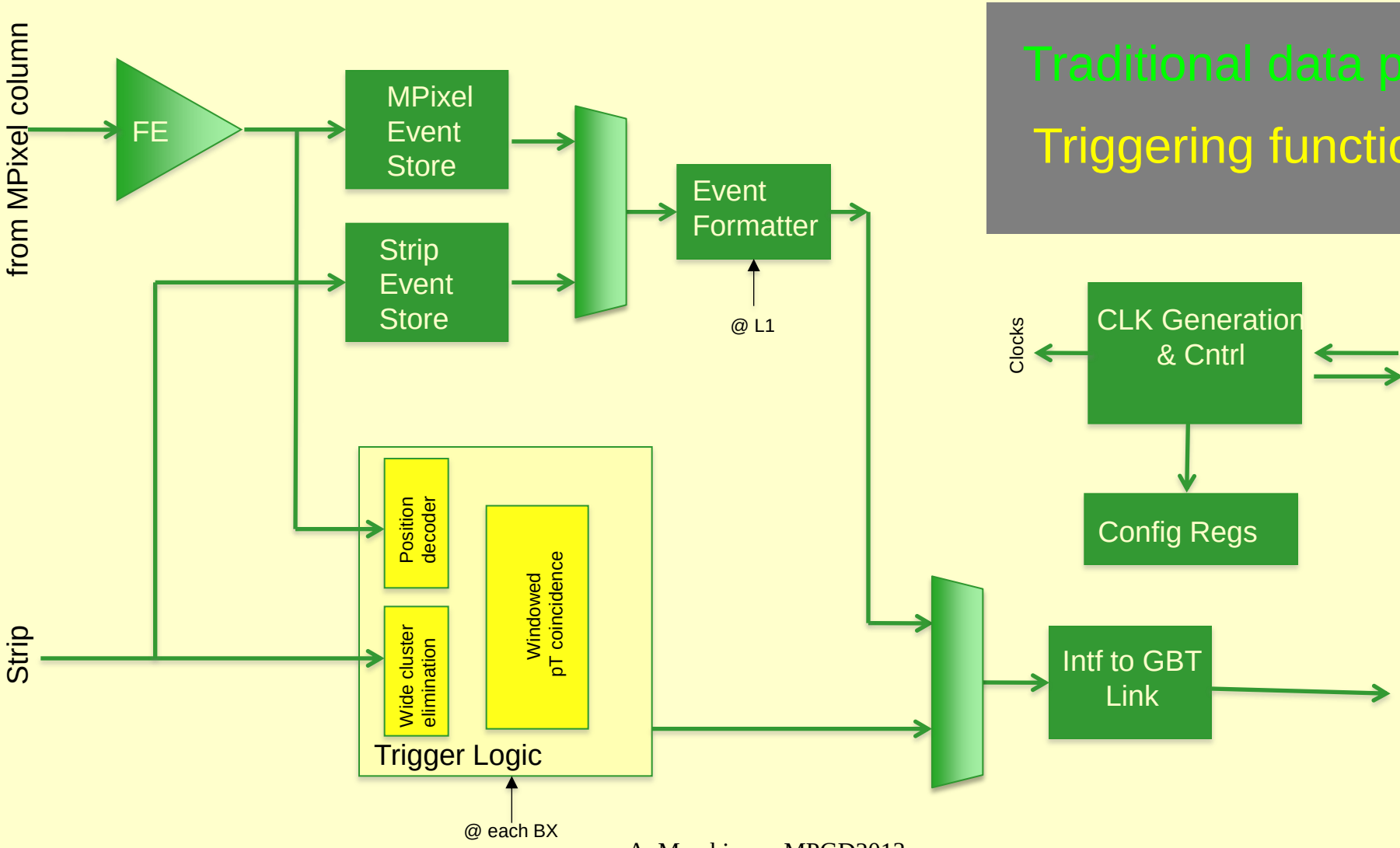


Simplified cross-section

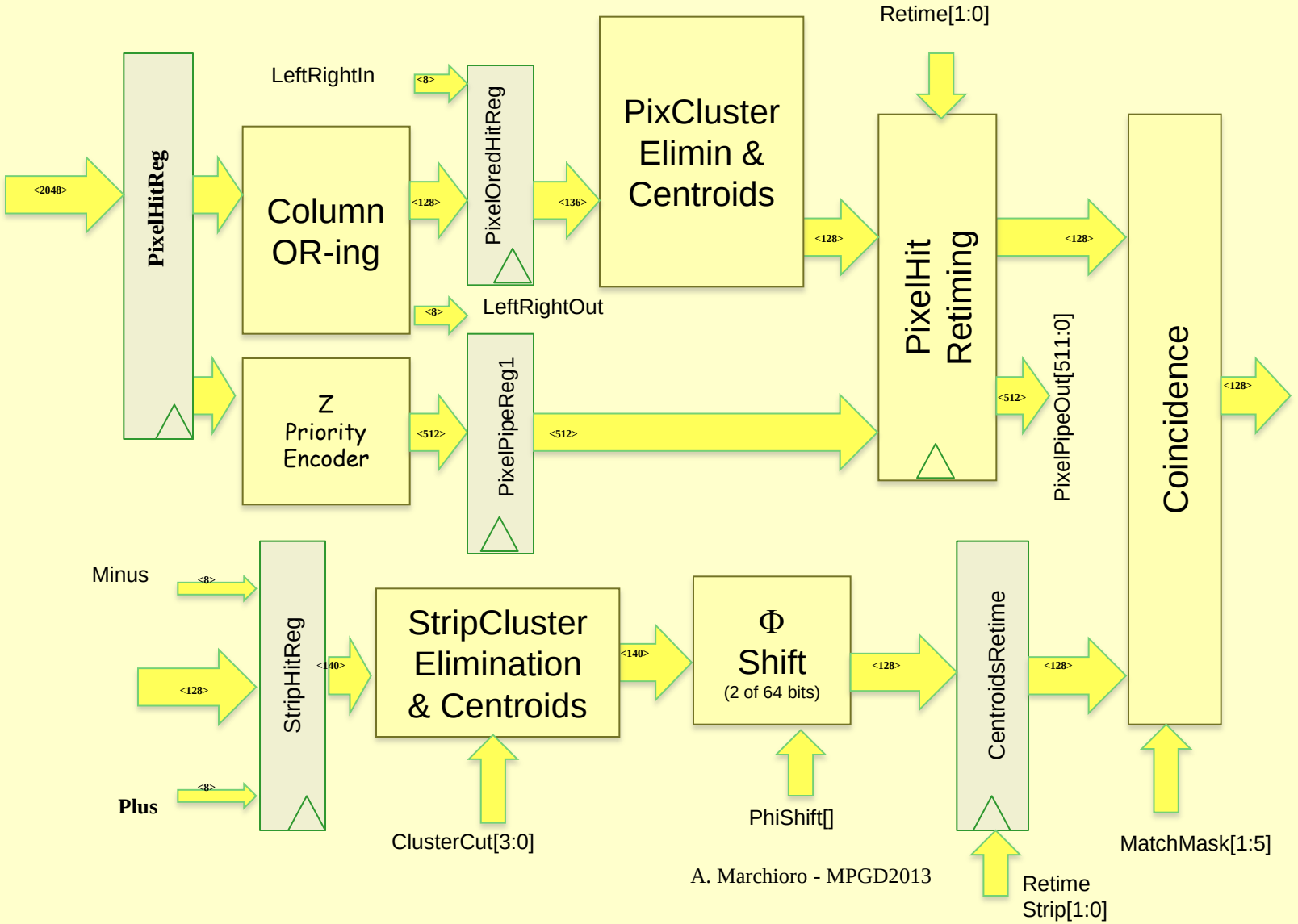


- One layer of strips + One layer of Strixels
  - r-Φ resolution: 100 μm
  - Z resolution: 1.5 mm

MPixel ASIC dataflow



MPA: Trigger (stub) generation

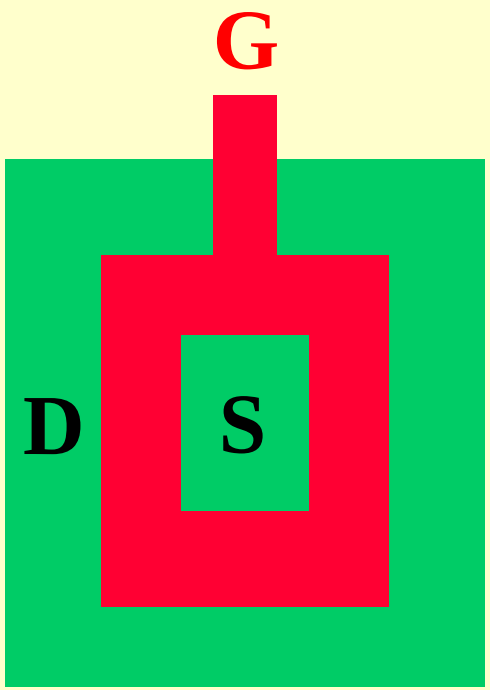


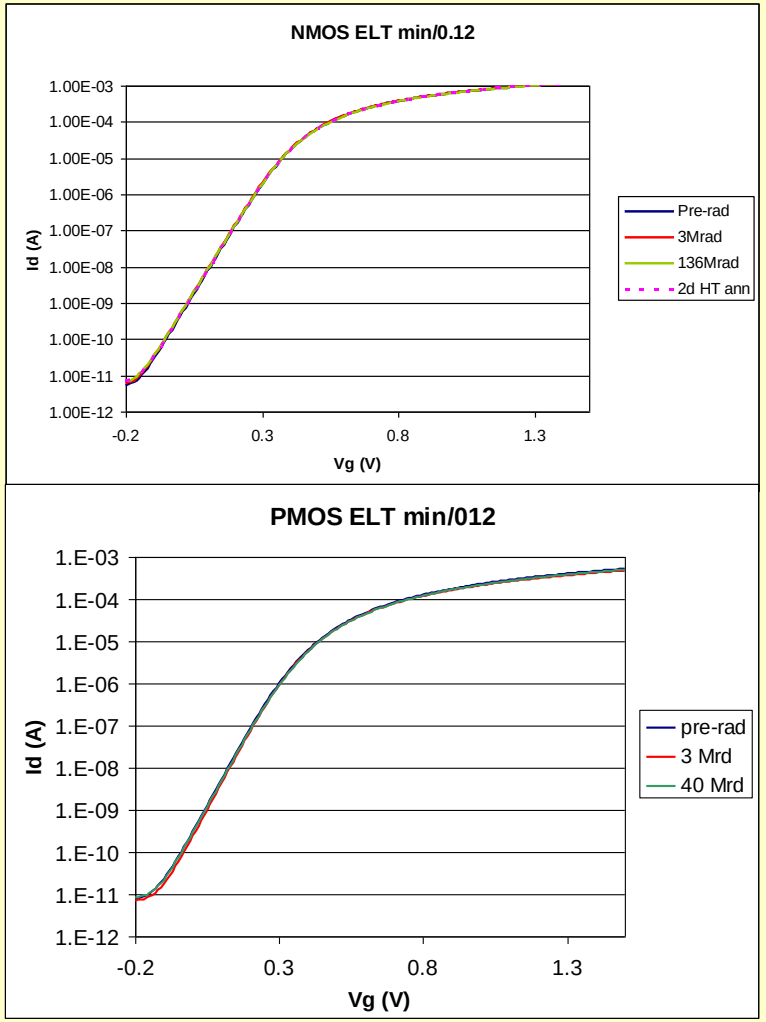
Conclusions

- Development is limited by (lack of) ideas, not by technology
  - … and not even by the "cost" of adv tech
- The HEP community has much to learn, (and to profit from) adopting standards, IP sharing, and avoiding NIH attitudes
- Detectors and microelectronics should be developed in parallel
  - much to be expected from jointly conceived SoC for detectors

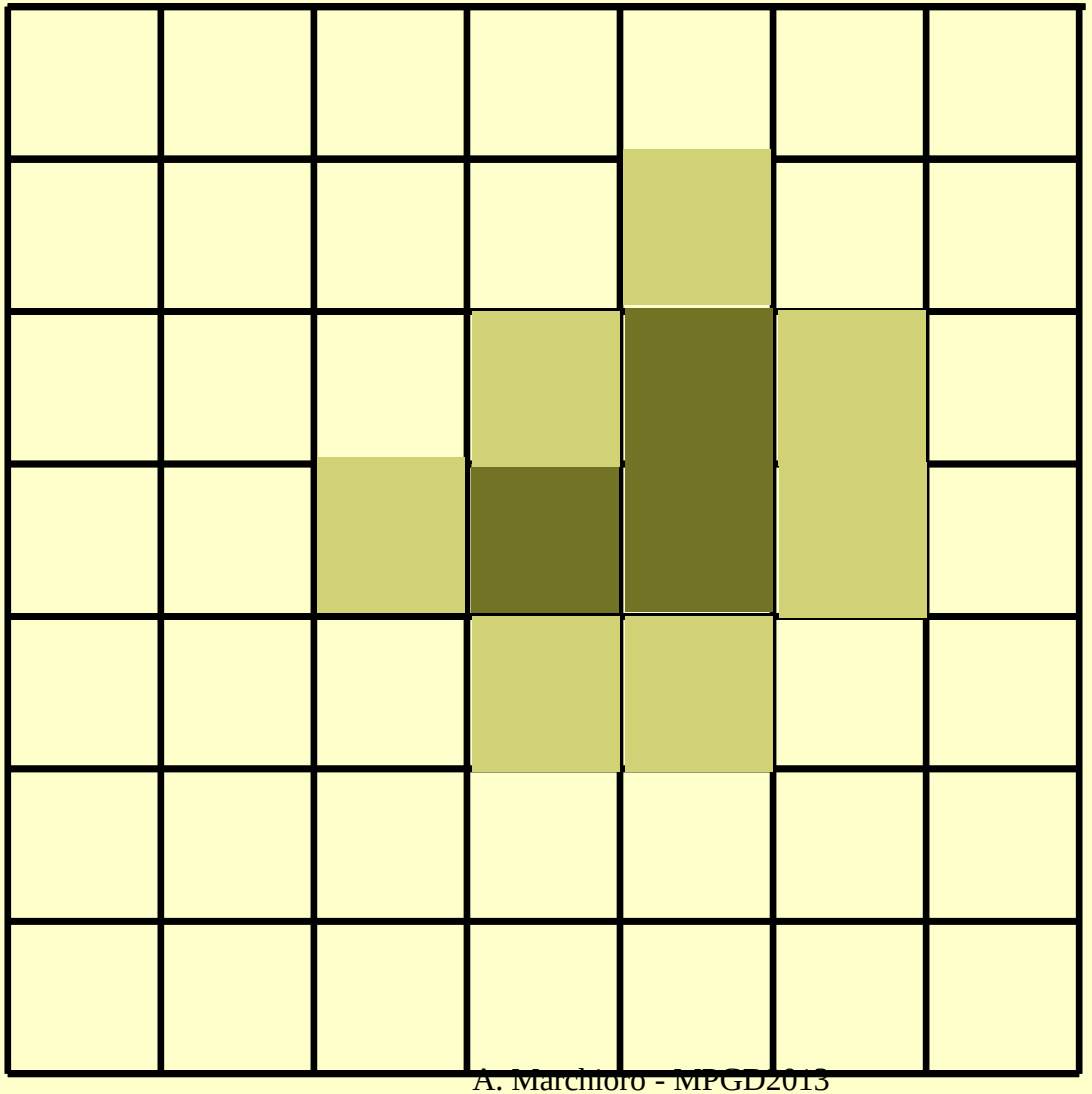
Spares

Core 130nm NMOS transistors, enclosed layout





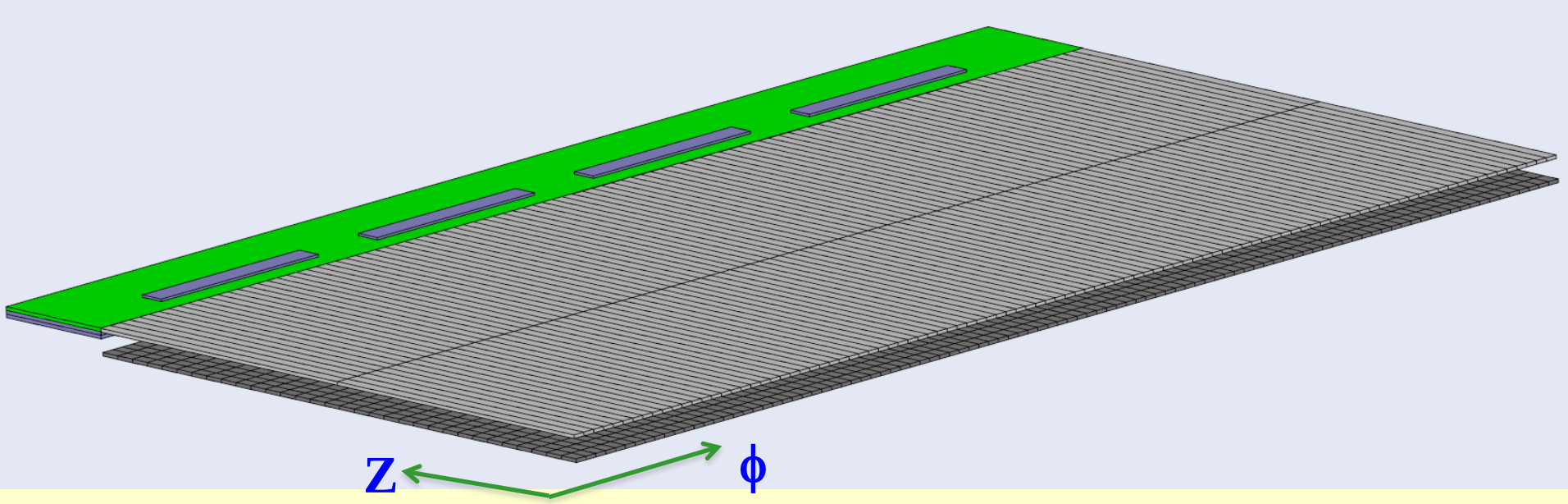
Halo Energy recovery for trigger in NA48



$$E_{Tot} = \sum_{>Thres} E_j + \sum_{Neigh} E_k$$

A. Gianoli et al., The NA48 LKr calorimeter readout electronics, RTC 1999

Hybrid strip-pixel Module Concept



- Use one layer of short strip: ~24 mm
  and one layer of ~1.5 mm long macro-pixels
- In the pixelated layer, perform the OR of the pixels in the Z direction and use it as single strip in Z
- *Coincidence of the two layers provides pT cut*
- *Pixel position provides Z coordinate*

- Thickness: two sensors + Pixel strip RO + cooling interposer + hybrid sideways