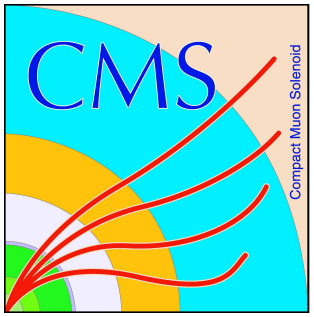

Report from Turin on Front-End design

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Turin, 27/08/2013

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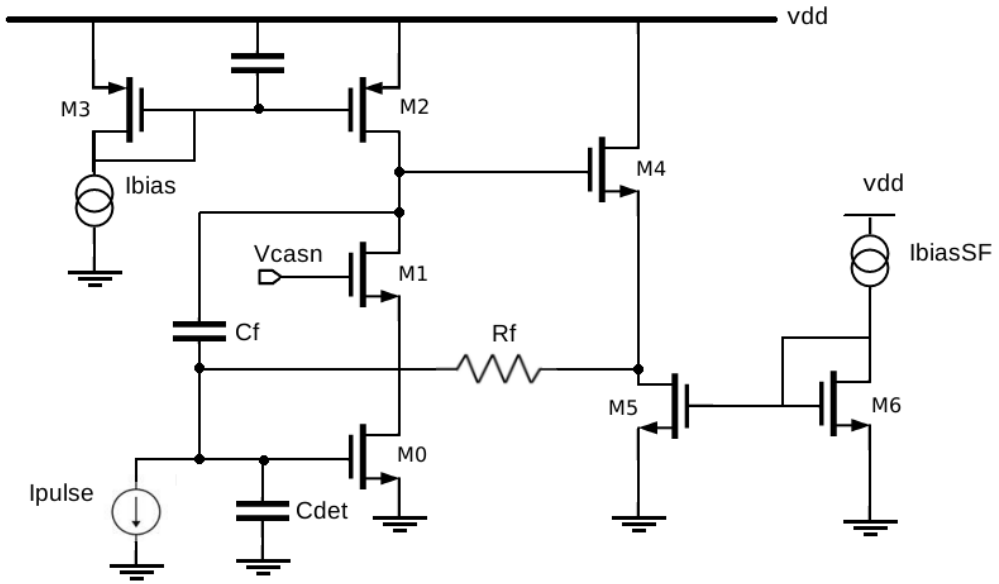
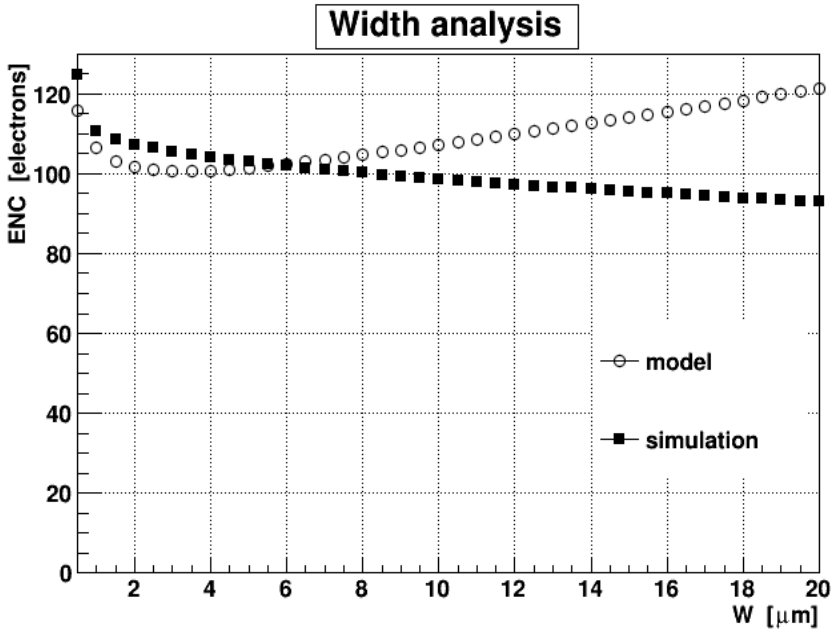
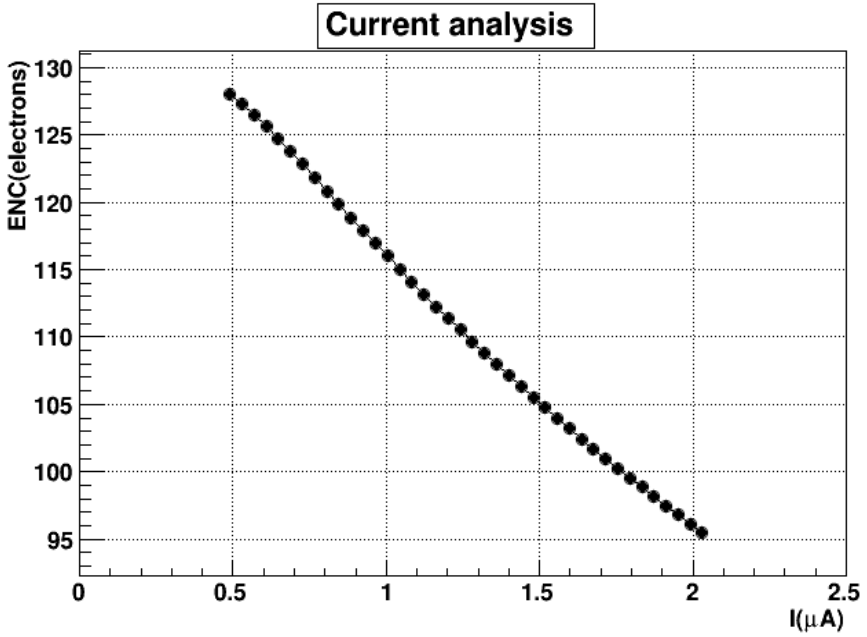
Charge Sensitive Amplifier

- Single-ended common source amplifier with a cascoded input
- Simulation of the ***noise contribution*** due to the electronics
- Comparison with the ***EKV model***
- Gain can be increased using a ***regulated cascode*** for the PMOS



CSA Noise analysis: results (1)





Constraints:

- L = 130 nm
- Peaking time Tp = 12.5 ns
- $C_{detector}$ = 100 fF
- I = 1.6 μA

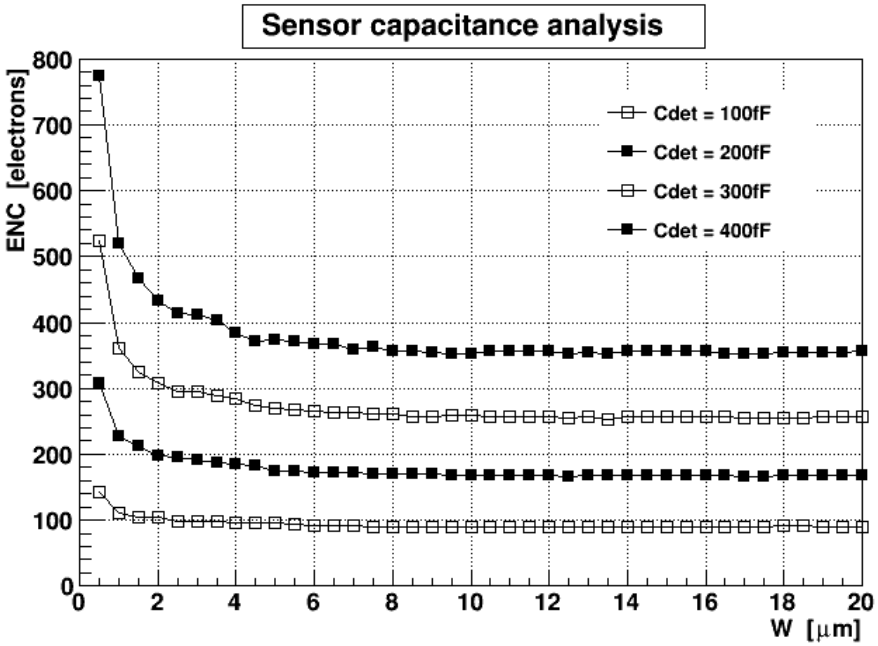
Good agreement with the EKV model(within 10%)

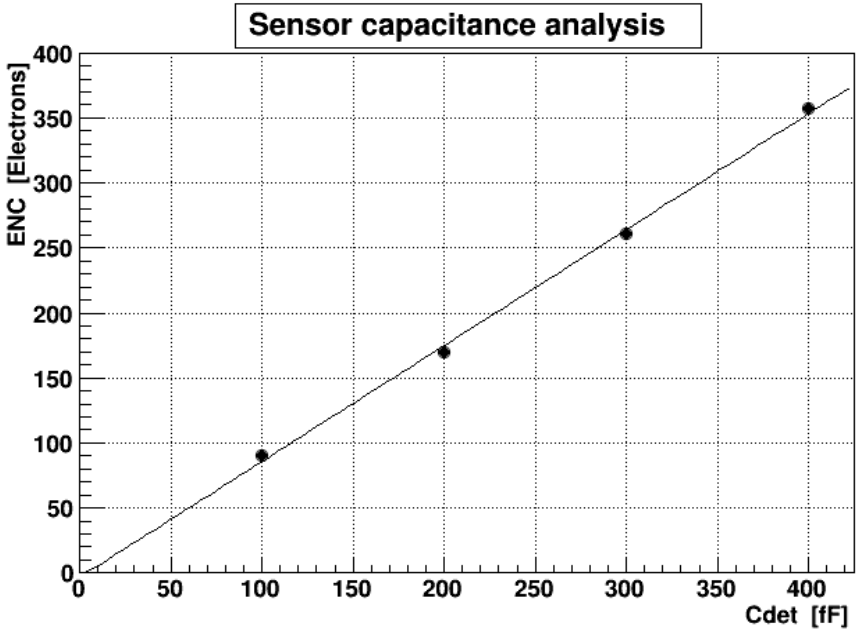
Constraints:

- W = 8 μm
- L = 130 nm
- Peaking time Tp = 12.5 ns
- $C_{detector}$ = 100 fF

Noise increases reducing power consumption: need to find the best compromise

CSA Noise analysis: results (2)



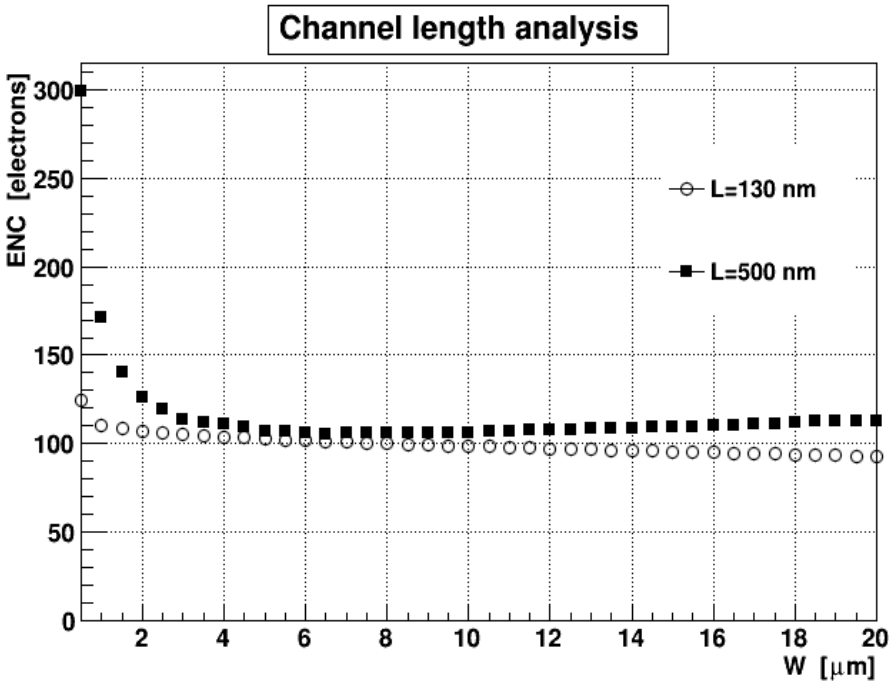


Constraints:

- L = 130nm
- Peaking time Tp =12 ns
- I = 1.6 μA

ENC linearly dependent on $C_{detector}$

CSA Noise analysis: results (3)



Constraints:

- Peaking time Tp = 12.5 ns
- I = 1.6 μA
- $C_{detector}$ = 100 fF

Noise ***does not increase sensibly*** with the channel length

Next steps

- Study of the ***feedback network schematic*** (bipolar architecture based on the Krummenacher scheme)
- Study of the ***gain linearity***
- ***Mismatch analysis***: MC simulation of the variation of the transistors parameters due to manufacturing fluctuations
- Simulation of the ***power consumption***
- Implementation of the ***leakage compensation*** circuit
- Connection of this stage with the ***comparator***

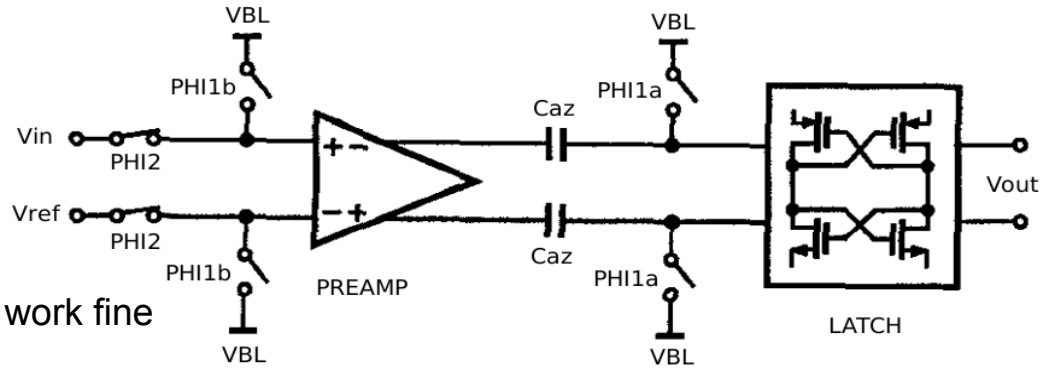
Comparator design (1)

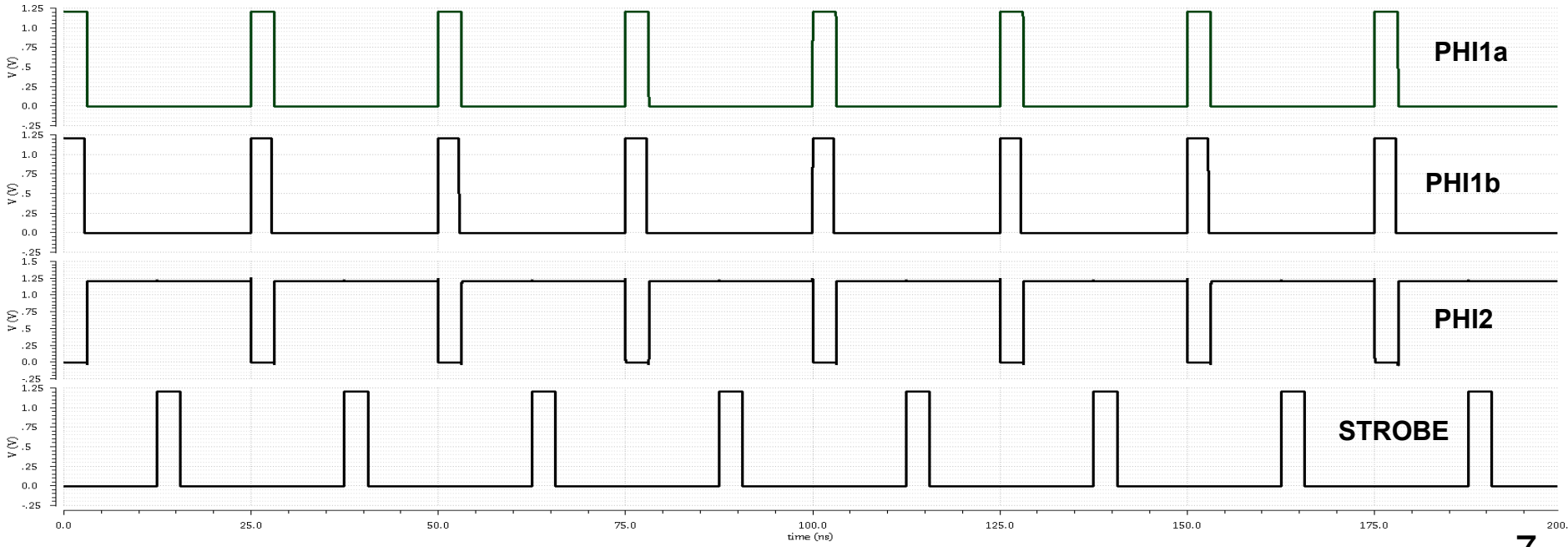
- build a full-featured front-end analog chain ⟶ complete VFE with ***synchronous binary readout***

- go ahead with ***discrete time*** comparators and ***autozeroing*** studies

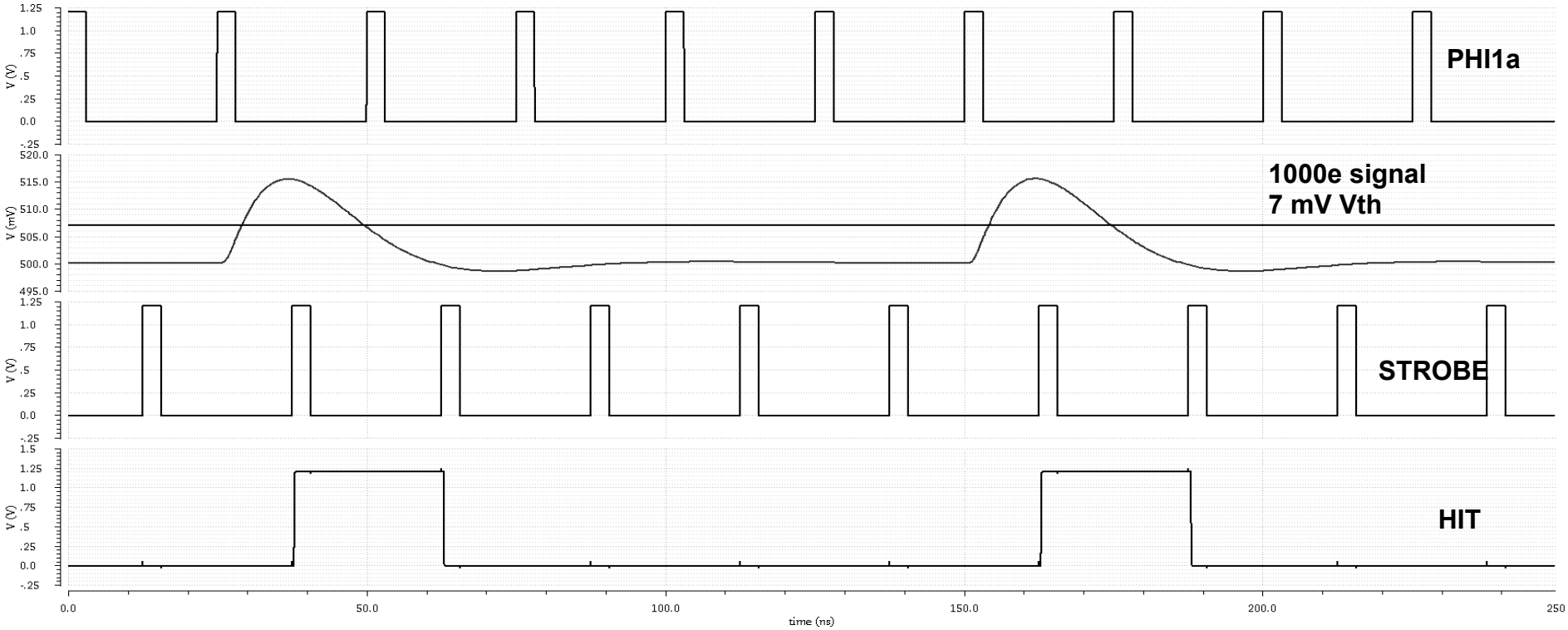
- try to keep the design as simple as possible

  ⟶ *one stage **PREAMP** + **LATCH** + **OOS*** work fine





Comparator design (2)

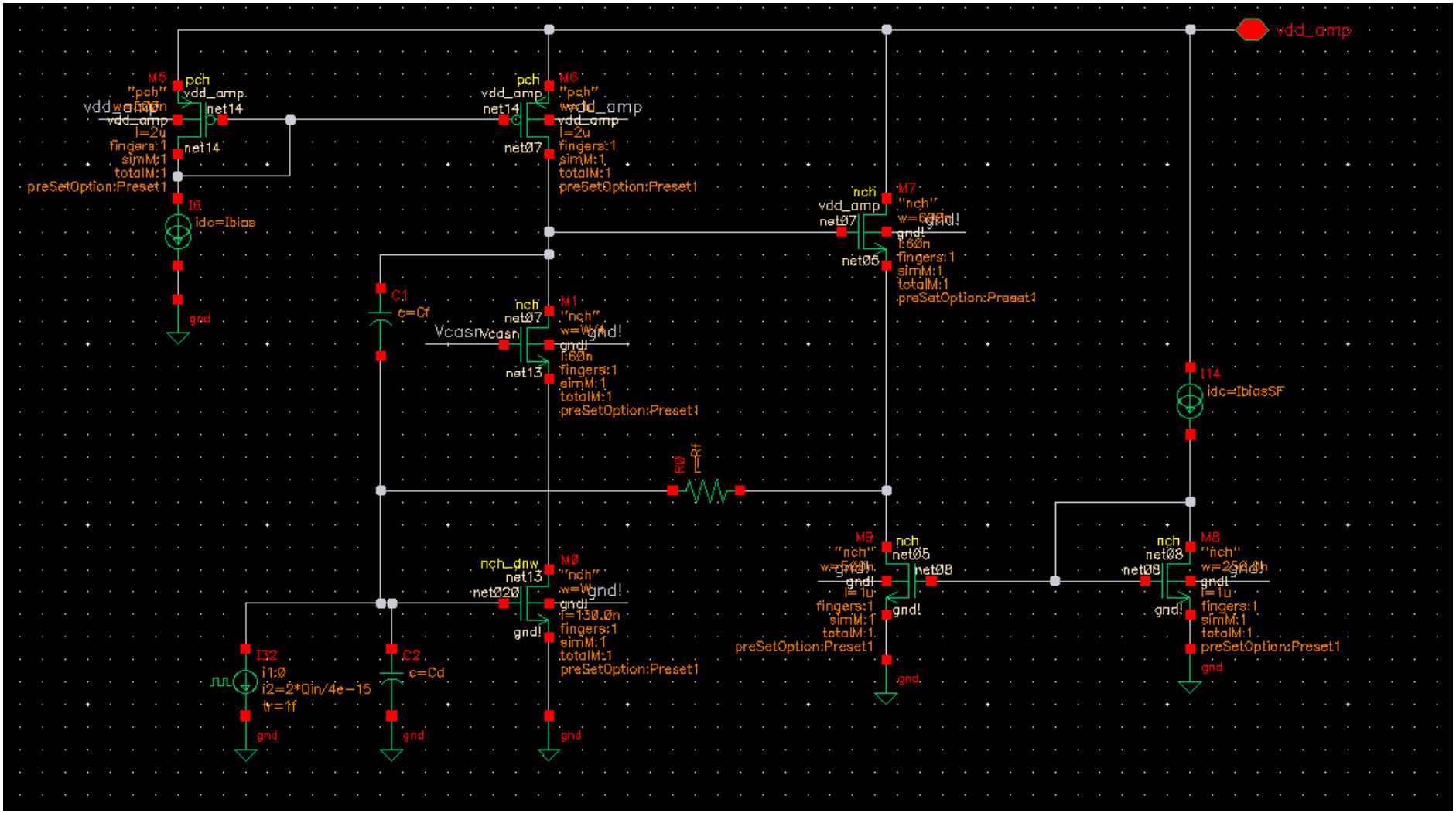


- at present, offset compensation performed ***each BX*** (maybe redundant ?)
- realistic analog pulses coming from the VFE fed to the comparator
- ***1000 electrons*** minimum detectable signal constraint fulfilled
- 100% hit efficiency verified in ***MC mismatches*** simulations (no missing/fake hits due to offsets)
- 'ad hoc' ***control signals***, move to a ***logic FSM algorithm*** for a more realistic design indeed

Thanks for your attention

Backup

Charge Sensitive Amplifier



Comparator - PREAMP schematic