Active pixel sensors in 180 nm HV CMOS technology for HL-LHC detector upgrades

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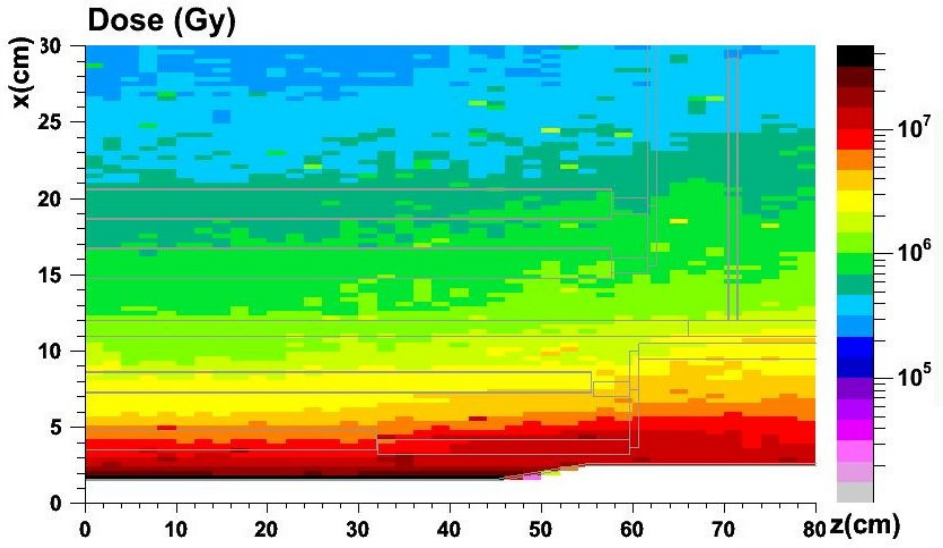
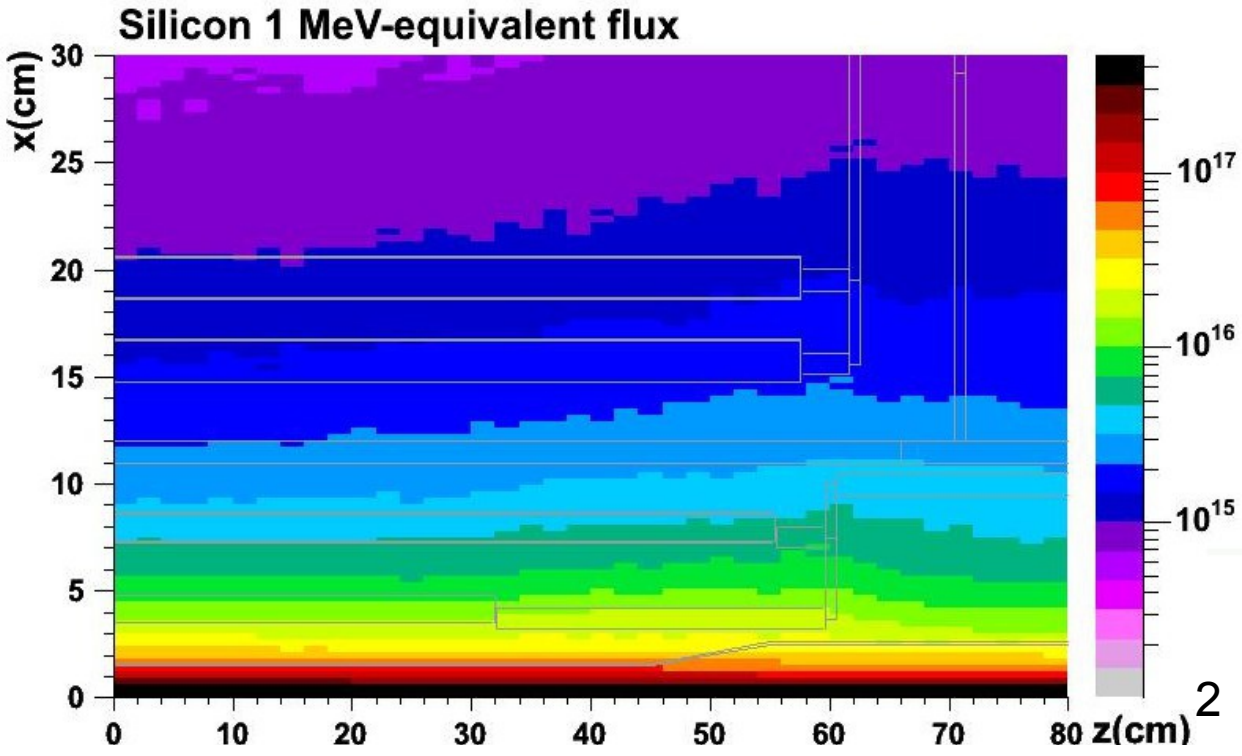
on behalf of the participating institutes:

U Bonn, CERN, CPPM Marseille, U Geneva,
U Glasgow, U Heidelberg, LBNL

Fluences at HL-LHC

- integrated luminosity: 3000 fb^{-1}
- including a safety factor of 2 to account for all uncertainties this yields for ATLAS:
  - at 5 cm radius:
    - ~$2 \cdot 10^{16}$ n_{eq} cm^{-2}
    - ~1500 MRad
  - at 25 cm radius
    - up to 10^{15} n_{eq} cm^{-2}
    - ~100 MRad
    - several m^2 of silicon
  - strip region
    - some 10^{14} n_{eq} cm^{-2}
    - up to ~200 m^2 of silicon





Implications

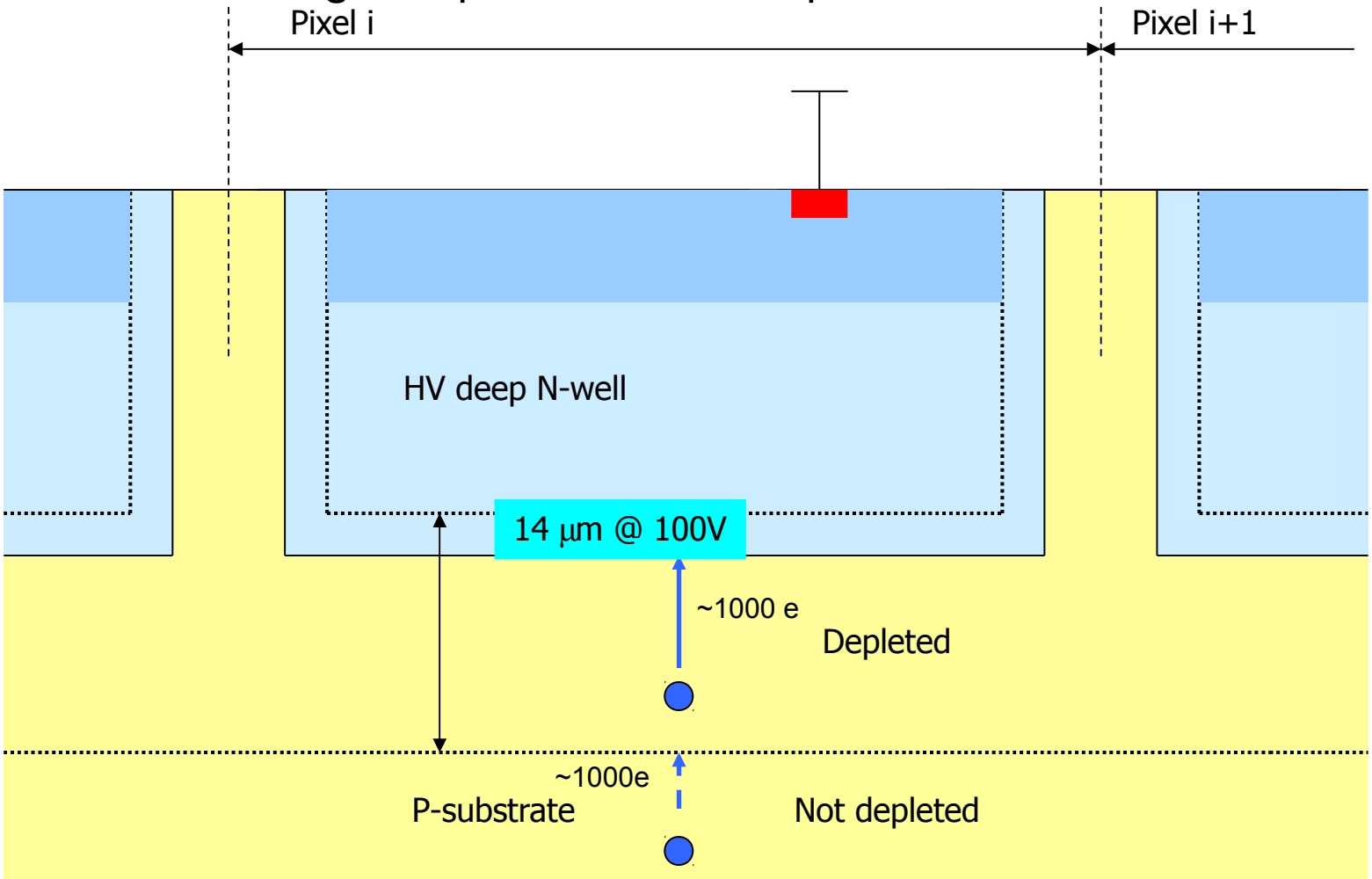
- High fluences: trapping dominant
  - reduce drift distance, increase field → reduce drift time:
    - thin planar, 3D sensors
- Large areas: low cost of prime importance
  - industrialised processes
  - large wafer sizes
  - cheap interconnection technologies
- **Idea: explore industry standard CMOS processes as sensors**
  - commercially available by variety of foundries
    - large volumes, more than one vendor possible
  - 8” to 12” wafers
    - low cost per area
  - (partially too) low resistivity p-type Cz silicon
    - thin active layer
    - wafer thinning possible (down to 75 μm is standard, even less is possible)

CMOS? Which flavours?

- Identified 3 main branches with several mixtures:
  - passive n-in-p planar sensors produced on 8” wafers
  - HV-CMOS active sensors
  - HR-CMOS active sensors/MAPS
- n-in-p planar sensors done by CMOS foundries
  - thanks to CMOS imaging sensors many foundries now offer
    - high-resistivity 8” p-bulk substrates
    - sensor thinning and post-thinning backside processing – but reticule-based
    - significantly lower cost for larger volumes
  - should be in general suitable for n-in-p sensors, but
    - unprecedented bias voltages to be applied → guard rings?
    - inter-pixel isolation: p-wells=p-stops? p-spray?
  - past and planned projects
    - apparently, there were already unsuccessful trials...
    - ATLAS plans to try again
    - key question likely to be implant profiles, p-stops and stitching

A HV-CMOS sensor...

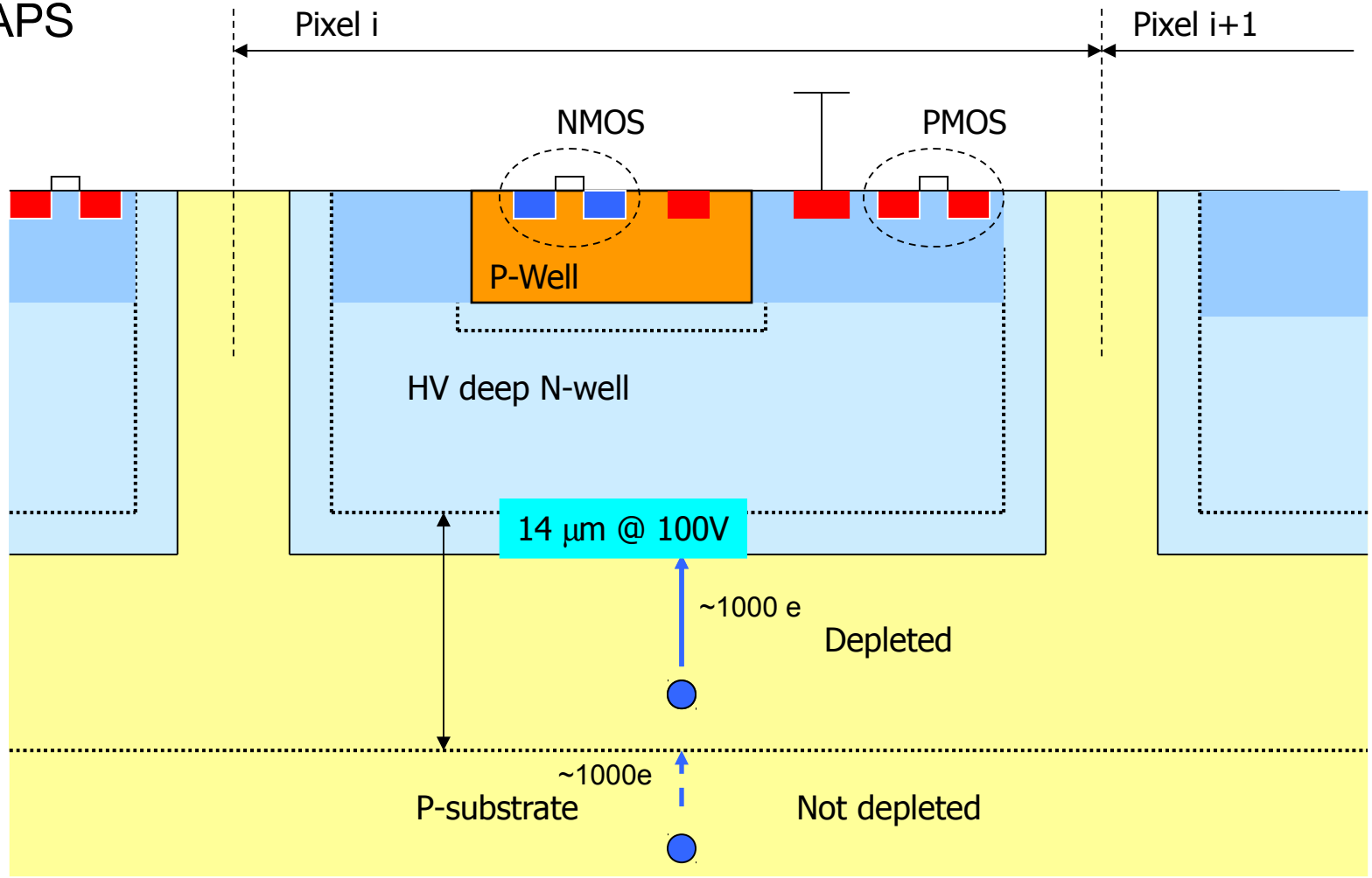
- essentially a standard n-in-p sensor
- depletion zone 10-20 µm: signal in the order of 1-2ke$^-$
  - quite challenging for hybrid pixel readout electronics
  - HR-CMOS would have larger depletion zone → "passive CMOS sensors"



The depleted high-voltage diode used as sensor (n-well in p-substrate diode)

...including active circuits: *smart diode array (SDA)*

- implementation of
  - first amplifier stages → most simple approach, e.g. Time/CLICpix
  - additional cuircuits: discriminators, impedance converters, logic, …
    - still avoids crosstalk by clock networks
  - finally: MAPS



CMOS electronics placed inside the diode (inside the n-well)

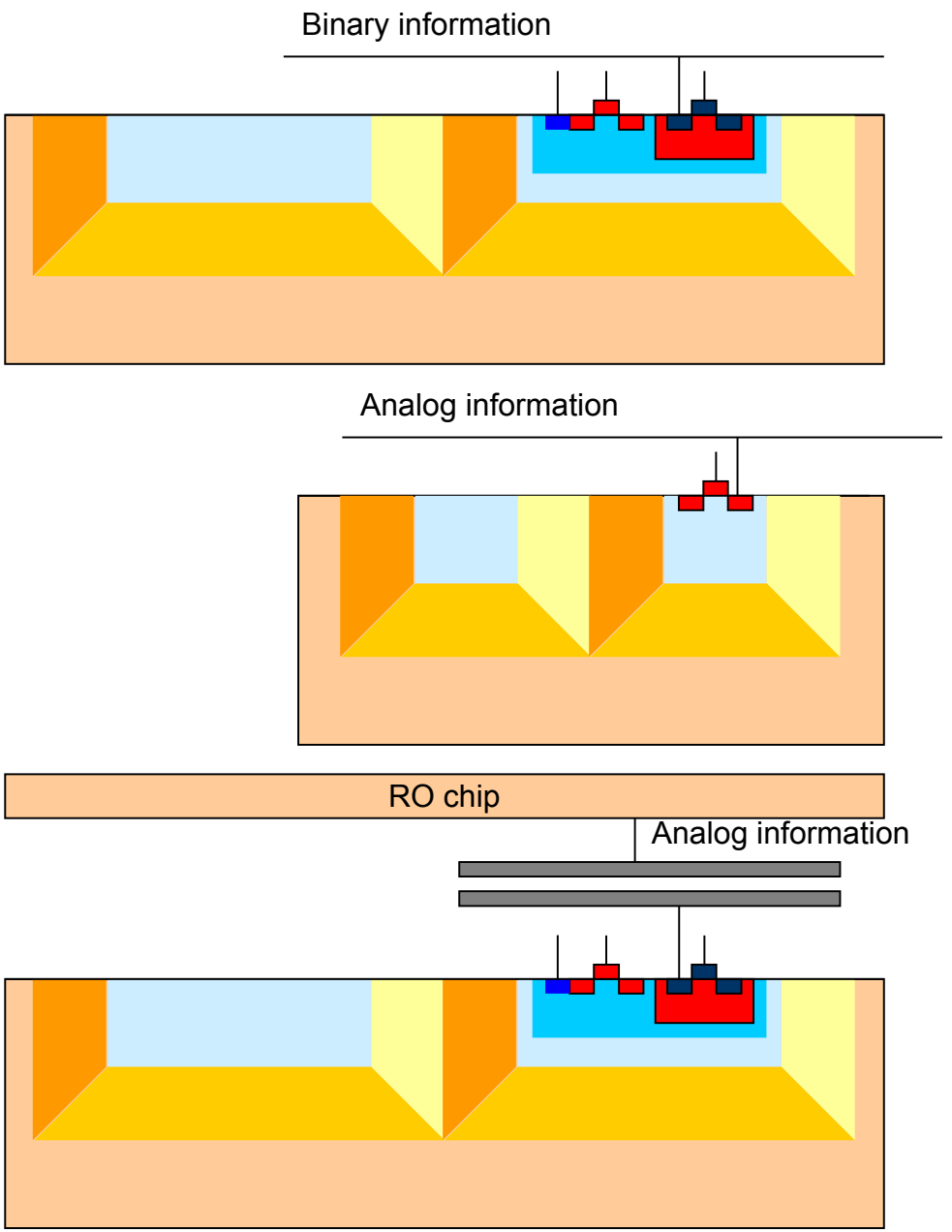
Prototypes

- Several test-chips already existing, see backup slides for more detailed results

SDA with sparse readout
(“intelligent” CMOS pixels)
HV2/MuPixel chip

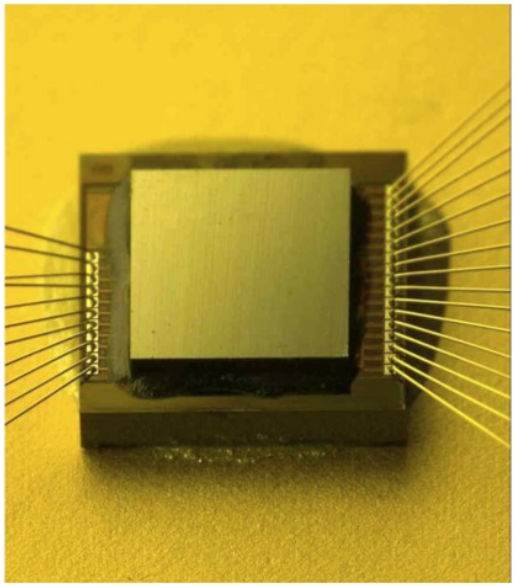
SDA with frame readout
(simple PMOS pixels)
HVM chip

SDA with capacitive readout
(“intelligent” pixels)
Capacitive coupled pixel
detectors
CCPD1 and CCPD2 detectors



Prototype summaries

First chip – CMOS pixels
Hit detection in pixels
Binary RO
Pixel size 55x55µm
Noise: 60e
MIP seed pixel signal 1800 e
Time resolution 200ns



Bumpless hybrid detecto

CCPD1 Chip
Bumpless hybrid detector
Based on capacitive chip to chip signal transfer
Pixel size 78x60µm
RO type: capacitive
Noise: 80e
MIP signal 1800e

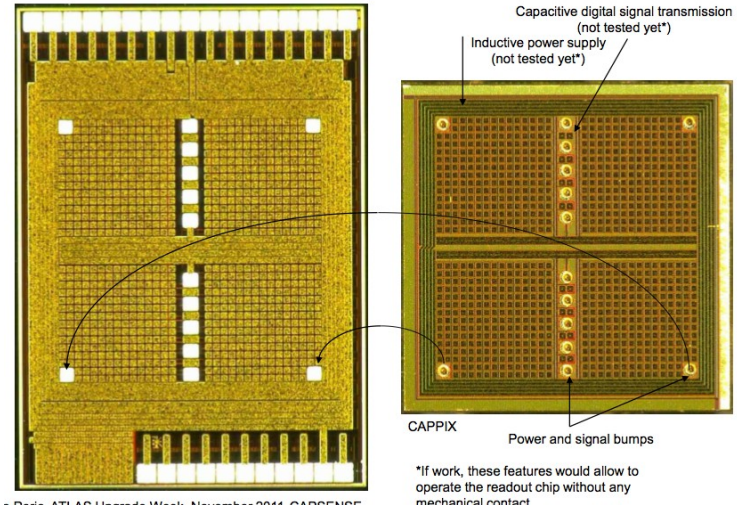
CCPD2 Chip
Edgeless CCPD
Pixel size 50x50µm
Noise: 30-40e
Time resolution 300ns
SNR 45-60

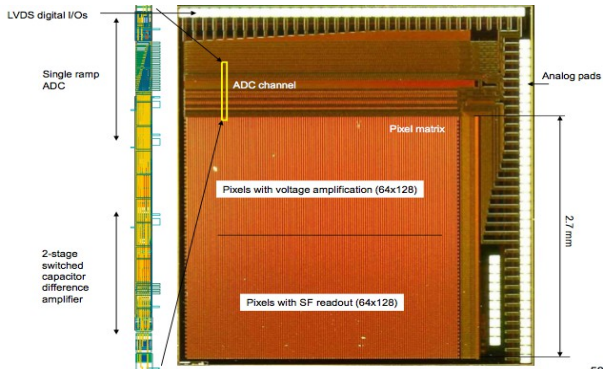
Irradiations of test pixels
60MRad – SNR 22 at 10C (CCPD1)
$10^{15} n_{eq}/cm^2$ – SNR 50 at 10C (CCPD2)

Frame readout - monolithic

PM1 Chip
Pixel size 21x21µm
Frame mode readout
4 PMOS pixel electronics
128 on chip ADCs
Noise: 90e
Test-beam: MIP signal 2200e/1300e
Efficiency > 85% (timing problem)
Spatial resolution 7µm
Uniform detection

PM2 Chip
Noise: 21e (lab) - 44e (test beam)
Test beam: Detection efficiency 98%
Seed Pixel SNR ~ 27
Cluster Signal/Seed Pixel Noise ~ 47
Spatial resolution ~ 3.8 µm



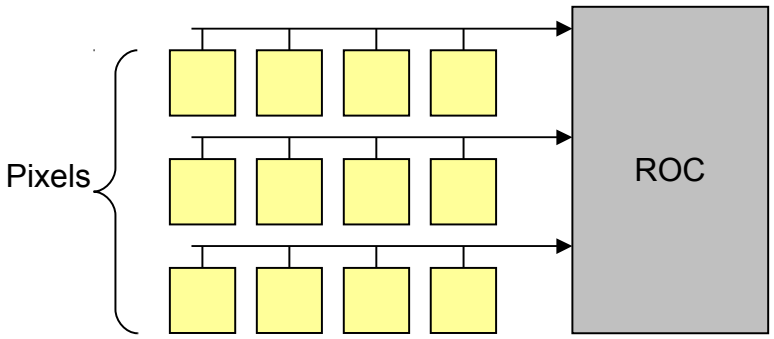


HV-CMOS

I. Peric

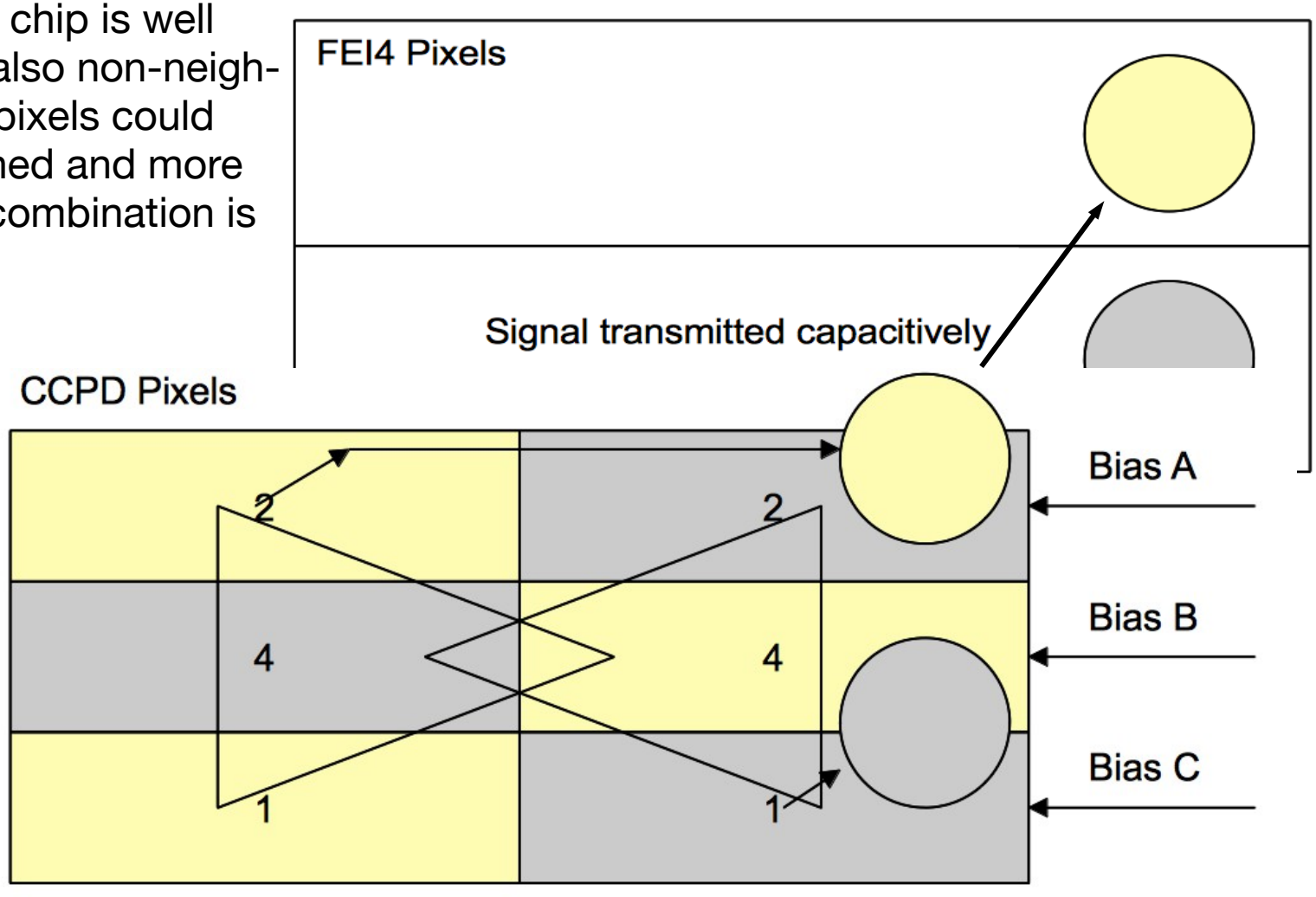
From MAPS to active sensors

- Existing prototypes would not suitable for HL-LHC, mainly because
  - readout too slow
  - time resolution not compatible with 40 MHz operation
  - high-speed digital circuits might affect noise performance
- Idea: use HV-CMOS as sensor in combination with existing readout technology
  - fully transparent, can be easily compared to other sensors
  - can be combined with several readout chips
  - makes use of highly optimised readout circuits
  - can be seen as first step towards a sensor being integrated into a 3D-stacked readout chip (not only analogue circuits but also charge collection)
- Basic building blocks: *small* pixels (low capacitance, low noise)
  - can be connected in any conceivable way to match existing readout granularity, e.g.
    - (larger) pixels
    - strips



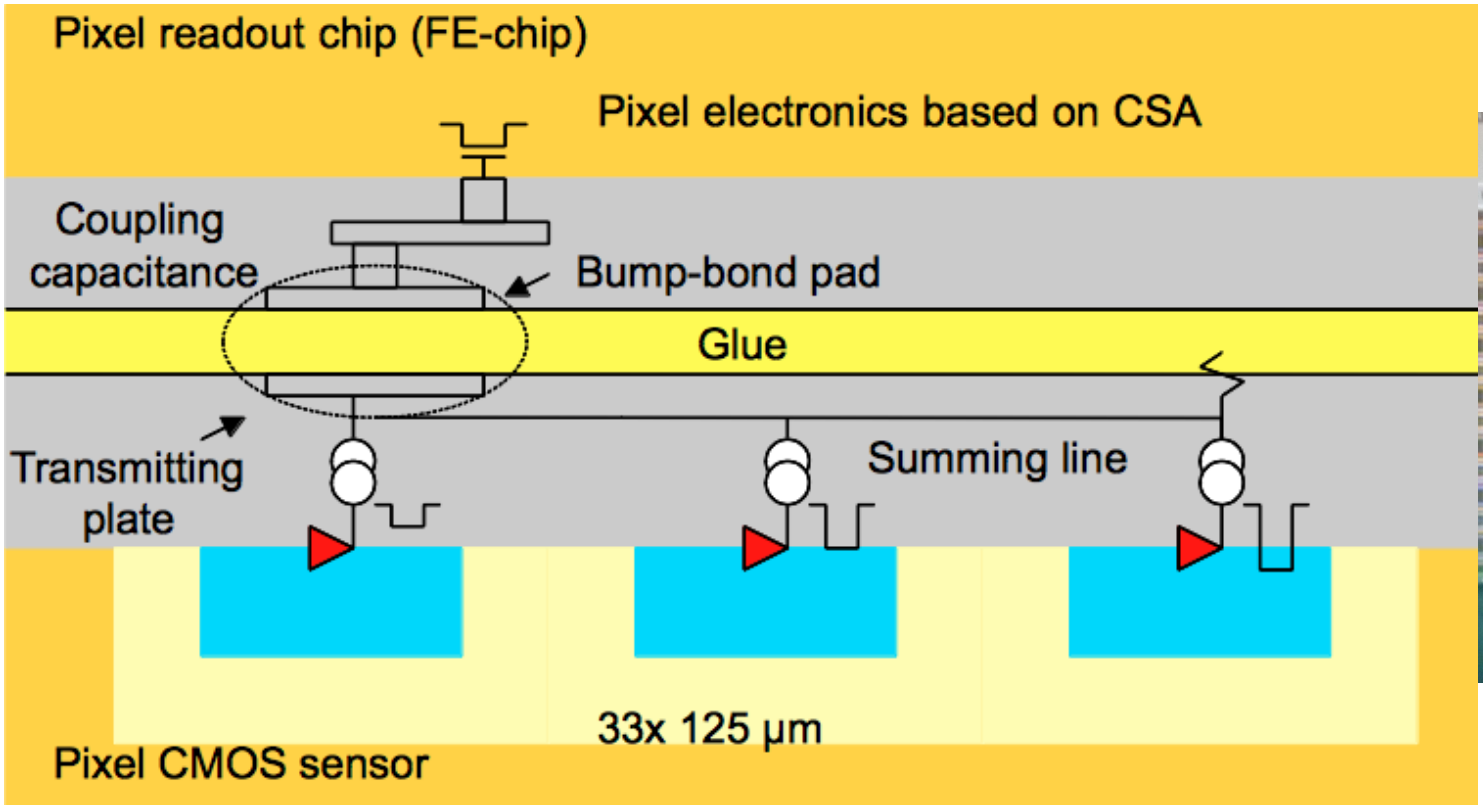
Pixels: sizes and combinations

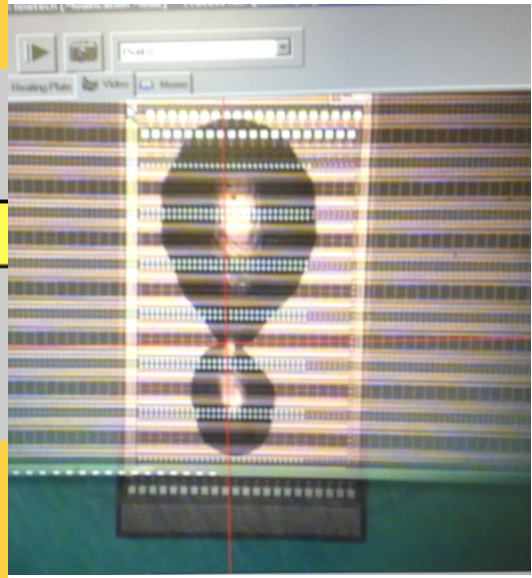
- Possible/sensible pixel sizes: 20x20 to 50x125 µm
  - 50x250 µm (current ATLAS FE-I4 chip) too large
  - combine several sensor “sub-pixels” to one ROC-pixel
    - sub-Pixels encode their address/position into the signal as pulse-height-information instead of signal proportional to collected charge
    - routing on chip is well possible, also non-neighbour sub-pixels could be combined and more than one combination is possible



Pixels: bonding?

- Only reason not to use AC coupling with pixel sensors up to now was small coupling capacitance in association with low signal
  - amplification possible, hence AC transmission not a problem at all
  - allows to get rid of costly bump-bonding
  - layer thicknesses below 5 μm have been reached with industry standard flip-chipping machines and rad-hard liquid epoxy glues
  - variations in glue thickness can be handled by tuning procedures and offline corrections if necessary

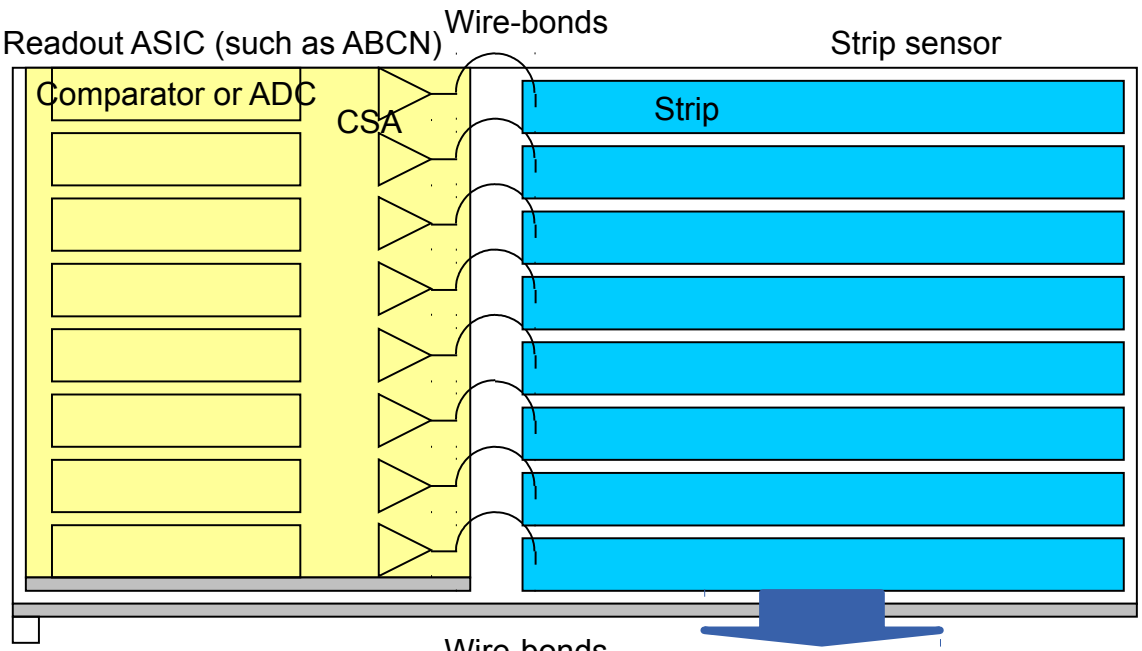


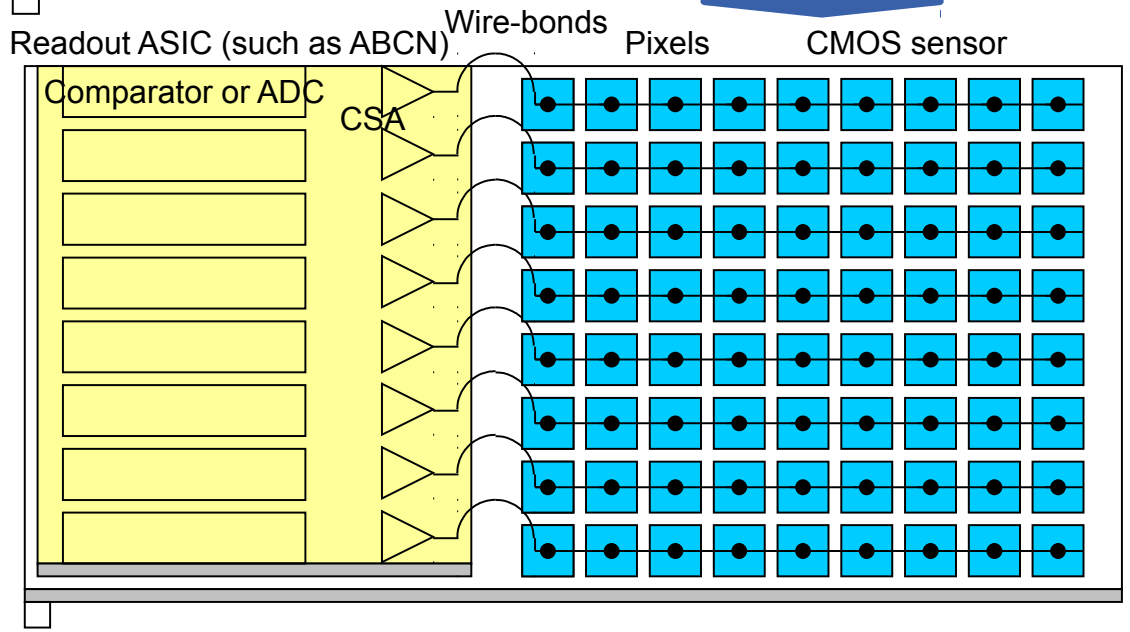


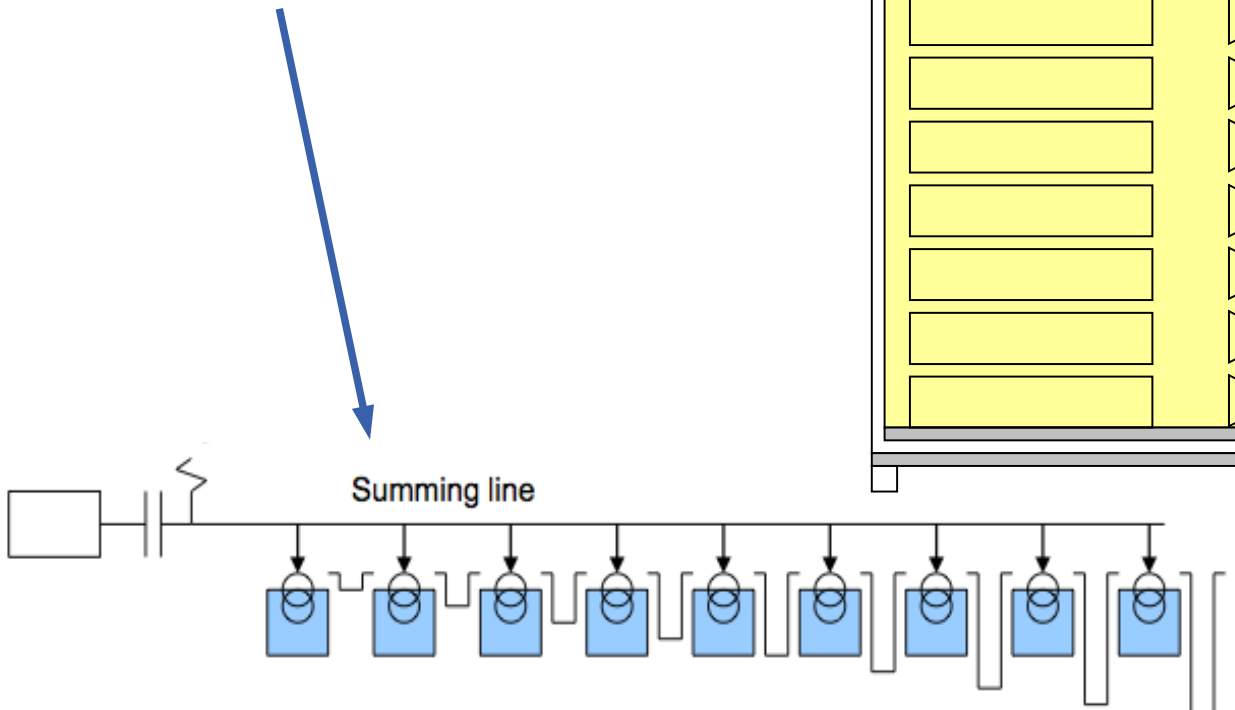
HV-CMOS

Strips

- Easiest idea would be to simply sum all pixels within a virtual strip
- Hit position along the strip can be again encoded by pulse height for analogue readout chips (e.g. Beetle)

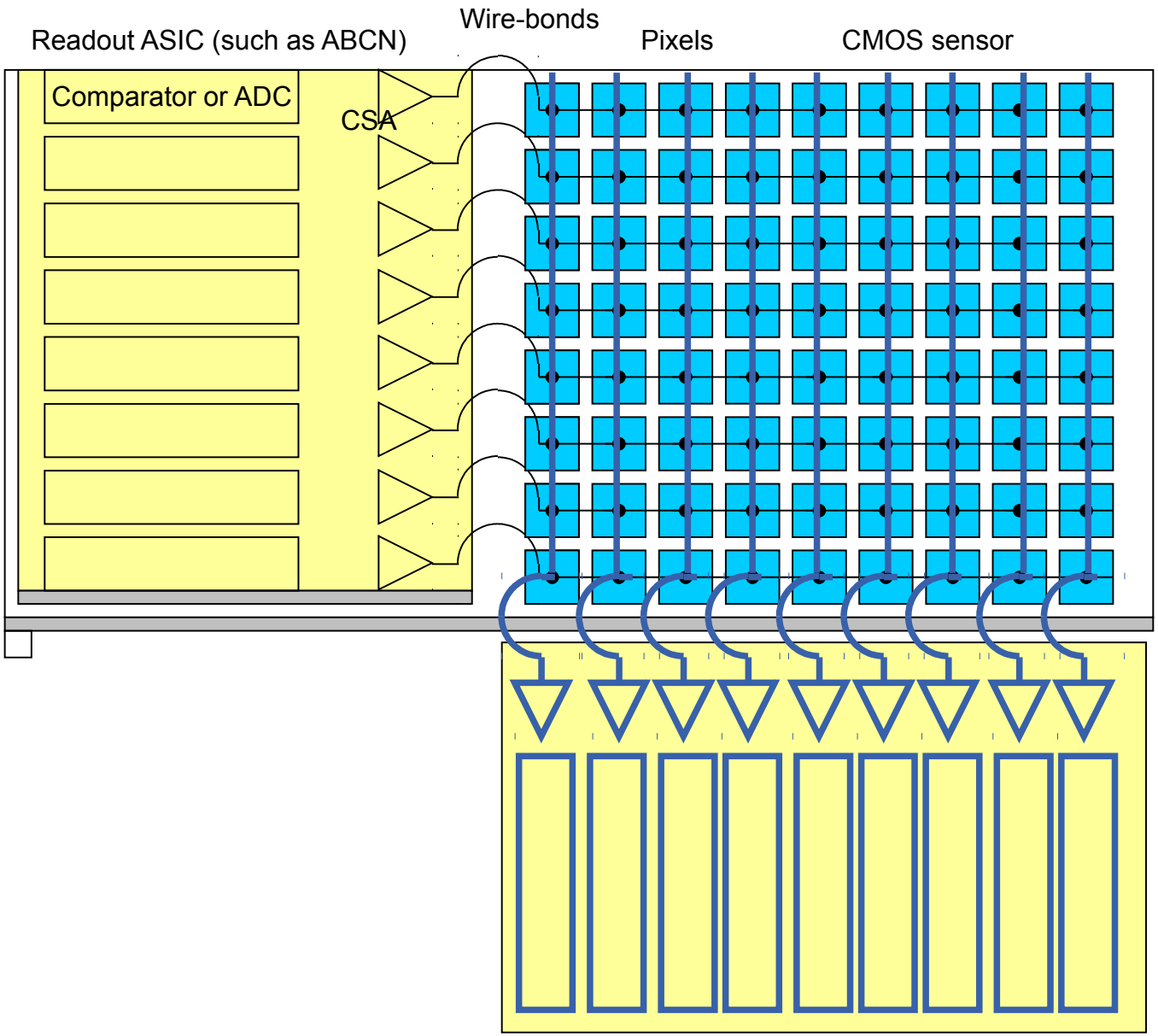






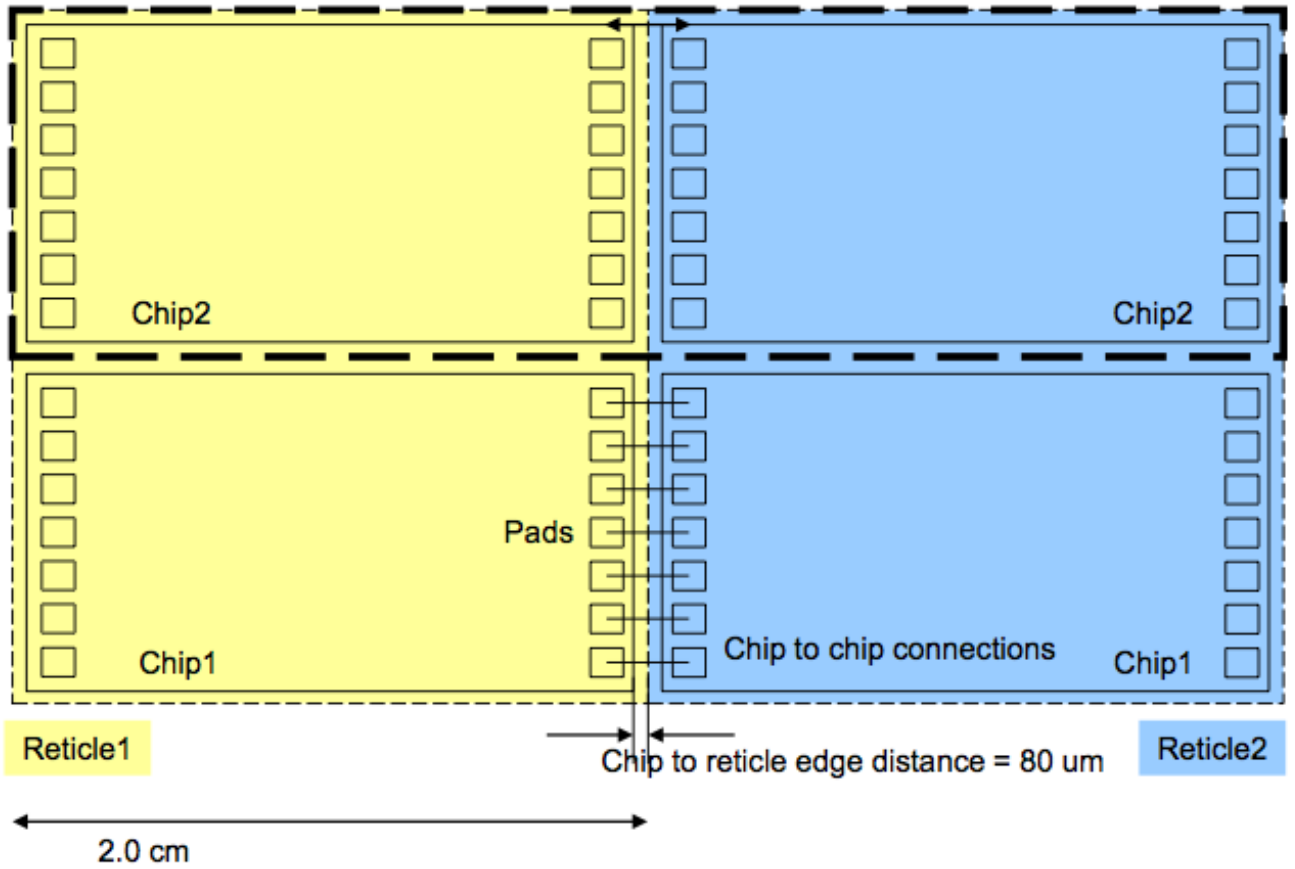
Strips

- Signals are digital so multiple connections are possible, e.g.
  - “crossed strips”
  - strips with double length but only half the pitch in r-phi

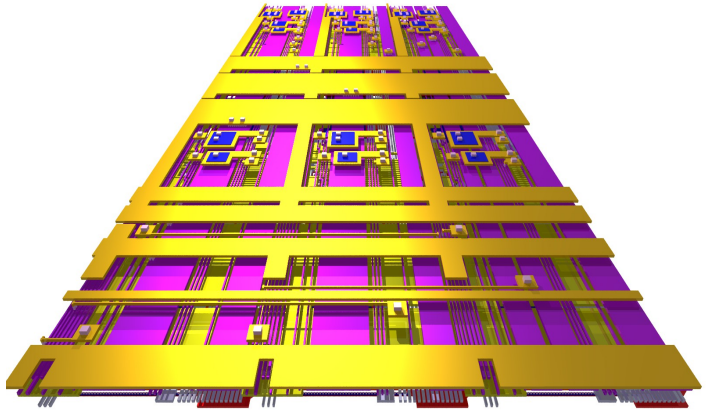


Reticule size/stitching

- Sensor size is currently limited by reticule size of ~2x2 cm
  - however, the yield should be good (very simple circuit, essentially no “central” parts) so it might be interesting to cut large arrays of sensors from a wafer and connect individual reticules by
    - wire-bonding
    - post-processing (one metal layer, large feature size)
- There are HV-CMOS processes/foundries which allow for stitching
- Very slim dicing streets
  - Gaps between 1-chip modules could be rather narrow



AMS H18 HV-CMOS



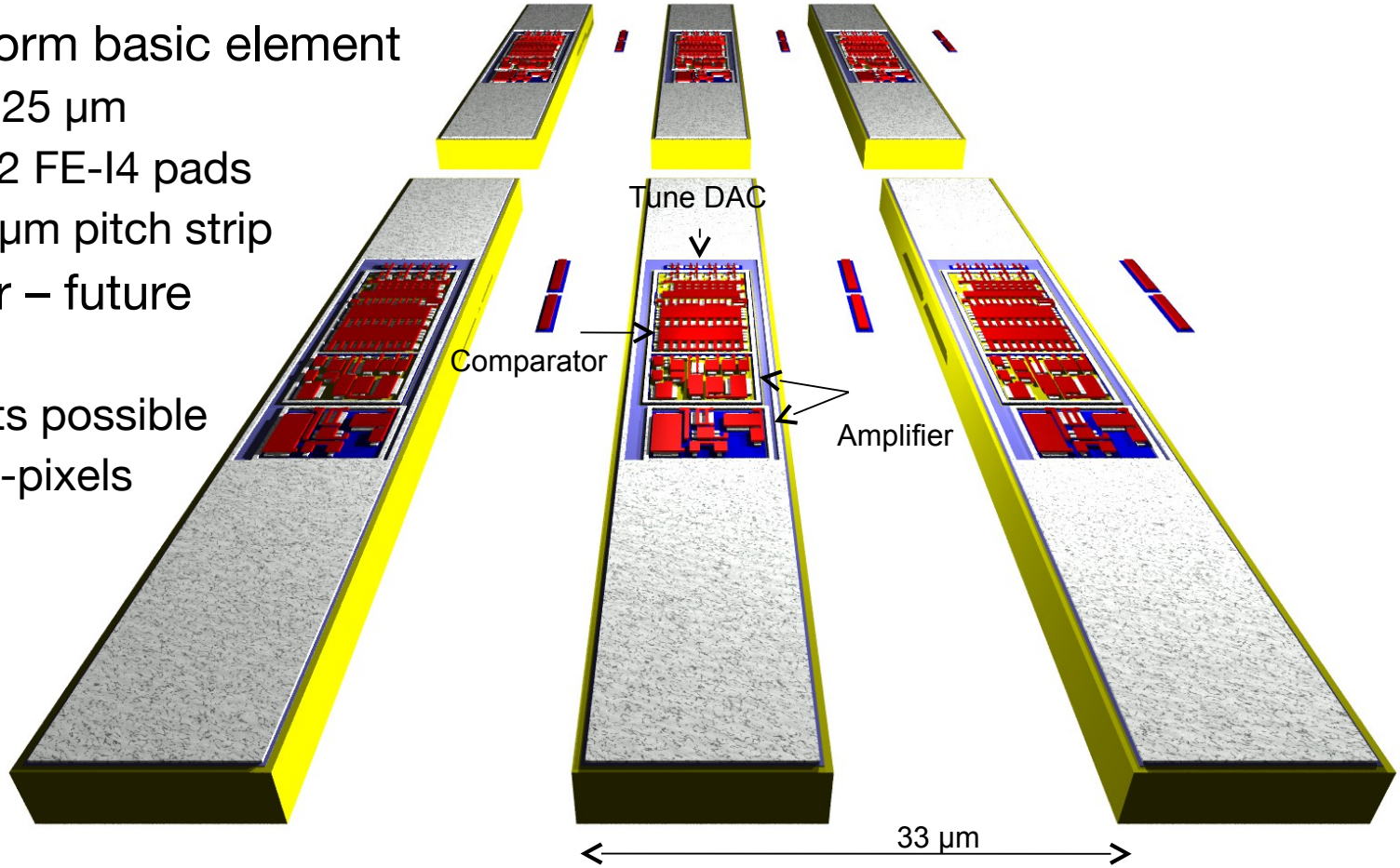
- Project initiated by Ivan Peric (U Heidelberg)
- Austria Micro Systems offers HV-CMOS processes with 180 nm feature size in cooperation with IBM
  - biasing of substrate to ~60-100V possible
  - substrate resistivity ~20 Ohm*cm → $N_{eff} > 10^{14}/cm^3$
    - radiation induced N_{eff} insignificant even for innermost layers
  - depletion depth in the order of 10-20 µm → signal ~1-2 ke^-
  - on-sensor amplification possible - and necessary for good S/N
    - key: small pixel sizes → low capacitance → low noise
  - additional circuits possible, e.g. discriminator
    - beware of 'digital' crosstalk
  - full-sized radiation hard drift-based MAPS feasible, but challenging
    - aim for 'active sensors' in conjunction with rad-hard readout electronics first
    - parallel project: MAPS for the m3e experiment at PSI, uses very similar analogue circuits, monolithic readout

ATLAS HV-CMOS R&D collaboration

- University of Bonn
  M. Backhaus, L. Gonella, T. Hemperek, F. Hügging, H. Krüger, T. Obermann, N. Wermes
- LBNL
  M. Garcia-Sciveres
- CERN
  M. Capeans, S. Feigl, M. Nessi, H. Pernegger, B. Ristic
- University of Geneva
  S. Gonzalez-Sevilla, D. Ferrere, G. Iacobucci, D. La Marra, A. La Rosa, A. Miucci, D. Muenstermann
- University of Goettingen
  M. George, J. Große-Knetter, A. Quadt, J. Rieger, J. Weingarten
- University of Glasgow
  R. Bates, A. Blue, C. Buttar, D. Hynds
- University of Heidelberg
  C. Kreidl, I. Peric
- CPPM
  P. Breugnon, P. Pangaud, D. Fougeron, F. Bompard, J.C. Clemens, J. Liu, M. Barbero, A. Rozanov

HV2FEI4

- A combined active strip/pixel sensor was designed and produced
  - strips compatible with ATLAS ABCN and LHCb/Alibava Beetle
  - pixels match new ATLAS FE-I4 readout chip
    - capacitive coupling
    - bump-bonding possible
- Structure
  - 6 sub-pixels form basic element
    - each 33 x 125 µm
    - connect to 2 FE-I4 pads
    - form a 100 µm pitch strip
  - small fill factor – future options:
    - more circuits possible
    - smaller sub-pixels

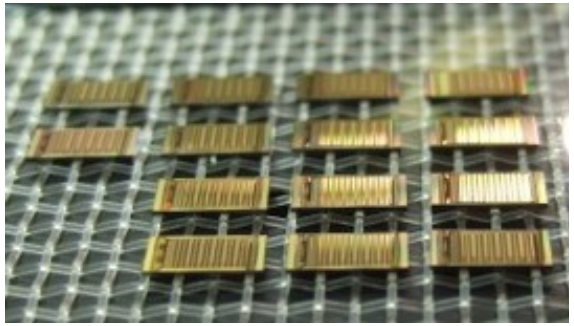


HV2FEI4 v1

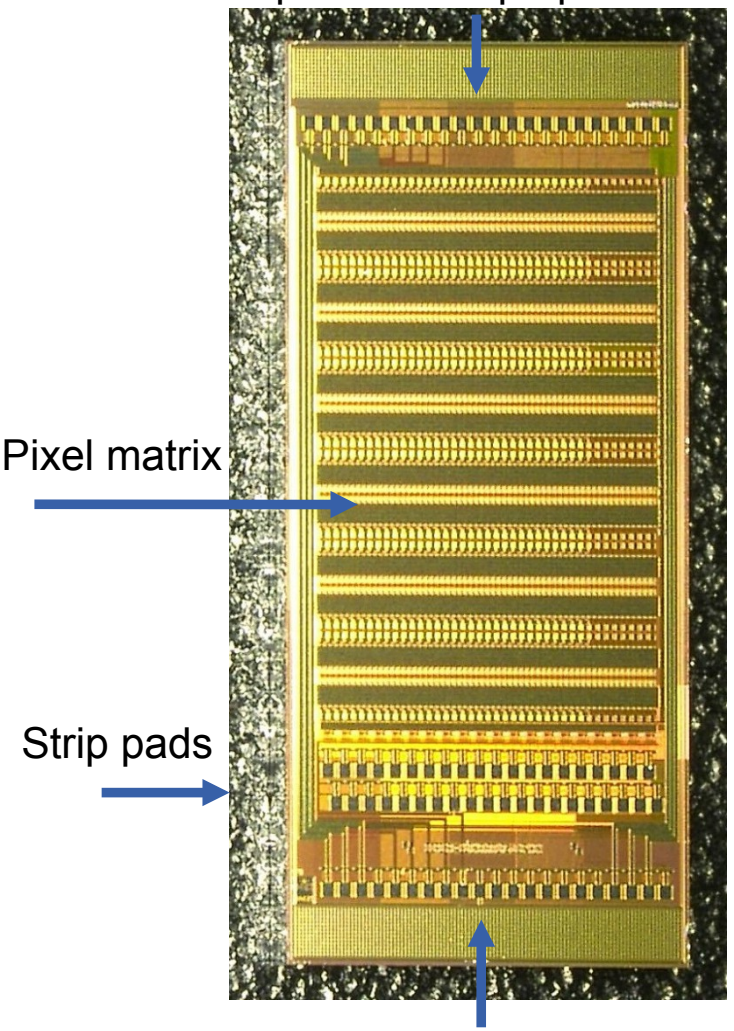
- Chip size: 2.2mm x 4.4mm
- Pixel matrix: 60x24 (sub-)pixels of 33 µm x 125 µm
- 21 IO pads at the lower side for CCPD operation
- 40 strip-readout pads (100 µm pitch) at the lower side and 22 IO pads at the upper side for (virtual) strip operation
- On chip bias DACs
- Pixels contain charge sensitive amplifier, comparator and tune DAC
- Configuration via FPGA or µC: 4 CMOS lines (1.8V)

3 possible operation modes

- standalone on test PCB
- strip-like operation
- pixel (FE-I4) readout

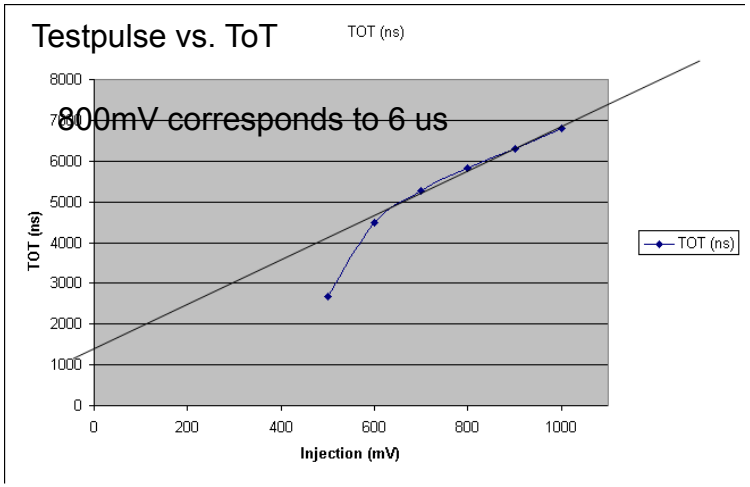


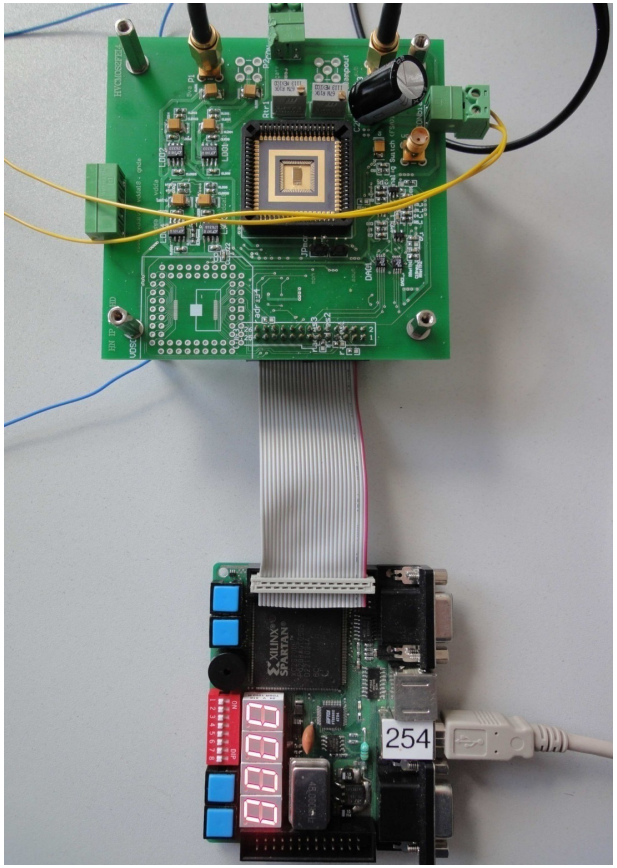
IO pads for strip operation

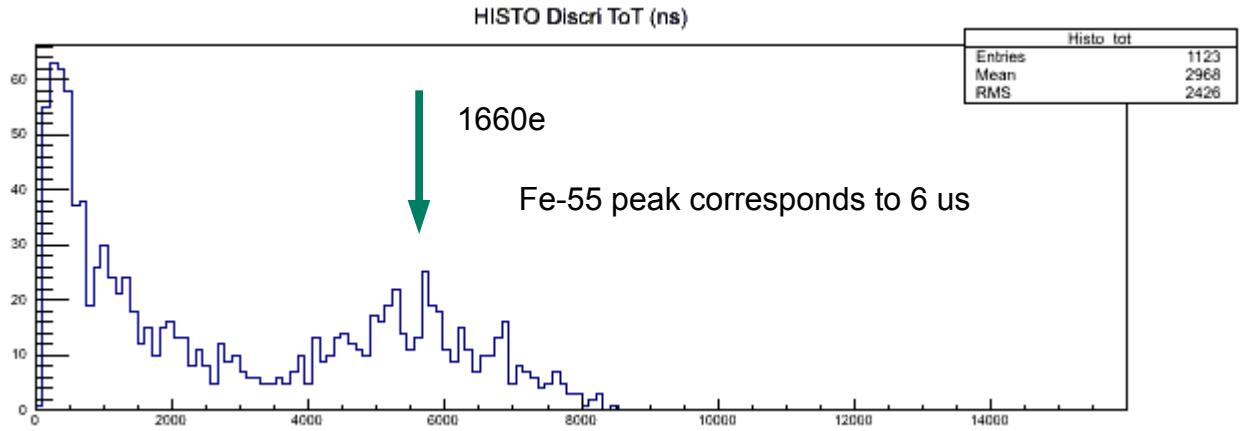


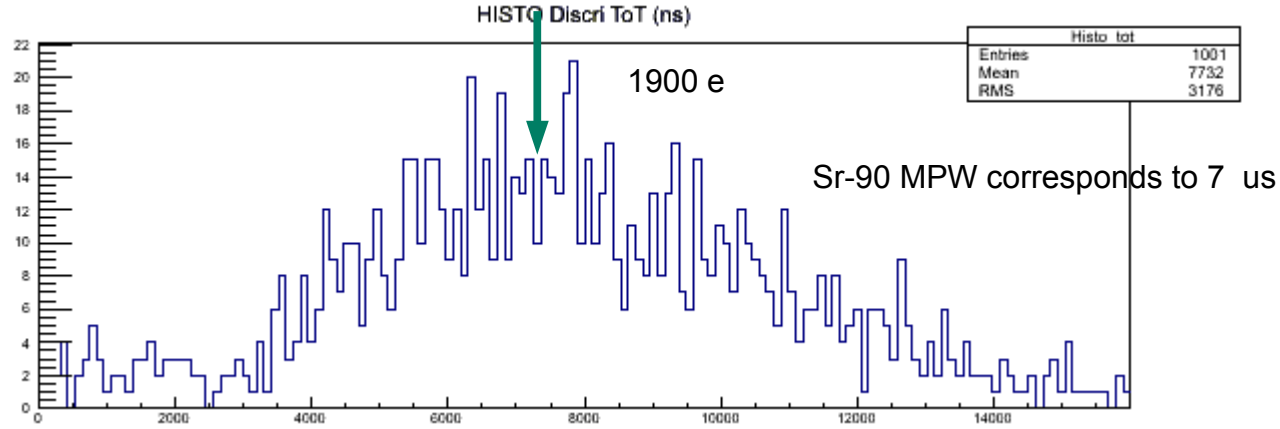
HV2FEI4: characterisation

- standalone, using monitor output
- noise: ~75 e^-
- MPW for ^{90}Sr at 60V: ~1900 e^-
  - would mean more than 20µm active depth? Diffusion? Unexpected field? → eTCT
  - corresponds to 900mV iniection







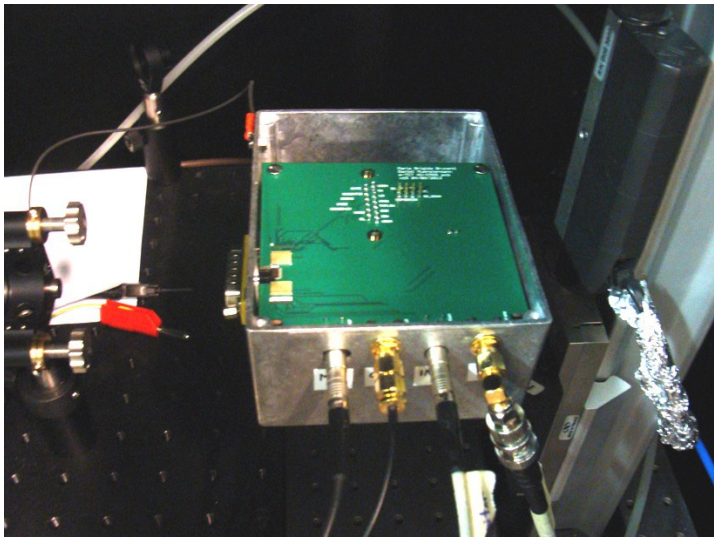


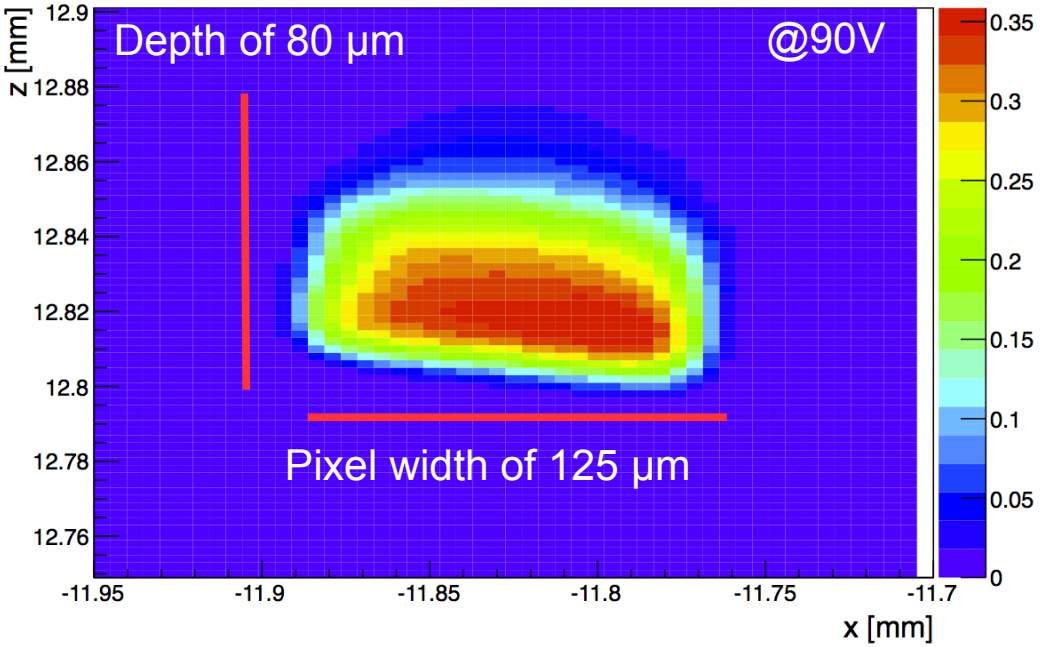
Sr-90 MPW corresponds to ~ 900mV injection amplitude

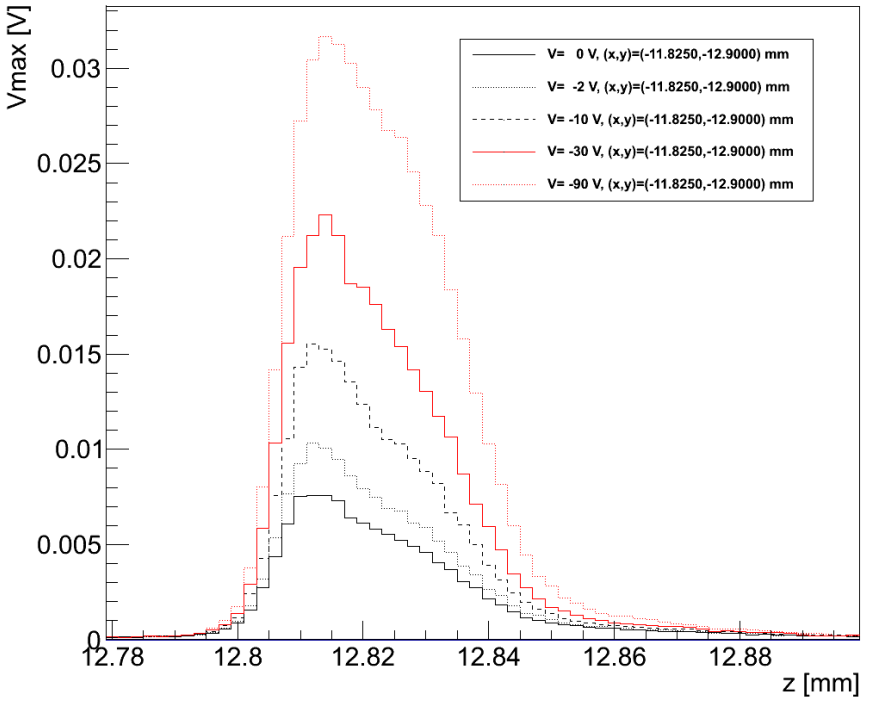
HV-CMOS

eTCT

- performed in M. Moll's group at CERN with Marcos Fernandez Garcia and Maria Brunetti
- access only to preamplifier output
  - direct access to n-well in next submission
- sidewall not polished for 1st attempt
- first indications of unirradiated sample:
  - much deeper signal detection than assumed
  - HV has not much influence → mainly diffusion?
- samples on their way to JSI for irradiation





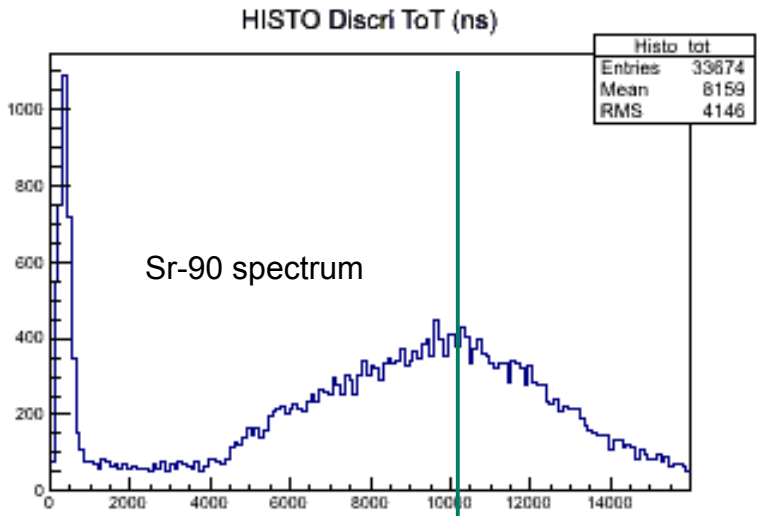


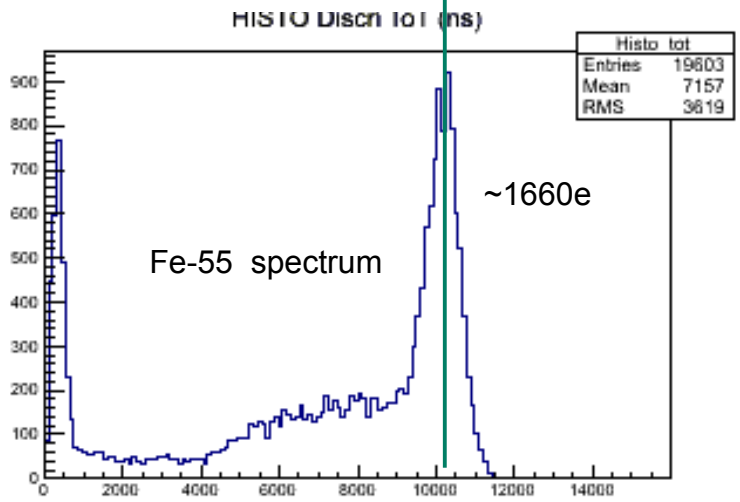
HV-CMOS

HV2FEI4: irradiation

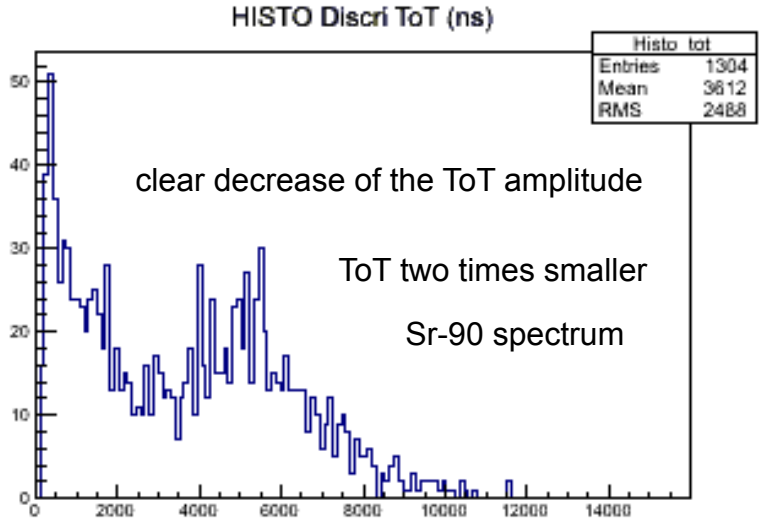
- First irradiations conducted at CERN/PS and with an x-ray tube
  - on special PCB allowing for remote operation, HV2FEI4 powered and read-out during irradiation

un-irradiated device



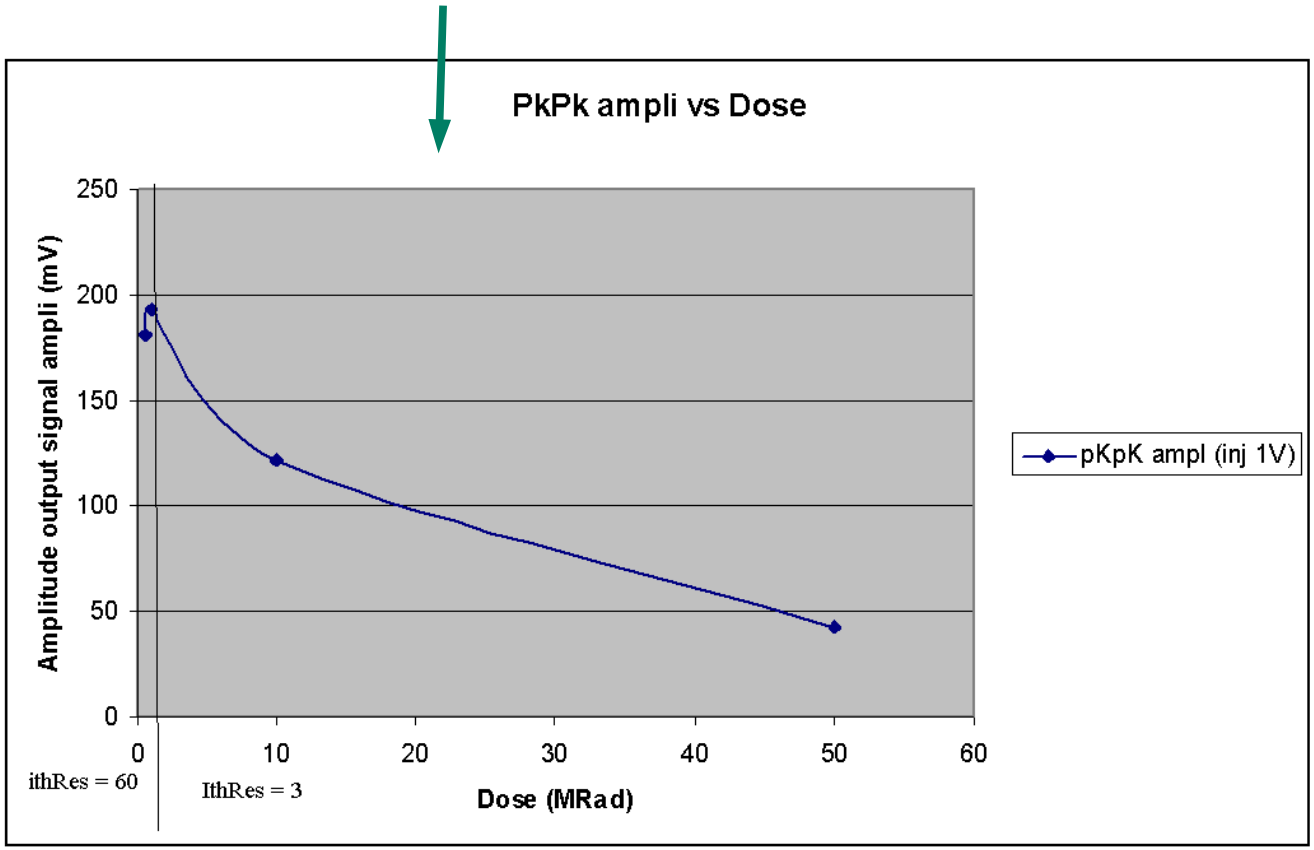


CCPD9 irradiated at 80 MRad



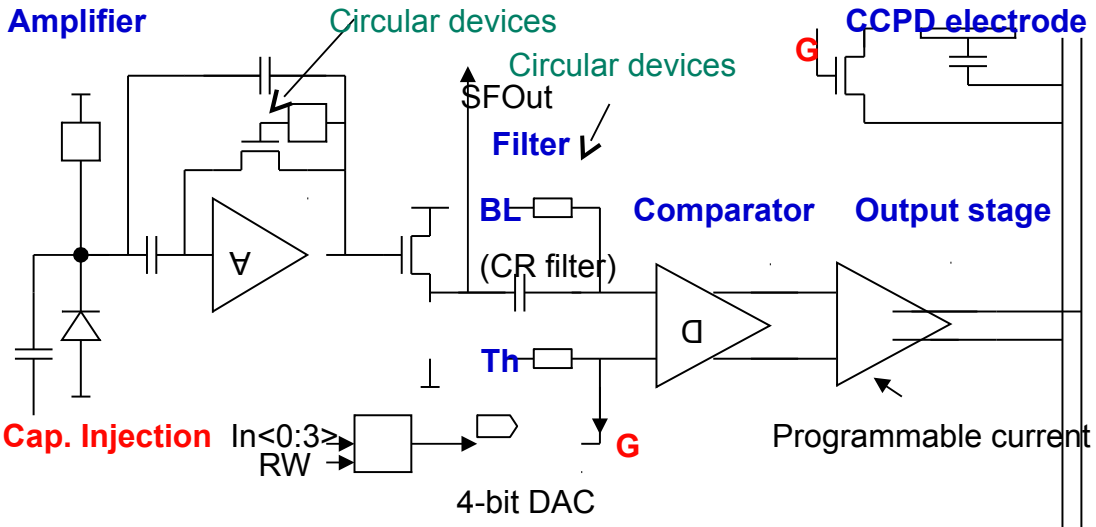
HV2FEI4: irradiation

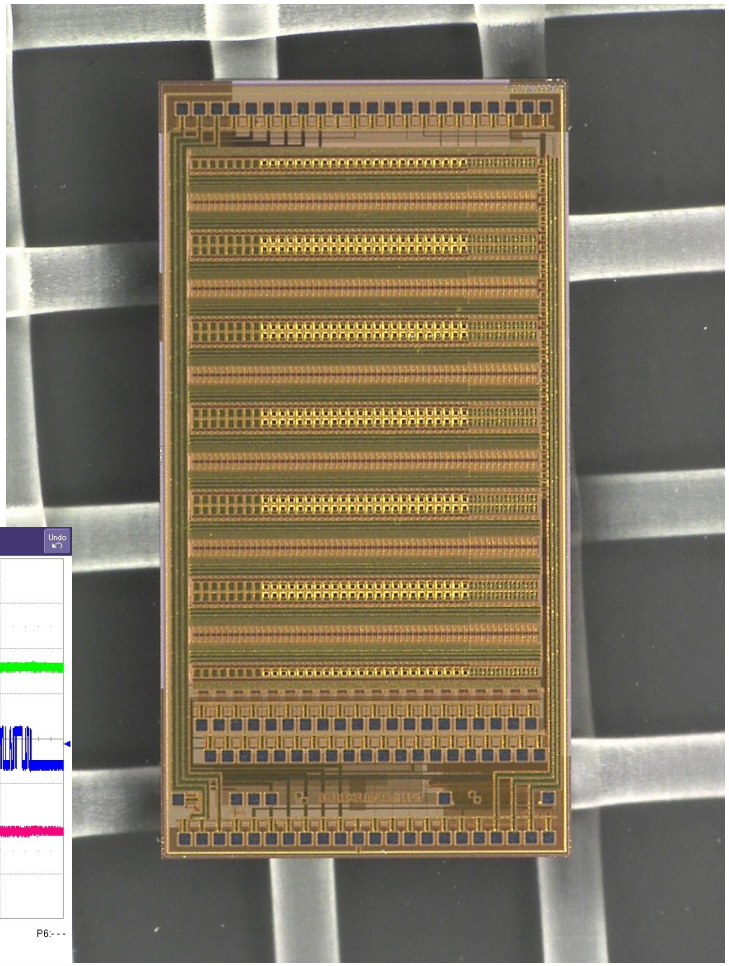
- First irradiations conducted at CERN/PS and with an x-ray tube
  - on special PCB allowing for remote operation, HV2FEI4 powered and read-out during irradiation
- clear radiation effects seen after proton and x-ray irradiation
  - drop in amplitude/amplification
  - also seen with test pulser input → electronics effect, rad-soft design

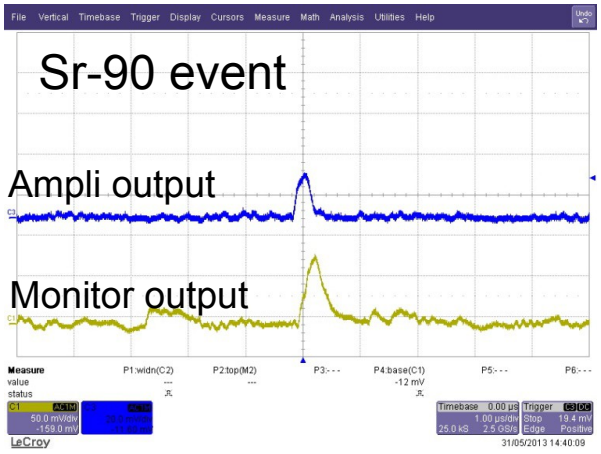


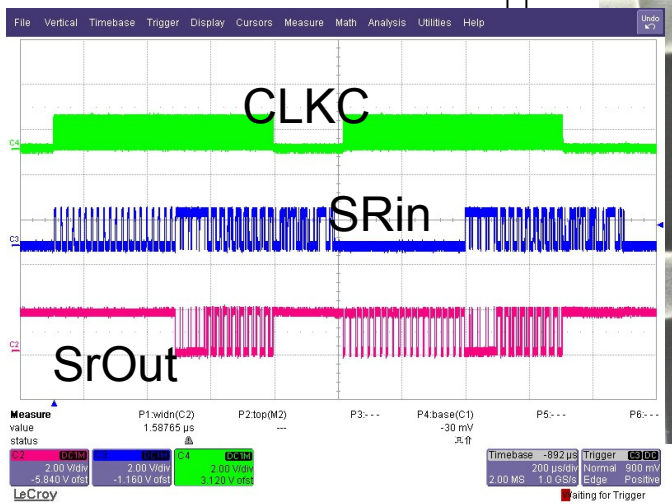
Rad-hardness: consequences

- deliberately chose “standard” design to see how far it would get
  - not far enough... → “harden” design by guard rings, circular transistors, …
- HV2FEI4_v2 was submitted in November and received in April





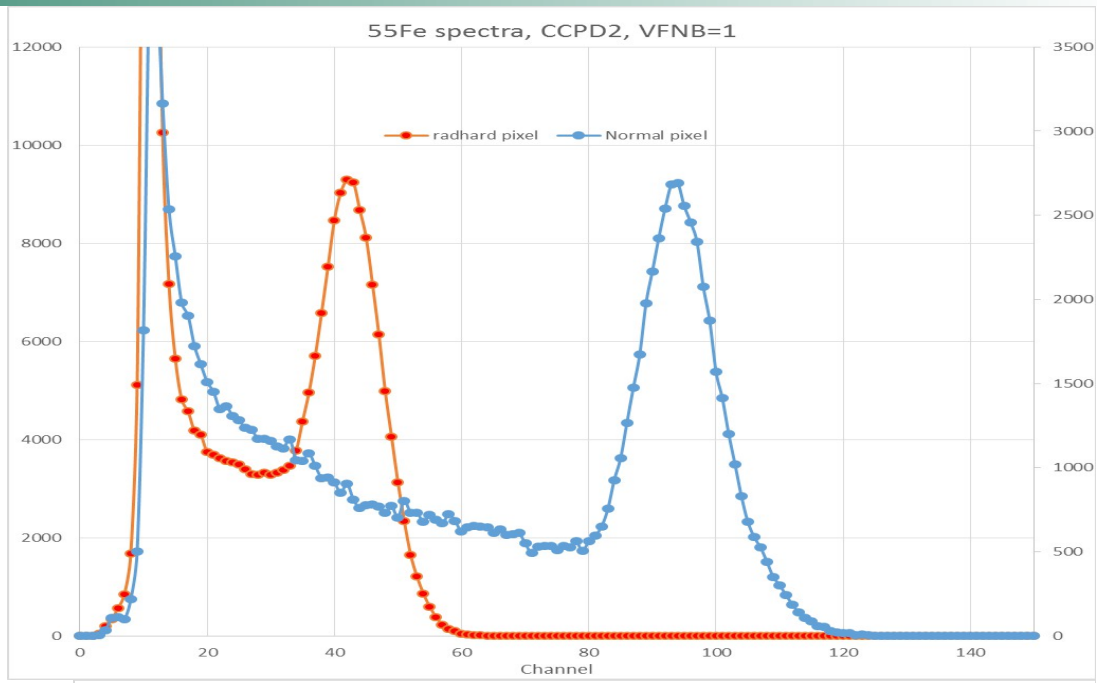


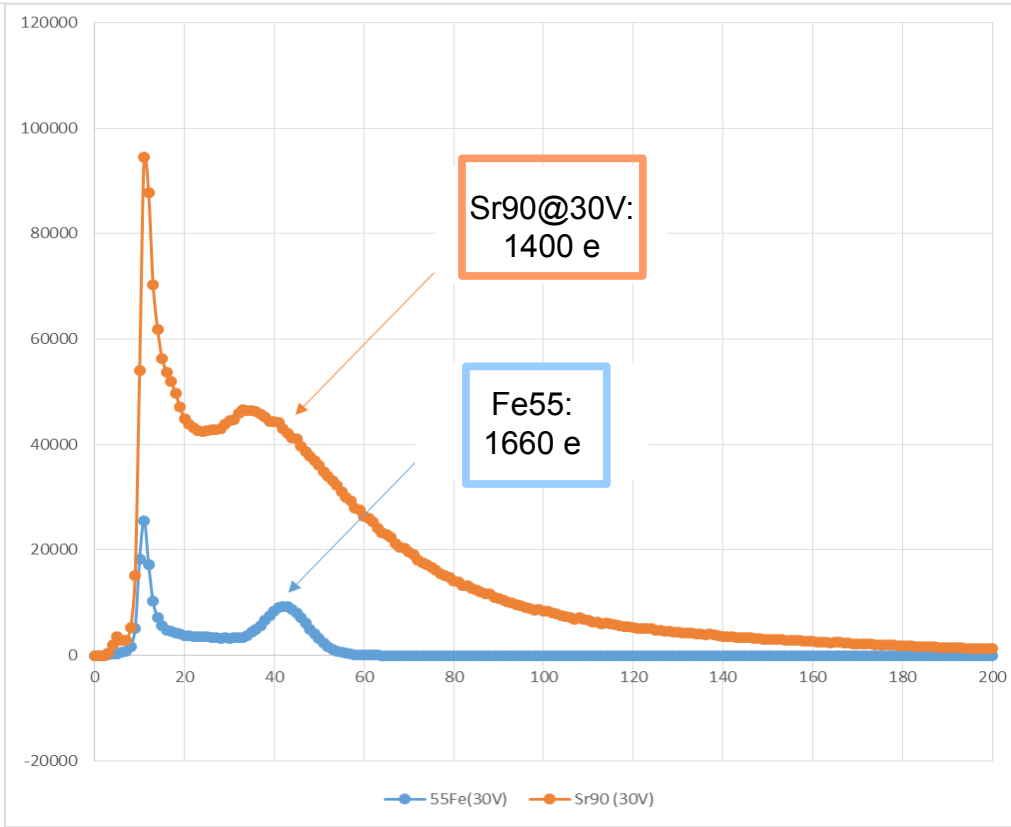


HV-CMOS

HV2FEI4_v2

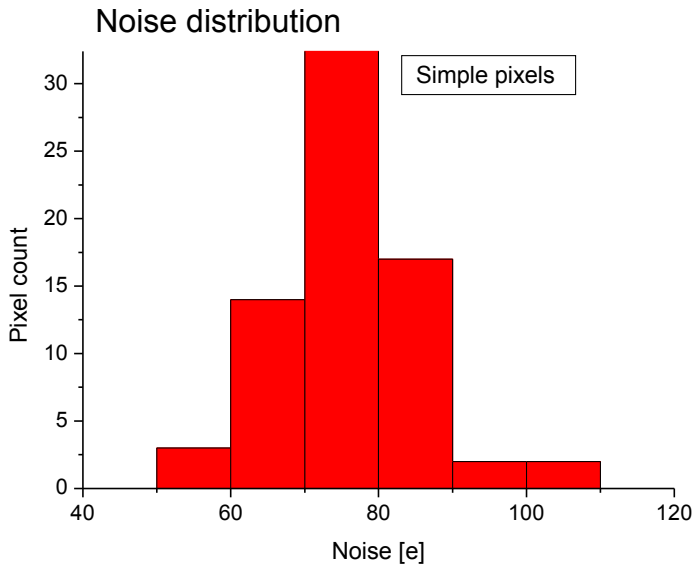
- Circuits generally optimised for rad-hardness, but 2 different designs tested:
  - "normal pixels": mainly added guard rings around transistors
  - "rad-hard pixels": all relevant transistors circular
    → more capacitance, lower gain at identical settings
- More measurements:
  - Sr-90 at 30V now at ~1400e

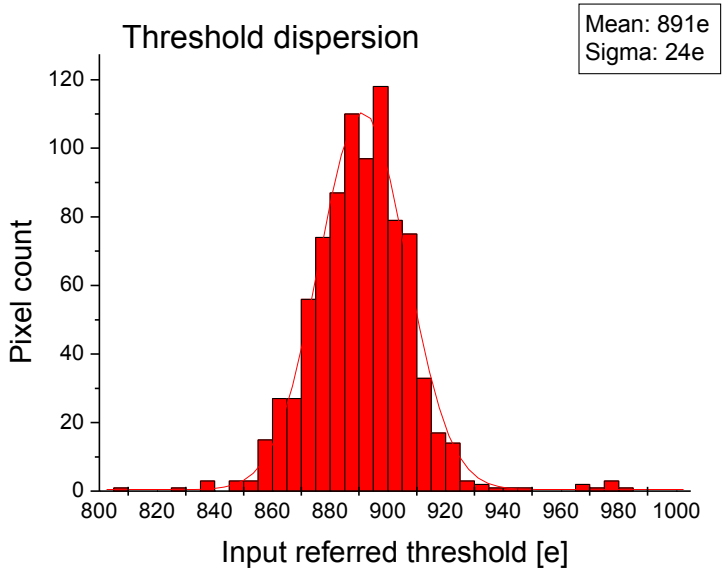


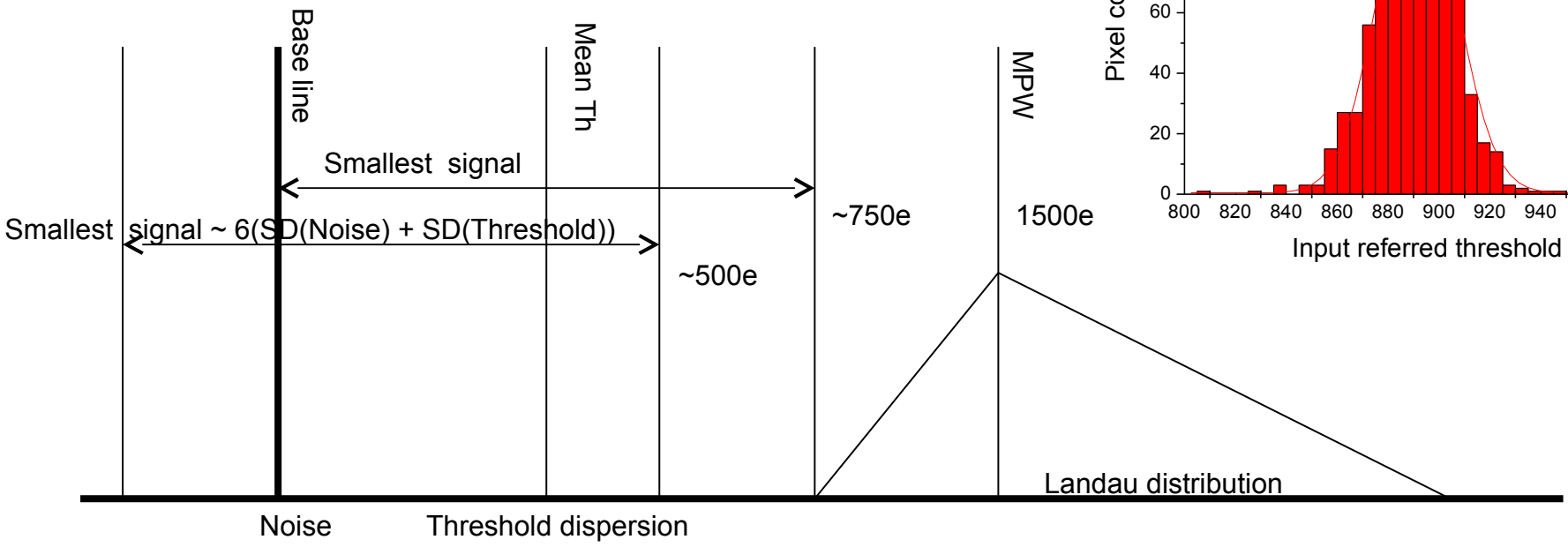


HV2FEI4_v2

- Noise inferred from threshold scan, now around 75e$^-$
- Threshold tuning implemented, threshold dispersion ~25e$^-$
- Fundamentally, the treshold is required to be lower than low energy end of the MIP landau
  - usually MPW/2 is specified
  - looks promising, but still work to do



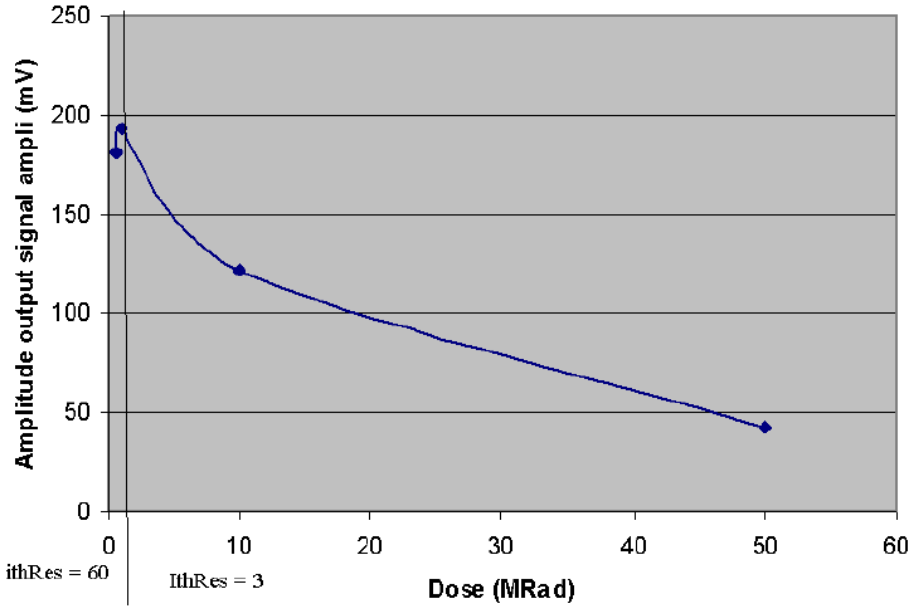




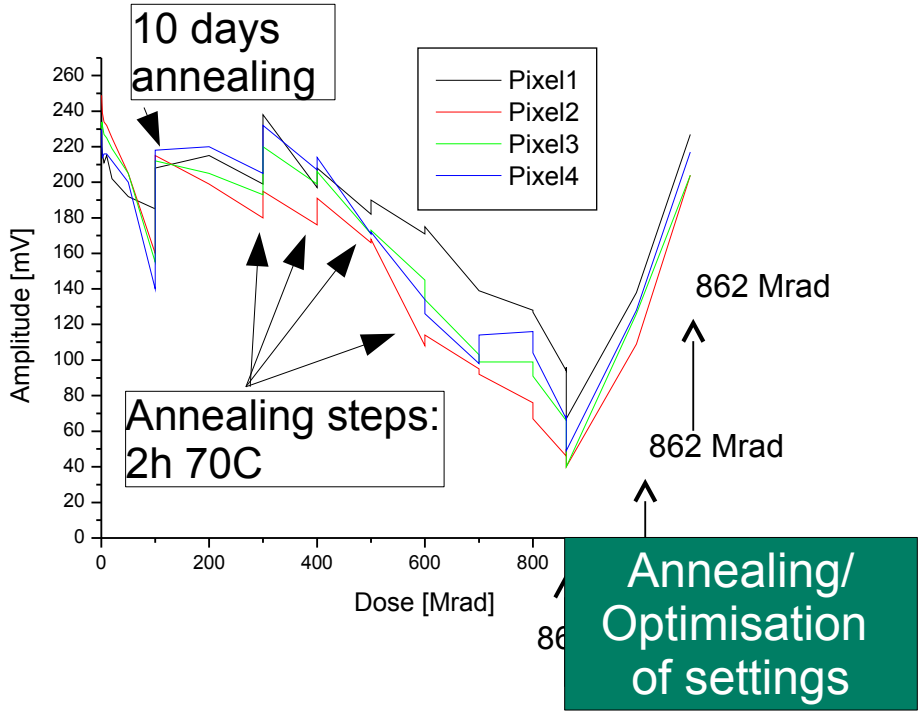
HV2FEI4_v2: rad-hardness

- Radiation effects due to dose, could be reproduced by x-ray irradiation
  - CERN PS currently down, but x-ray tube available
  - very fast irradiation, requires annealing to be mimic realistic dose rate
- Signal amplitude clearly much more stable
  - irradiated up to 862 Mrad (!), drop visible after ~500 MRad
    - dose rate effect, annealing brings signal back to ~100%

➔ rad-hardness significantly improved, hadron irradiations to follow



CCPD1 irradiated with x-rays
Amplifier gain loss

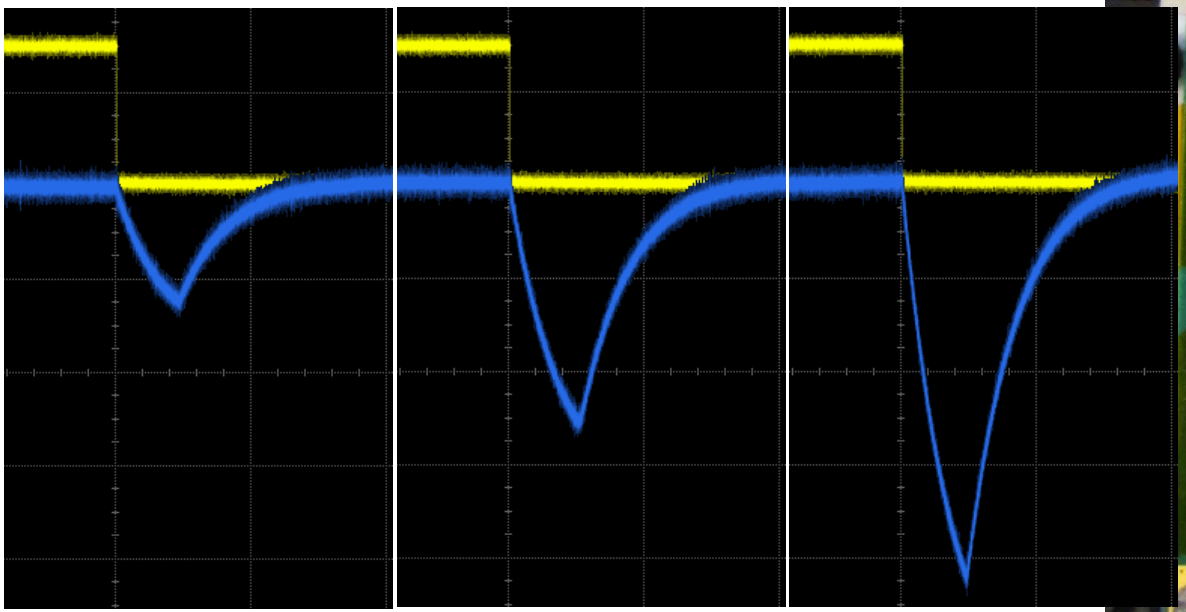


CCPD2 irradiated with x-rays
Amplifier gain loss
Rad hard pixels

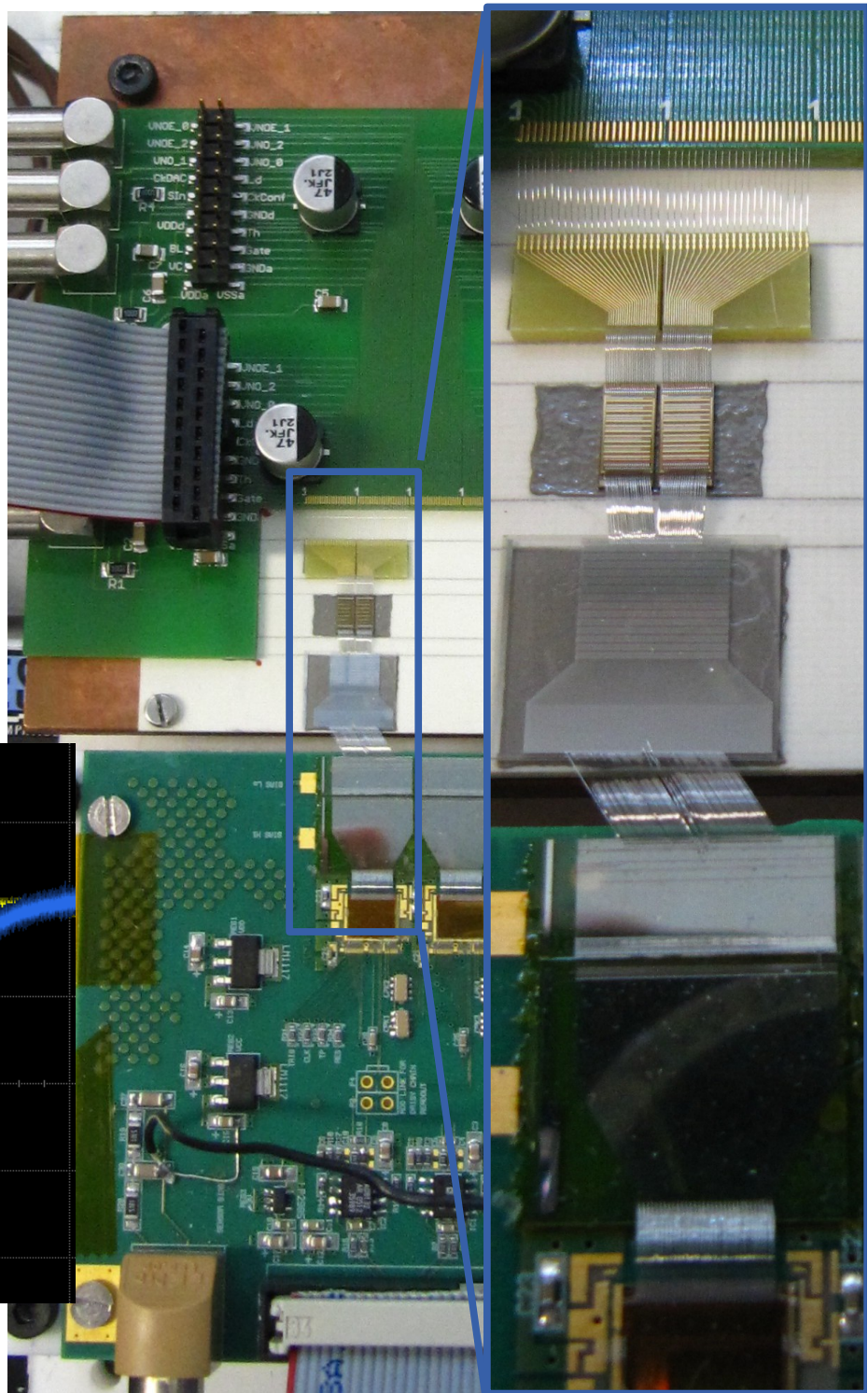
HV-CMOS

HV2FEI4: strip readout

- Beetle/Alibava readout had issues with noise/common mode pickup
- configuration worked, “strips” could be switched on/off
- however, position-encoding works:
  - monitor output on scope
  - same principle on strip readout pads
- Supply PCB design changed
  - threshold now at reasonable values

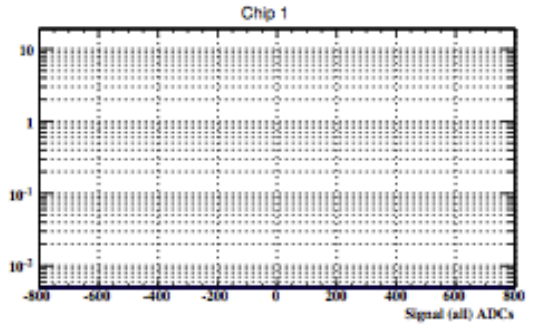


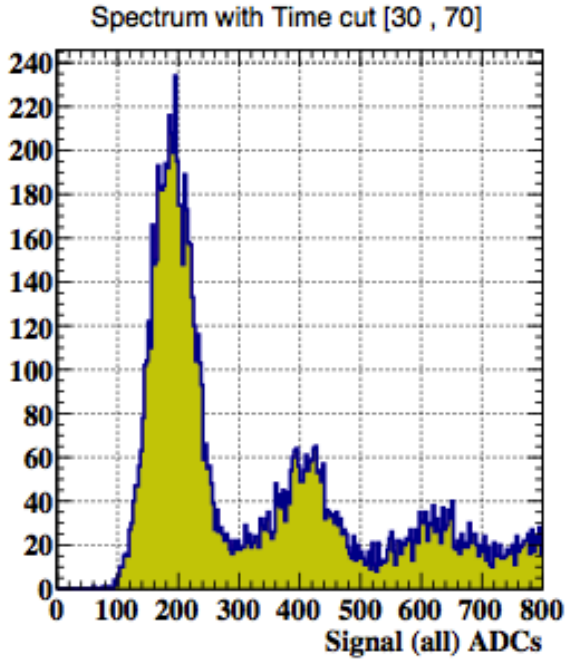
Row 0 Row 12 Row 23

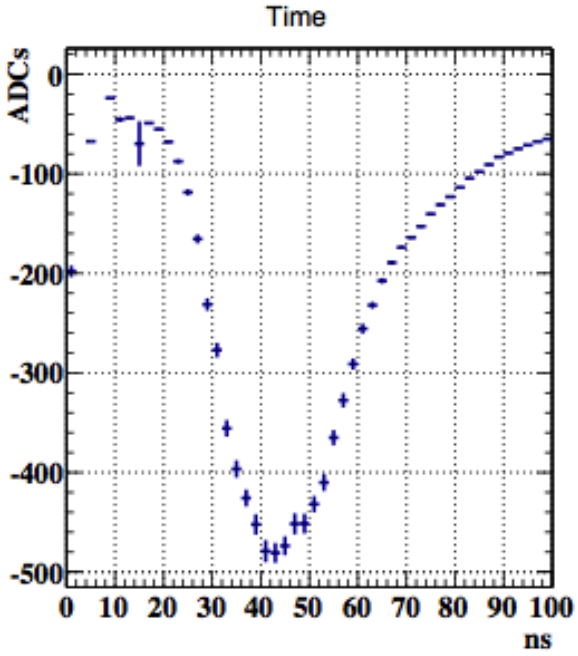


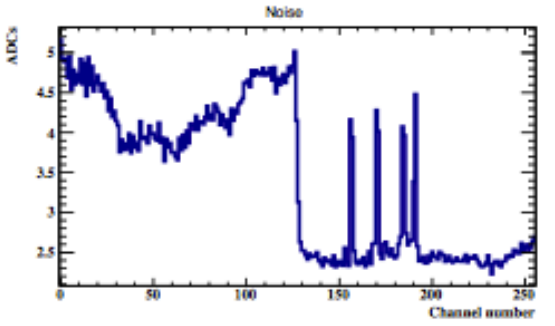
HV2FEI4: strip readout

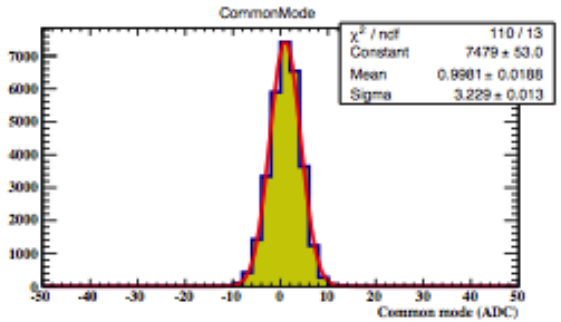
- First results with Alibava readout
- Signals too large → strange effects
- Working on offline-analysis taking into account all HVMCOS specifics





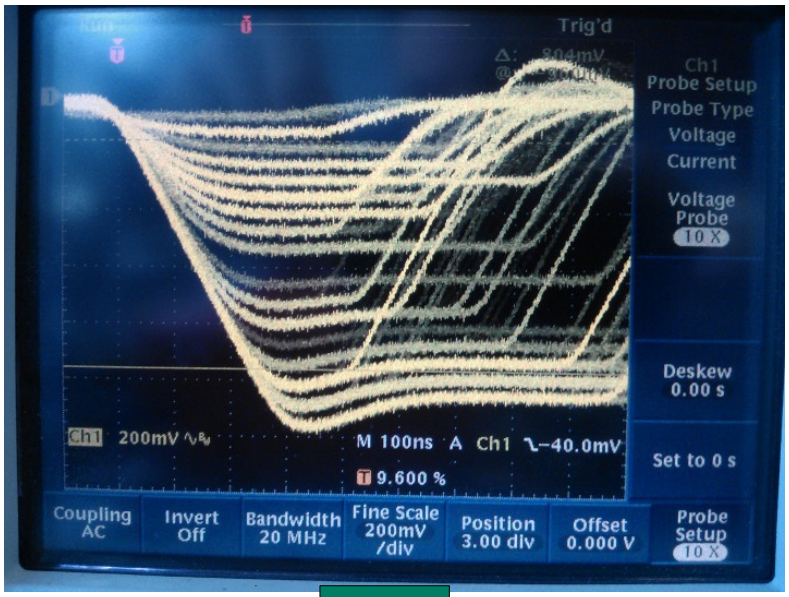


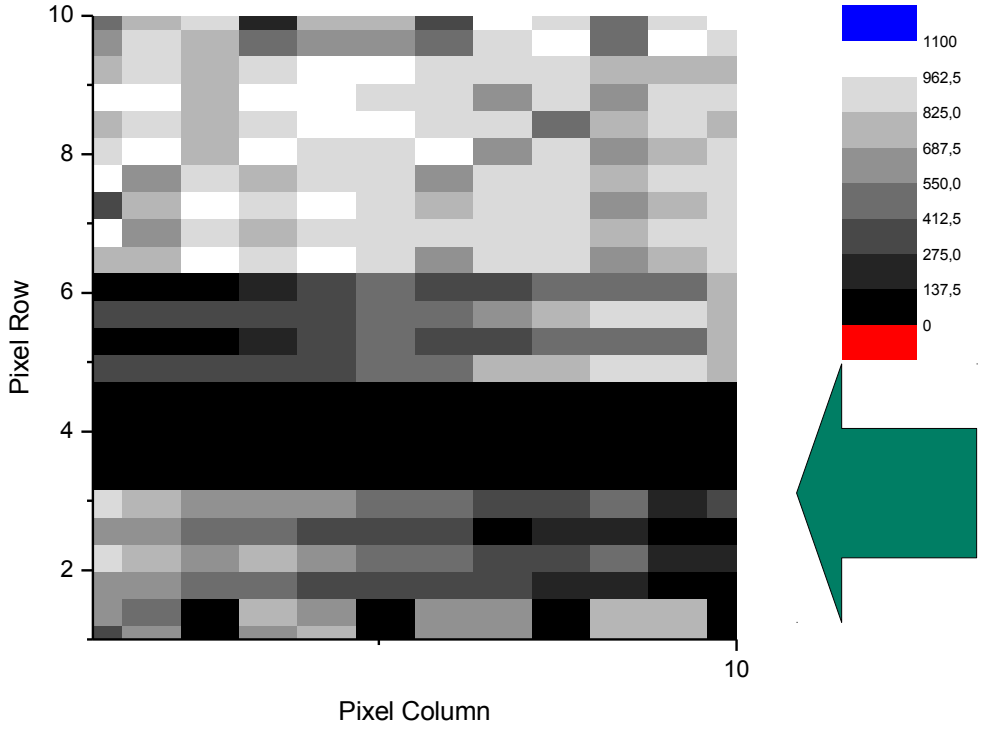


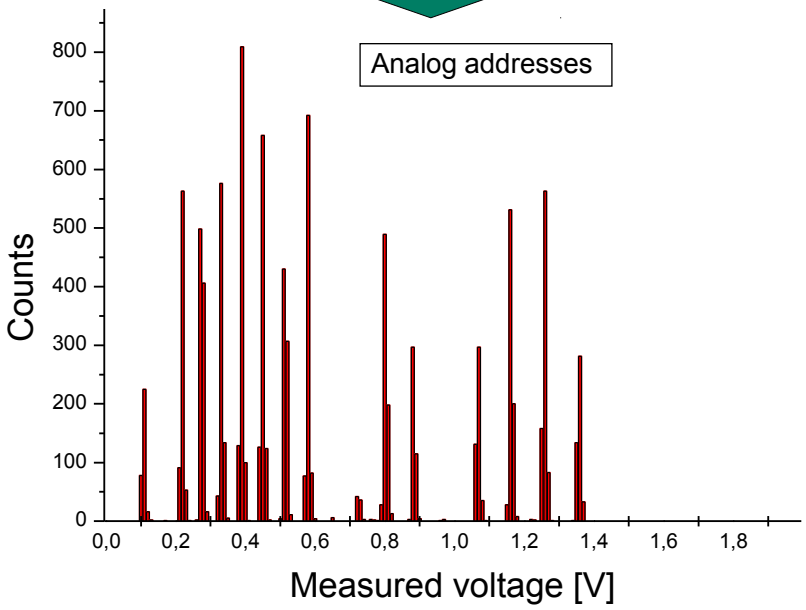


HV2FEI4_v2: strip performance

- First measurements again using an oscilloscope
- Fe-55 source illuminating a wire
  - shadow ~visible in pulse heights
  - can be decoded to give a pixel hitmap using only strip information



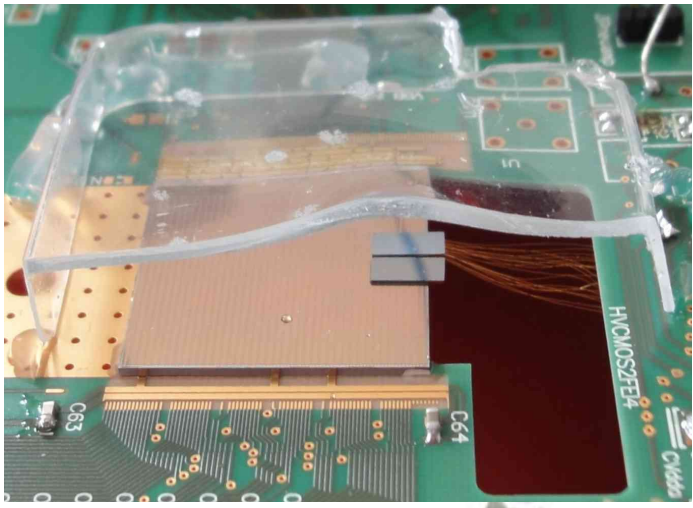


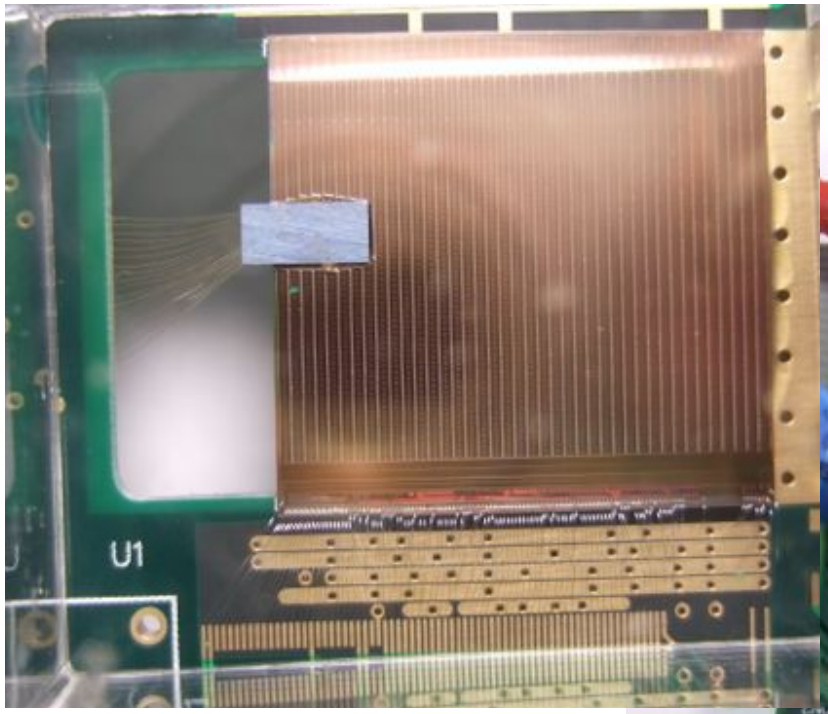


HV-CMOS

HV2FEI4: Pixel readout

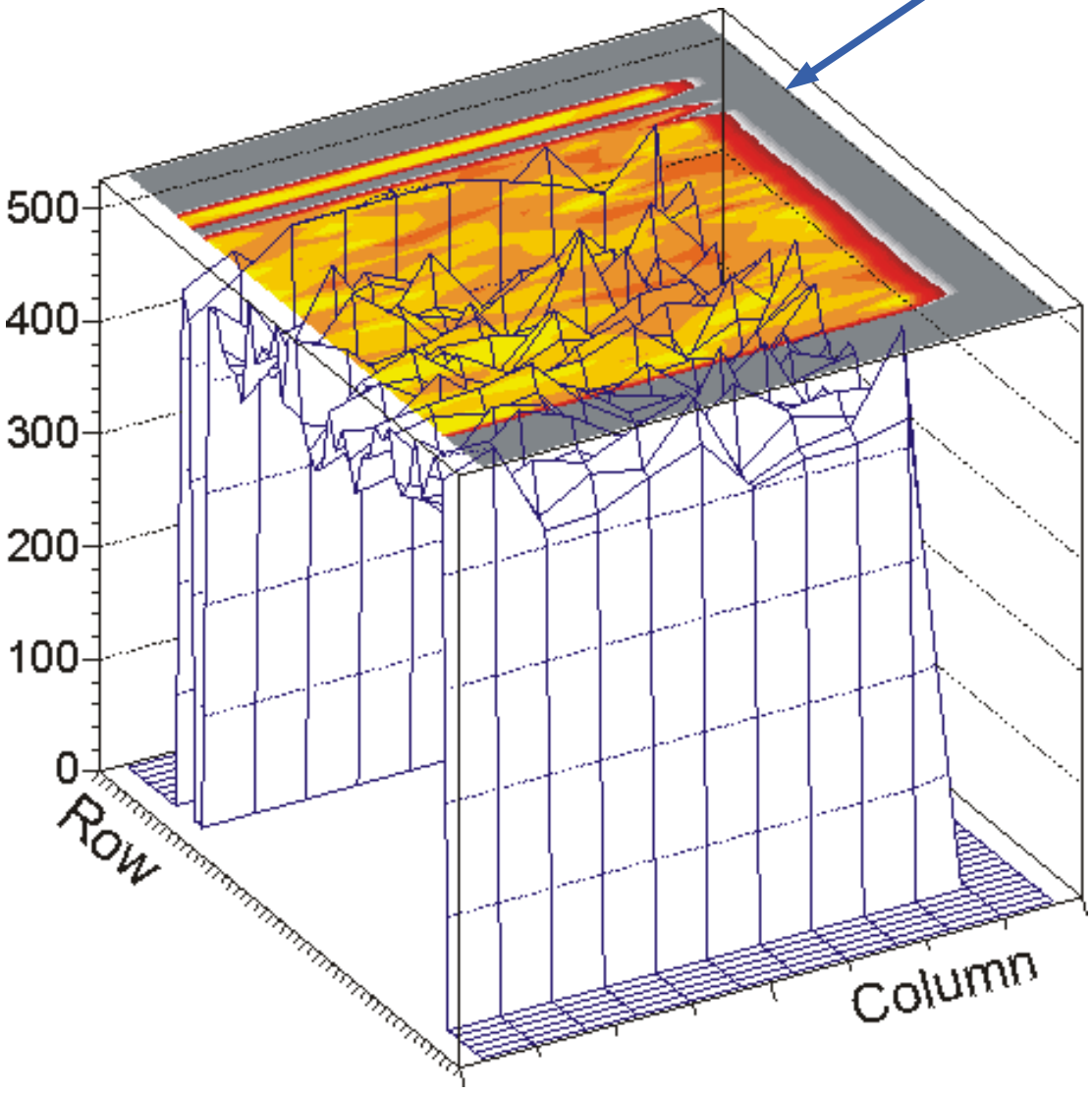
- Several HV2FEI4s glued to FE-I4A and FE-I4B
- HV2FEI4 wirebonds done through hole in PCB
  - could be bumps or TSVs later

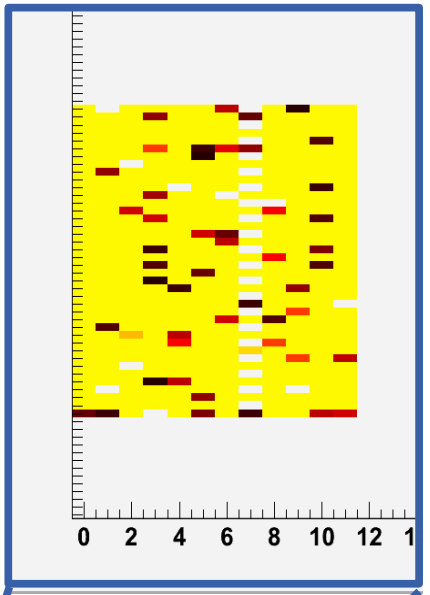


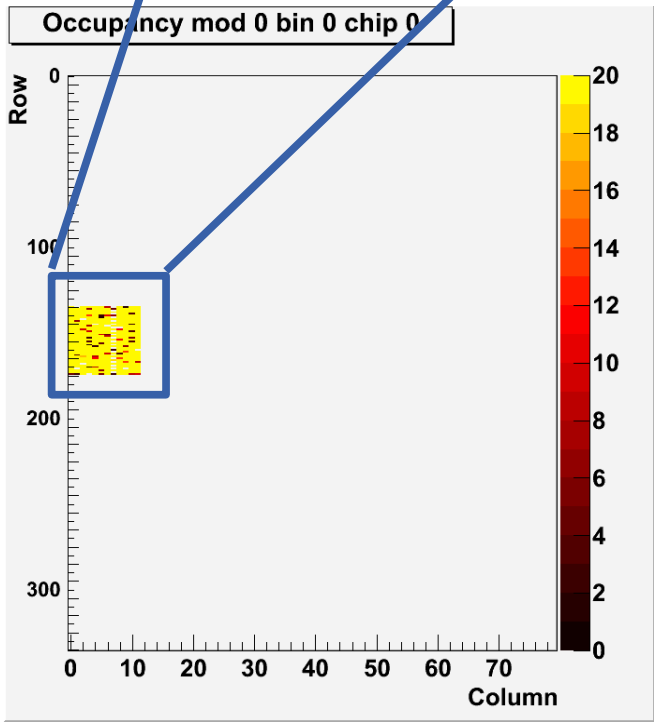


HV2FEI4: Pixel readout

- First measurements:
  - FE-I4A (w/ bumps) sees HV2FEI4 being glued to it
  - Physics (^{22}Na source) is seen by FE-I4B (w/o bumps)

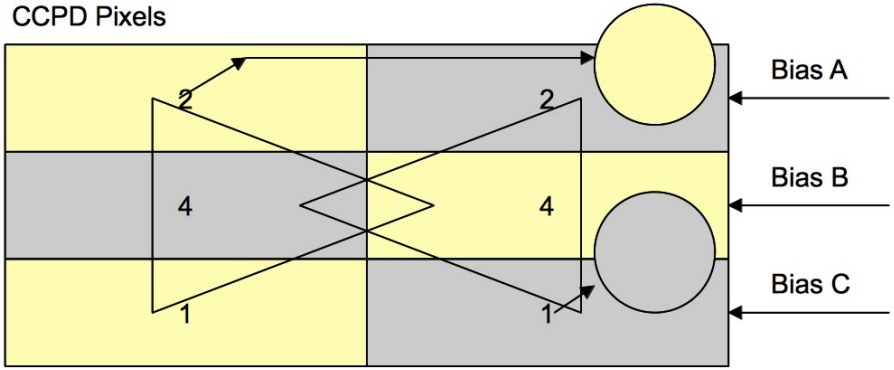




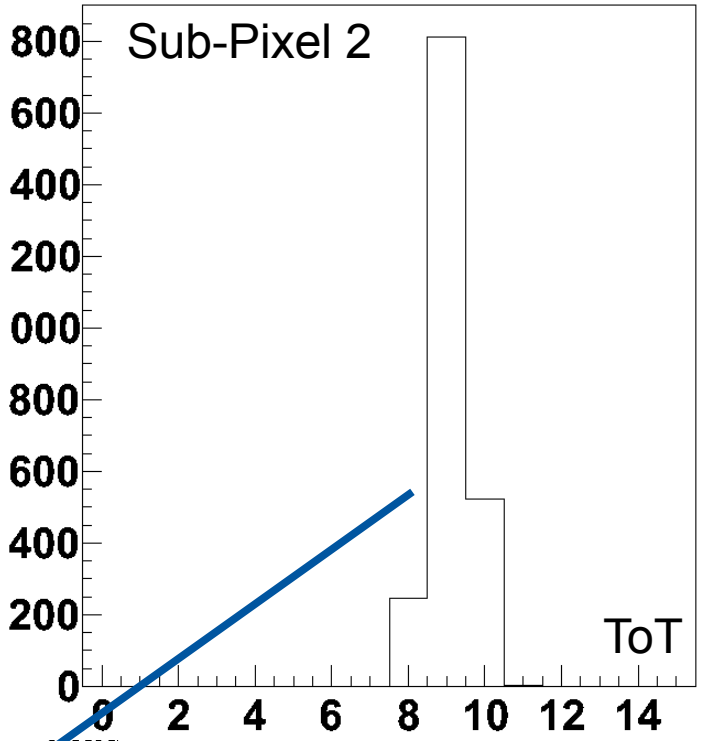


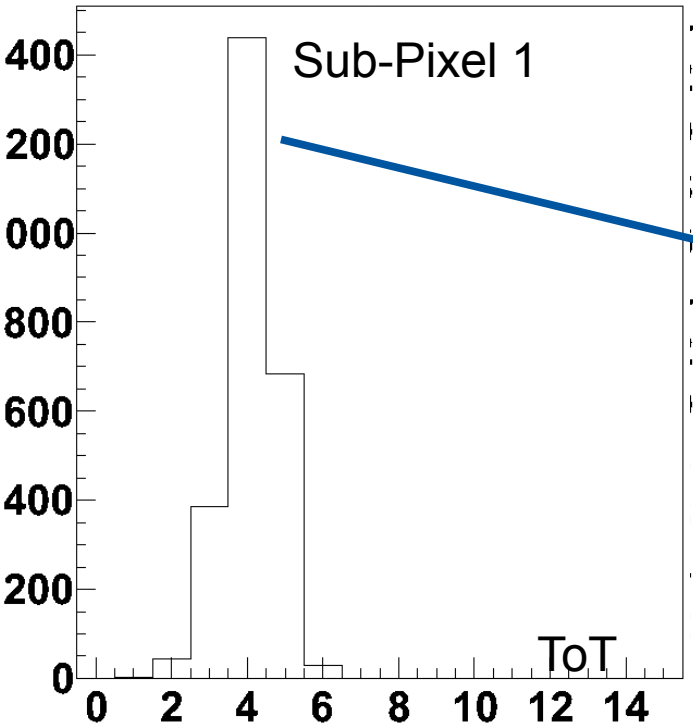
HV2FEI4: Pixel readout

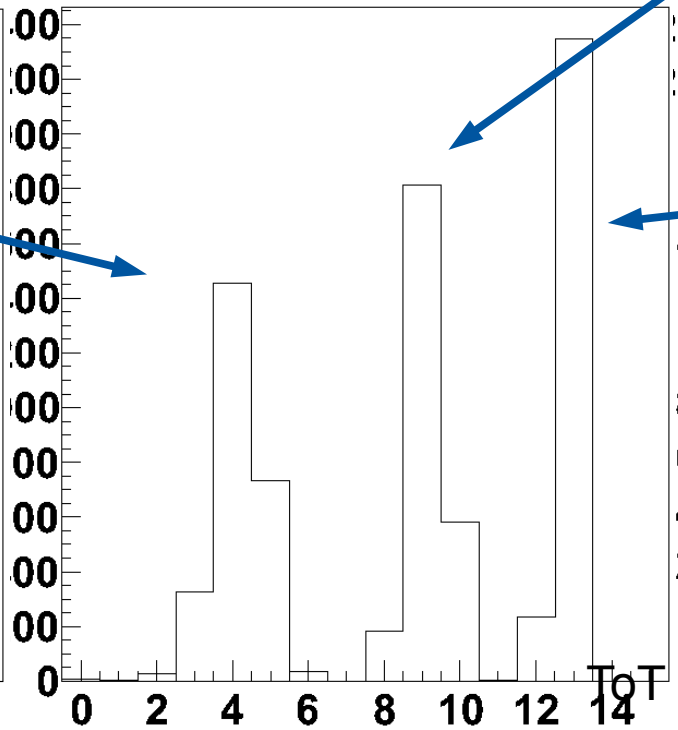
- ToT encoding:
  - 3 sub-pixels clearly distinguishable
    → sub-pixel encoding works!
  - to do: dynamic range matching, array tuning

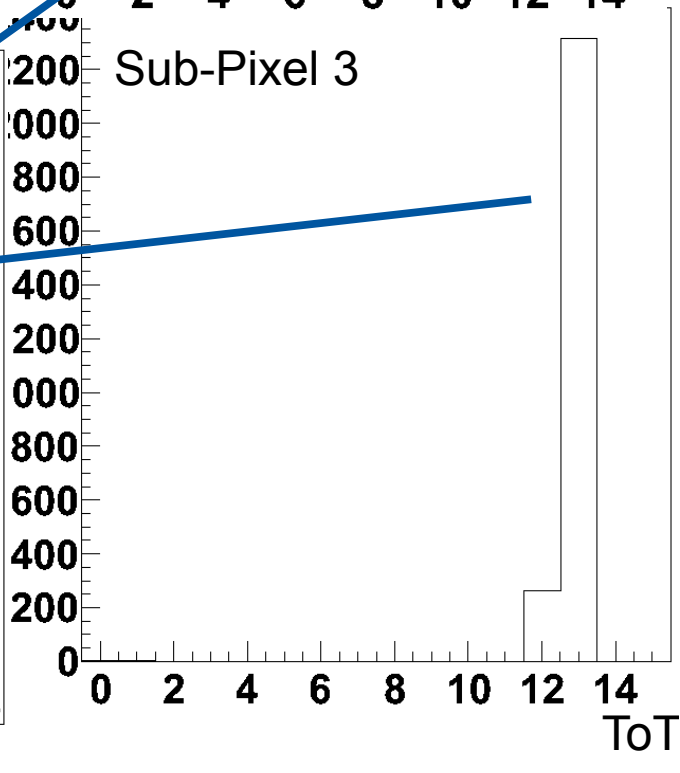


All on



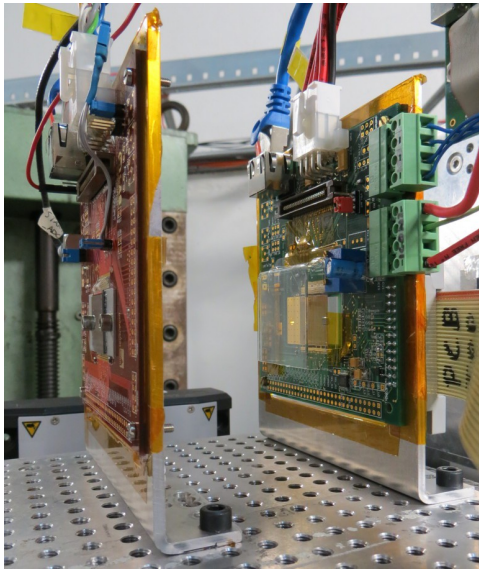


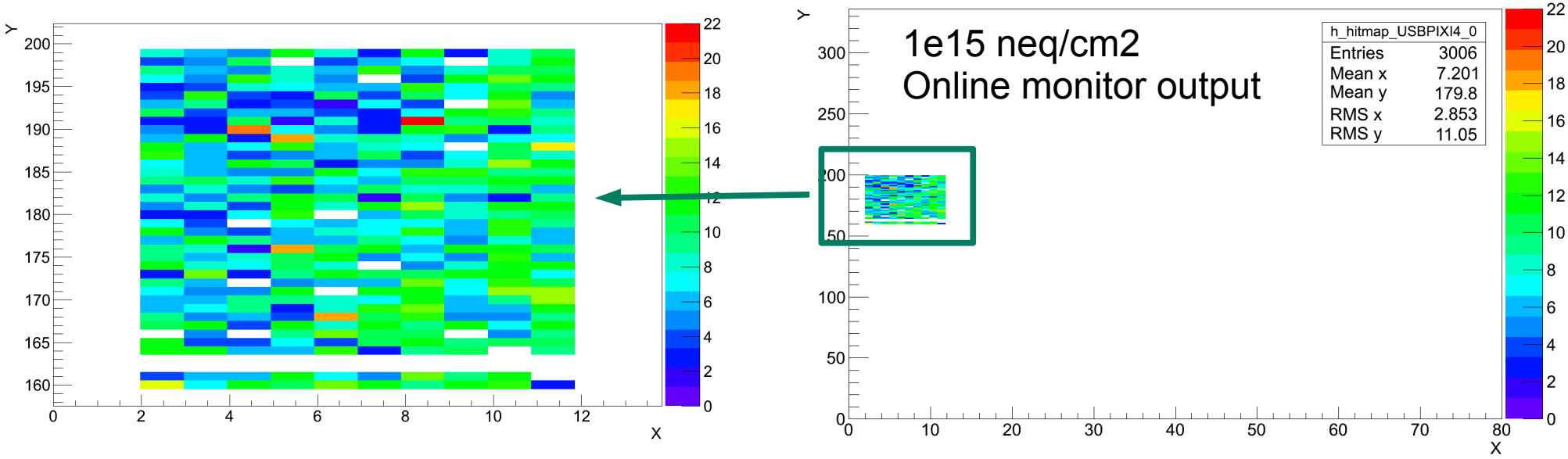




HV2FEI4: Pixel readout in testbeam

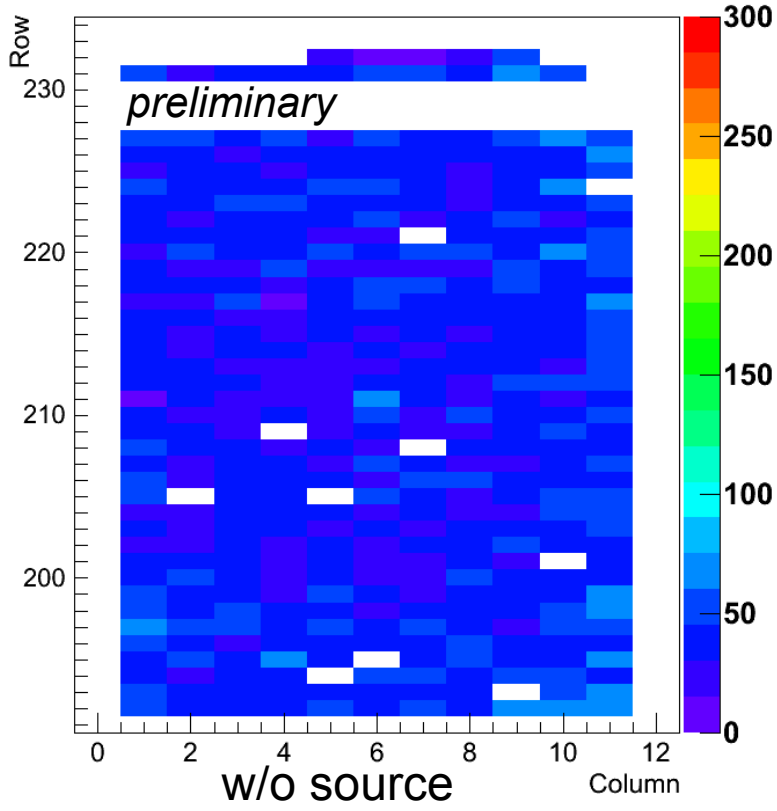
- First data taken at DESY testbeam in August
  - unirradiated and reactor neutron (JSI) irradiated devices: 1e15, 1e16 neq/cm2
- Issues with DUT data stream merging, reconstruction efforts still ongoing
- Nevertheless, clear evidence
  - HV-CMOS also works in “hostile” testbeam environment
  - unirradiated and 1e15 neq/cm2 sample yield similar rates (even w/o cooling!)
    - indication(!) for reasonable efficiency at 60V and after full strip fluence
    - noise still around ~80e$^-$
  - 1e16 sample sees increased, but low rate with beam

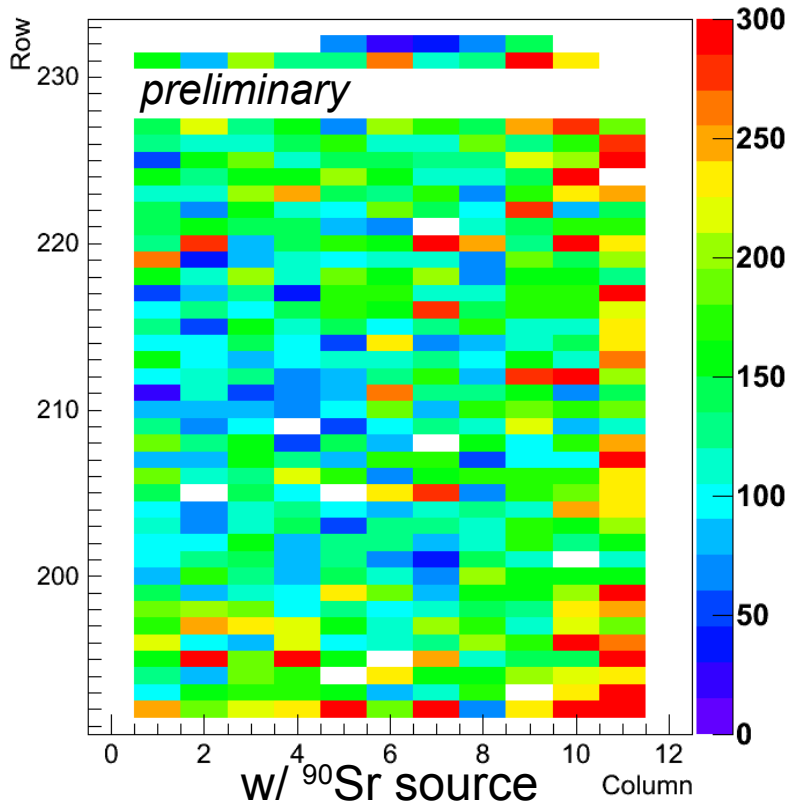




n-irradiated behaviour: 1e16 n_{eq}/cm^2

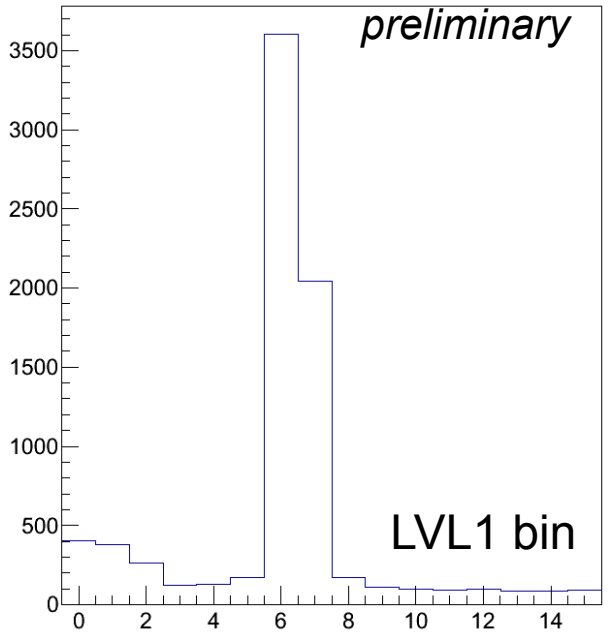
- irradiation done at JSI Ljubljana w/o biasing, low TID
- up to now measurements at room temperature (!)
- following measurements with (only) -20V to -25V bias voltage
- noise at RT ~280 e^- → rather high threshold (uncalibrated) necessary to obtain a noise occupancy of ~10^{-10}
- below: about ~10 minutes exposure, self-trigger (!) source scan with and without ^{90}Sr source

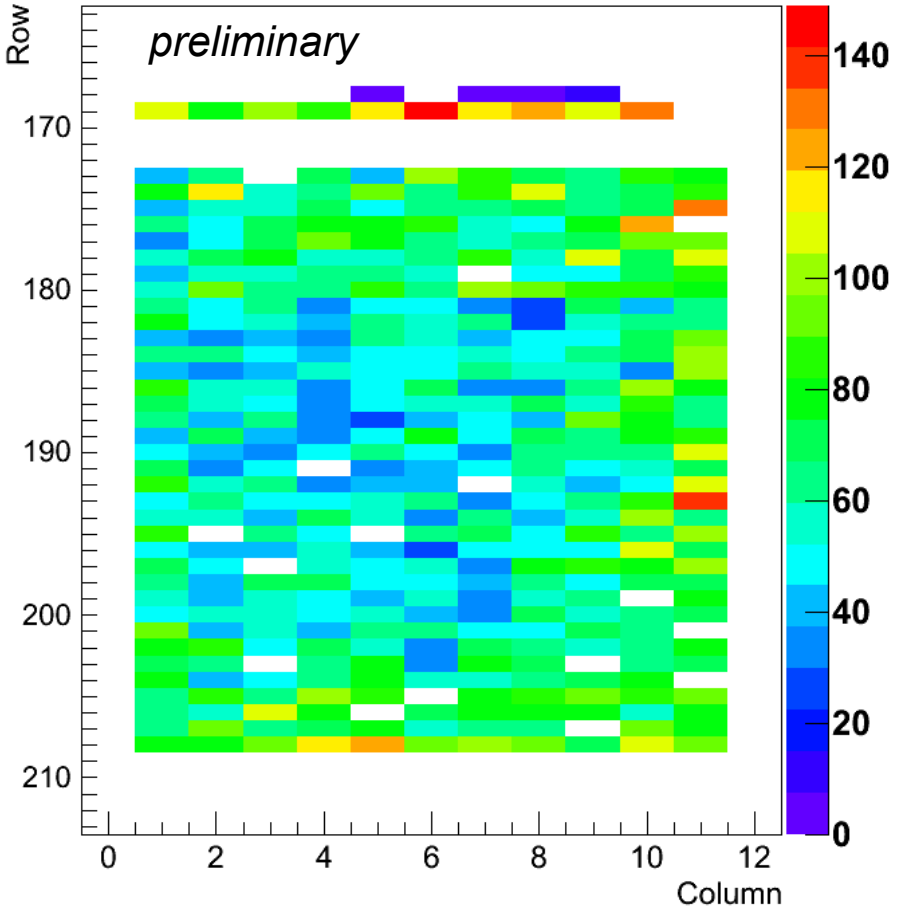


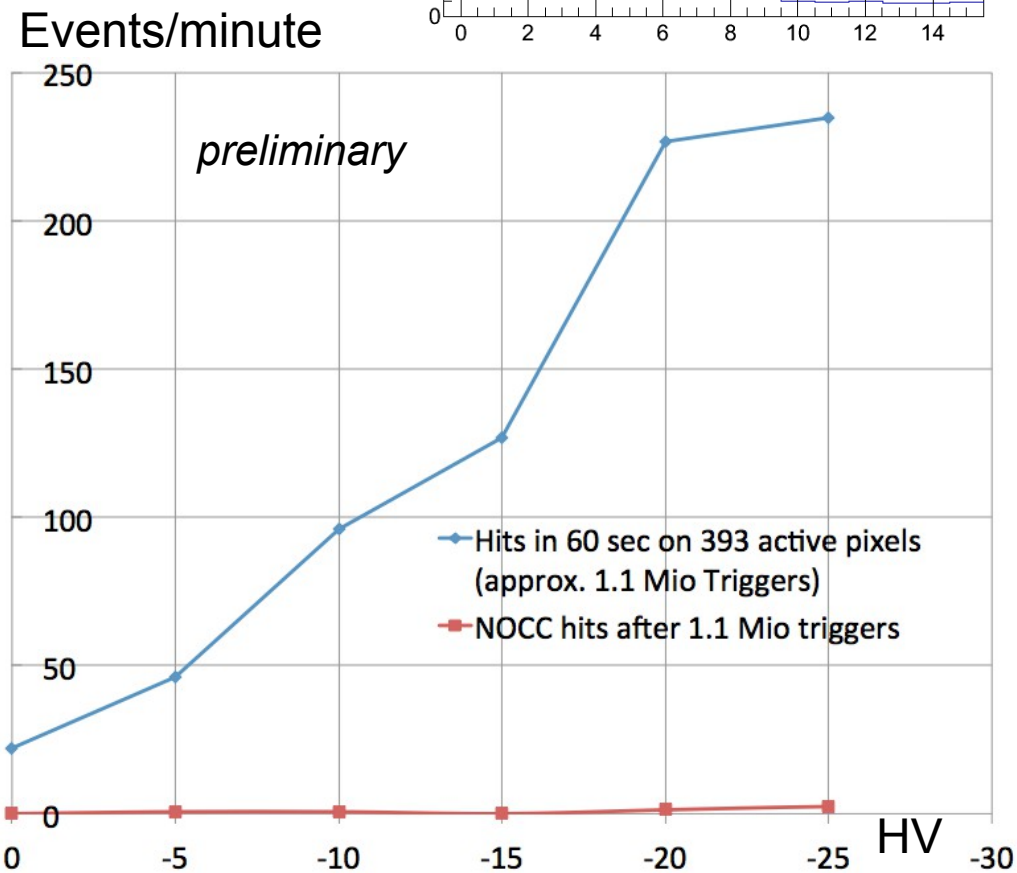


Irradiated behaviour: 1e16 n_{eq}/cm^2

- measurements with scintillator trigger
  - makes sure we select MIP-like electrons
  - avoids “noise” triggers
  - rate rises with HV as expected, but (rate) saturation not yet seen → go higher in HV, cool
- next steps: calibration, cooled operation





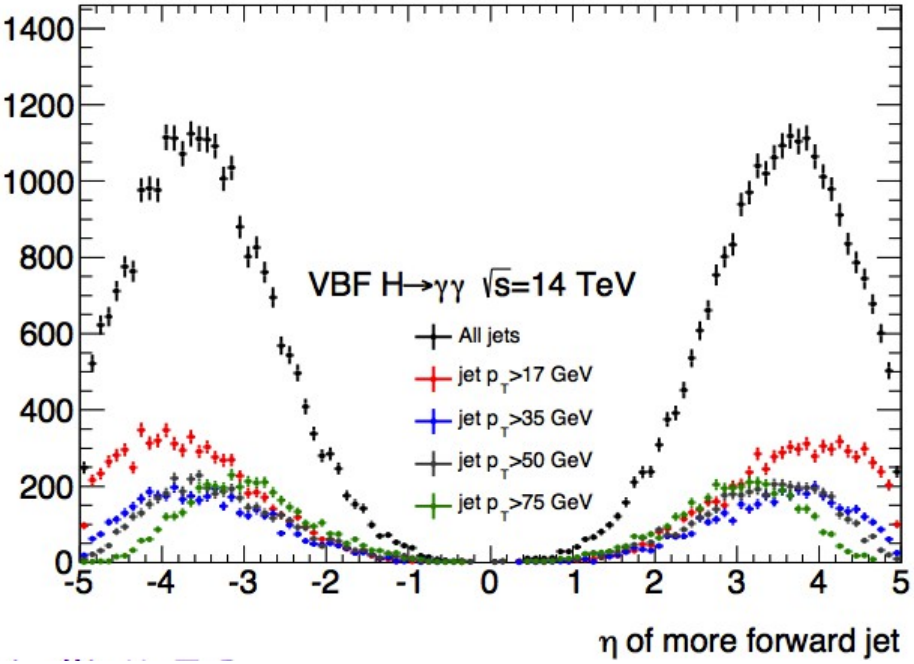


Future plans

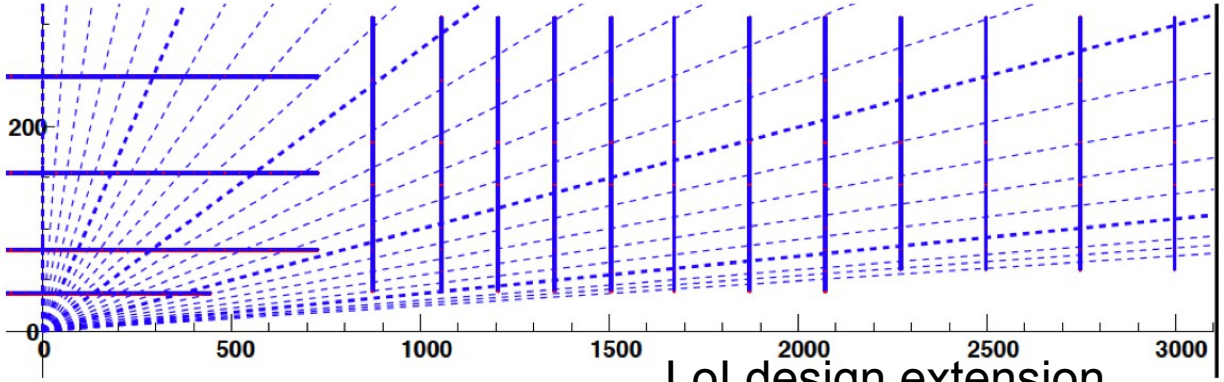
- USBPix is being modified to enable configuration only with USBPix/STControl
  - makes implementation of scans much easier
  - will probably enable sub-pixel disentanglement for the whole matrix without the need for pixel-by-pixel analysis
- further submissions are being discussed
  - one ATLAS/CLIC submission in November
    - array of 25x25 µm pixels for the CLICpix demonstrator (only preamps)
    - in addition 6 different versions of rad-hard pixel circuits for trials
    - some R&D structures: direct n-well access for eTCT, test transistors, …
    - for comparison: area only 2.3x2.8mm, cost ~6.5 kEUR
  - dedicated to strip readout
    - optimised sub-strip pitch (50 µm? 25 µm?) in combination with z-resolution
  - dedicated to disks
    - square pixels preferred
    - 50x50 µm should be achievable with FE-I4
    - sensor candidate for “standard disks” and for very forward tracking

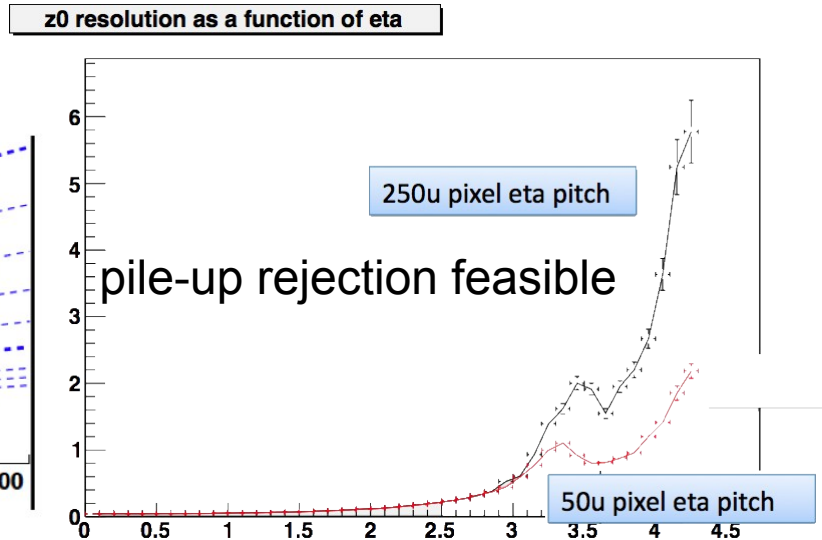
Case study: Very forward tracking

- Limitation to pseudorapidity of eta = 2.5 inappropriate wrt VBF/VBS
- Design studies ongoing for an extension to eta~4 (phase 2 upgrade)
  - physics: Higgs self-coupling, vector boson scattering
  - layout: acceptable area increase
  - sensor challenges: mass production, rad-hardness at small radii, square pixels/small eta pitch preferred → HV-CMOS?



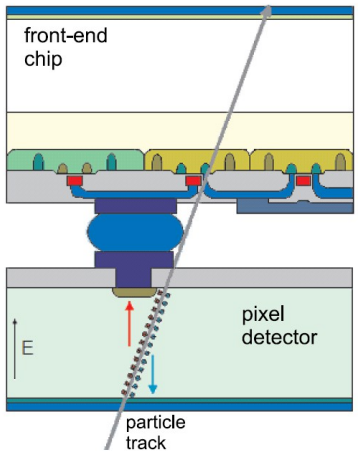
HV-CMOS



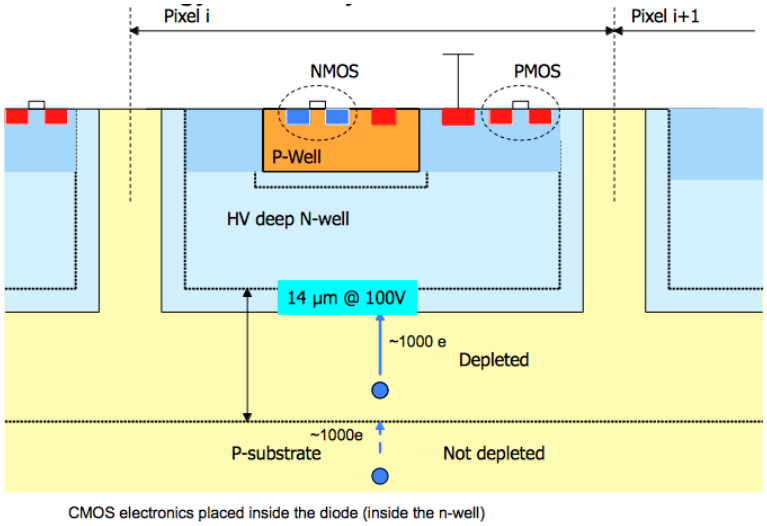


HR-CMOS

- As mentioned, main requirement for drift-based MAPS is a deep n-well
- Higher substrate resistivity would allow for full depletion
  - certainly larger initial signal, reduction of depletion depth to be studied
  - charge sharing possible again allowing to higher resolution at low fluences
- Several CMOS imager processes available from different foundries
  - back-side illumination requires full depletion and thin sensors
  - high-resistivity FZ base material available in an industrialised process
- First HR-CMOS efforts started at University of Bonn

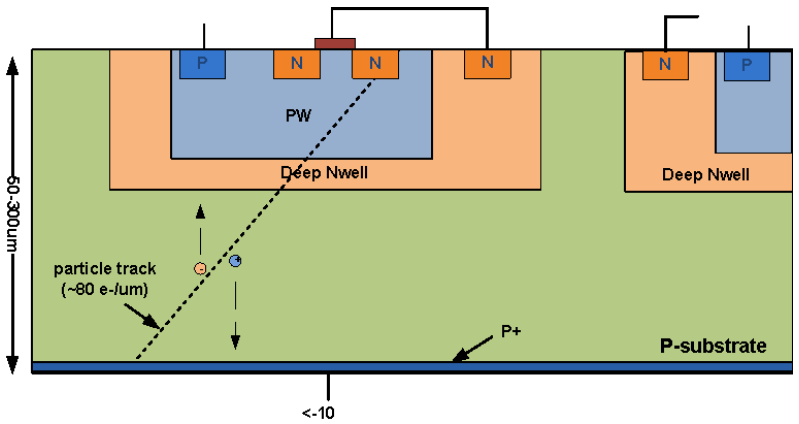


Hybrid



CMOS electronics placed inside the diode (inside the n-well)

HV-CMOS

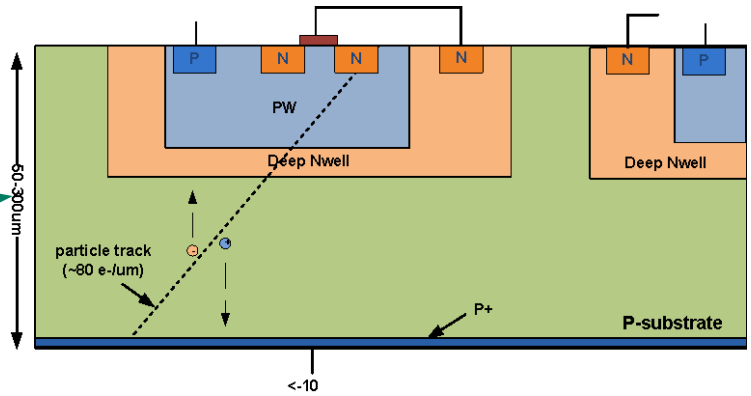


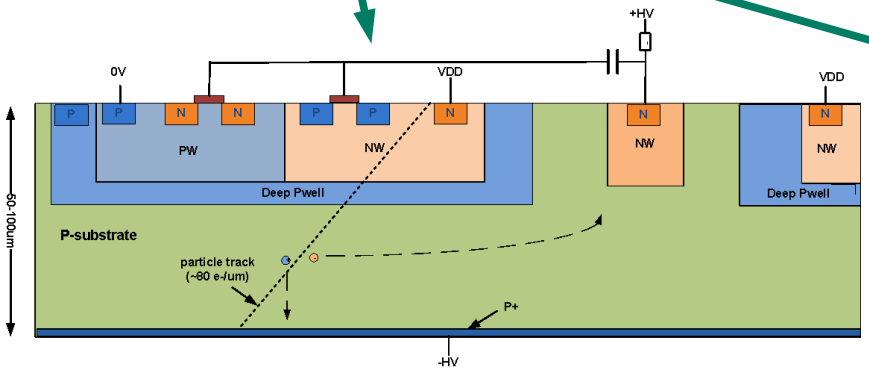
HR-CMOS

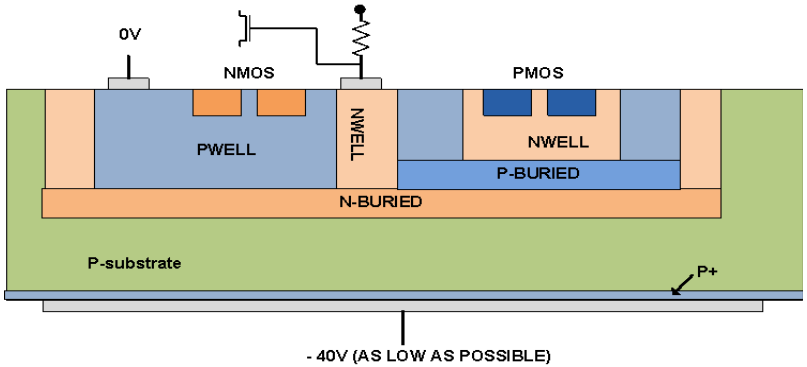
HV-CMOS

HR-CMOS

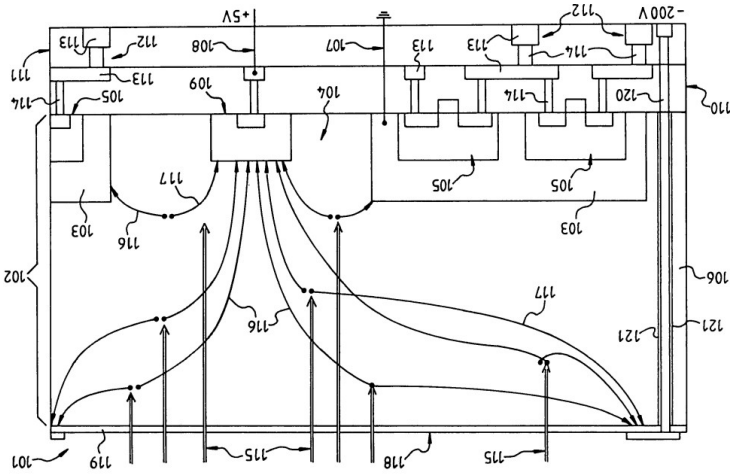
- Many different designs possible:
  - HV-CMOS like (deep n-well, no triple-well)
  - triple-well
  - Alice-like

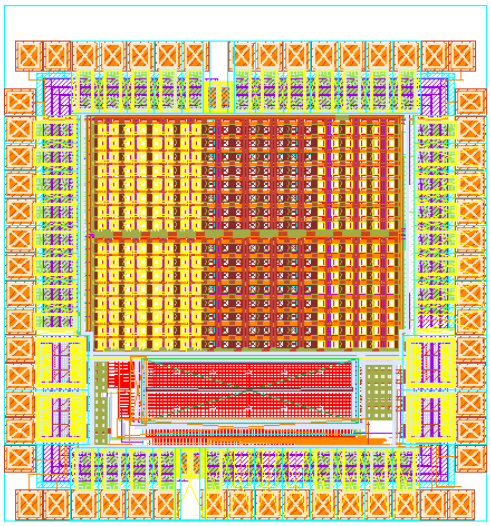


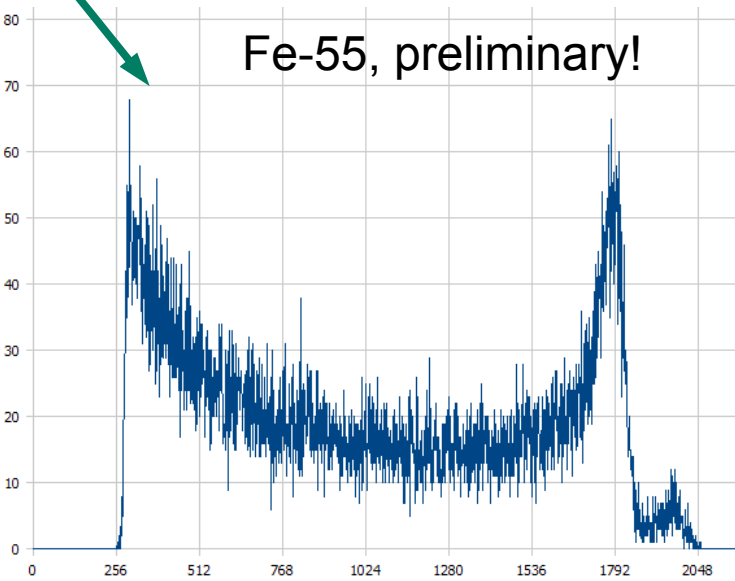




- First prototypes back from ESPROS, see physics
  - characterisation, irradiations to follow







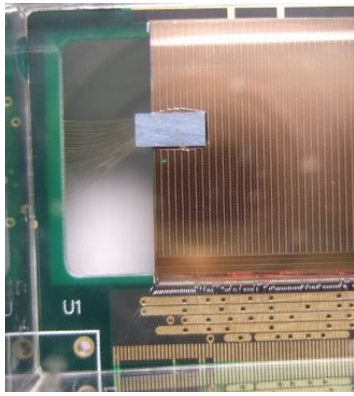
HV-CMOS

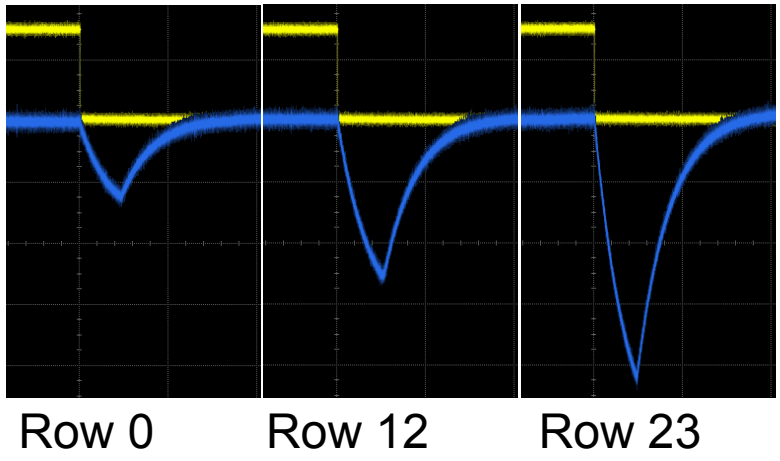
(HV-)CMOS and RD50

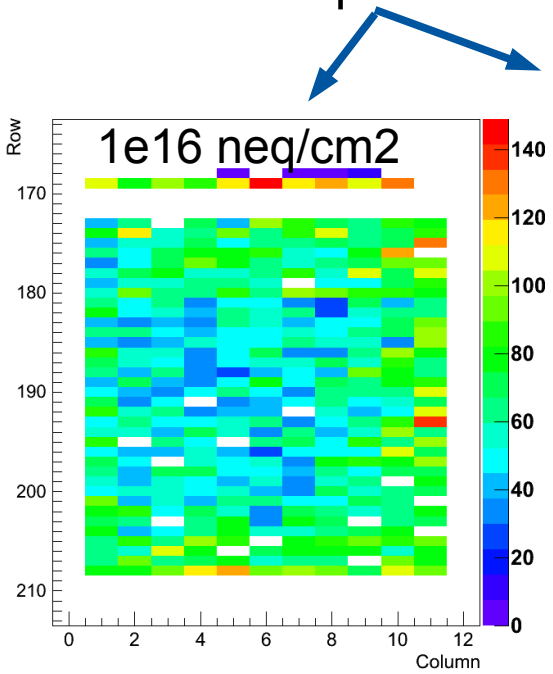
- It has been proposed to cover (HV-)CMOS within RD50
- I'd like to support this idea:
  - CMOS developments up to now driven by chip design institutes
    → lack of bulk (damage) knowledge
  - CMOS sensors are n-in-p pixel sensors, often on Cz substrates
    - quite some background in RD50
  - Many current developments rely on test systems/readout chips/methods well known within the RD50 community
  - Test chip productions well suited for RD50
    - fast turnaround (3-6 months, depending on foundry)
    - small test chips cheap (well below 10kEUR)
    - many flavours to choose from
  - Radiation hardness with hybrid sensors has progressed well, now it might be the time to look into
    - “affordable” solutions (also including low mass)
    - enhanced features: e.g. very fine-pitch, data reduction for industrial-pitch bump-bonding, …

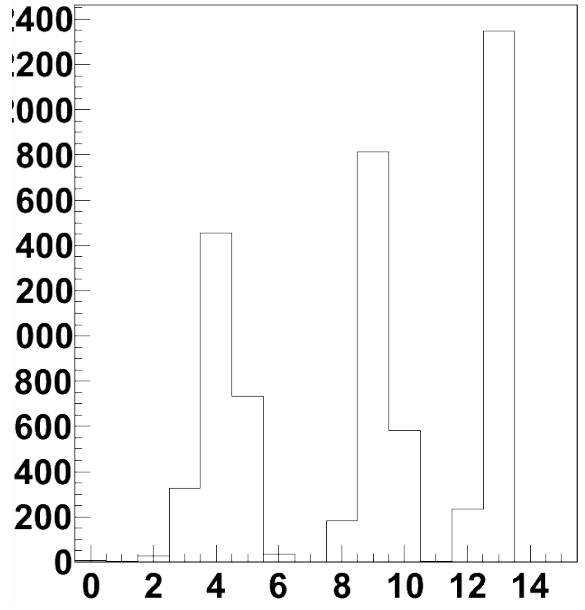
Conclusions

- HV/HR-CMOS processes might yield radiation-hard, low-cost, improved-resolution, low-bias-voltage, low-mass sensors
- Process can be used for
  - “classical” passive n-in-p sensors
  - 'active' n-in-p sensors (with capacitive coupling)
  - drift-based MAPS chips
- First prototypes being explored
  - very first HR-CMOS measurements encouraging
  - results with capacitively coupled HV-CMOS pixel sensors look promising
  - “virtual” strip sensors – z-position encoding works







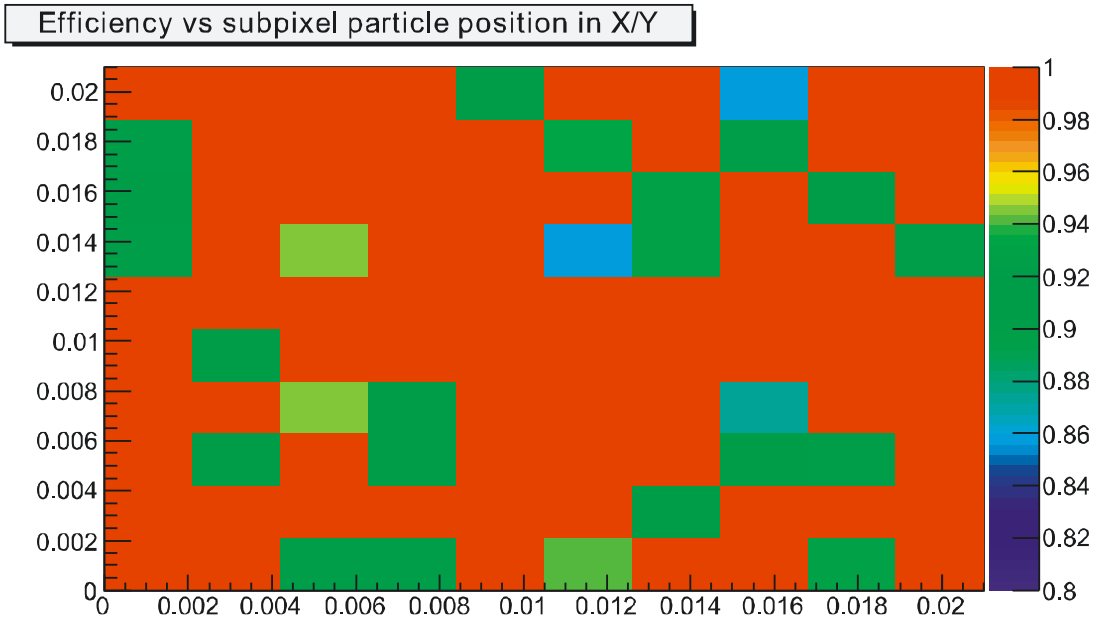


HV-CMOS

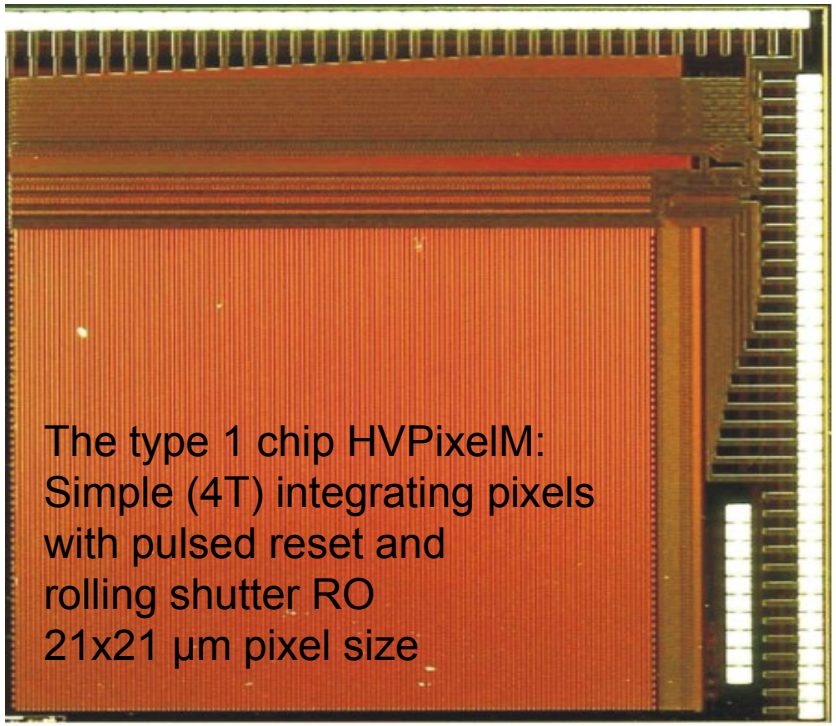
Backup slides

Test beam results: monolithic

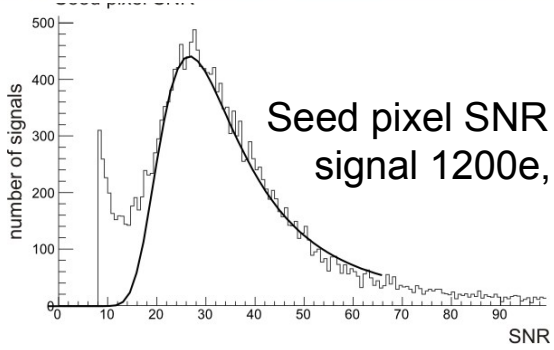
- excellent resolution
- very good S/N ratio
- efficiency limited by readout artifacts:
  - column-based readout
  - row not active during readout
  - data analysis did not correct for this
  - very small chip → low statistics



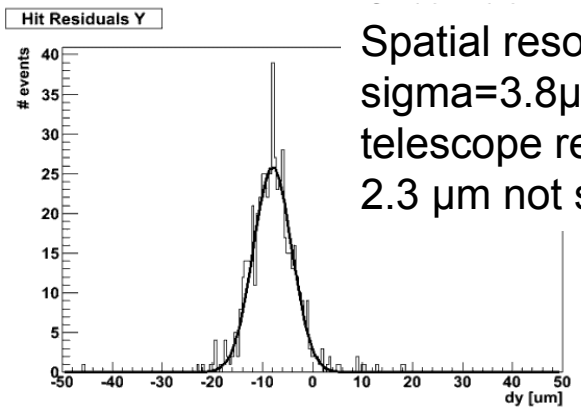
Efficiency vs. the in-pixel position of the fitted hit.
Efficiency at TB: ~98% (probably due to a rolling shutter effect)



The type 1 chip HVPixelM:
Simple (4T) integrating pixels with pulsed reset and rolling shutter RO
21x21 µm pixel size



Seed pixel SNR 27, seed signal 1200e, cluster 2000e

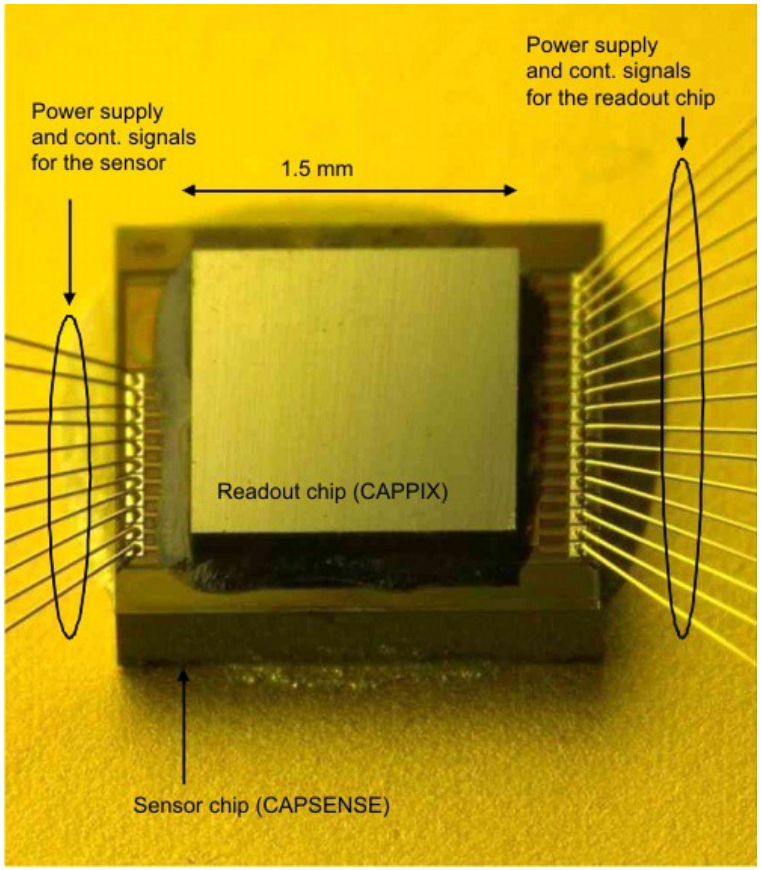


Spatial resolution: sigma=3.8µm, telescope resolution of 2.3 µm not subtracted

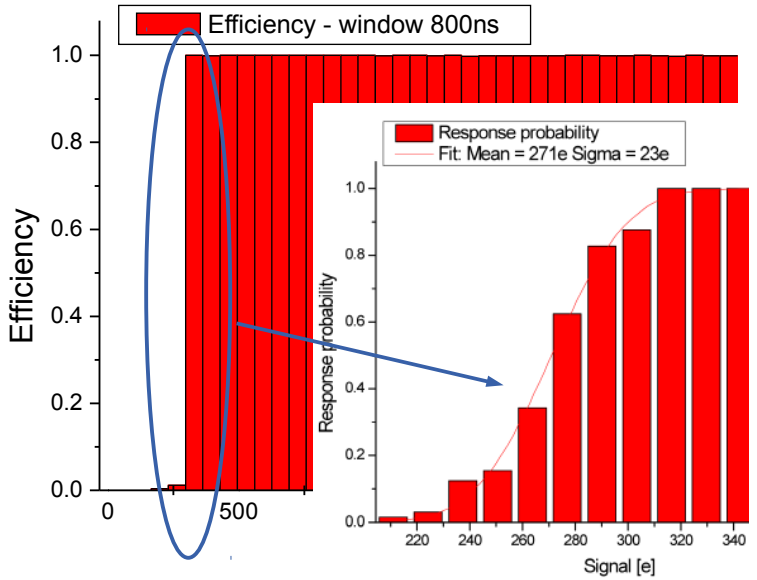
HV-CMOS

CPPD prototype results

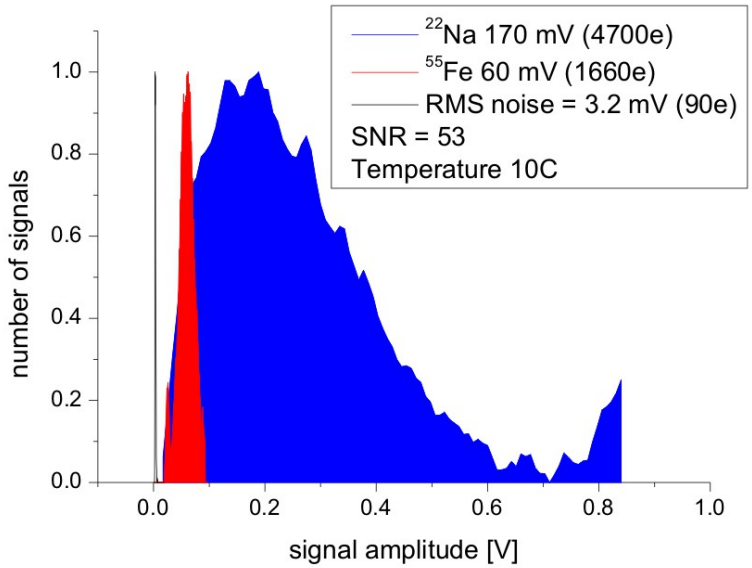
- excellent noise behaviour: stable threshold at ~330 electrons
- good performance also after irradiation



CAPPIX/CAPSENSE edgeless CCPD
50x50 µm pixel size



Detection efficiency vs. amplitude
Detection of signals above 330e possible with >99% efficiency.



Signals and noise of a CAPSENSE pixel after $10^{15} n_{eq}/cm^2$

HV-CMOS

CPPD prototype results

- Irradiation with 23 MeV protons: 1e15 neq/cm2, 150MRad
- FE-55 performance recovers after slight cooling