Status of the Low-Resistance (LowR) Strip Sensors Project

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Outline

- Motivation
- Proposed solution
- Technology and design
- First batch tests
- New batch
- Additional solutions
- Conclusions

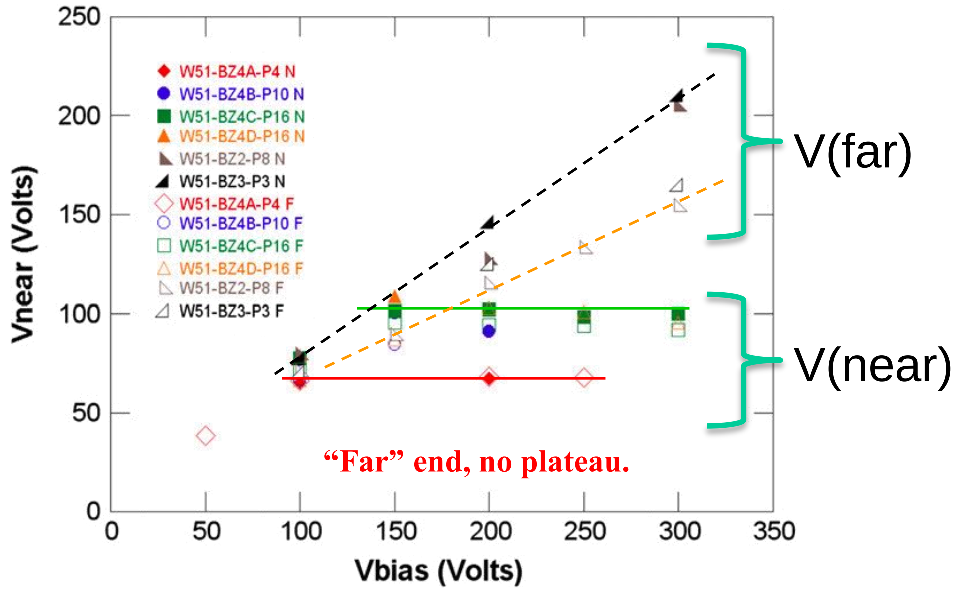
Motivation

➢ In the scenario of a **beam loss** there is a **large charge deposition** in the sensor bulk and **coupling capacitors can get damaged**

➢ Punch-Through Protection (PTP) structures used at strip end to develop low impedance to the bias line and evacuate the charge

But…

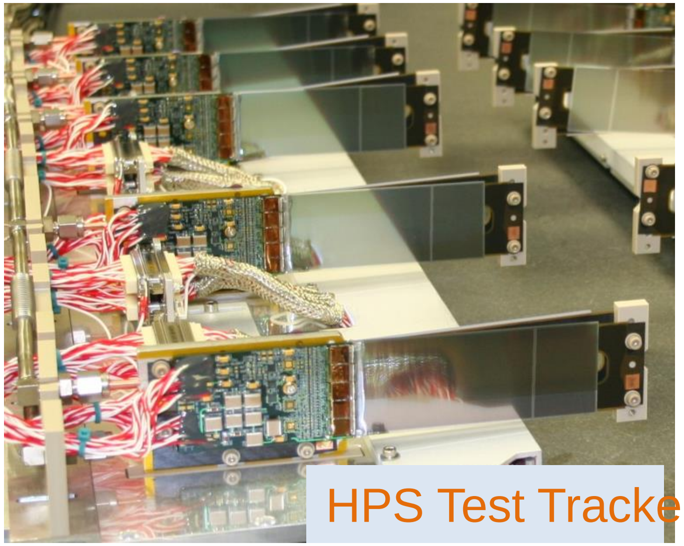
➢ Measurements with a large charge injected by a laser pulse showed that the strips can still be damaged
  - The **implant resistance** effectively **isolates** the “far” end of the strip from the PTP structure leading to the large voltages



Example: HPS experience

- Heavy Photon Search (HPS) is an experiment where Si sensors are intentionally put in close proximity to intense electron beam in JLab.
- APV-25 as FE chips; and HPK sensors for D0 run2b: P-on-n, 10 cm long.
- R(strip) ~ **1.8 MΩ** (=> 180 kΩ/cm, compared to 15 kΩ/cm in ATLAS07).

- There is a danger of beam loss with showering the innermost strips.
- => Beam test in SLAC e- beam simulating the shower.
- Saw issues at higher Bias and flux.



HPS Test Tracker

P. Hansson et al (SLAC)

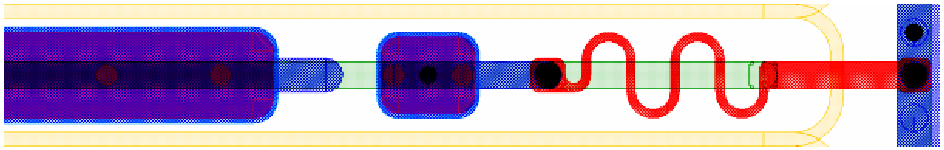
Time	Bunch Charge [pC]	Bias [V]	Flux/strip	Comment
~11:00	~0.001	180	10^1 e-	
11:36	1	180	10^4 e-	
	1	250	10^4 e-	
	1	350	10^4 e-	
	1	400	10^4 e-	
	1	500	10^4 e-	
12:00	10	180	10^5 e-	
	10	350	10^5 e-	onset
	10	500	10^5 e-	onset
	100	180	10^6 e-	problems
	100	250	10^6 e-	
	100	350	10^6 e-	

Note: The onset of problems showed up at ~ order of magnitude less flux than expected in ATLAS. But the strip resistance was 2 orders of magnitude higher!
⇒ Initially suspected damaged coupling capacitors.
⇒ Currently think FE ASICs are damaged.

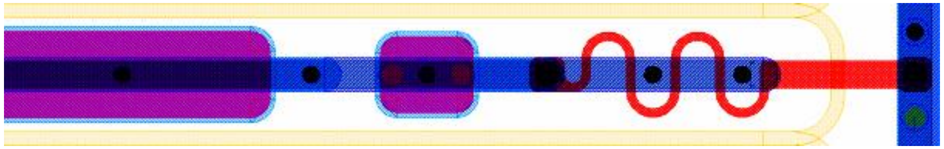
Proposed solution

- To **reduce the resistance of the strips** on the silicon sensor.
- Not possible to increase implant doping to significantly lower the resistance. Solid solubility limit of the dopant in silicon + practical technological limits (~ 1 x 10^{20} cm^{-3})
- Alternative: **deposition of Aluminum** (Metal 1) on top of the implant:
  - $R_{\square}(Al) \sim 0.04\ \Omega/\square \Rightarrow 20\ \Omega/cm$

Standard

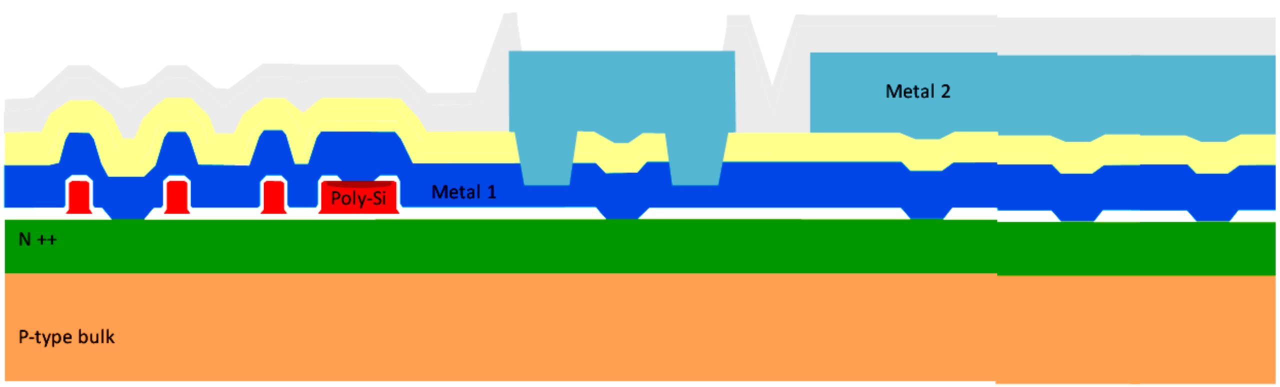


Low-R

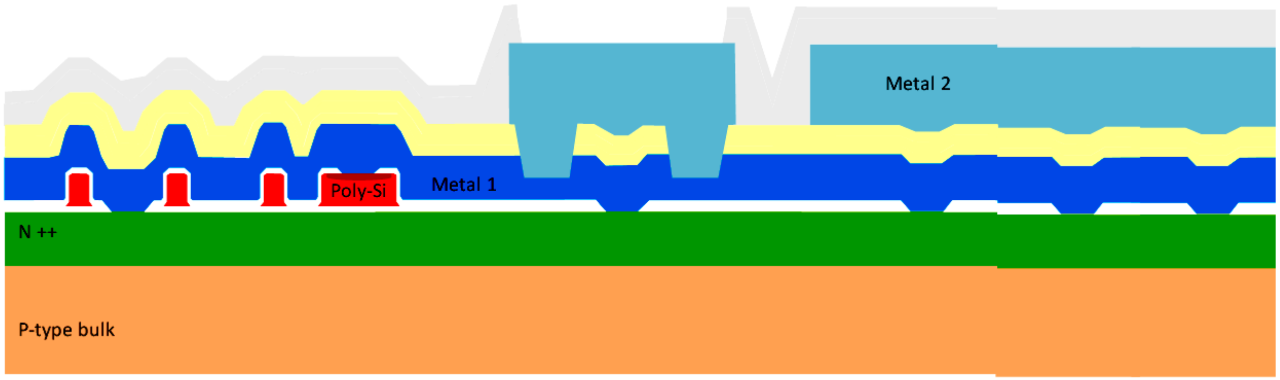


Technology

- Metal layer deposition on top of the implant (first metal) before the coupling capacitance is defined (second metal).
  - Double-metal processing to form the coupling capacitor
  - A layer of high-quality dielectric is needed between metals.
    - – Deposited on top of the first Aluminum (not grown)
    - ☞ Low temperature processing needed not to degrade Al: T < 400 ºC



Technology



- Initial experiments with MIM capacitors
  - Low temperature deposited isolation:
    - Plasma Enhanced CVD (PECVD): Process at 300-400 ºC
    - > 20 pF/cm ➔ ~ 3000 Å
  - 3 technological options:

    Silane: 3000 Å of SiH_4-based silicon oxide (SiO_2) deposited in 2 steps.

    TEOS: 3000 Å of TEOS-based oxide deposited in 2 steps ("Tetra-Etil Orto-Silicate")

    Nitride: 1200+1200+1200 Å of TEOS ox. + Si_3N_4 + SiH_4 ox. (Tri-layer)
  - Yield results for the largest caps (> 1 mm^2):

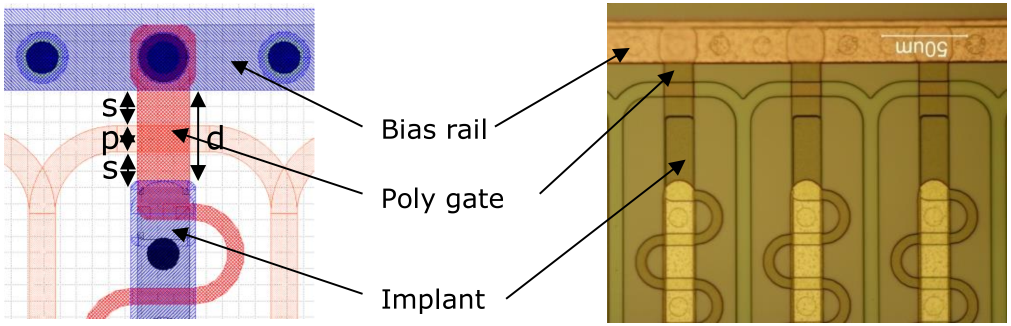
%	Silane	TEOS	Nitride
C1	81%	86%	94%

Best for nitride ⇒ Less pinholes due to Tri-layer

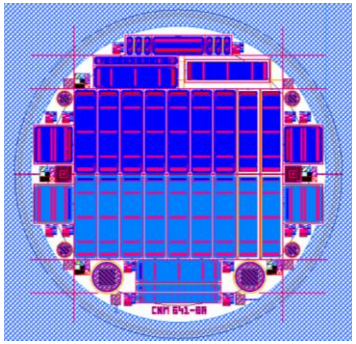
Design

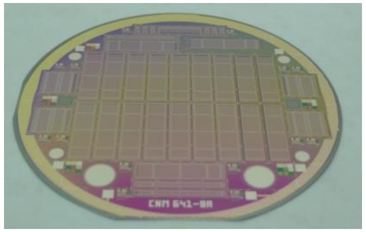
- PTP design:
  - Design of experiments (DOE): varying p, s $\Rightarrow$ d

DOE		N–P separation 's' [um]		
		12	8	6
P-stop width 'p' [um]	8	32	24	20
	6	30	22	18
	4	28	20	16
		Total PTP distance 'd'		



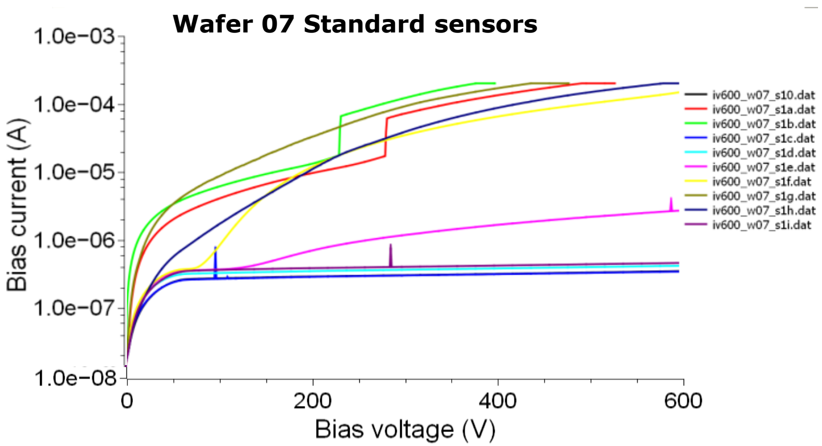
- Wafer design:
  - 10 ATLAS-barrel-like sensors: "LowR sensors"
    - 64 channels, ~2.3 mm long strips
    - First metal connected to the strip implant to reduce R_{strip}
    - Each sensor with a different PTP geometry (with polysilicon bridge)
  - 10 extra standard sensors for reference (no metal in implant). Identical design to the LowR but without metal strip on top of the implant

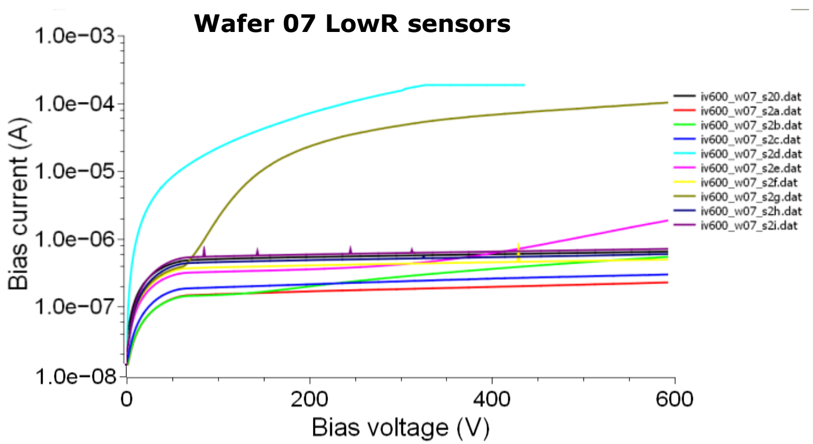




First batch general tests

- IV measurements, sensors were scanned from 0 to 600 V.
- CV, V_{FD}, Bias resistor (R_{BIAS}), coupling capacitance (C_{COUP}), Inter-strip resistance, …
- Both standard and LowR sensors show similar general characteristics.



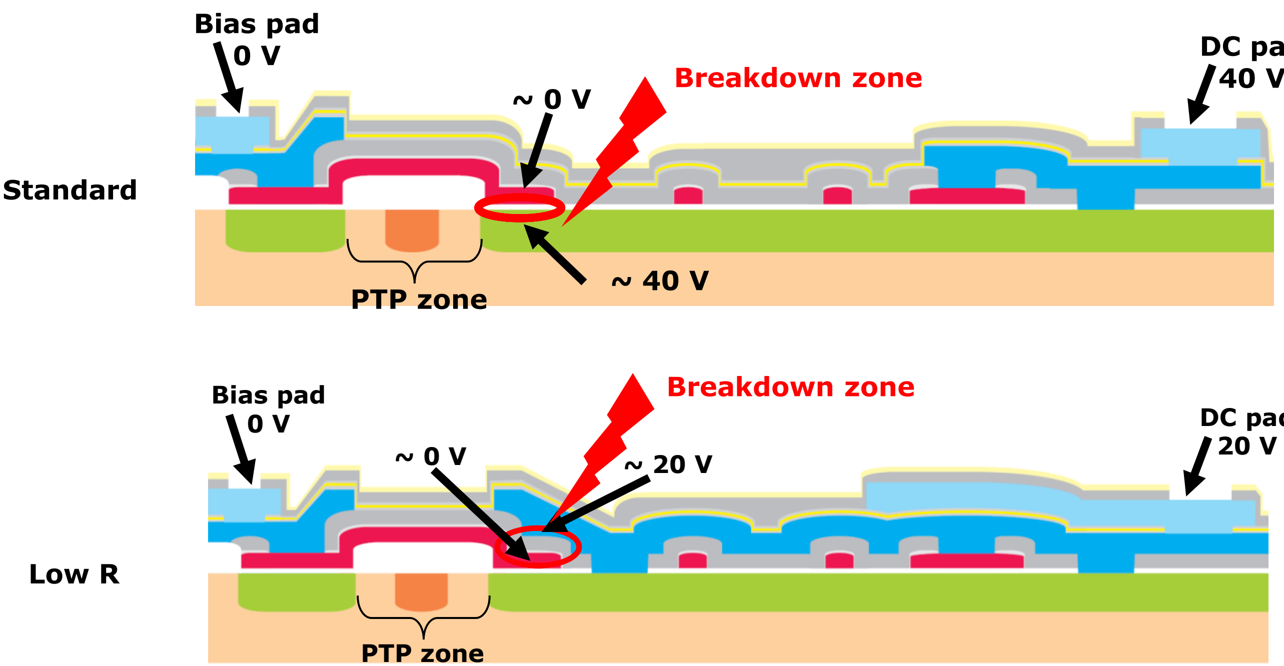


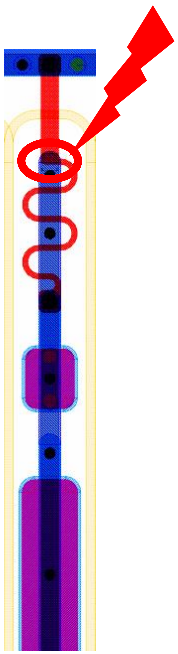
- R(implant) is reduced by ~3 orders of magnitude:

  13.6 kΩ/cm (standard) → 23 Ω/cm (LowR).

First batch PTP tests

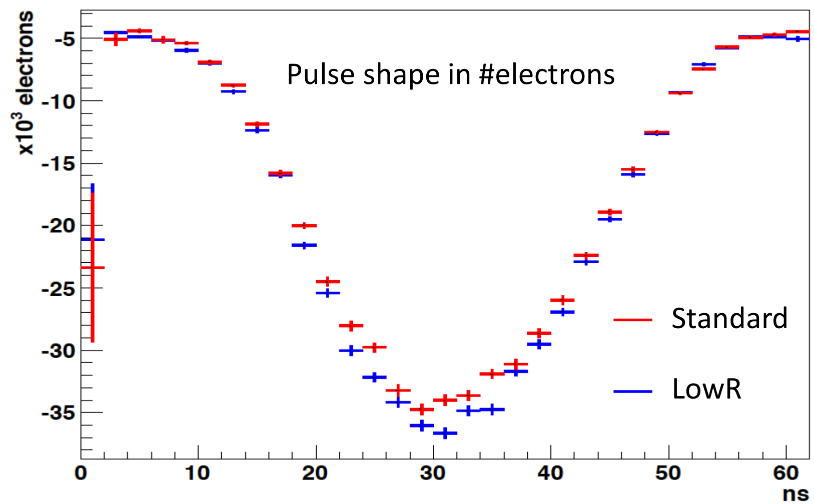
- PTP tests show unexpected behavior:
  - Breakdown voltage independent of PTP structure geometry
  - at ~40 V in standard sensors and at ~20 V in LowR sensors
  - Oxide breakdown at a different place in the strip occurs before PTP is activated.
    - Thin oxides overlooked during fabrication
    - Only critical when PTP structures are present and tested





Pulse shape

- Concerns about possible pulse shape change in LowR sensors
- Standard and LowR sensors are tested with the ALIBAVA System and an IR laser.
- Each sensor is read by one Beetle ASIC



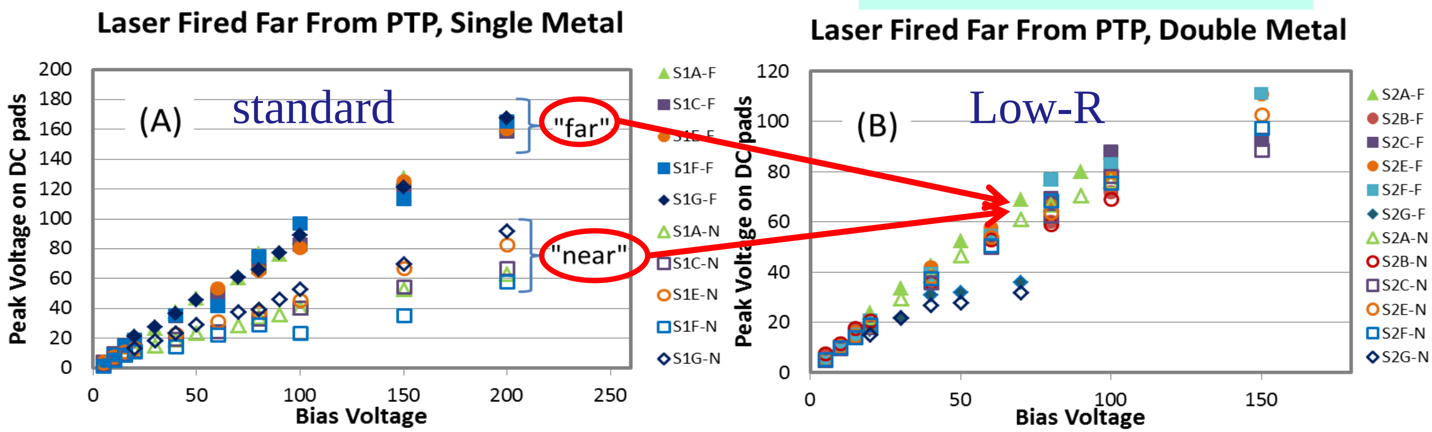
- Pulse shape with the sensor fully depleted. The pulse shapes are identical for standard and LowR detectors with a small, negligible difference at the peak

Laser PTP: initial tests

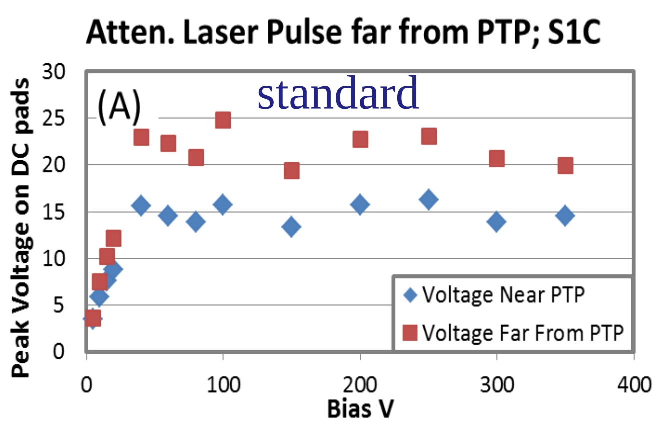
- We also evaluated dynamic response with laser tests.
- The oxide issue notwithstanding, the laser tests show that the low strip resistance technology equalizes the potential along the strip, as intended.

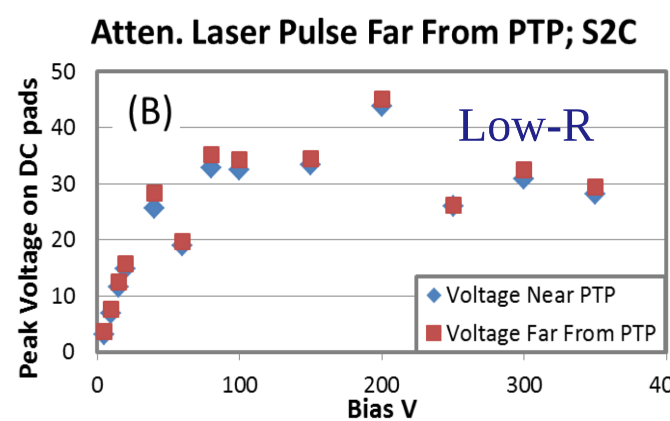
J. Wortman et al (UCSC)

Much reduced ΔV along the strip for Low-R sensors



Similar effect at reduced light intensity where the signals plateau in the safe range.





New batch

- New batch being processed correcting this:
  1) Thicker thermal oxide in the coupling capacitor area to avoid breakdown in standard sensors
  2) Thicker and tri-layer oxide deposited between poly and metal in LowR sensors to avoid breakdown in LowR sensors
  3) In some extra sensors, new metal mask (METAL-B) with no metal on top of bias resistor area to avoid the possibility of breakdown in that area
  4) Some wafers will have a reduced p-stop doping to make sure we have PTP

- The process is well advanced. We expect the wafers ready for middle of December

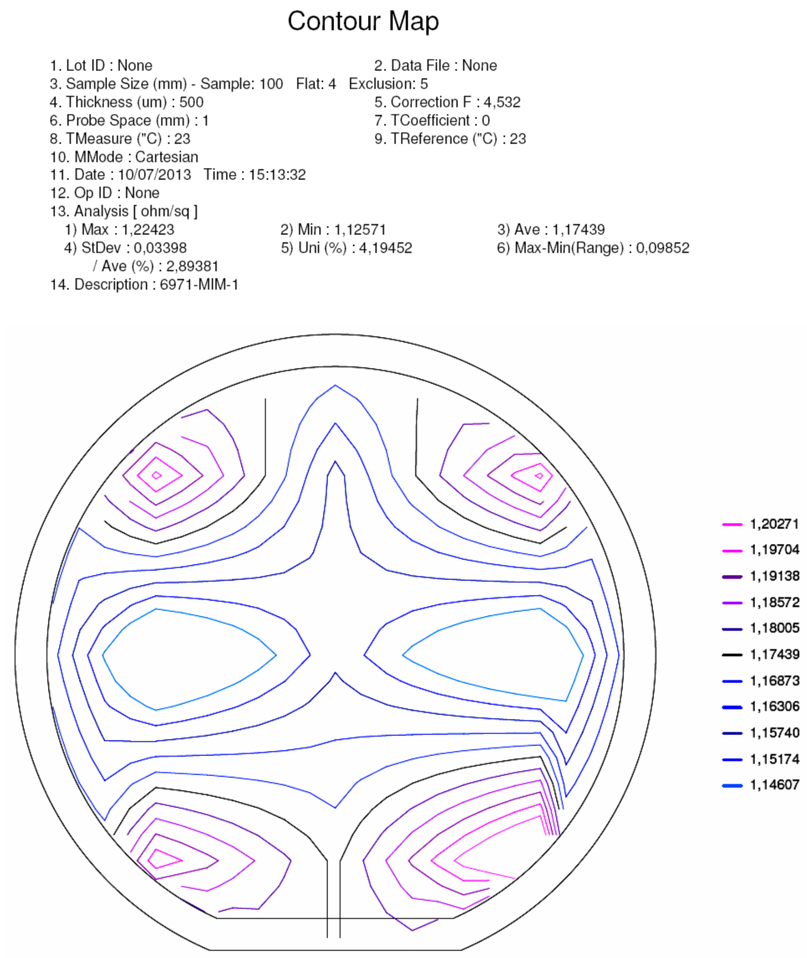
Additional solutions

- Other methods to obtain LowR sensors being studied:
  - $TiSi_2$: allows the use of high temperature steps after the oxide deposition
    - → oxide densification → higher yield
  - Highly doped polysilicon: allows the growth of thermal oxide after it
    - → high quality oxide
    - → back to “standard” process

	sheet R (Ohm/#)	kOhm/cm	strip R (kOhm)
Implant	22	11	25.3
Metal	0.04	0.02	0.05
Metal-B			0.946
TiSi2	1.2	0.6	1.38
Poly	3	1.5	3.45

Titanium Silicide ($TiSi_2$)

- $TiSi_2$ formation technology at CNM
  - Good formation of $TiSi_2$ layer
  - Low sheet resistance: ~1.2 Ω/□
  - Densification at 900 ºC , 30 min
  - Self aligned process
- $TiSi_2$ MiM capacitors fabricated
  - 100 % yield up to 20 V
  - More tests up to 100 V
  - Risk of higher leakage currents because $TiSi_2$ layer «consumes» Si.
- Polysilicon-Metal capacitors to be fabricated next



Conclusions

- Low resistivity strips (LowR) proposed to protect strip sensors in the event of a beam loss making the PTP more effective
- First implementation with Aluminum layer in contact with the implant to drastically reduce strip resistance
  - LowR sensors show similar behavior as standard sensors
  - Initial dinamic laser tests show an effective reduction of the implant voltage
  - New batch being processed to overcome a technological problem in the first batch that prevents full test
- New possible implementations being tried with $TiSi_2$ and polysilicon to assure a better coupling capacitor formation, and a more standard processing