Automatic inspection of SEE sensitivity in pixel microelectronics

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Outline

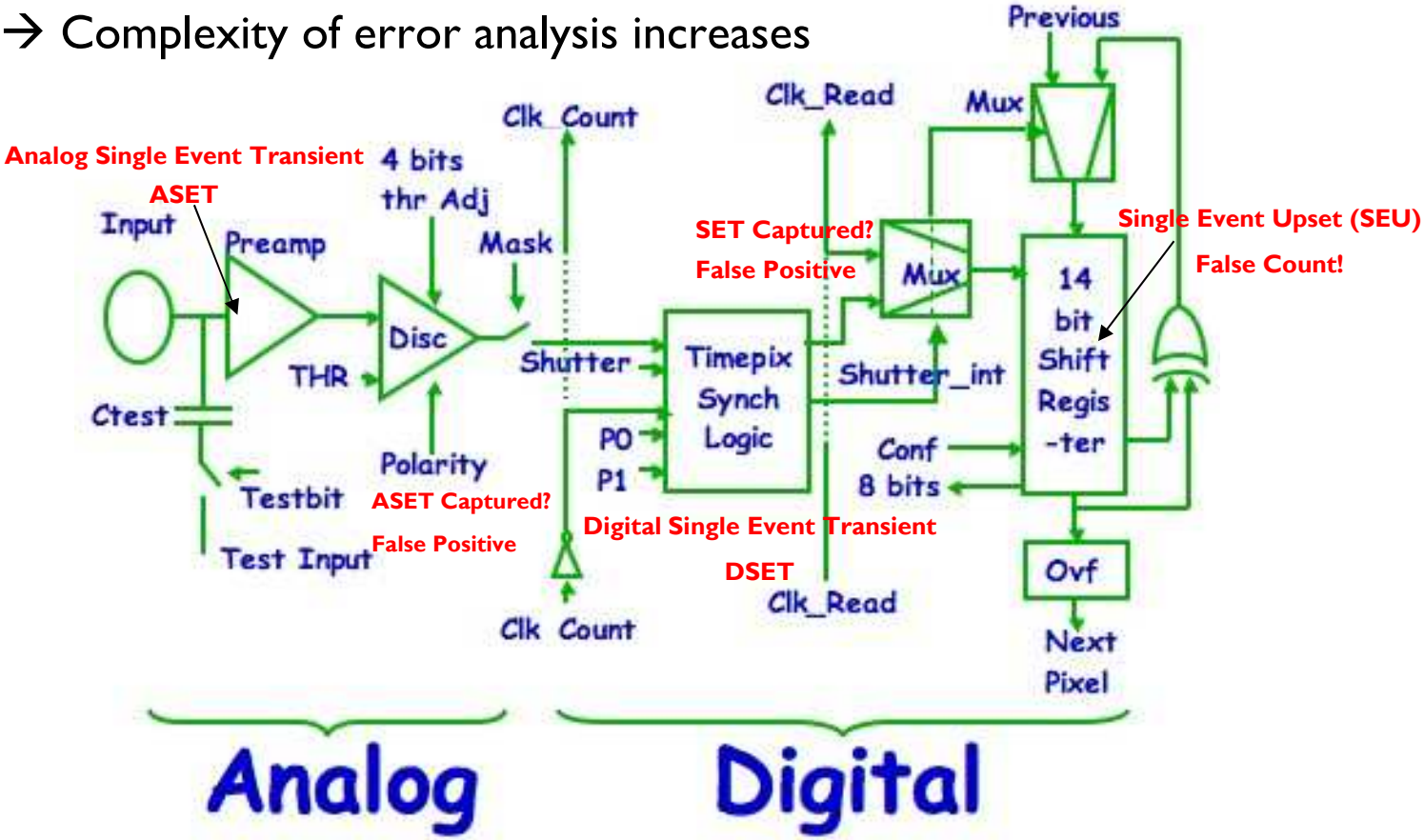
- Introduction
- Motivation and goals
- SEE sensitivity analyzer
  - Applied methodology and tool performance
  - Case studies
- Conclusions and future work

Introduction

- Under the Silicon Detector we find the pixel electronics and it is sensitive to particle tracks too!
- As technologies shrinks, transient effects (SEE) can become critical
  - Higher frequencies and lower dimensions →

→Not only affects to digital, but also analog cells →

→ Complexity of error analysis increases



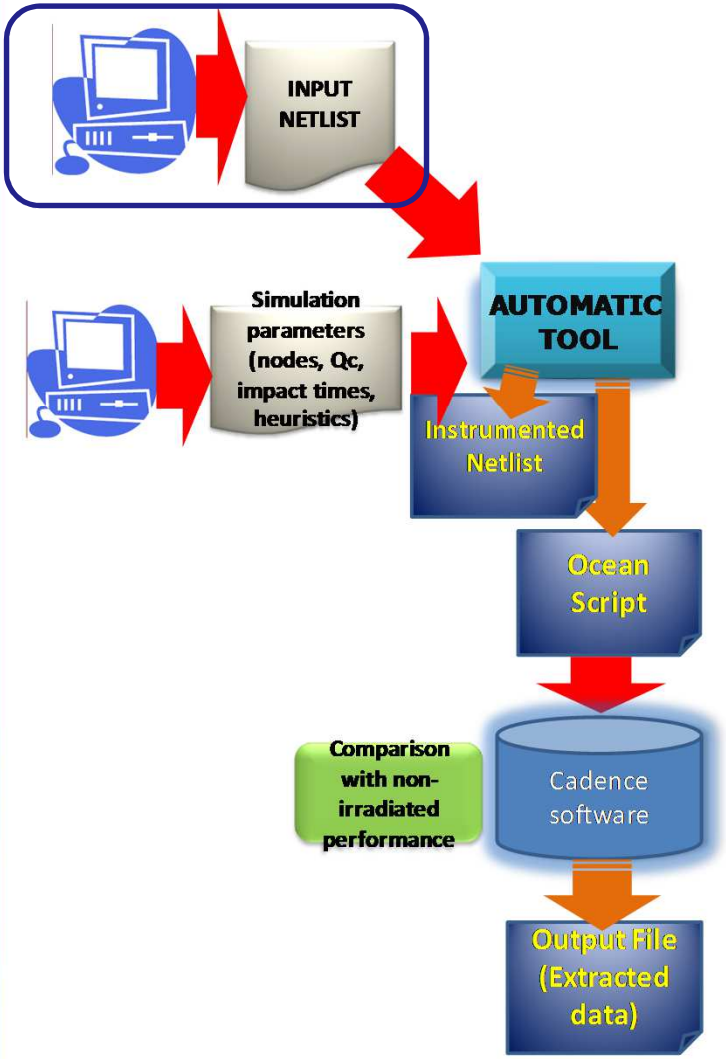
- TimePix Electronics, as an example

Motivation

- Need for a rapid diagnose of vulnerabilities in previous stages of design → Radiation-hardened systems
- Dealing with SEE sensitivity analysis as the number of transistors increase is a challenging thread.

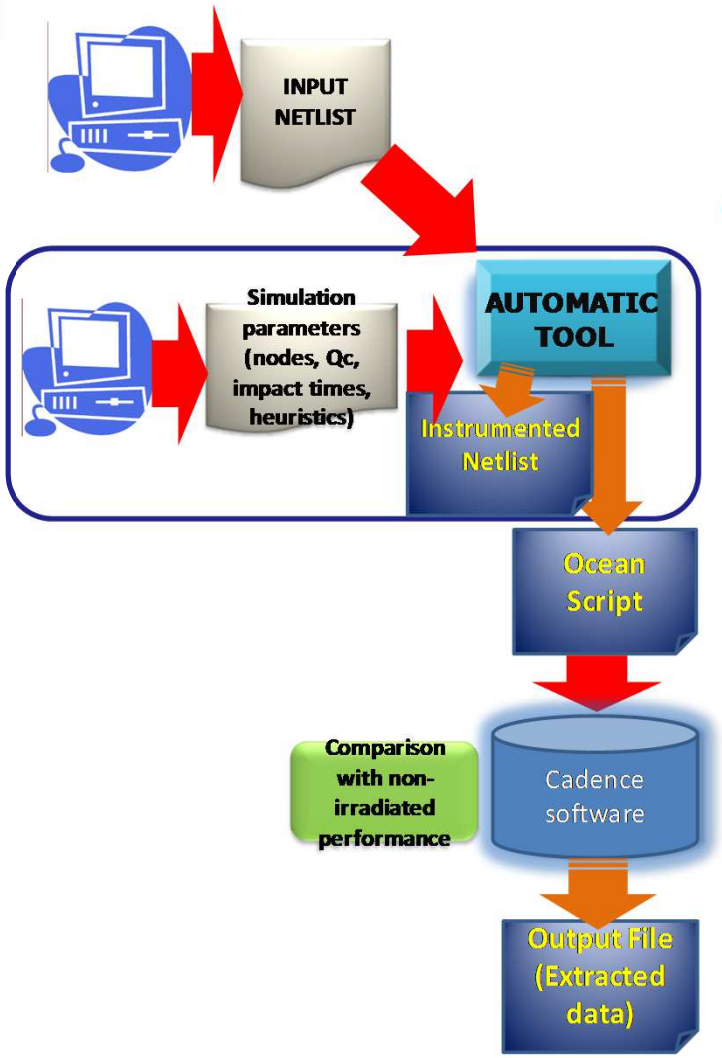
- Objective: an *automatic tool for SEE sensivity analysis*
  - Provide a useful information about critical nodes of the circuit under test to the analog designer.
  - Fast evaluation of complex analog circuits' vulnerabilities to radiation at transistor level.
  - Elaborate a SEE sensitivity map of the circuits on test.

SEE sensitivity methodology



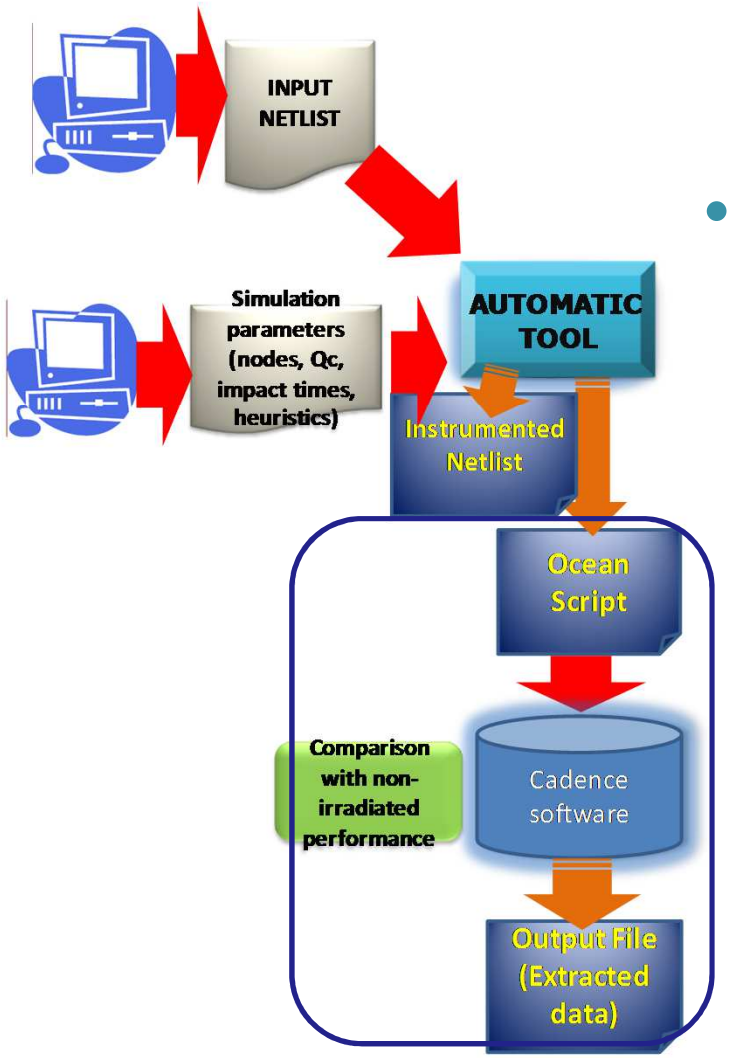
- Starting point: circuit definition by the designer.
  - A Spectre netlist (extracted from simulation test-bench) is taken as an input.

SEE sensitivity methodology



- From the input netlist, the tool will:
  - Generate an instrumented netlist for SEE emulation.

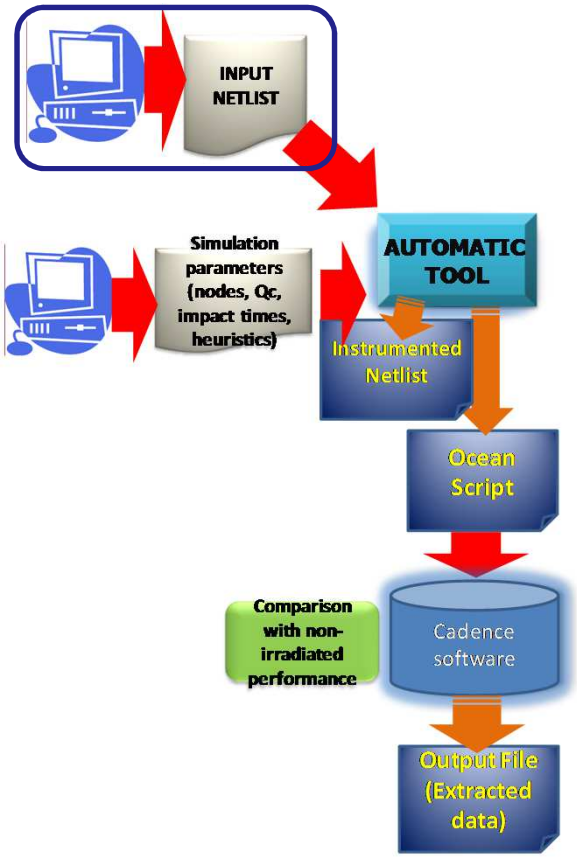
SEE sensitivity methodology



- From the input netlist, the tool will:
  - Generate an instrumented netlist for SEE emulation.
  - Create a simulation script that automatically:
    - Analyzes the SEE sensitivity of the analog circuit .
    - Provides an output file with critical information.

Starting point

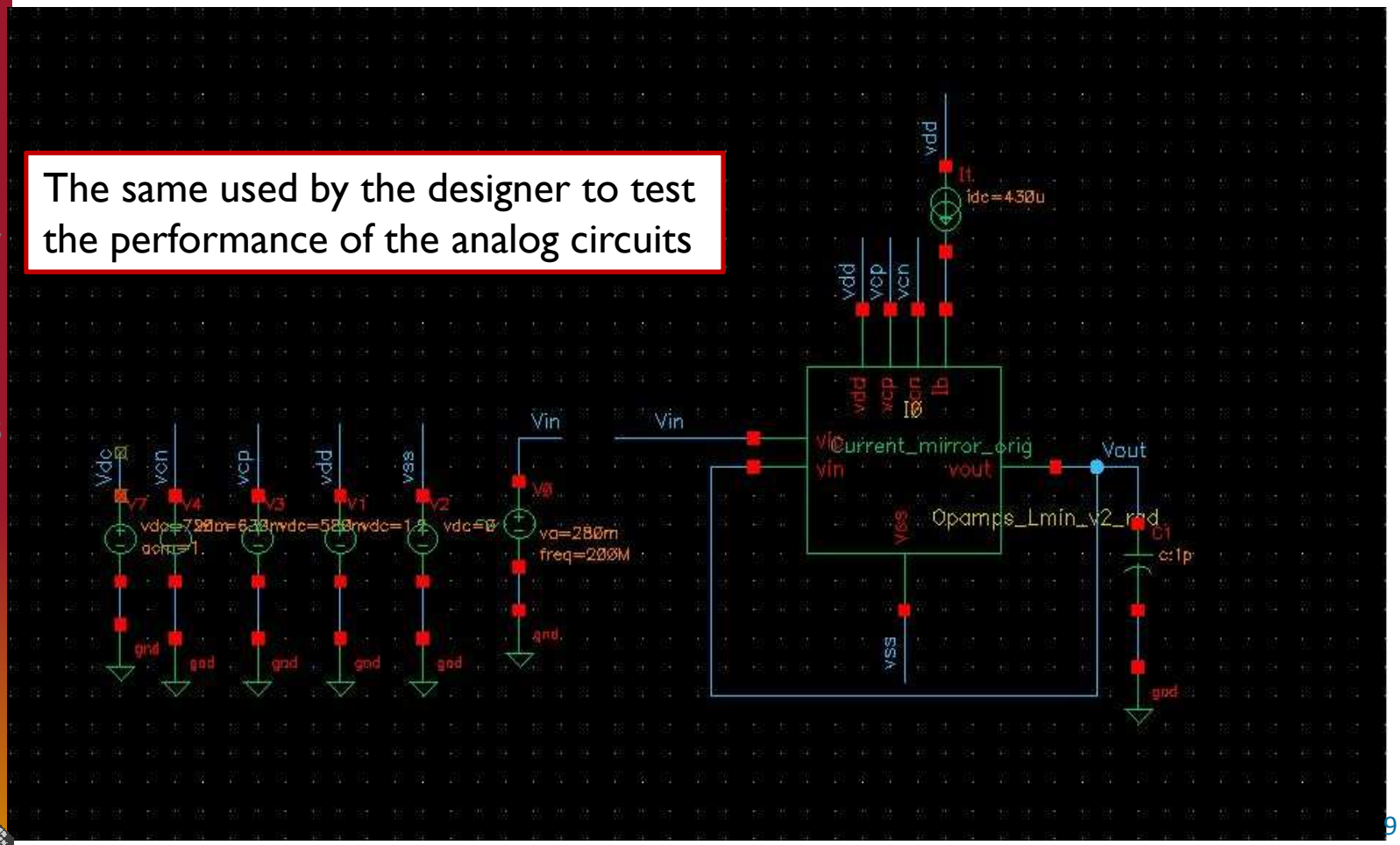
- Input netlist
  - extracted from the designer's test bench



Starting point

- Circuit test-bench

The same used by the designer to test the performance of the analog circuits



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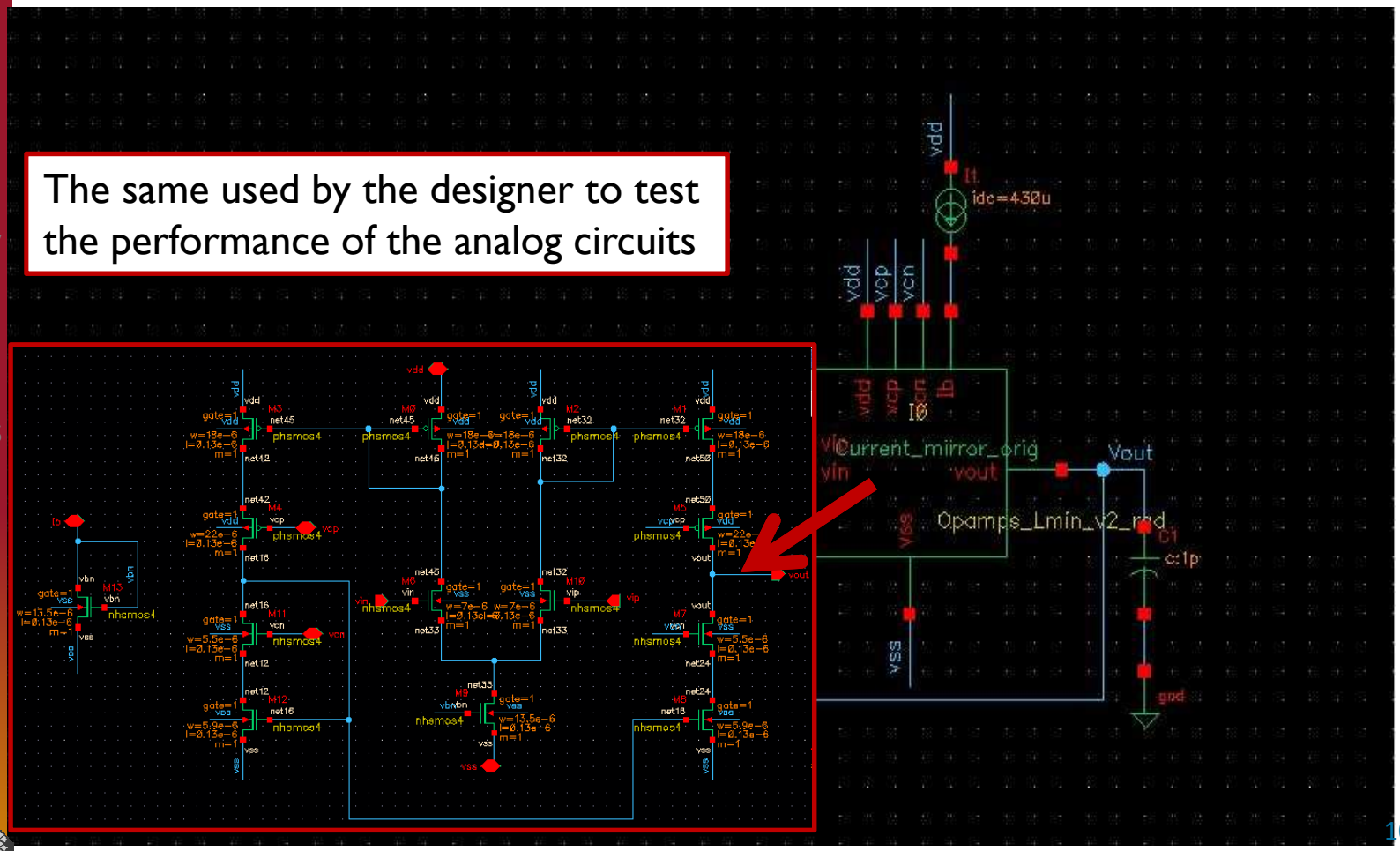
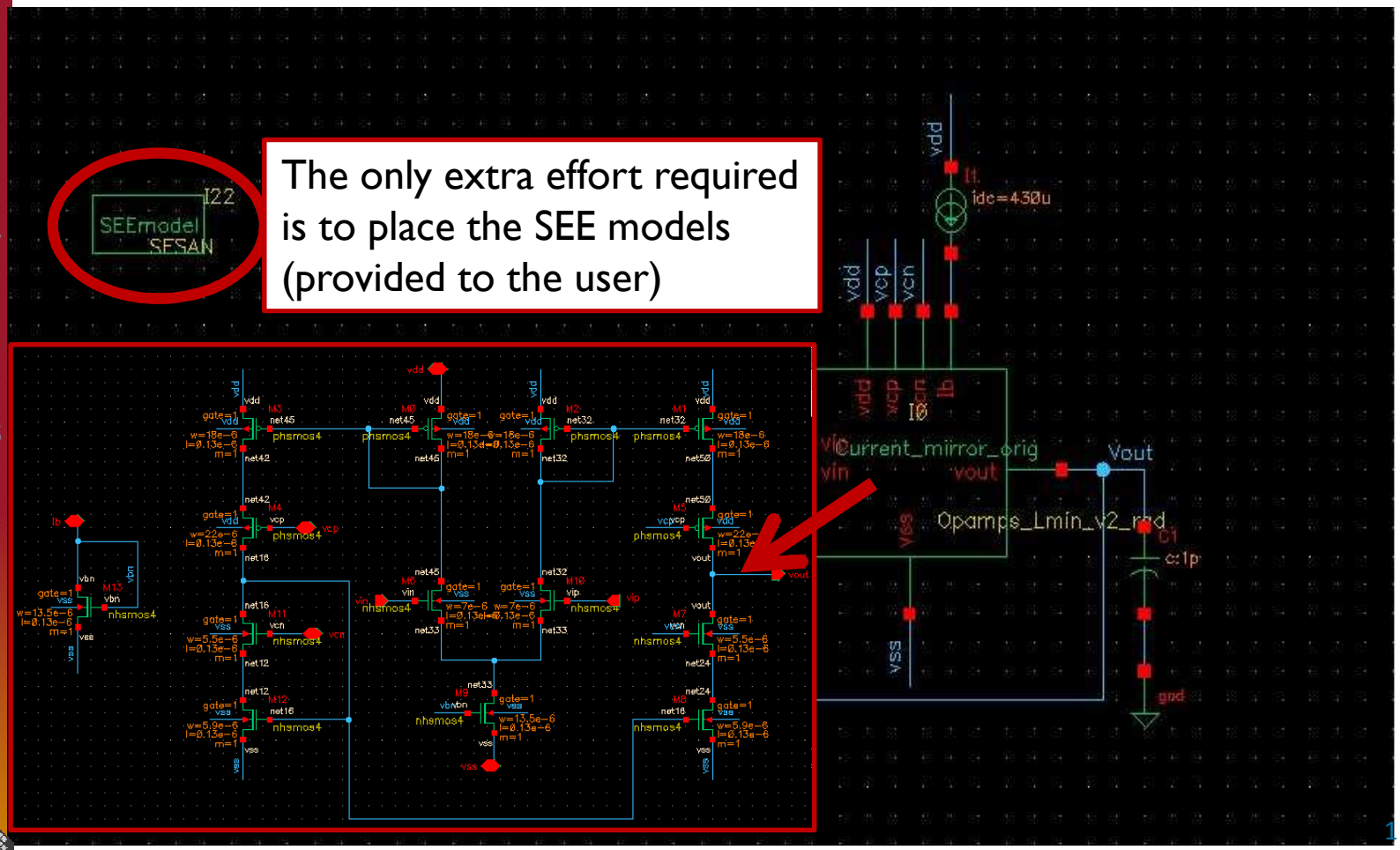


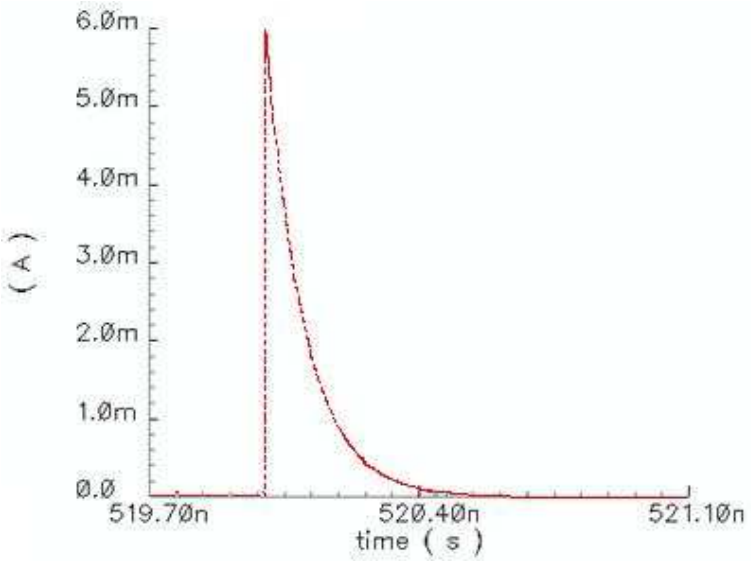
Starting point

- Circuit test-bench



Single Event Effects modeling

- SEE emulation based on charge injection models:
  - Current sources with double exponential dynamics*
  - Use of configurable parameters (AHDL implementation)

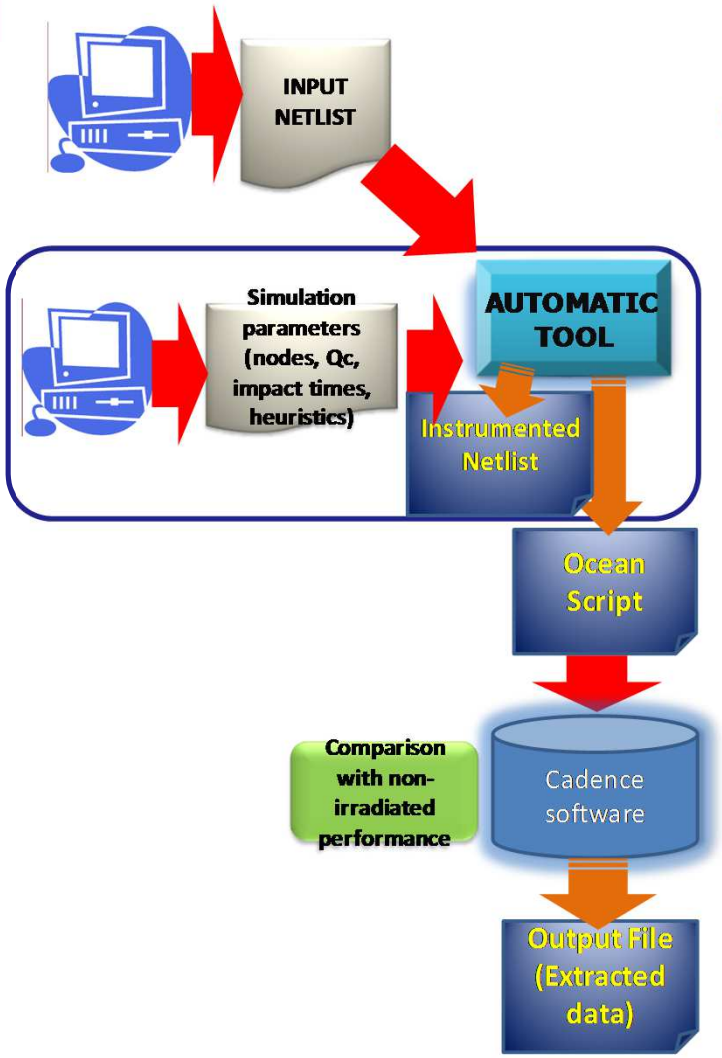


$$I_{rad} = \frac{Q_c}{\tau_d - \tau_r}\left(e^{-\frac{\tau}{\tau_d}} - e^{-\frac{\tau}{\tau_r}}\right)$$

$$Q_c = \frac{\rho \cdot LET \cdot d}{3.6}$$

***REF: G. Messenger,** "Collection of Charge on junction nodes from ion tracks", *IEEE Transactions on nuclear science*, vol.29, n° 6, Dec. 1982

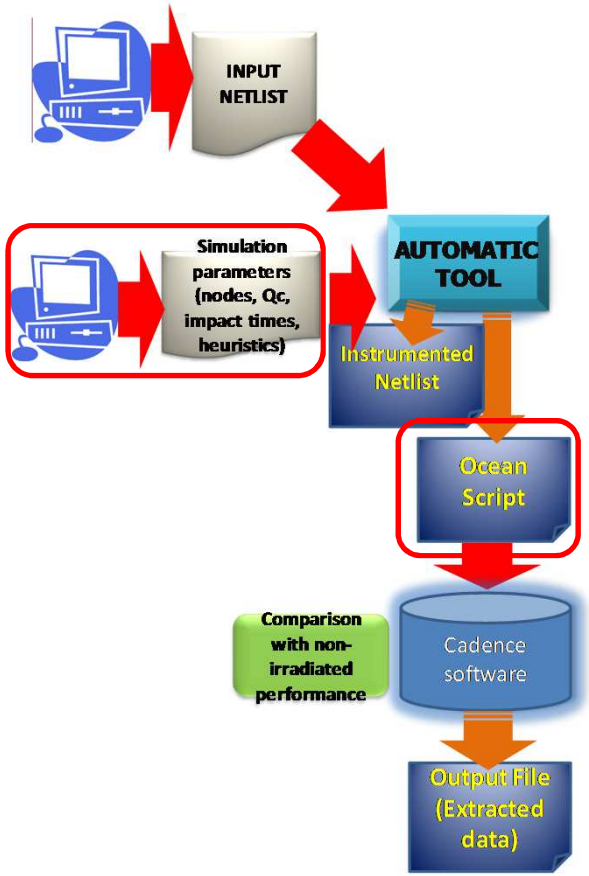
Tool performance



- Step I: a new instrumented netlist is generated.
  - SEE models for impacts emulation are added to every possible target.
  - The user has to provide configuration parameters for simulation and analysis of the circuits (step 2).

2. Script generation

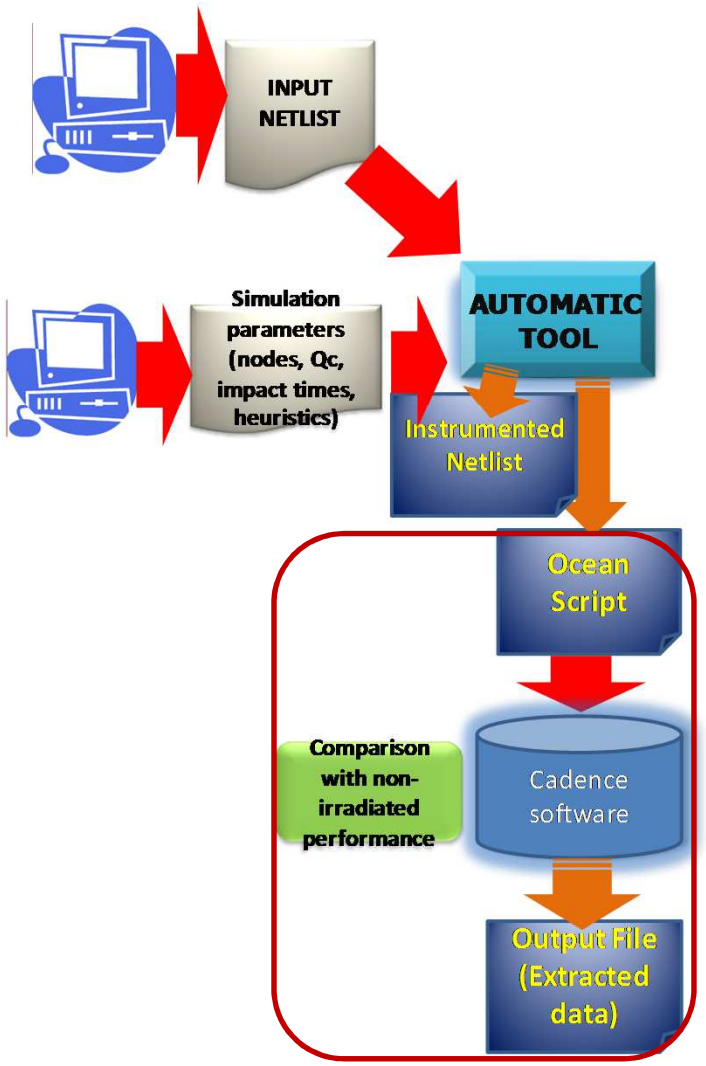
- Configuration parameters should be defined for automatic script generation:
  - ***Impact nodes.***



2. Script generation

- Configuration parameters should be defined for automatic script generation:
  - Impact nodes.
  - SEE model parameters:
    - *Injected charge*
    - *Impact times*
  - ***Outputs selected***

2. Script generation

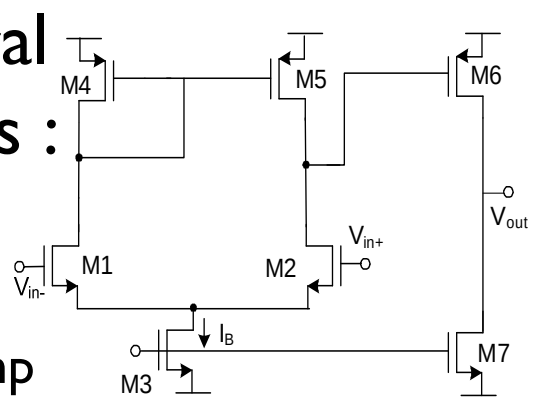


- A simulation script is automatically created.
  - Compares an ideal (non-irradiated) output and the signal affected by injected SEEs.
  - Results of the analysis of circuit's vulnerabilities are automatically analyzed and extracted into an output file.

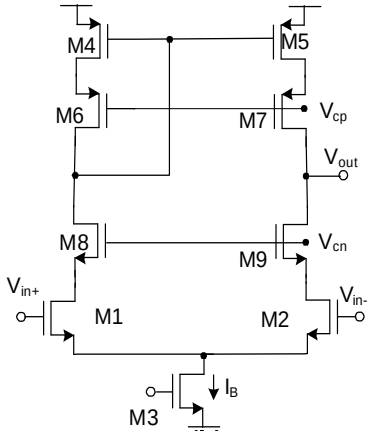
Case studies

- Analysis of several analog topologies :
  - a) Two stage Miller OpAmp
  - b) Telescopic OpAmp
  - c) Fully cascoded two stage OpAmp
  - d) Current mirror OpAmp (OTA)

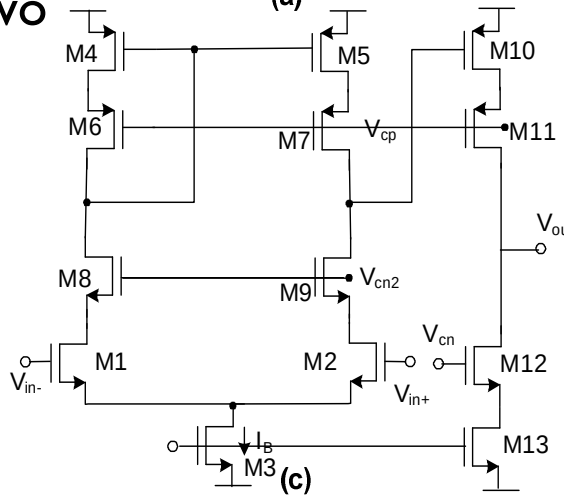
(ST130nm tech.)



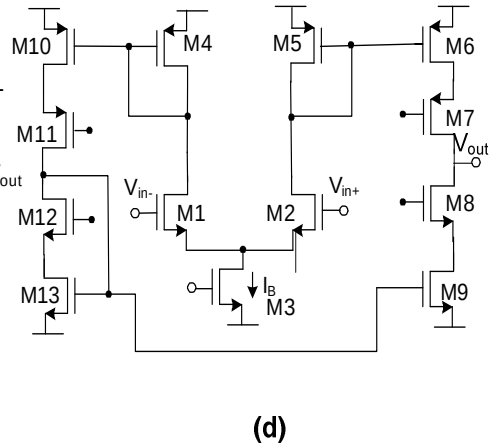
(a)



(b)



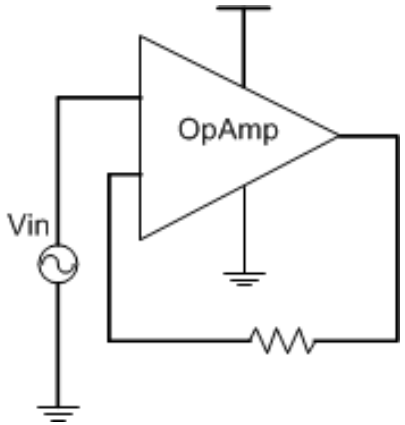
(c)



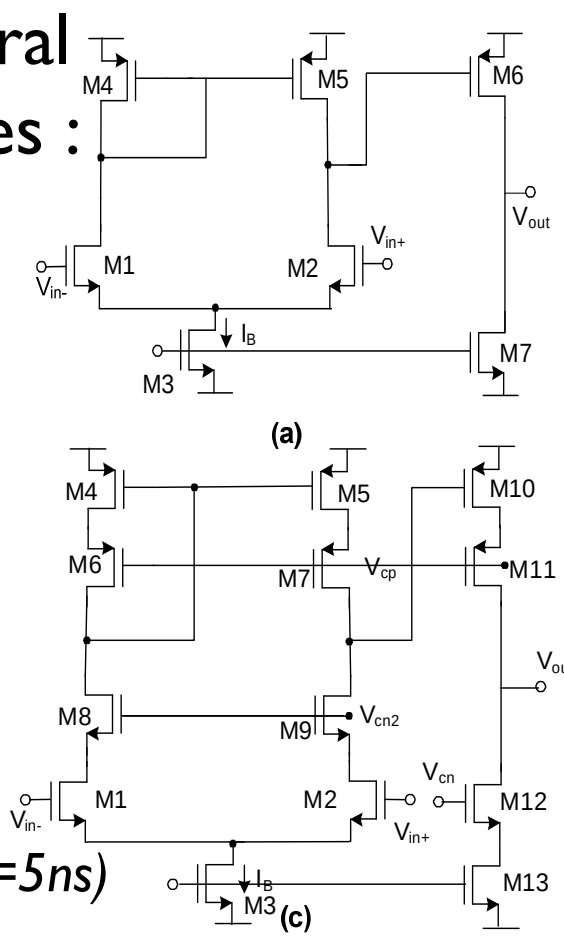
(d)

Case studies

- Analysis of several analog topologies :
  - Test-bench:



  - Input signal:
    - *A= 400mV*
    - *Fin= 200MHz (T=5ns)*



Case studies

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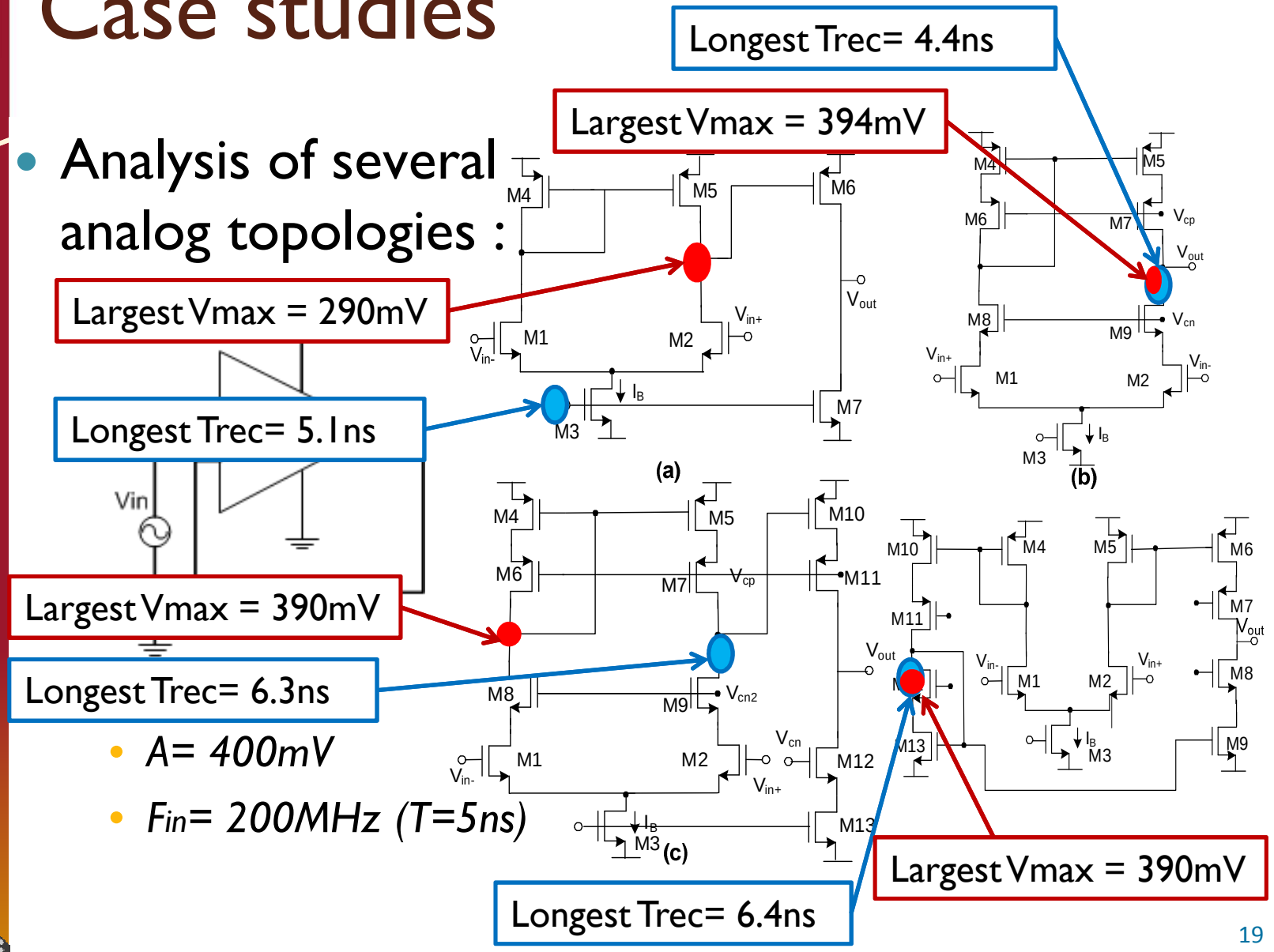
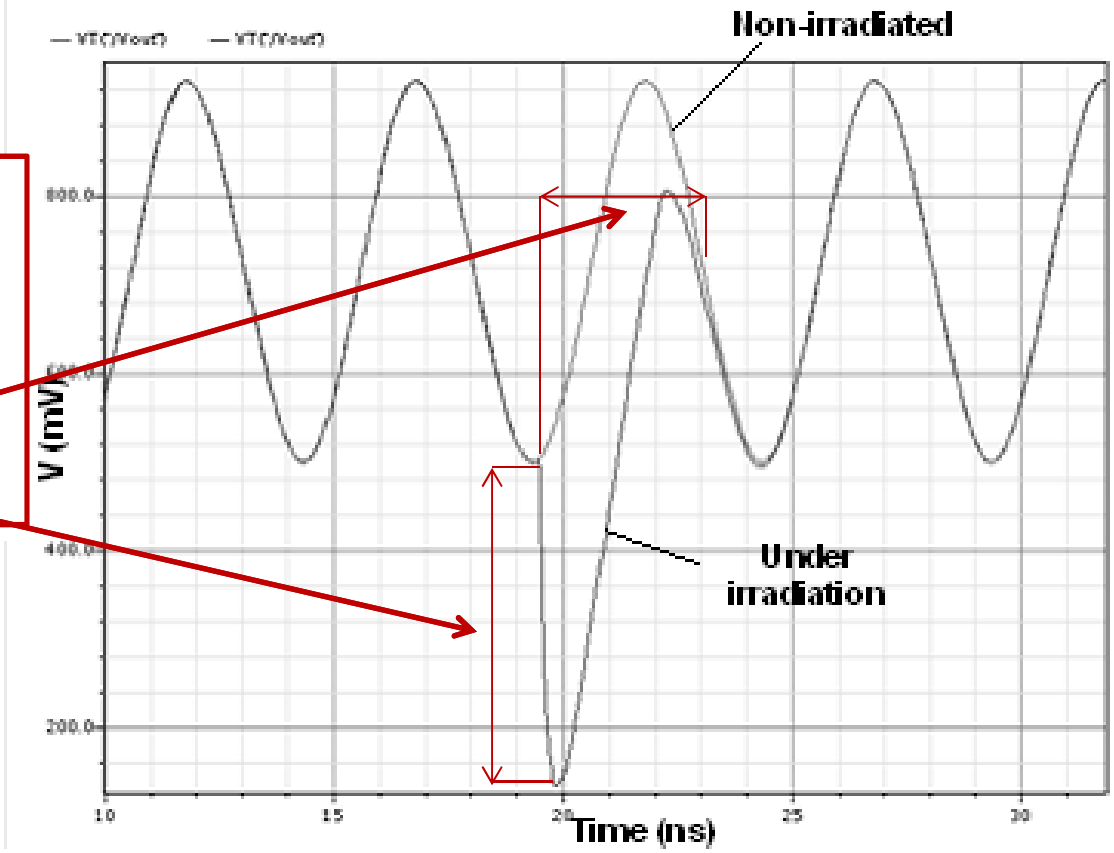


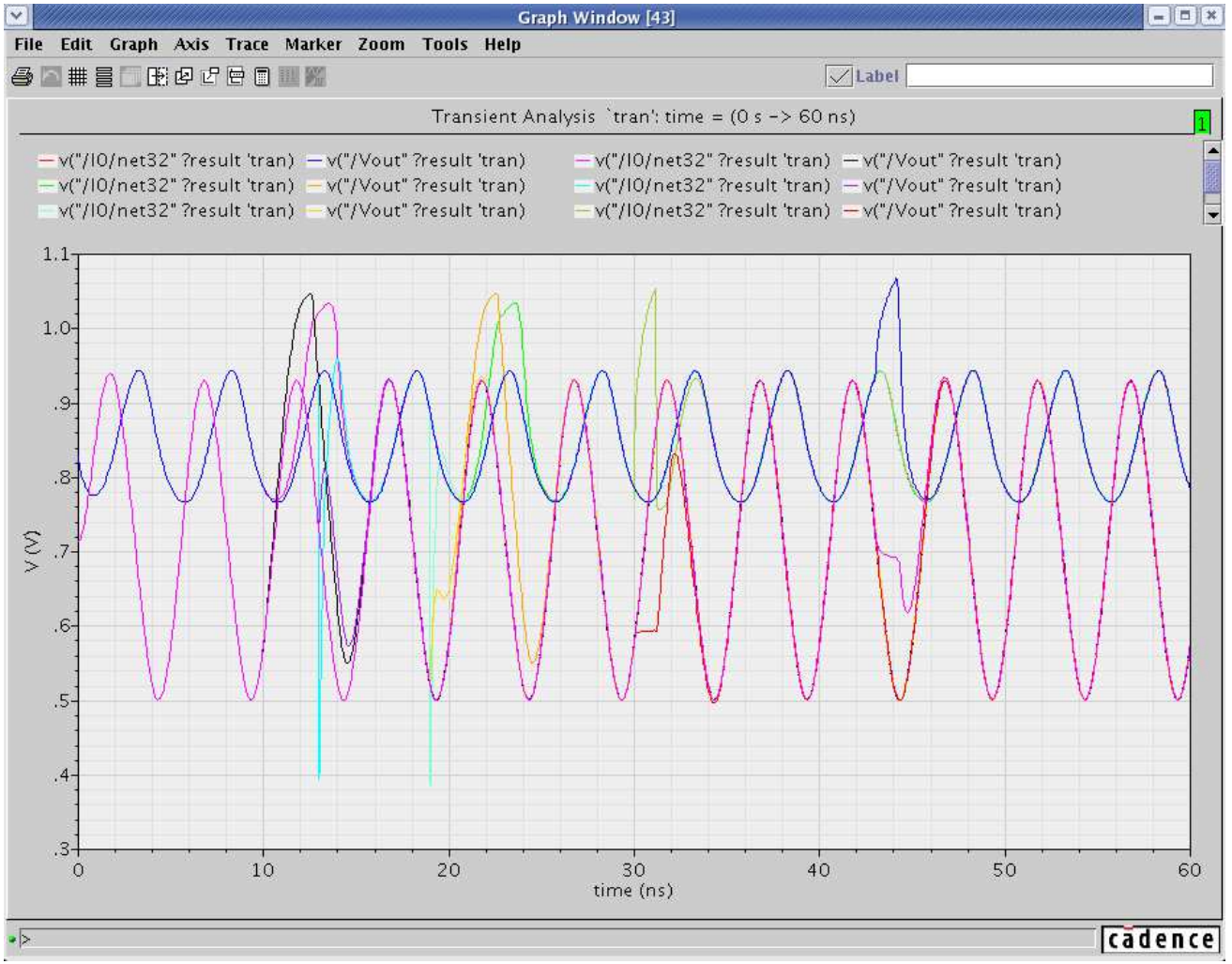
Heuristic analysis

Two main transient parameters have been considered for the analysis:

- *Recovery time*
- *Voltage deviation*



Transient simulations



Generated output database

Output	Impact	Qc	Timp	Trec	Vmax
/I0/net32	I0_M5	5,00E-13	1,00E-08	5.100.000	0.109233
/Vout	I0_M5	5,00E-13	1,00E-08	6.400.000	0.225535
/I0/net32	I0_M5	5,00E-13	2,00E-08	5.100.000	0.109186
/Vout	I0_M5	5,00E-13	2,00E-08	6.400.000	0.225493
/I0/net32	I0_M7	5,00E-13	1,3e-08	2.300.000	0.426629
/Vout	I0_M7	5,00E-13	1,3e-08	3.600.000	0.183520
/I0/net32	I0_M7	5,00E-13	2,6e-08	2.300.000	0.370461
/Vout	I0_M7	5,00E-13	2,6e-08	3.000.000	0.147083
/I0/net32	I0_M10	2,50E-13	1,00E-08	2.800.000	0.205726
/Vout	I0_M10	2,50E-13	1,00E-08	3.900.000	0.186725
/I0/net32	I0_M10	2,50E-13	2.0e-08	3.300.000	0.143872
/Vout	I0_M10	2,50E-13	2.0e-08	4.600.000	0.231184
	.				
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	.				
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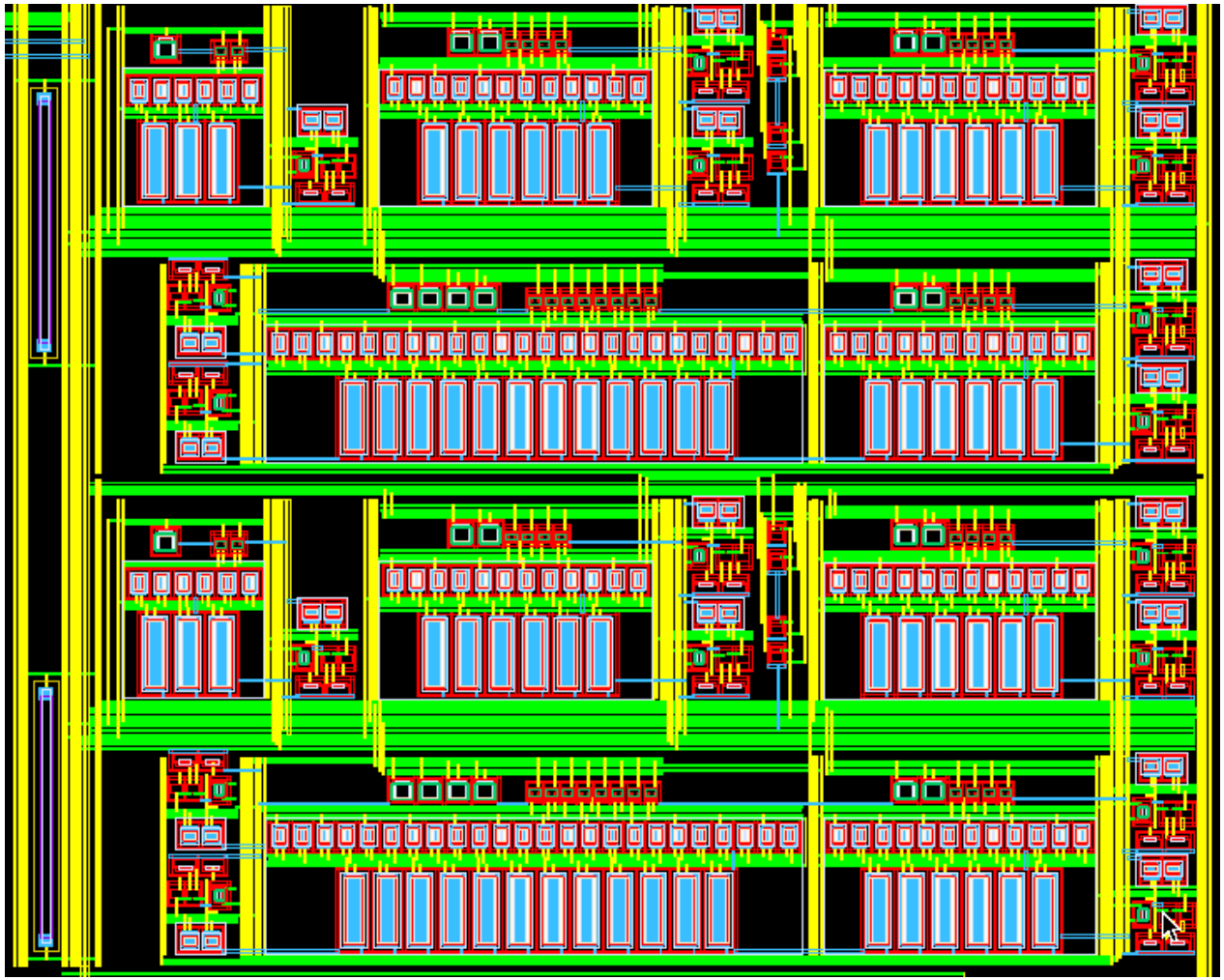
	.				

Future work

- Objective : create a SEE sensitivity map



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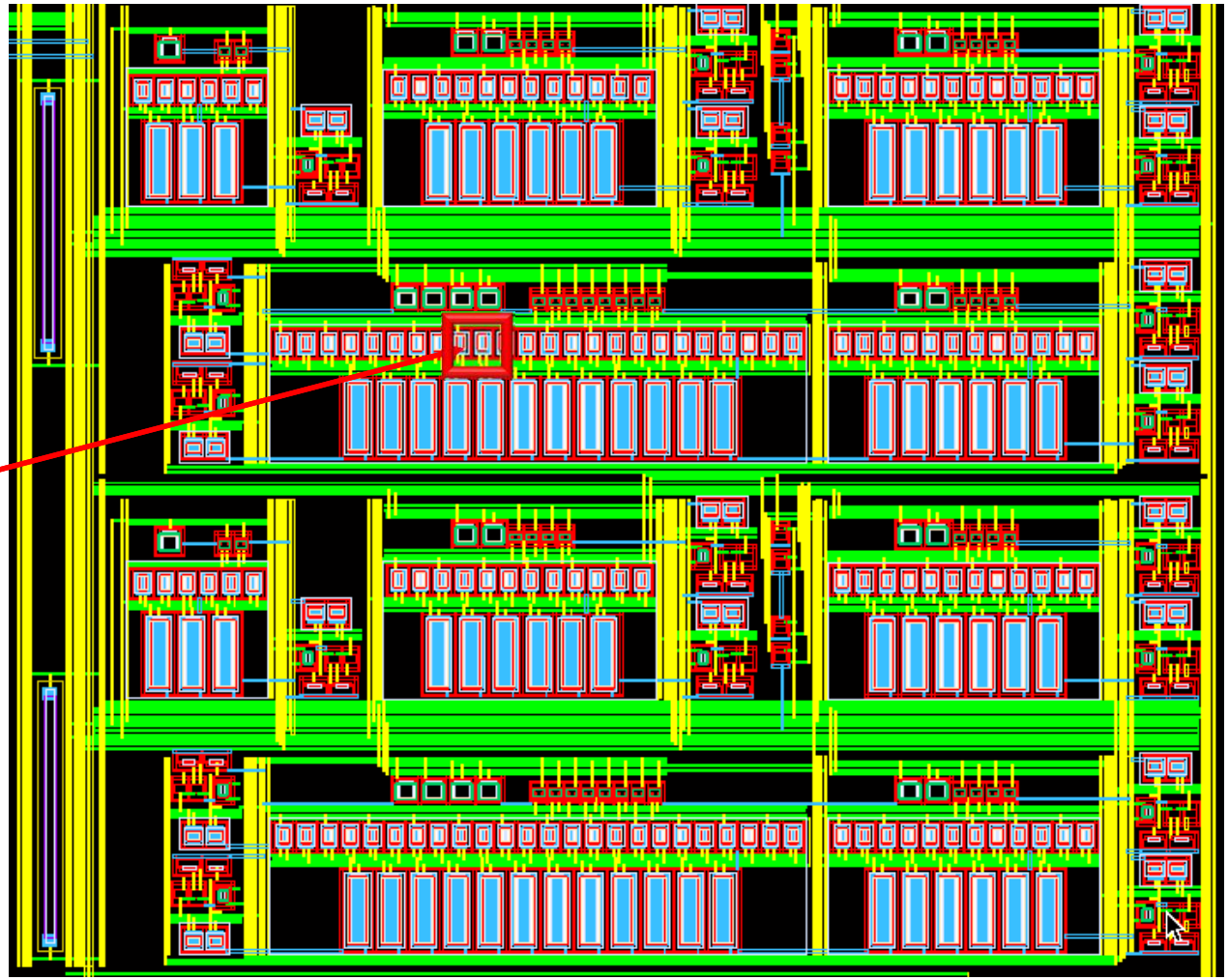
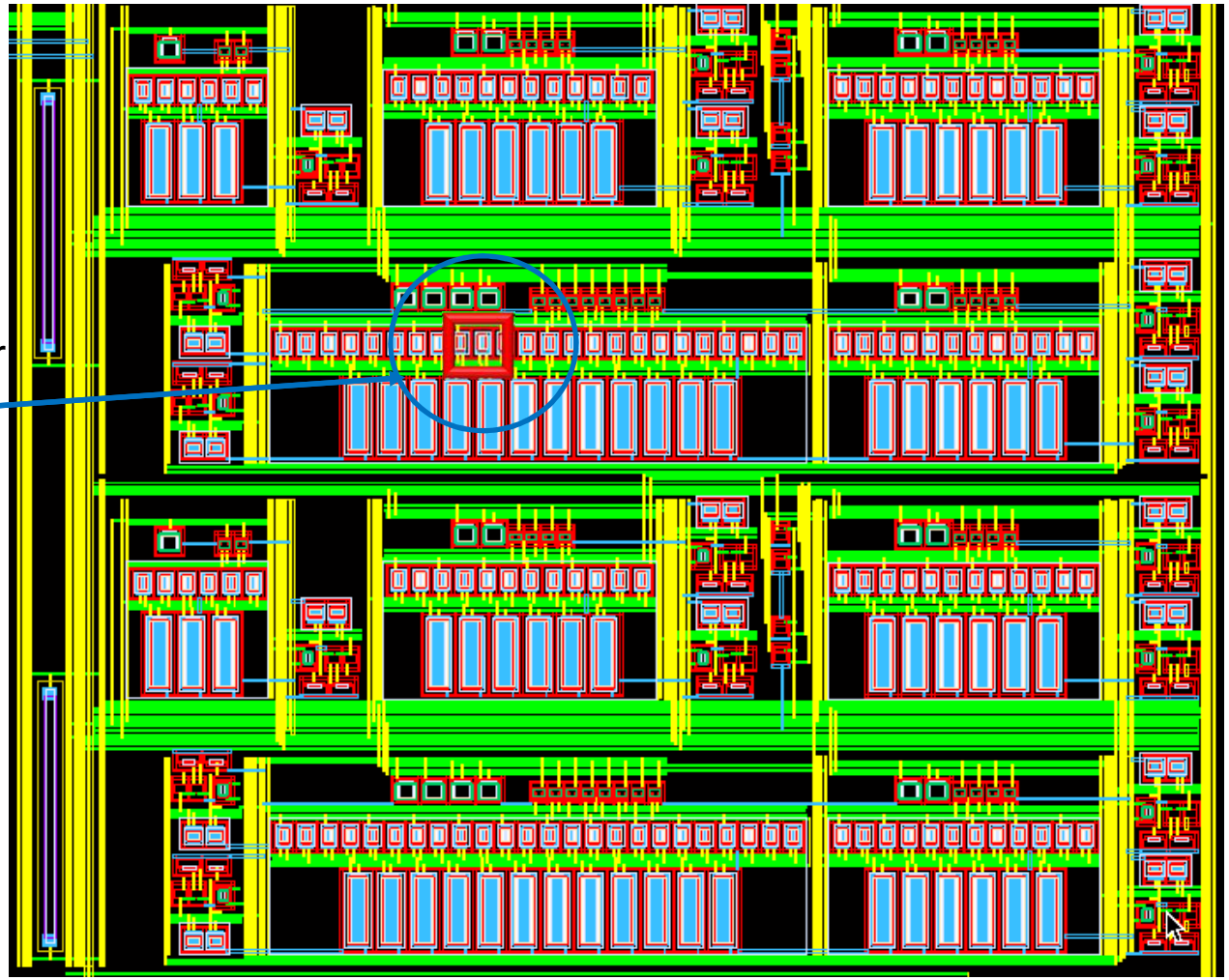


Future work

- Objective : create a SEE sensitivity map

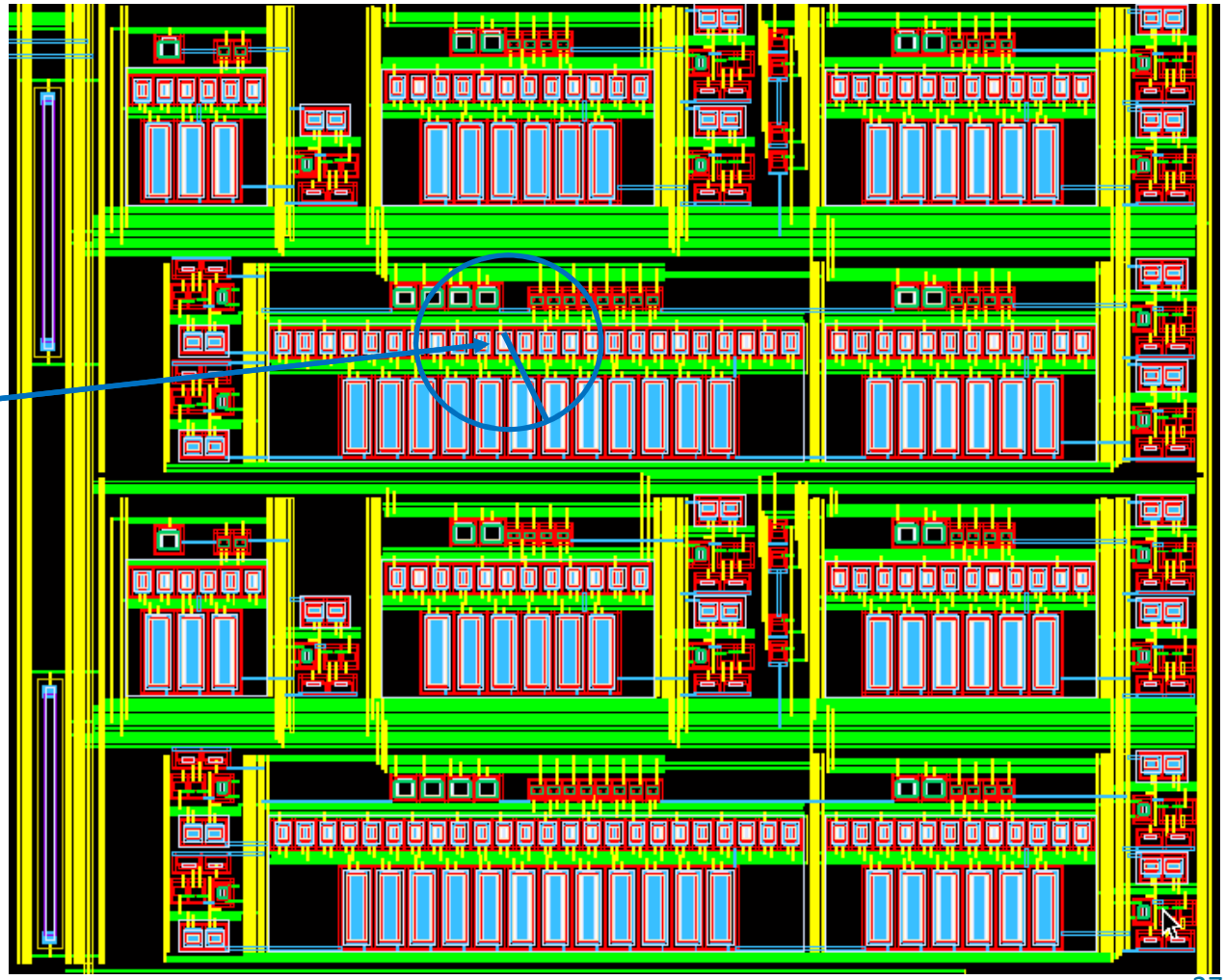
Influence on neighbour transistors



Future work

- Objective : create a SEE sensitivity map

Transistors inside an influence area should be taken into consideration for SEE emulation



Conclusions and future work

- A preliminary tool for automatic inspection of SEE in analog schemes has been developed.
  - Allows a rapid analysis of critical nodes at schematic level.
  - Technology independent.
- Future work
  - Experimental verification of results.
  - Implementation of alternative SEE models.
  - Extension of the analysis to layout level.

Future work

- Objective : create a SEE sensitivity map
  - Several transistors can be affected by an impact
  - Need of incorporing layout information to simulations
  - Use of geometrical criteria to define the test benchs →

→Emulation of impacts influence on neighbour transistors

Thanks for your attention

Contact:

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