Future Sensor-Chip Packaging Technologies at CiS

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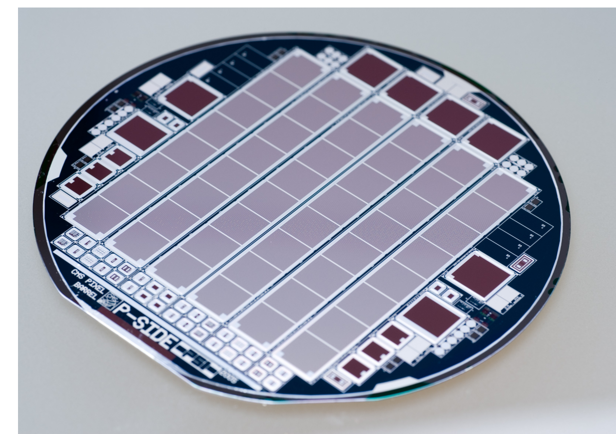
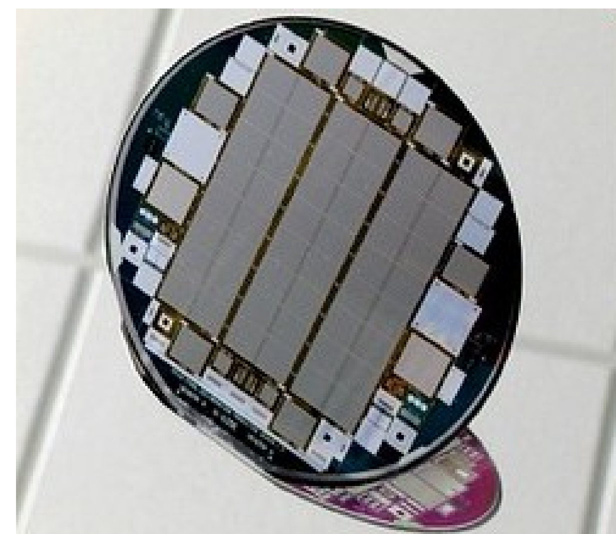
motivation

- CiS as a vendor of planar Si sensors
  - CiS has significantly contributed to sensor productions of various HEP experiments in past and present
    - ATLAS pixel, CMS pixel, ...
    - ATLAS IBL, CMS pixel upgrade



- involvement of CiS ended after wafer production
- idea: participate at the sensor/module processing as long as possible, i.e. up to bump bonding assembly step
  - technological requirements are present
    - in-house
    - outsourcing
  - reduction of unnecessary steps: packaging, shipments
  - technological value added
  - possibility of providing
    - flip-chip-able sensors
    - complete sensor-chip assemblies



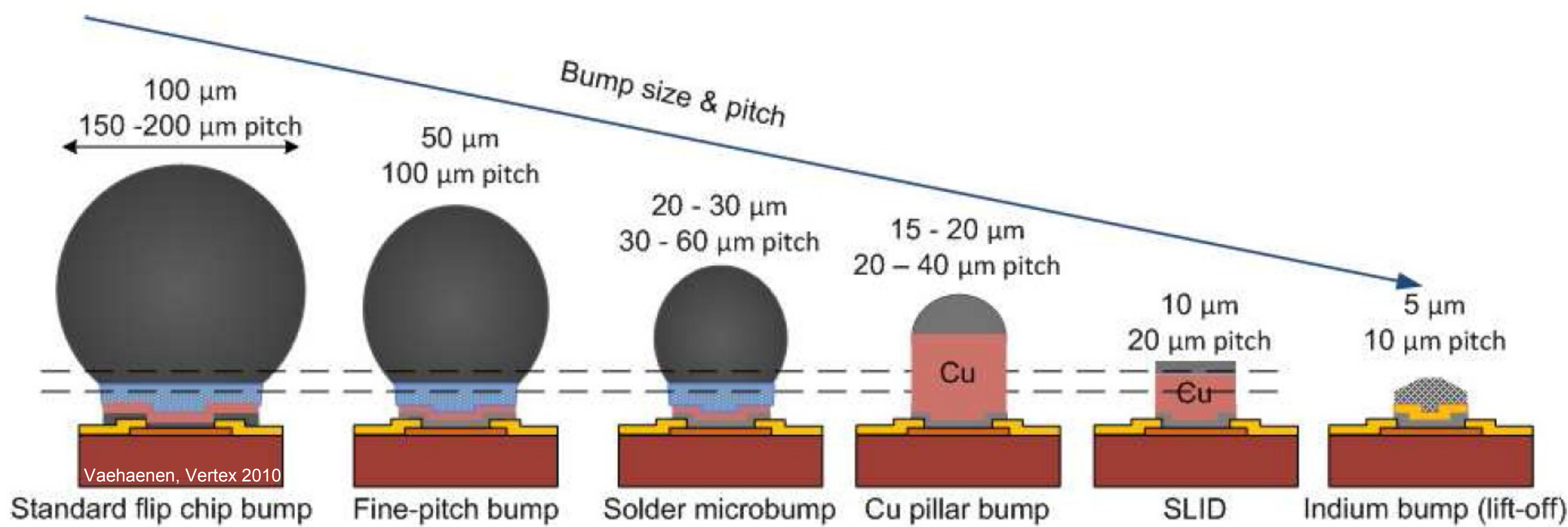
challenges for future bump bonding concepts

large radii

- bump bonding still one of the main cost driver
- cost reduction is essential
- batch wise processes preferable
- minimization of dimensions is secondary

small radii

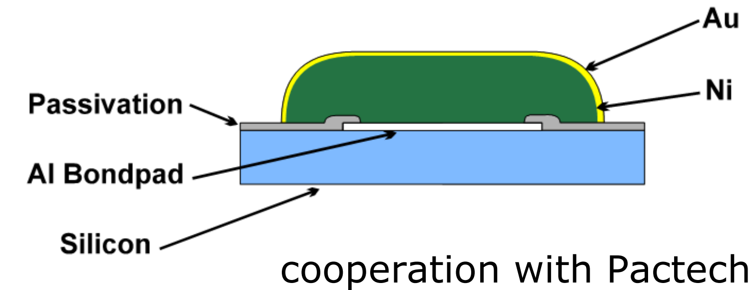
- minimization of bump size & pitch
- e.g. ATLAS:
  - pitch 50µm -> 25µm
  - => bump size < 25µm
- radiation hardness



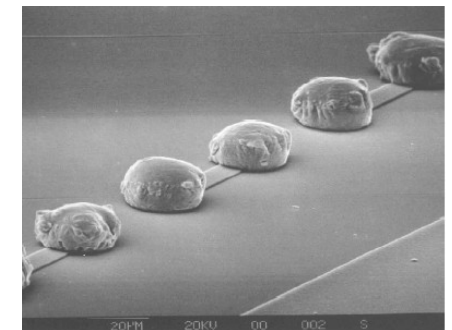
electroless Ni-UBM + solder ball bumps

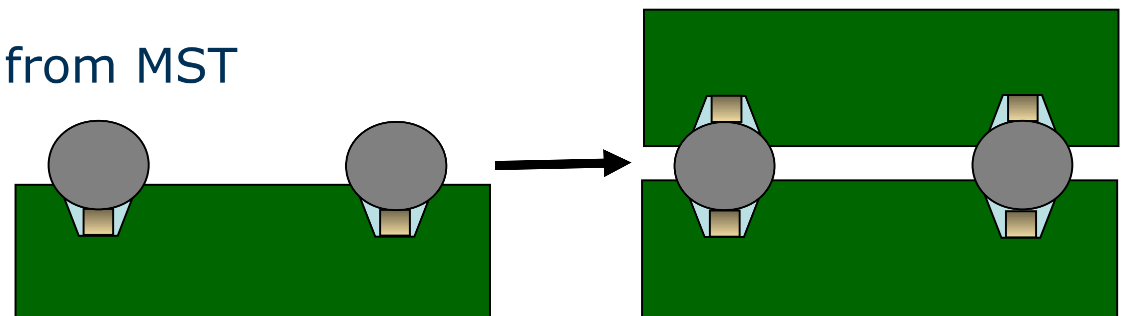
- wet-chemical
- passivation is used as a mask, no additional mask necessary
- optimizations of
  - AlSi quality
  - pretreatment steps
  - Ni-electrolyte for very small pad openings

- option to place contact pads into a cavity
  - simplification for flip-chip positioning? esp. if aiming at small dimensions
  - if lowering of pads in cavities prove to be an advantage for flip chip positioning, cavities could also be implemented on ASIC by polymer layers
  - experiences are existing at CiS from MST

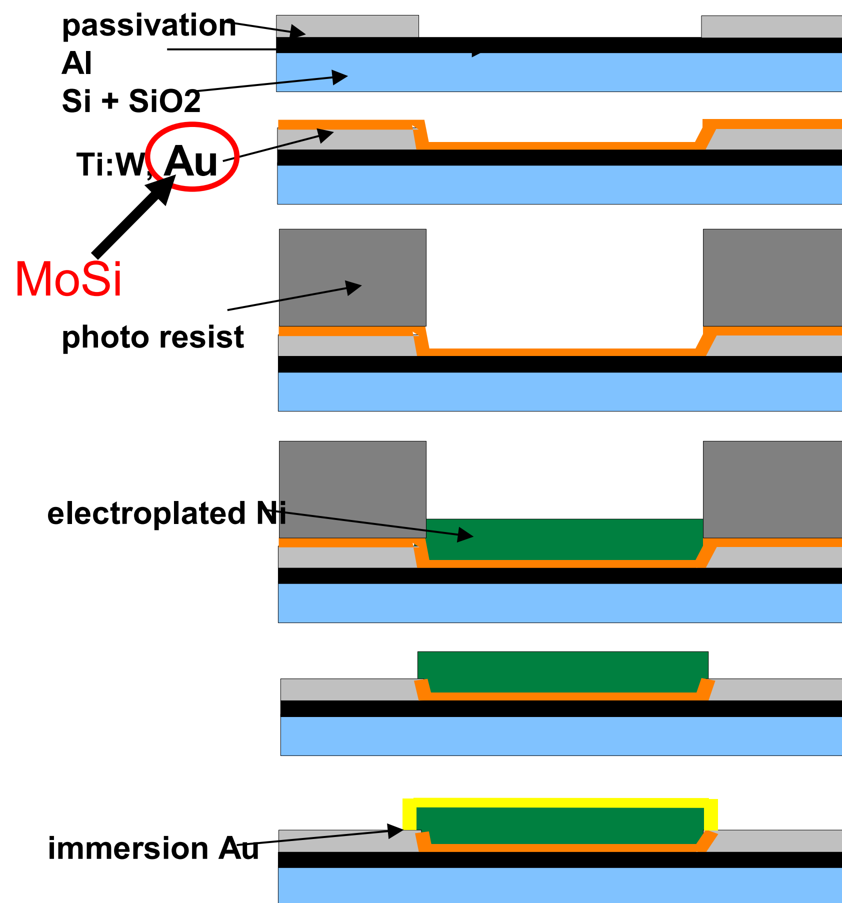


cooperation with Pactech

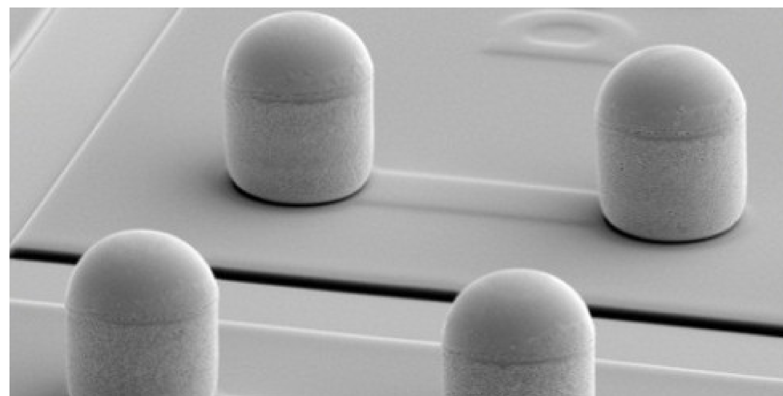




MoSi based electroplating

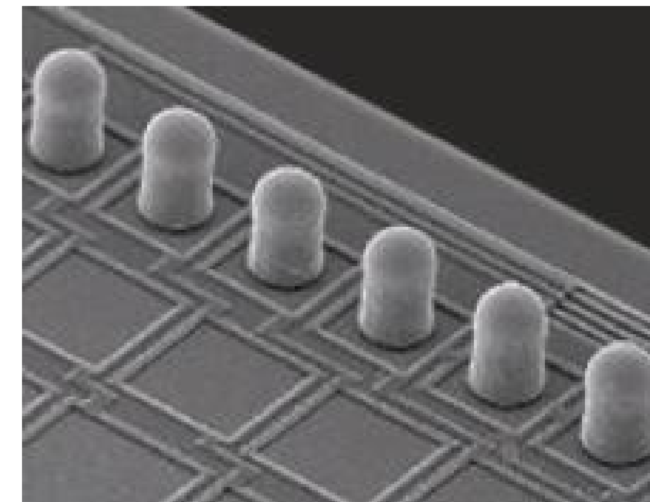


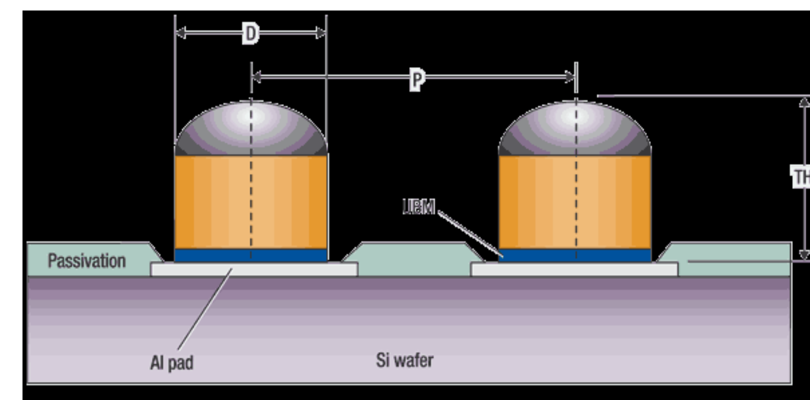
- Au/Cu plating base can be replaced by MoSi
  - properties are expected to be similar
- process could be conducted completely in-house

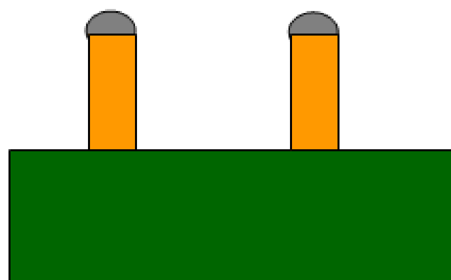


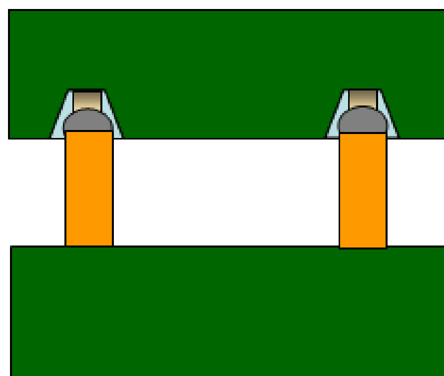
Copper Pillars

- building of pillars by combination of thick film lithography and electroplated copper deposition
- top is tin-coated, act as solder
- small diameter feasible
- esp. advantageous in combination with cavity contacts



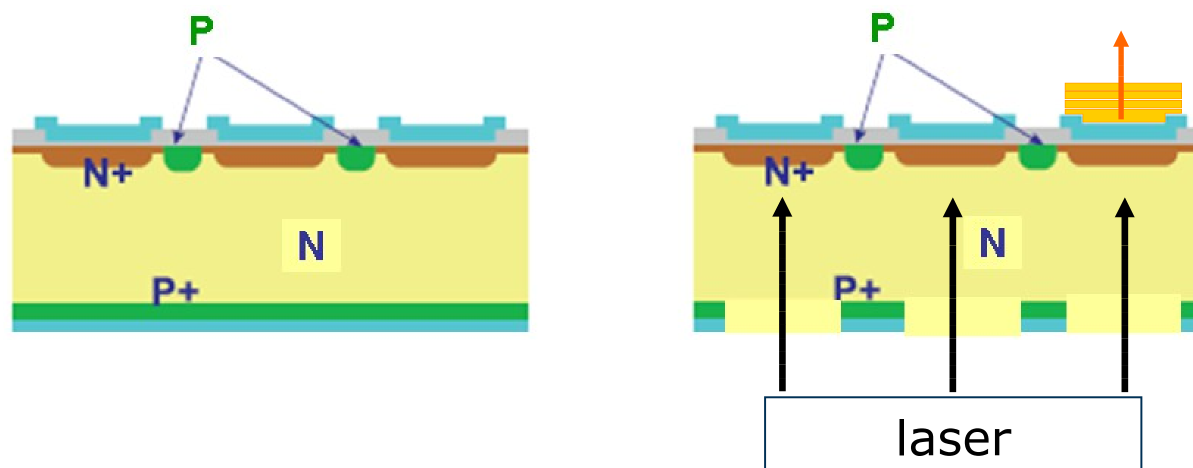






LIP-Ni - light induced plating

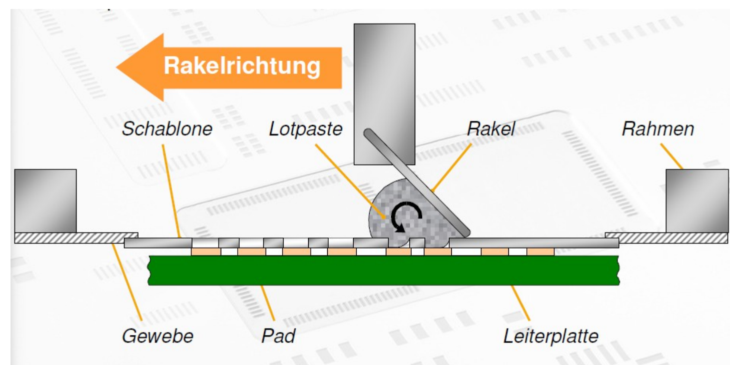
- concept from photovoltaics sector
- epitaxial growth of the UBM is stimulated by a laser
- UBM is only growing on the passivation openings
- openings in the back side metal could be necessary
- no additional process steps necessary
  - no plating base / resist
  - no stripping / etching
- less cost & time consuming



cooperation with TU Illmenau

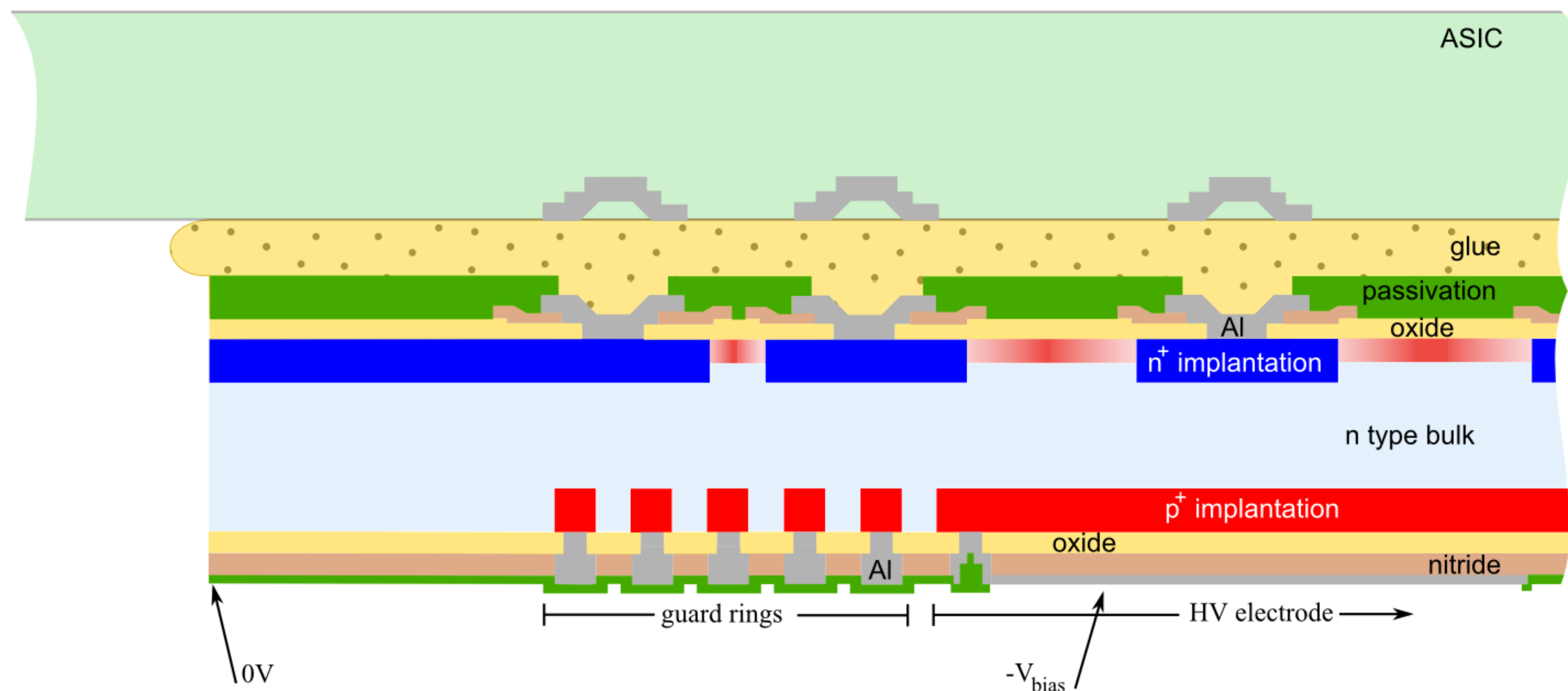
mechanical alternatives

- Studbumping
  - e.g. on ASIC side in combination with Ni-UBM & Sn bump on sensor
- minimization of screen printing
- optimization of stencil printing
  - already available with 20µm openings
  - investigation of very fine-grained powder as solder paste



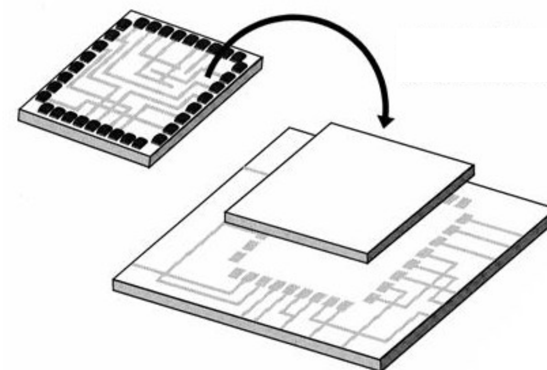
capacitive coupling

- sensor and ASIC are glued together
- significant cost reduction could be achieved
- initial tests with CiS n-in-n sensors have started
  - advantage that pixel side is completely on ground
  - HV & ground potential can be applied via back side
  - Uni Bonn, Uni Geneva, TU Dortmund

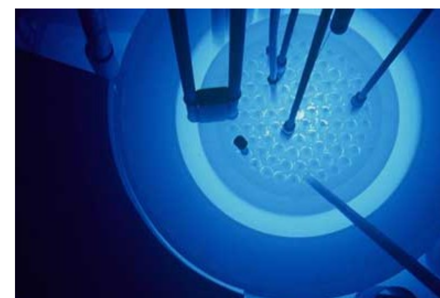


strategy

- testing of flip chip process itself
  - daisy-chain dummies
  - real sensors & ASICs

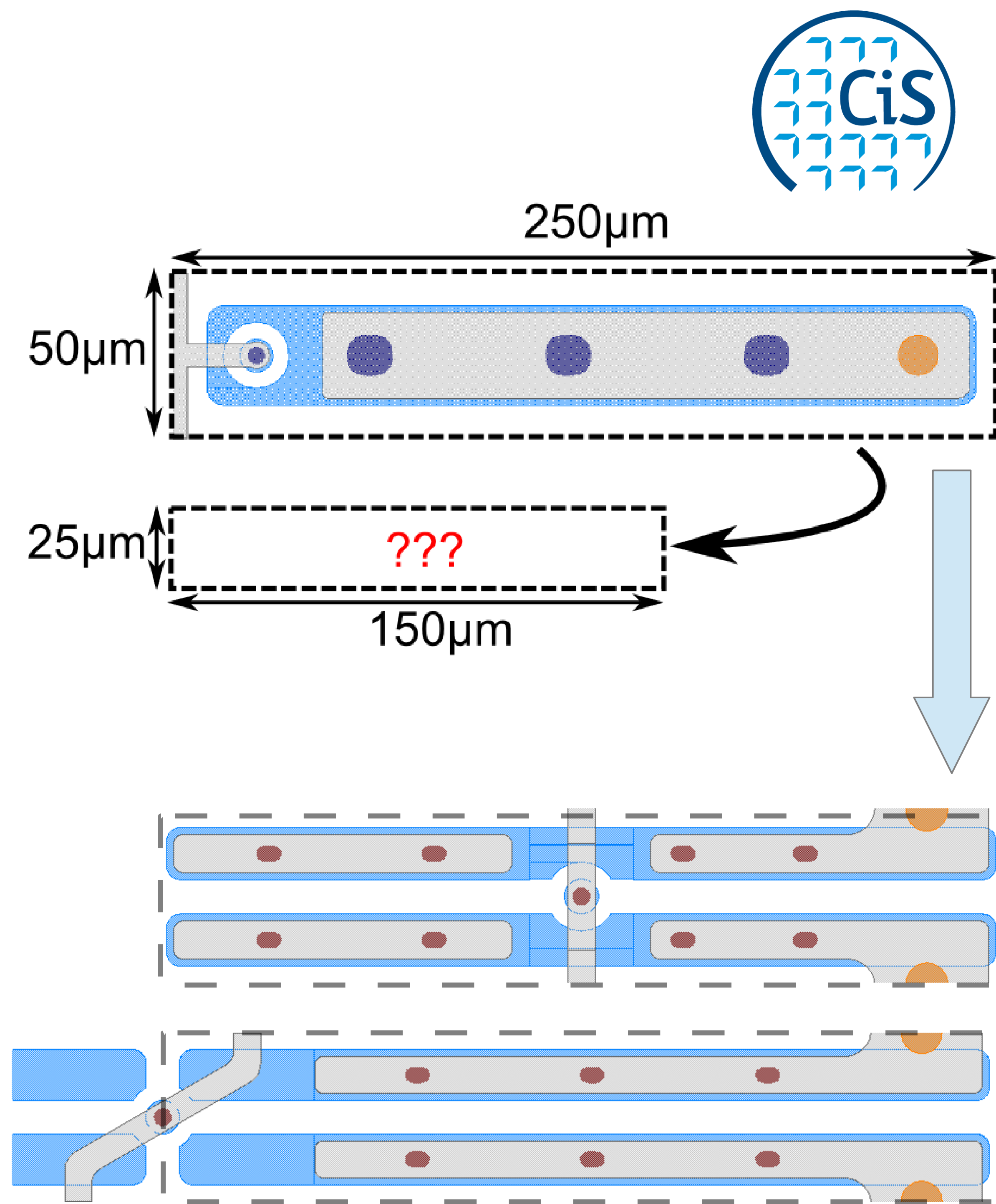


- testing of reliability
  - defect engineering
    - establish automatical optical inspection
  - stress tests
    - operation at low temperatures
    - fast temperature cycles
    - irradiations up to HL-LHC fluences



sensor design challenges

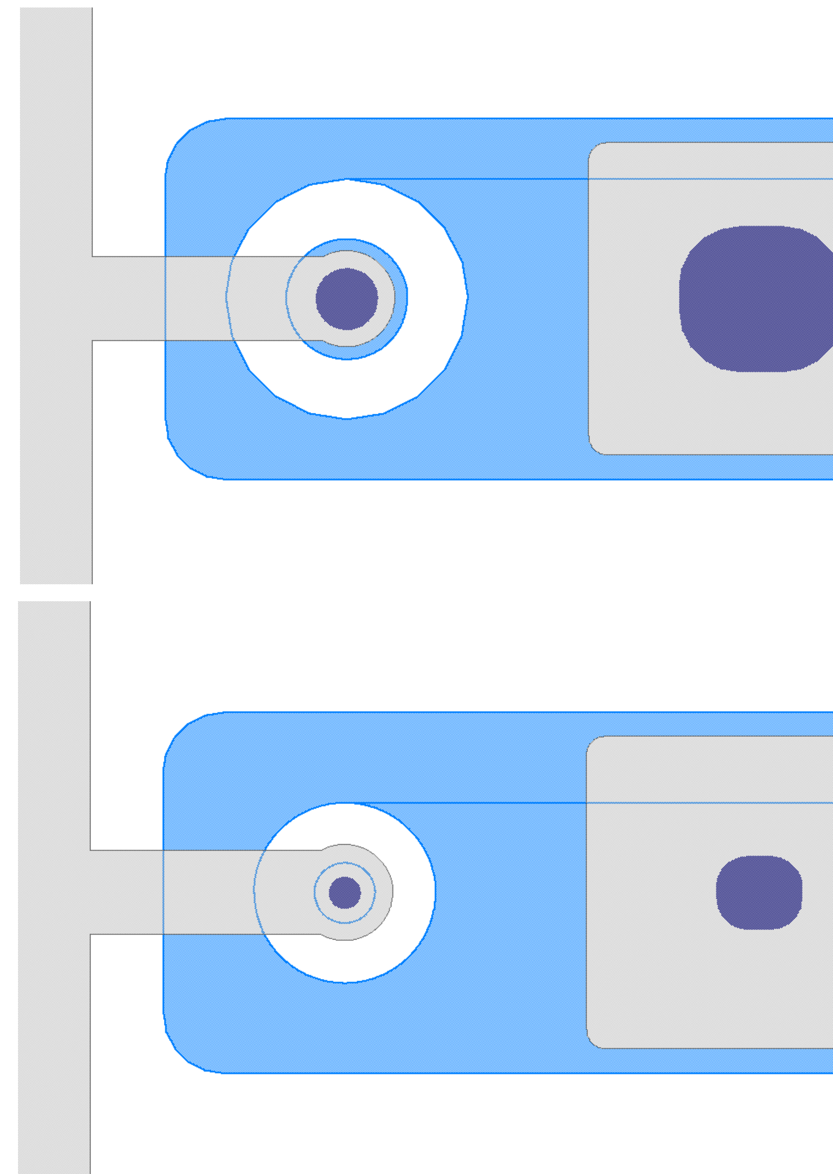
- smaller pitch aswell represents challenge to future sensor designs
- esp. conventional bias grid is not usable anymore
- testing different bias grid versions on current wafer productions
- variations of
  - bias dot position
  - bias dot diameters
  - pixel implant width



sensor design challenges

laser direct imaging (LDI)

- alternative to the currently used projection exposure
- no masks necessary anymore
- expect to be able to process smaller dimensions (O(2-3µm))
  - implantations
  - oxide openings
- current production combines projection exposure and LDI



conclusion

- besides the production of planar Si-sensors for HEP experiments, CiS is aiming for an extension of the possibilities of sensor-chip packaging
- points of interests are
  - cost reduction
  - minimization of the bump dimensions
- various technological approaches are planned
- as many process steps as possible should be done in-house
- the possibility to produce complete sensor-chip assemblies is given