INFN-Torino in RD50

We would like to join RD50 to work on the development of UFSD

The group is currently made of 5-6 persons, plus a PhD student and two undergraduates.

Given our strong VLSI group, we are interested in working on the concurrent development of the sensor and the electronics.

➔ We want to concentrate on the study of the optimization of the sensor's parameters to match a possible read-out chip.

We want to pursue this project by leveraging on our expertise in several aspects:

1. Fully equipped silicon lab (CV, IV, laser, thermal boxes…)
2. Use the VLSI chip developed for NA62: these chips are ready to be used, need to develop the appropriate USFD sensors
3. Start the development of dedicated VLSI chips
4. Collaboration with the FBK team that has worked on SiPM (Boscardin, Piemonte, Dalla betta)
5. Advanced mechanical and electronic shops
6. Use our connection with SELEX for bump-bonding

UFSD: Ultra-Fast Silicon Detector

- Basic goals of UFSD
- A parameterization of time resolution
- State of the art of current pixel detectors
- The effect of gain
- What can we do next

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with
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UFSD goals

Create a silicon detector with a factor of ~ 10 larger signal

1) **10 - 20 ps time resolution:** large signals allow for much better timing capabilities

2) **Very high rate capability:** excellent counters for charge particles

3) **30 - 50 μm thin detector:** ideal for low mass system

4) **Very rad-hard**: charge trapping has a moderate effect

Here I examine 1) & 2), most relevant to our current research

3) & 4) are a direct consequence of larger signals

Current Silicon sensor R&D

Sensors

Radiation Resistance
- Vert. Electr., 3D
- n-in-n
- n-in-p
- Silicon Substrate (FZ, CZ)
- Diamond
- CMOS 3T, 4T pixel

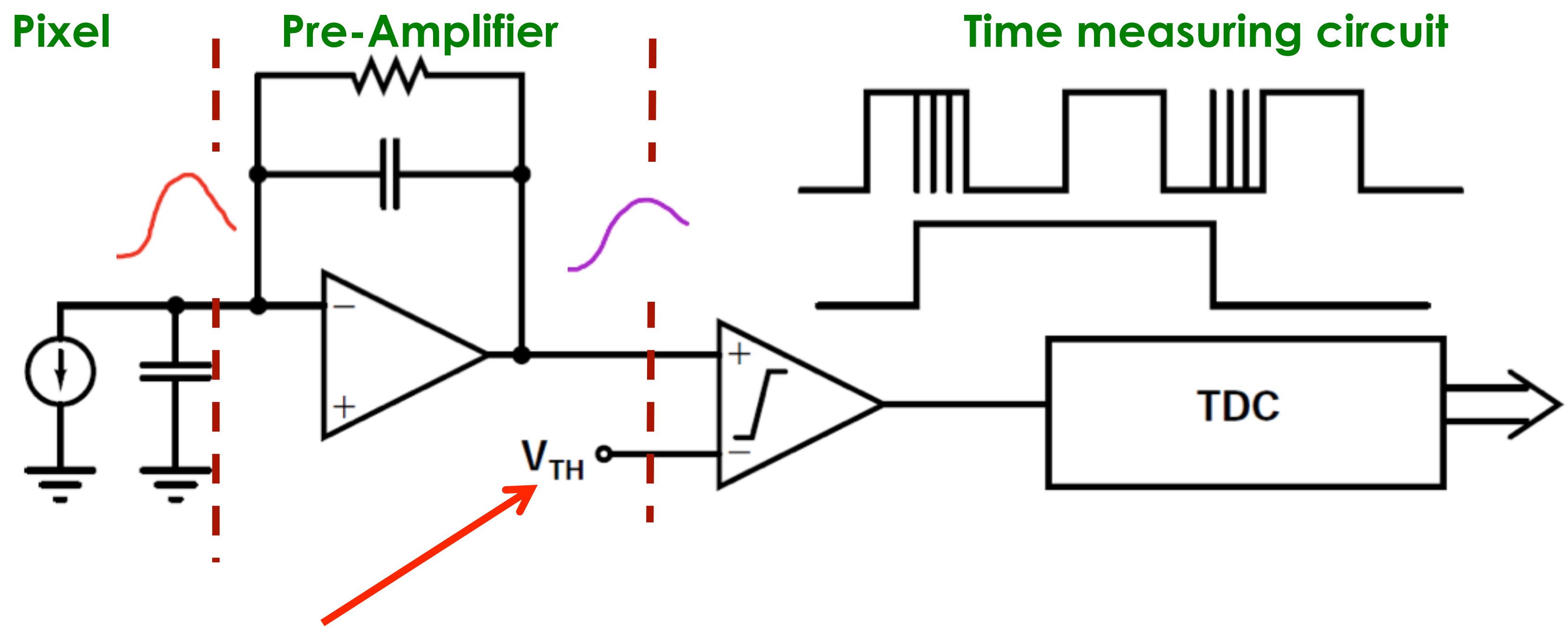
Integrated
- Semi-monolithic, DEPFET
- CMOS monolithic, MAPS
- SOI
- HV CMOS, LePix
- 3D IC

Low Mass
- Thinned
- Self Supporting
- Active Edge
- Vertical Vias
- Micro-channel cooling

Large signal
- UltraThin
- **ps precision**
- **GHz rate**
- Very rad-hard

Need appropriate electronics

UFSD: a time-tagging detector



Time is set when the signal crosses the comparator threshold

The timing capabilities are determined by the characteristics of the signal at the output of the pre-Amplifier and by the TDC binning:

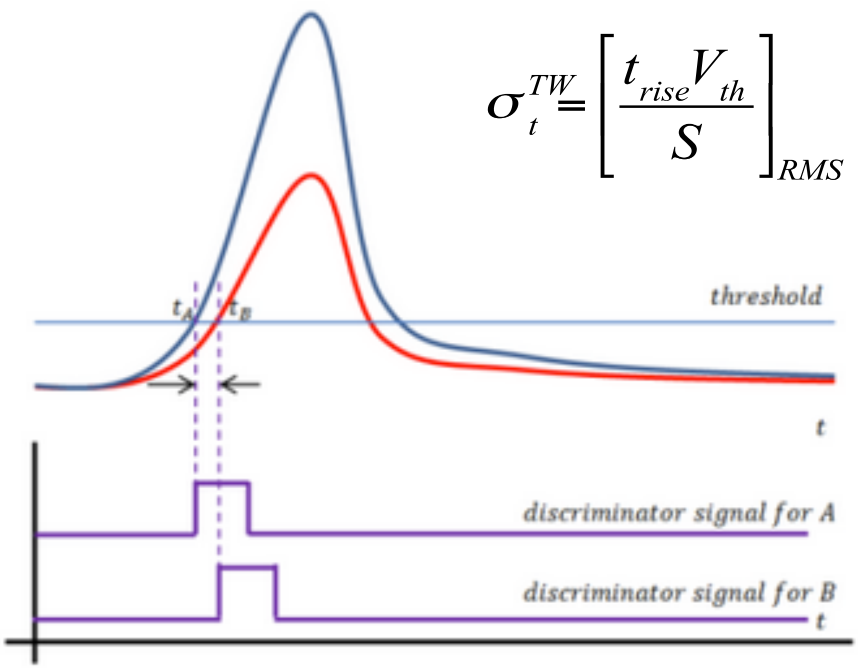
$$\sigma_{Total}^2 = \sigma_{Jitter}^2 + \sigma_{Time\ Walk}^2 + \sigma_{TDC}^2$$

Time walk and Time jitter

Time walk: the voltage value Vo is reached at different time for signal of different amplitudes

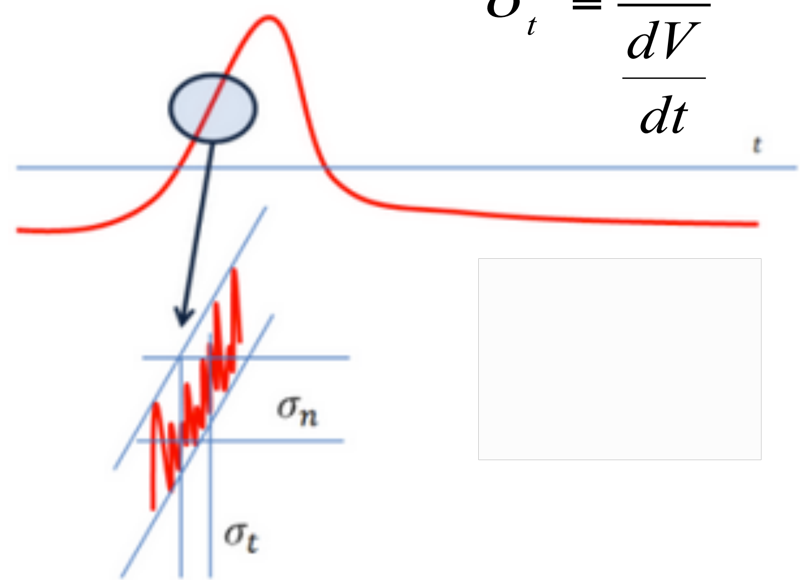
Jitter: the noise is summed to the signal, causing amplitude variations

$$\sigma_t^{TW} = \left[\frac{t_{rise} V_{th}}{S} \right]_{RMS}$$



Time walk effect

$$\sigma_t^J = \frac{N}{\frac{dV}{dt}}$$



Jitter effect

Due to the physics of signal formation

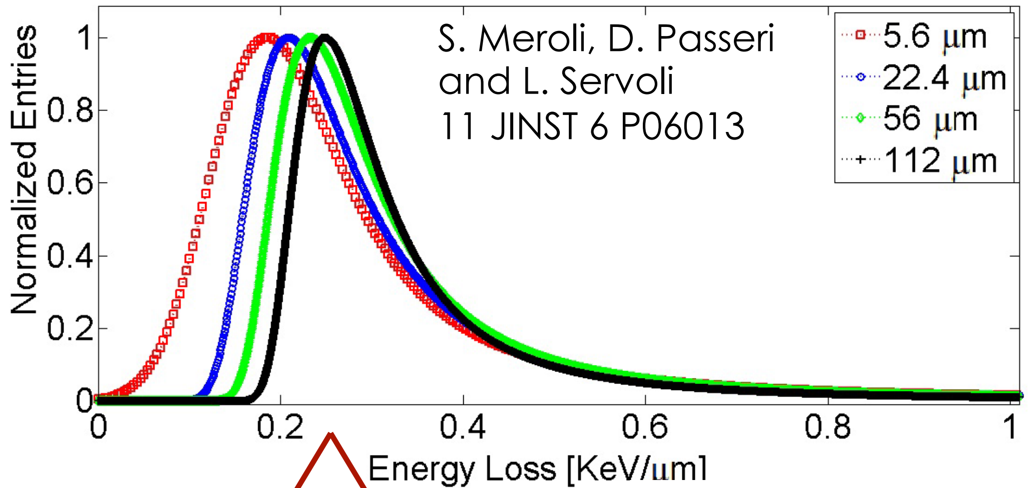
(see backup slides for full calculation and reduction techniques)

Mostly due to electronic noise

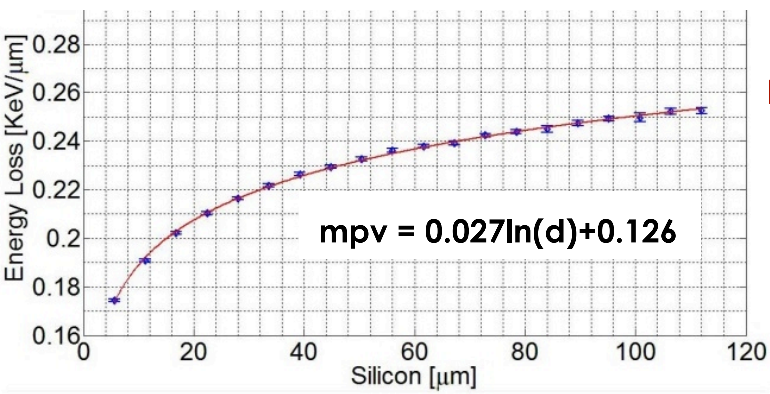
(see backup slides for capacitance and noise values used)

Details of Collected Charge in Sensors

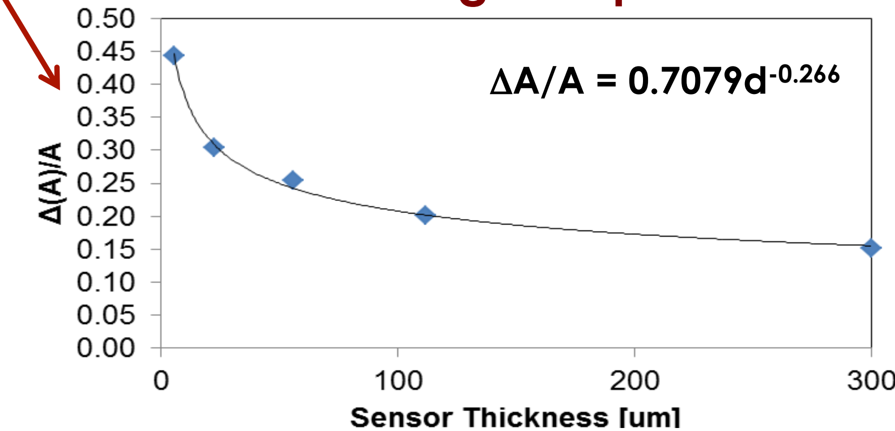
To calculate time walk, we need a parameterization of the energy loss



Most Probable Value



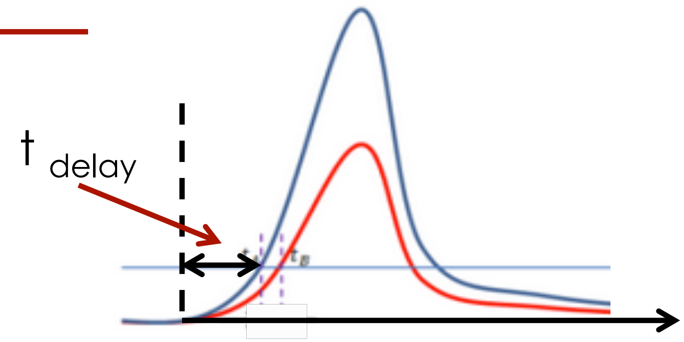
Pulse Height Dispersion



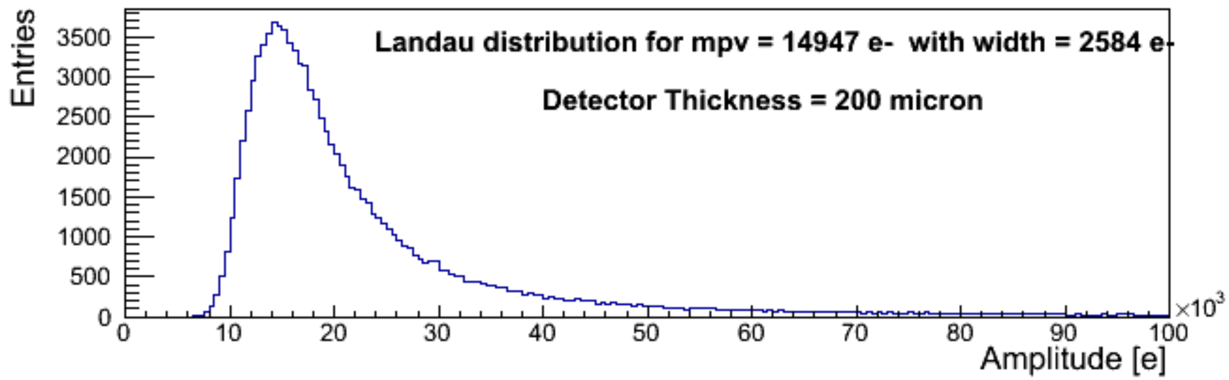
- Thin sensors have a lower yield of e-/h pairs **per micron,**
- Their signal amplitude spread is larger

Time walk calculation

Signals cross a given threshold with a delay that depends on their amplitude, on the rise time and on the value of the threshold:



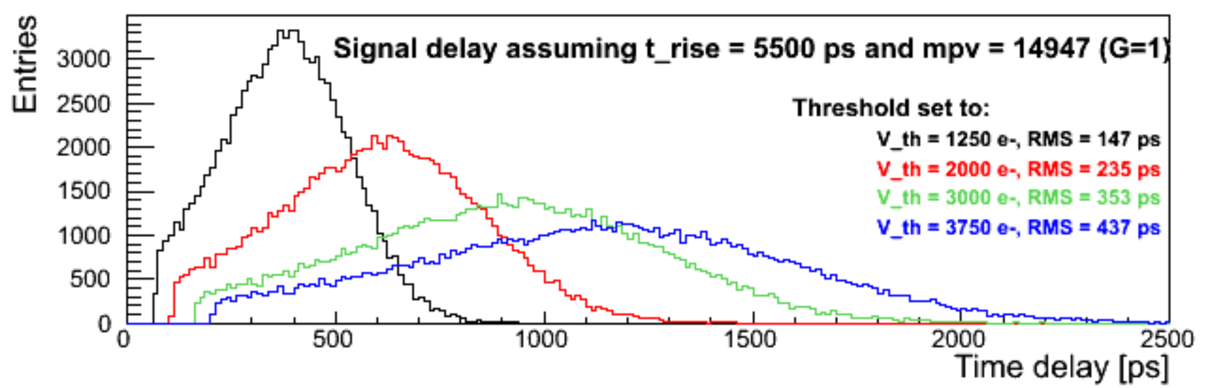
$$t_{delay} = t_{rise} \frac{V_{th}}{V}$$



The rms of the time delay is a measure of the time walk.

$$\sigma(t_{delay}) = 40 - 80\,ps$$

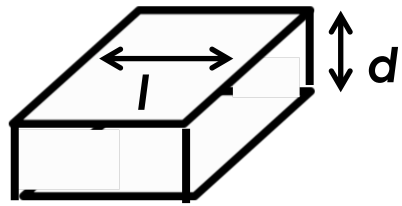
The electronics will reduce this value using time walk compensating circuits



A parameterization of σ_t

$$\sigma_t^2 = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{t_{rise}V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2 \qquad \textbf{(1)}$$

Jitter — Time Walk — TDC



d: detector thickness [micron]

l: pitch [micron]

C: Detector capacitance [fF]
Depends on the pitch and thickness

N: Noise at preamp.
Dominated by the voltage term

S: Signal

t_{rise}: Pre-Amp Shaping time

V_{th}: Comparator threshold
Depends on the noise level

TDC:Width of the TDC LSB [ps]

$$C_{Det} = \varepsilon\varepsilon_o \frac{l*l}{d} + 0.2*4l + 50$$

$$N \propto \frac{C_{Det}}{\sqrt{t_{rise}}}$$

Use eq. slide (7)

$$V_{th} = 10*N$$

$$LSB = 20$$

What is the best shaping time (t_{rise}) ?

$$N \propto \frac{C_{Det}}{\sqrt{t_{rise}}}$$

$$S \propto \begin{cases} t_{rise} \xrightarrow{if} t_{rise} \leq t_{col} \\ Const \xrightarrow{if} t_{rise} > t_{col} \end{cases}$$

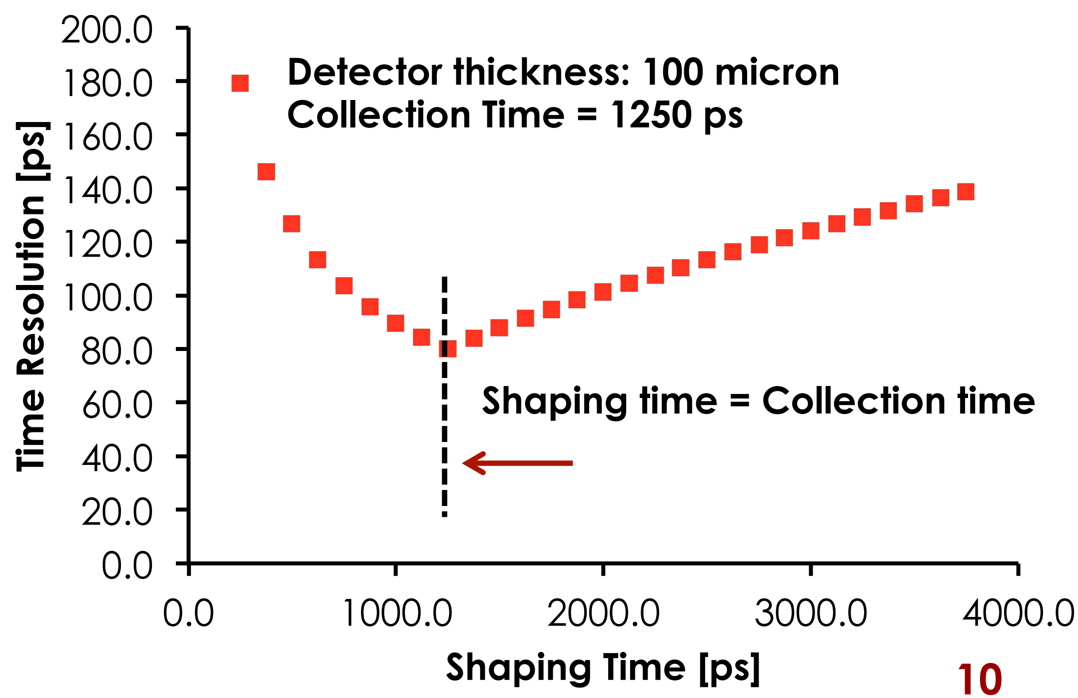
$$V_{th} \propto N$$

$$\Rightarrow \sigma_t \propto \begin{cases} \frac{C_{det}}{\sqrt{t_{rise}}} \xrightarrow{if} t_{rise} \leq t_{col} \\ C_{det} * \sqrt{t_{rise}} \xrightarrow{if} t_{rise} > t_{col} \end{cases}$$

To minimize time resolution:

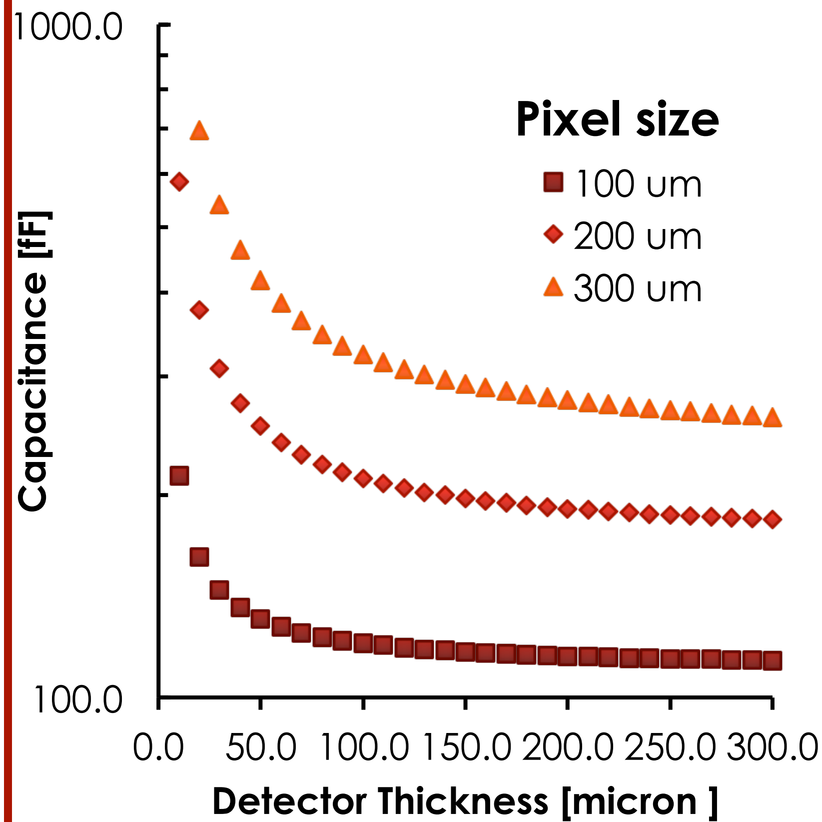
$$t_{rise} \sim t_{col}$$

Note: This value also minimizes fake signals in neighboring pixels.

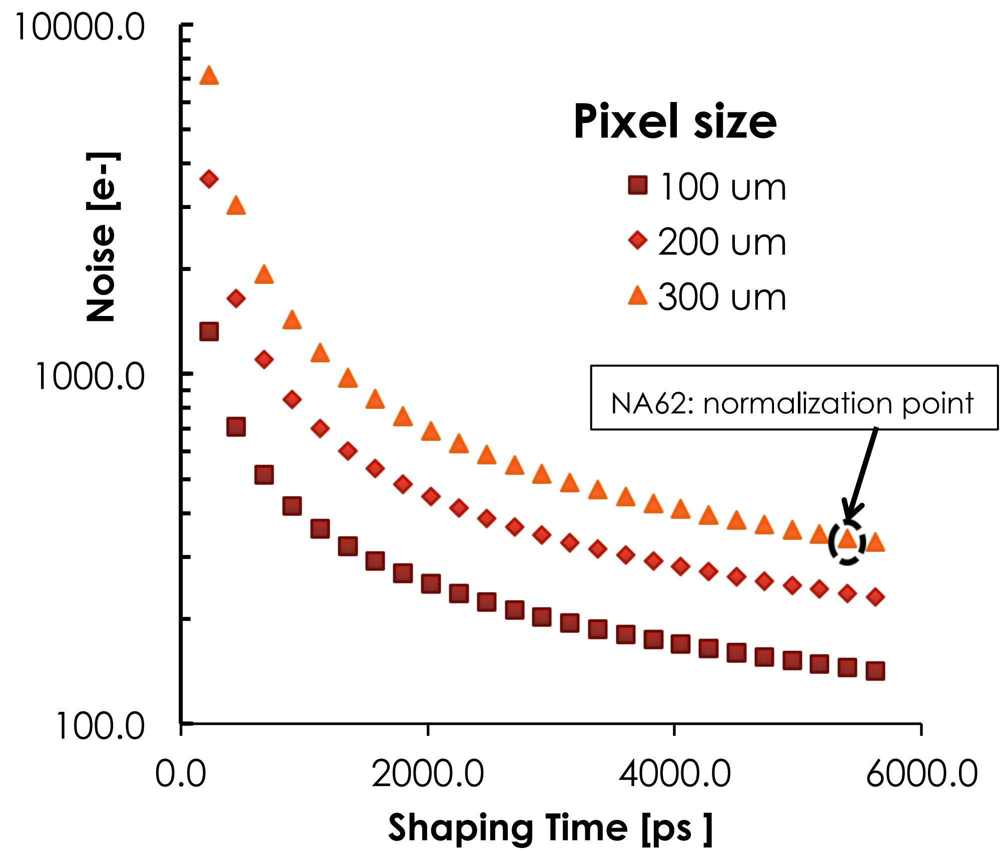


Values used in the parameterization

Capacitance vs Thickness



Noise vs Shaping Time



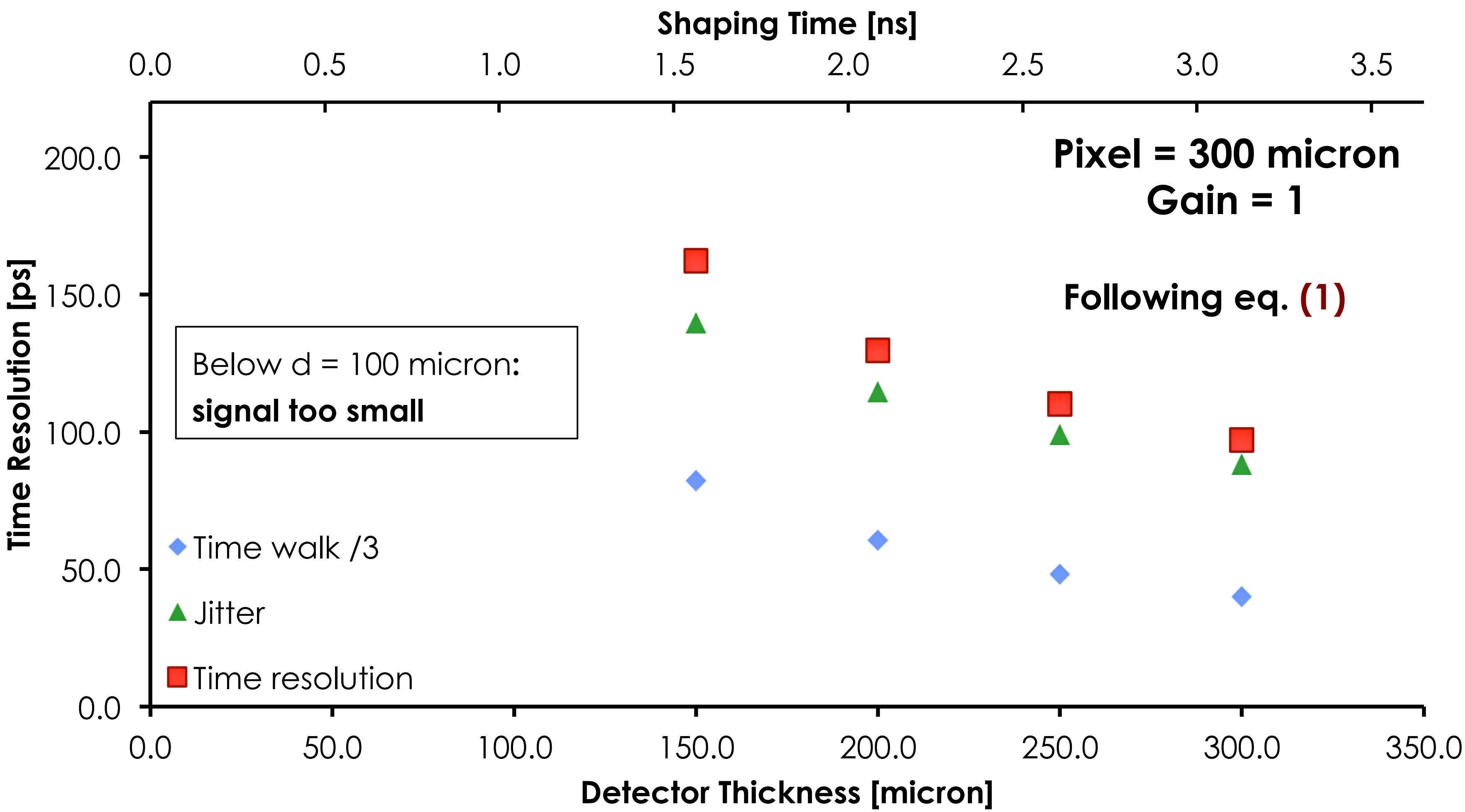
Capacitance:

backplane + 0.2 fF/μm (perimeter) + 50 fF (fix term)

Noise normalized to NA62:

Shaping time ~ 5500 ps, noise ~ 300 e-

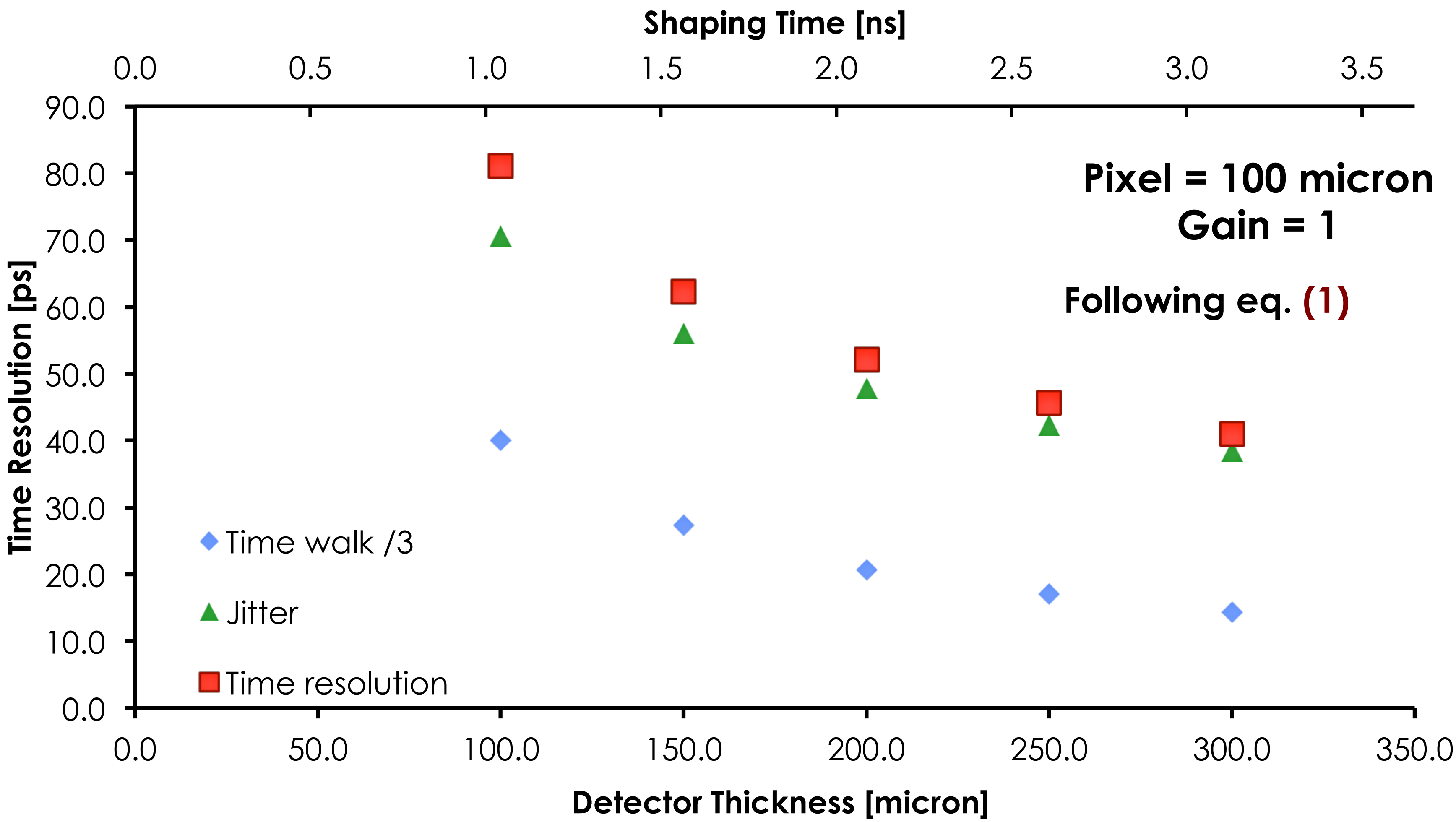
State of the Art



Best resolution achievable: ~ 100 ps

(assuming Time Walk reduction of ~ 3)

State of the Art



Best resolution achievable: ~ 50 ps

(assuming Time Walk reduction of ~ 3)

How can we do better?

$$\sigma_t^2 = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{t_{rise}V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2$$

Boost the signal: **introduce gain**

$$S \Rightarrow G * S$$

Impact ionization model: if the electric field is high enough, the carriers are multiplied according to:

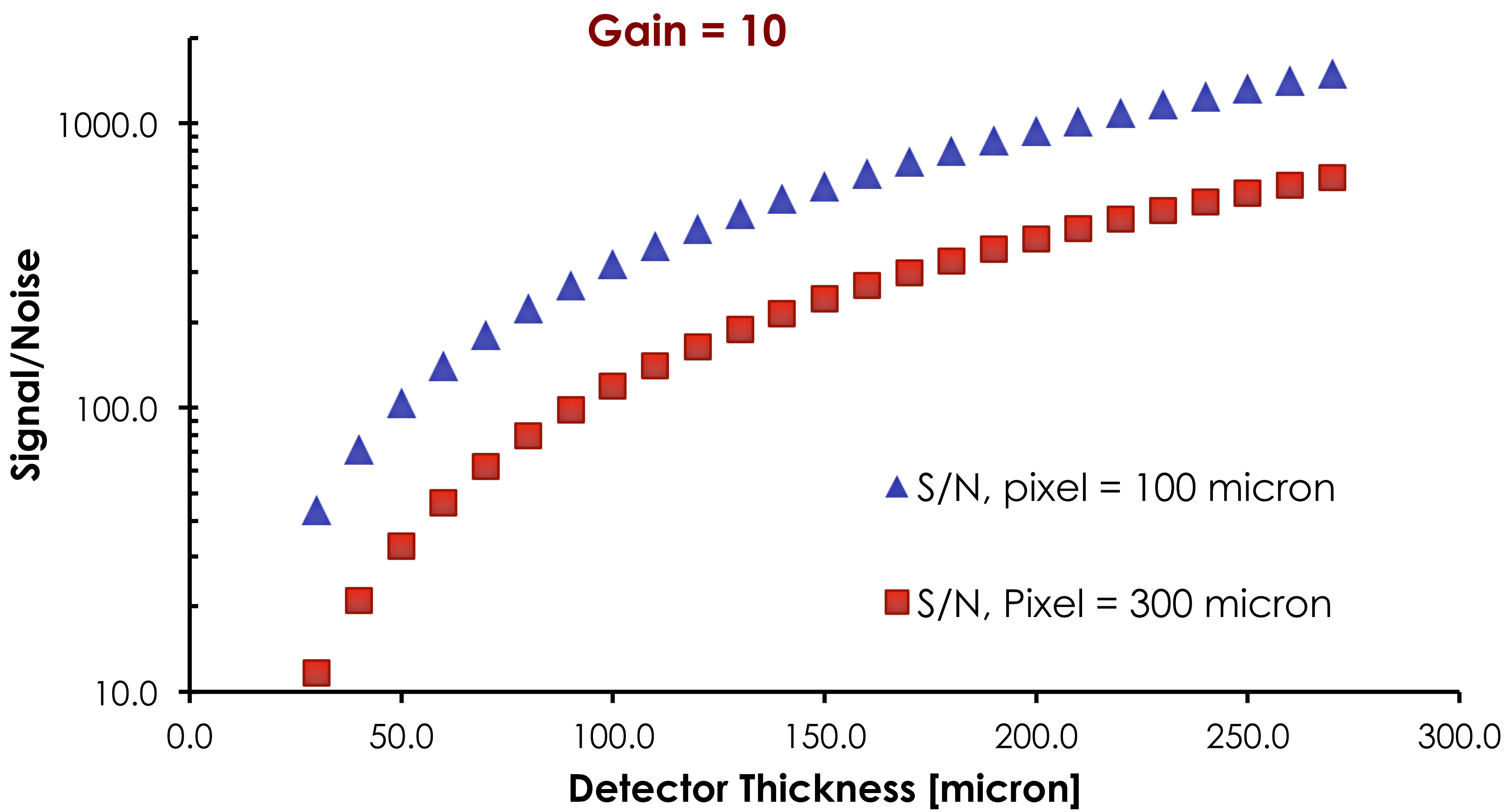
$$N(\ell) = N_0 * e^{(\alpha * \ell)} = G * N_0$$

In Silicon, at 270kV/cm:

- $\alpha_e \approx 0.7$ pair/μm
- $\alpha_h \approx 0.1$ pair/μm

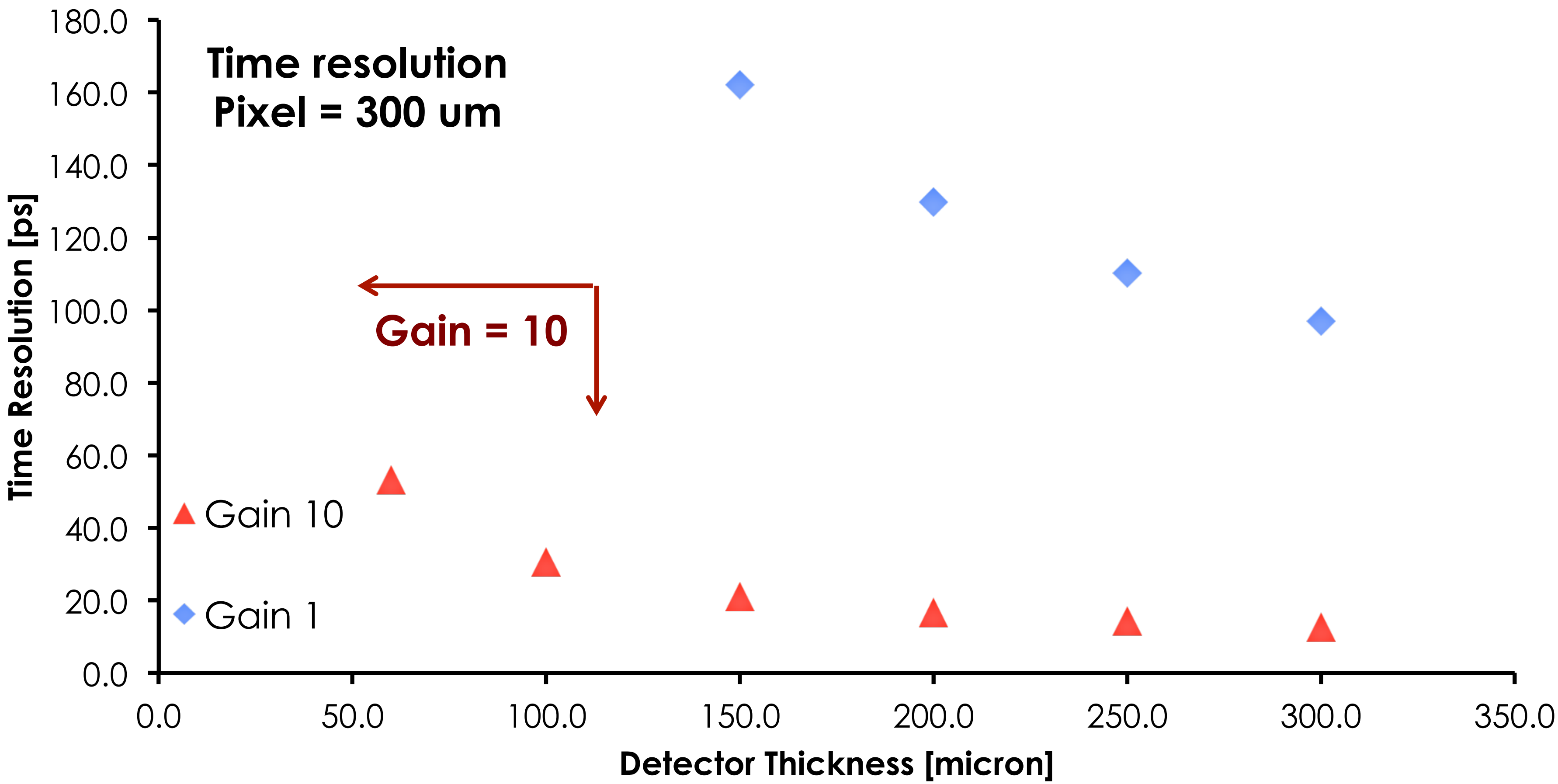
(see backup slides for details)

UFSD: Signal-to-Noise



UFSD offers an excellent S/N ratio even with very thin detectors

The effect of gain



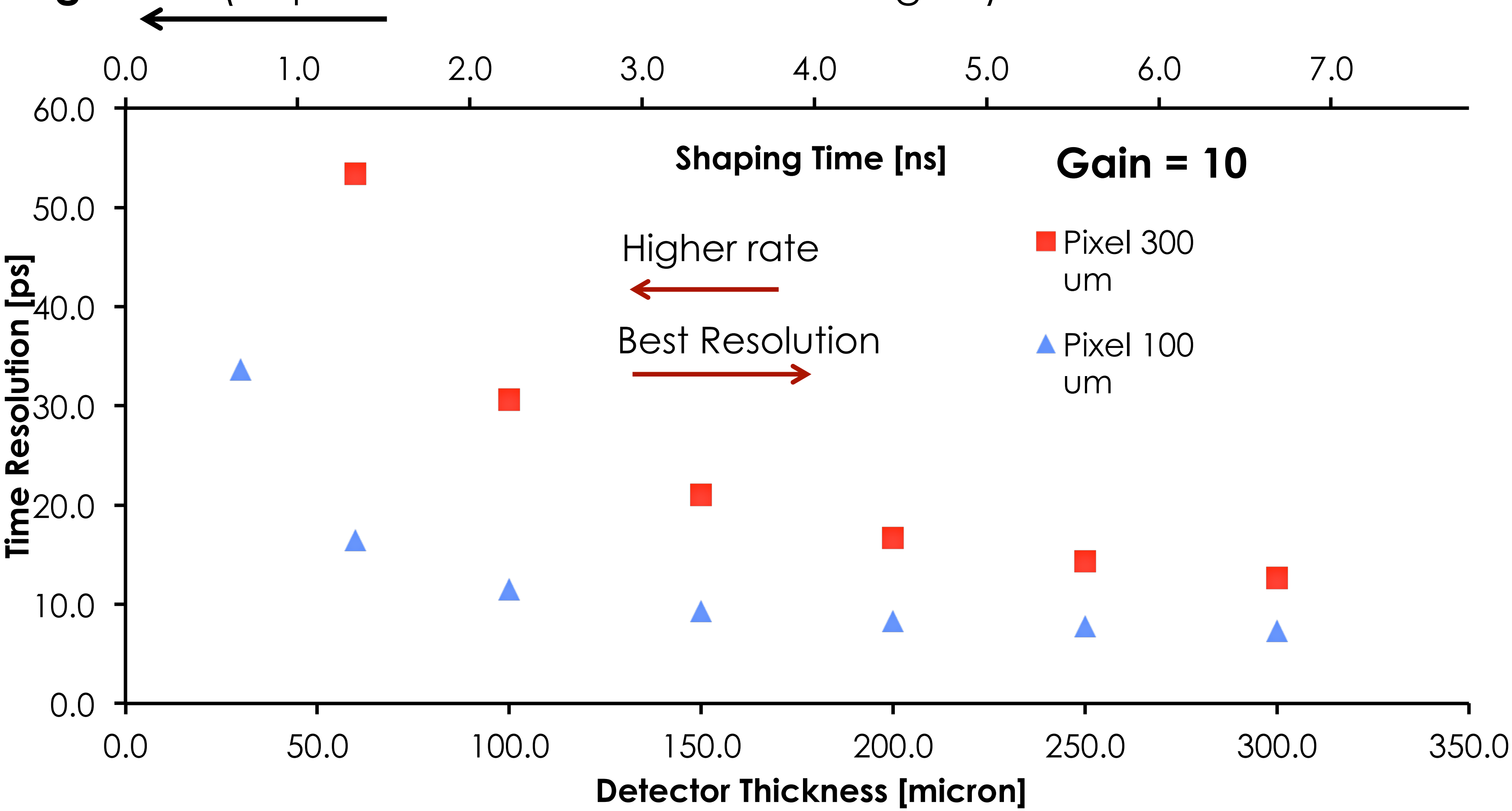
Effect of gain: thinner detectors and smaller time resolution

Best resolution achievable ~ 15 ps

(assuming Time Walk reduction of ~ 3)

Resolution for 100 and 300 μm pixel

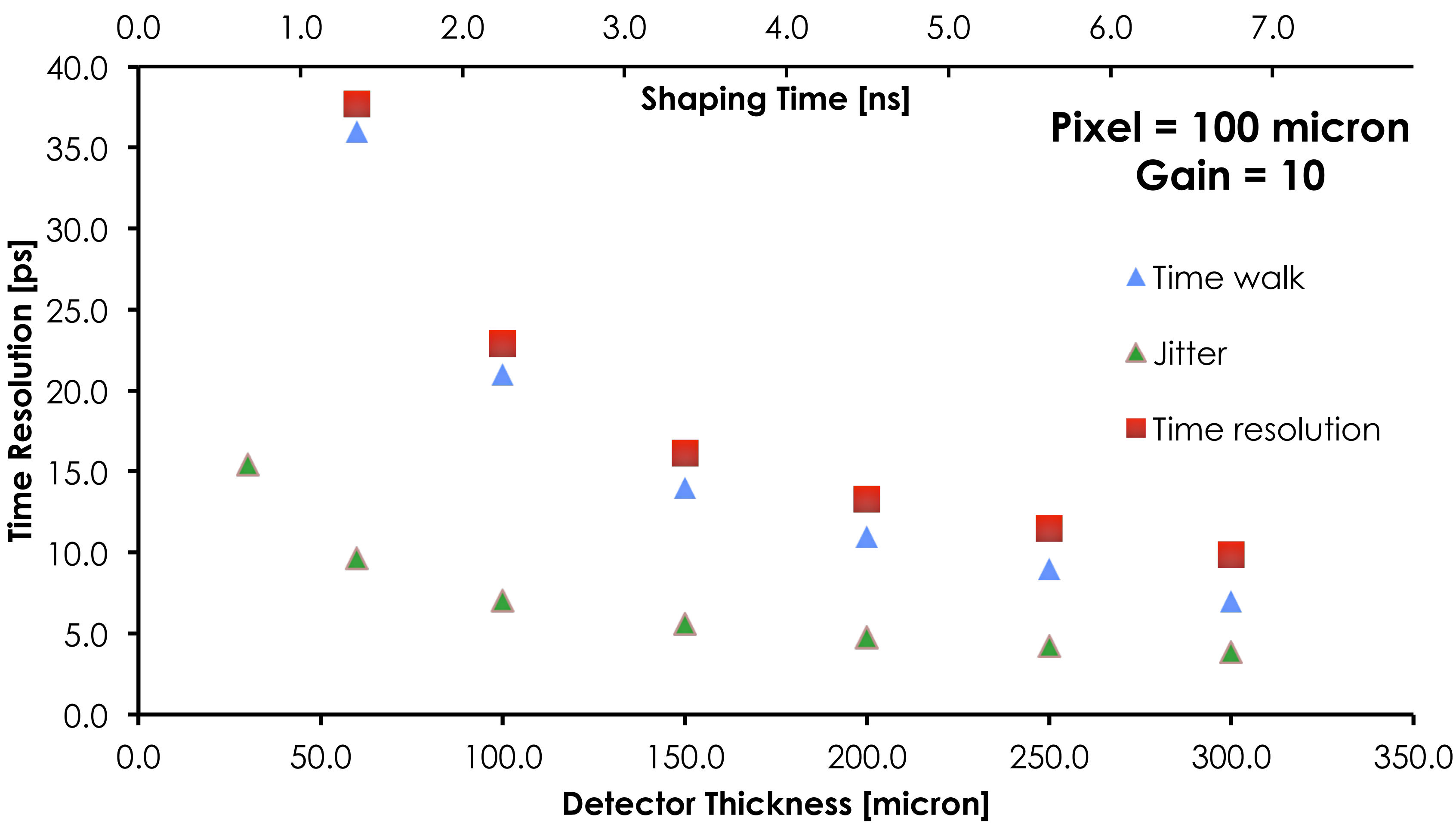
High Rate (depends on the fall time of the signal)



- **High rate** capability requires **thinner detectors**
- **Excellent time resolution** requires **thicker detectors**

Rate capability ⟺ Time resolution

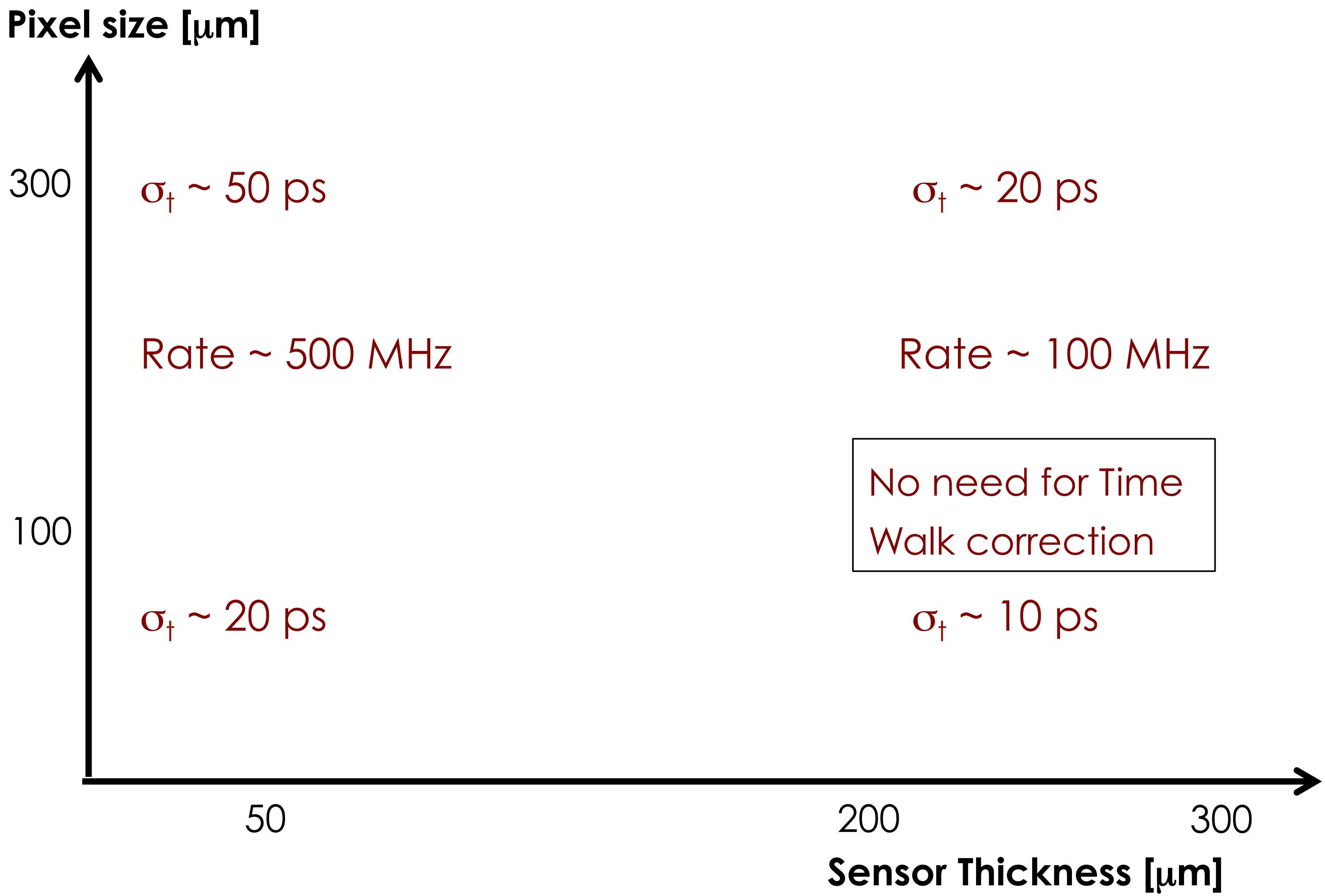
No Time Walk Correction



Excellent timing resolution even **without Time Walk correction**

➔ Much simpler electronics

UFSD - Summary



UFSD – Next Steps in Turin

1) Use the Torino version of the NA62 Gigatracker chip (several available):

Geometry: 300 x 300 micron, shaping time ~ 2 ns

Current resolution with traditional pixel ~ 200 ps

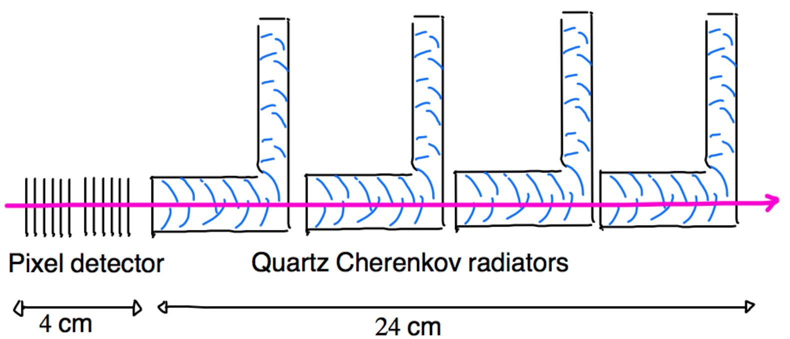
Can we do better with UFSD?

Need sensors of appropriate geometry and thickness

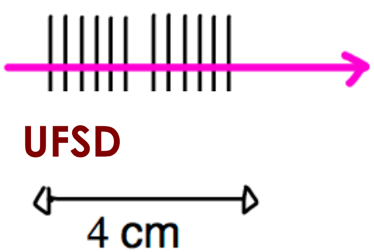
2) Turin is in charge of the sensors for PPS (forward tagger in CMS)

Currently 3D, in the future UFSD? **Need resolutions: 30 micron, 30 ps per plane**

PPS Current design for Low Luminosity:
Position: Pixel silicon detector
Timing: Quartz Cherenkov radiators



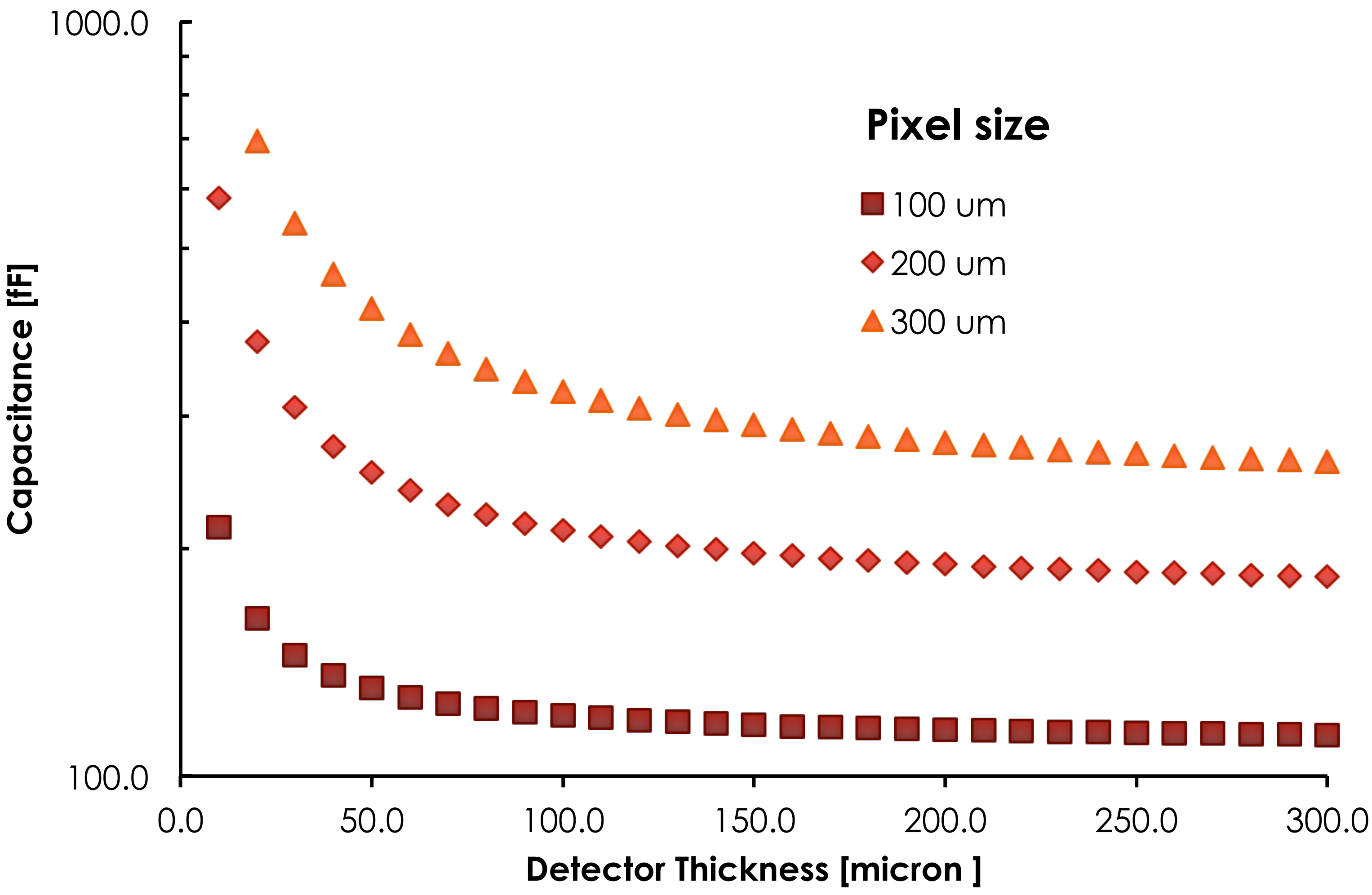
PPS Upgrade for High Luminosity:
Timing and Position: UFSD



A much lighter detector allows collecting more data near the beam line

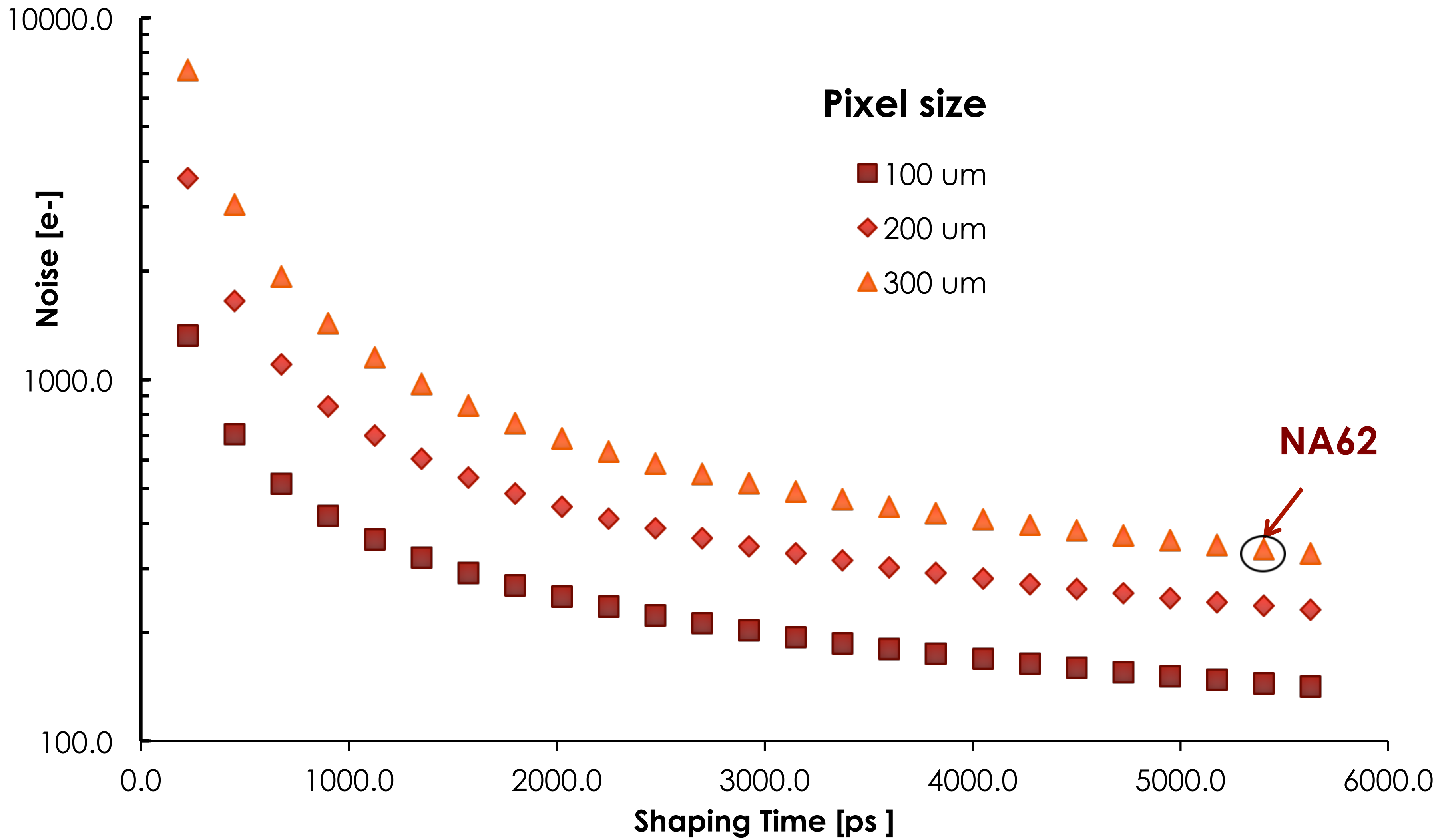
Backup slides

Capacitance vs Thickness



Capacitance: backplane + 0.2 fF/μm (perimeter) + 50 fF (fix term)

Noise vs Shaping Time

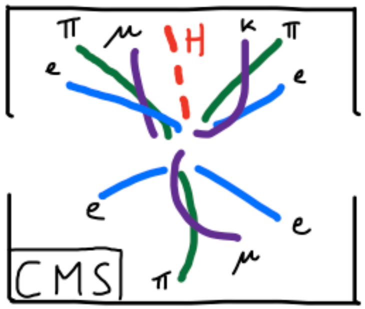


Noise values used in the parameterizations

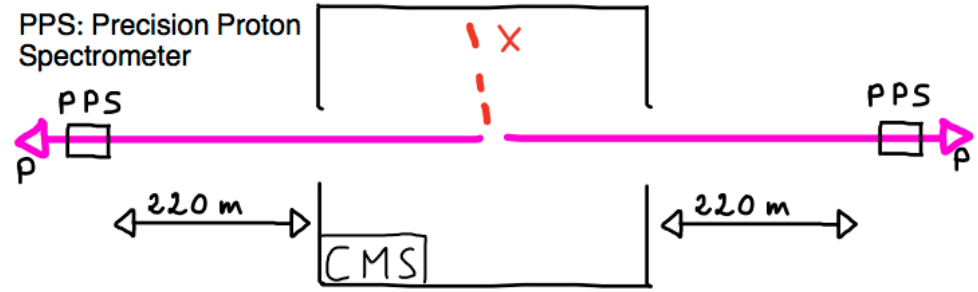
(NA62: Shaping time ~ 5500 ps, noise ~ 300 e-)

UFSD: The PPS project at LHC

Can we measure the exclusive production of new particles at LHC?

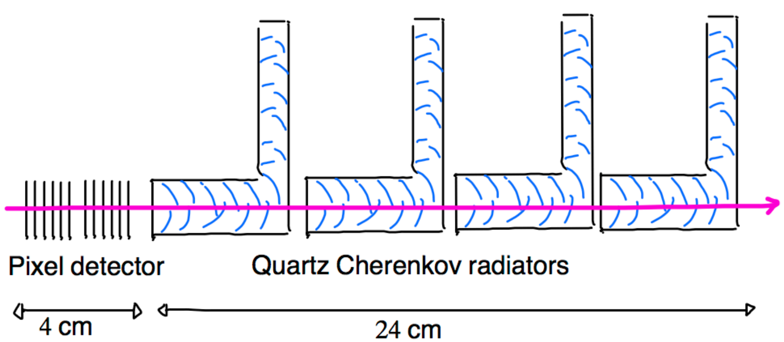


Standard event:
pp → many particles

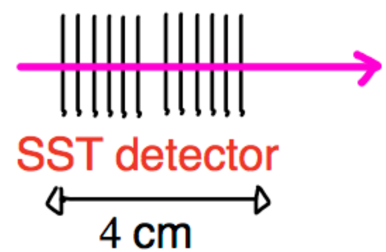


Central Exclusive Production:
pp → X p p

PPS Current design for Low Luminosity:
Position: Pixel silicon detector
Timing: Quartz Cherenkov radiators



PPS Upgrade for High Luminosity:
Timing and Position: UFSD



A much lighter detector allows collecting more data near the beam line

Charge Multiplication

Charge multiplication in path length ℓ:

$$N(\ell) = N_0 * \exp(\alpha * \ell) = g * N_0$$

$$\alpha_{e,h}(E) = \alpha_{e,h}(\infty) * \exp\left(- \frac{b_{e,h}}{|E|} \right)$$

At the breakdown field in Si of 270kV/cm:

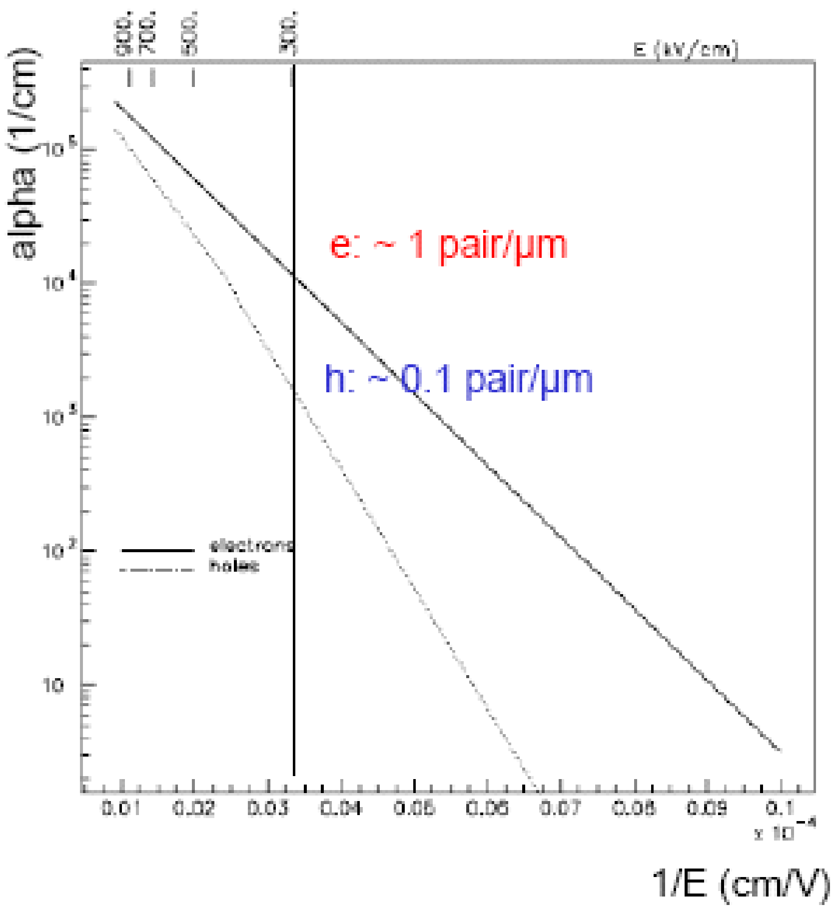
$\alpha_e \approx 0.7$ pair/μm

$\alpha_h \approx 0.1$ pair/μm

→ gain g = 33 possible in *l* = 5 μm.

→ In the linear mode (gain ~10), consider electrons only

Overstraeten impact ionization model



Need to raise E-field as close to breakdown field as possible for high gain but not too much to prevent breakdown!

A. Macchiolo,16th RD50 Workshop Barcelona, Spain, May 2010

Are TDC fast enough?

Ref	Technology	Architecture	Resolution (ps)	Sampling rate (MS/s)	Range (ns)	Power (mW)	Area
1	130 nm	GRO	1	50	12	2.2-21	0.04
2	130 nm	Vernier-ring	8	15	32	7.5	0.26
3	90 nm	Passive inter.	4.7	180	0.6	3.6	0.02
4	90 nm	Delay line	20	26	0.64	6.9	0.01
5	65 nm	2D delay line	4.8	50	< 0.6	1.7	0.02
6	90	Time Amp.	1.25	10	0.64	3	0.6
7	90	Vernier+GRO	3.2	25-100	40	3.6-4.5	0.027

- TDCs are now reaching the sub-ps resolution
- Many different architectures
- Dynamic range low in many high resolution TDC

UFSD – Gran Plan

We propose to realize a **low-gain ultra-fast sensor** that will concurrently measure:

Time ~ 10 - 20 ps:

- It depends on gain, noise levels and pixel size

Space ~ 30 – 100 μm:

- Edge effects might be important, forcing larger pixels.

Rate ~ 0.2. – 1 GHz:

- The rate is determined by the detector thickness
  collection time = shaping time.