Status of SCP Slim Edge Technology

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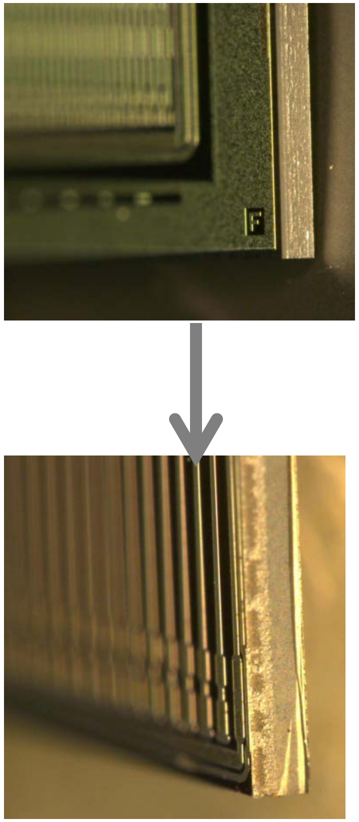
1) Technical Guidance and Support by
Marc Christophersen*, Bernard F. Phlips*
(*) Code 7654, U.S. Naval Research Laboratory

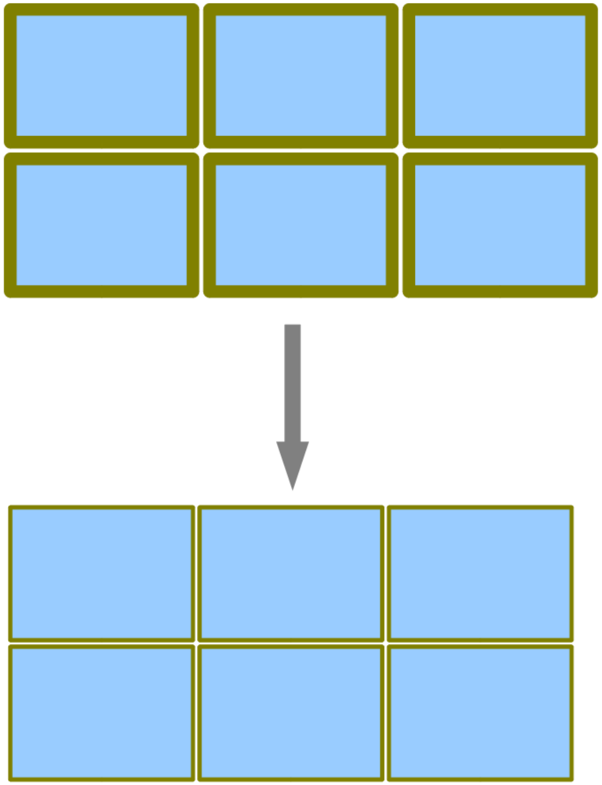
2) Our numerous collaborators from ATLAS and RD50,
in particular, results are shown from
Anna Macchiolo (MPI Munich)
Andy Blue and Richard Bates(U. of Glasgow)

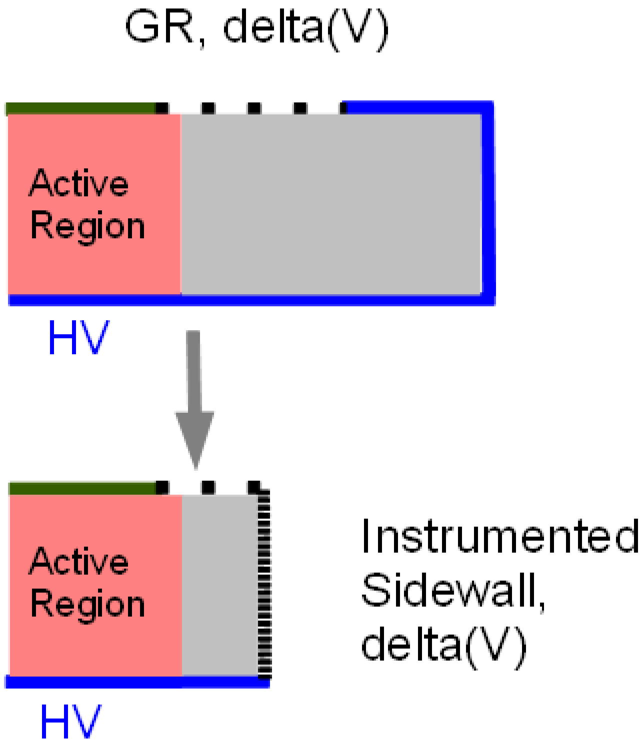
Slim Edges -- Motivation

Basic Idea: To minimize ~1 mm wide inactive peripheral region. This is relevant for “tiling” (as opposed to “shingling”) of large-area detector composed of small sensors.

Method: To instrument the sidewall in a close proximity to active area, such that it’s <u>resistive</u>.

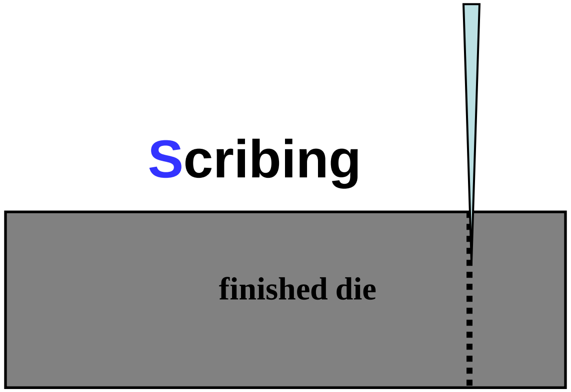






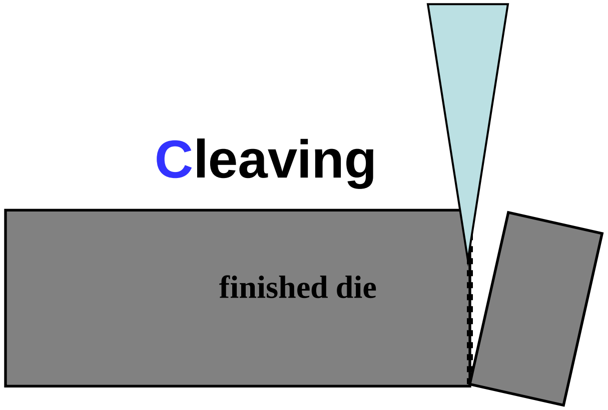
Method -- SCP Treatment

Scribing



- Diamond stylus
- Laser
- XeF_2 Etch
- DRIE Etch
- Saw cut (with cleanup step)

Cleaving



- Tweezers (manual)
- Loomis Industries, LSD-100
- Dynatex, GTS-150

Passivation

Native Oxide
+ Radiation
or:

N-type
(Qf > 0)

- Native SiO_2 + UV light or high T
- PECVD SiO_2
- PECVD Si_3N_4
- ALD “nanostack” of SiO_2 and Al_2O_3

P-type
(Qf < 0)

- ALD of Al_2O_3

All Treatment is post-processing & low-temp (Etch-scribing can be done during fabrication)

Basic requirement: 100 wafers (for rectangular side cleaving) with reasonably good alignment between sensor and lattice.

Current Efforts

We had a lot of technical development, with different fabrication options explored. For details, see recent publications:

- M. Christophersen et al., "Alumina and Silicon Oxide/Nitride Sidewall Passivation for P- and N-Type Sensors", NIM A 699 (2013) 14
- M. Christophersen et al, “The effect of different dicing methods on the leakage currents of n-type silicon diodes and strip sensors”, Solid-State Electronics 81 (2013) 8.
- M. Christophersen et al, “Scribing-Cleaving-Passivation for High Energy Physics Silicon Sensors”, Proceedings of Science, accepted for publication.
- V. Fadeyev et al, “Scribe-cleave-passivate (SCP) slim edge technology for silicon sensors”, NIM A 731 (2013) 260

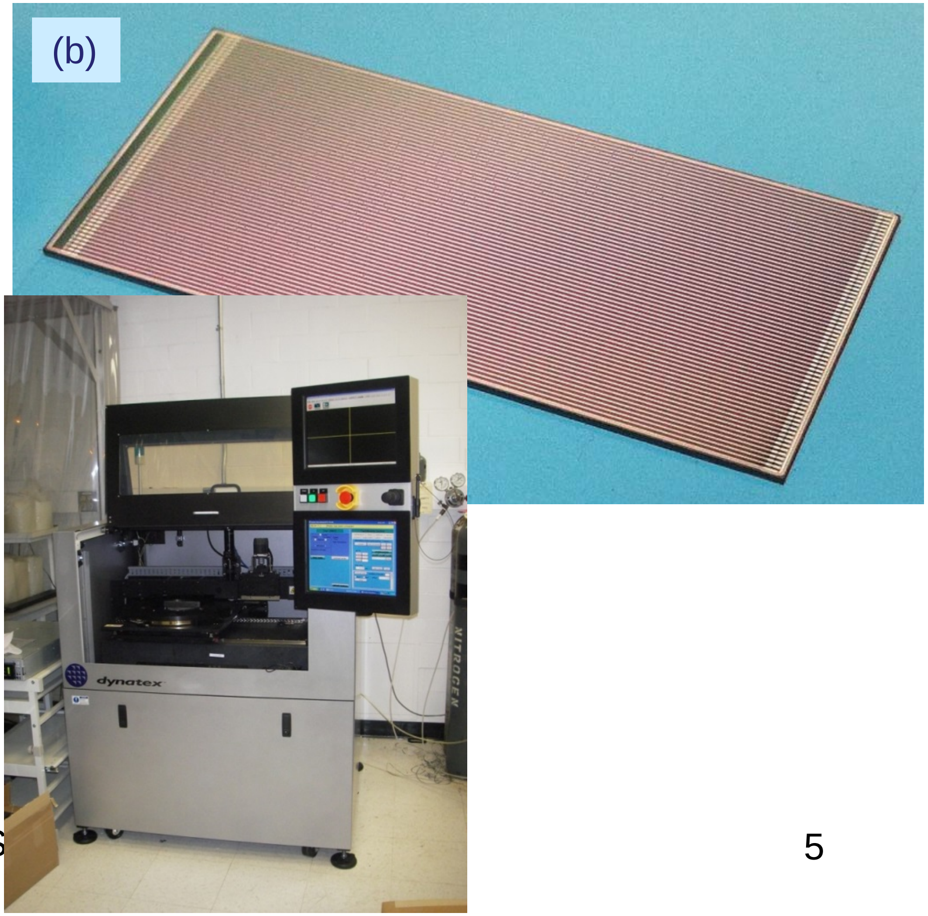
Recent work is focused on:

- <u>Technical development:</u>
    - Wafer-level processing
    - Simplified processing for N-type
- <u>Device performance:</u>
    - CCE near the edge
    - Radiation hardness

Wafer-based Processing

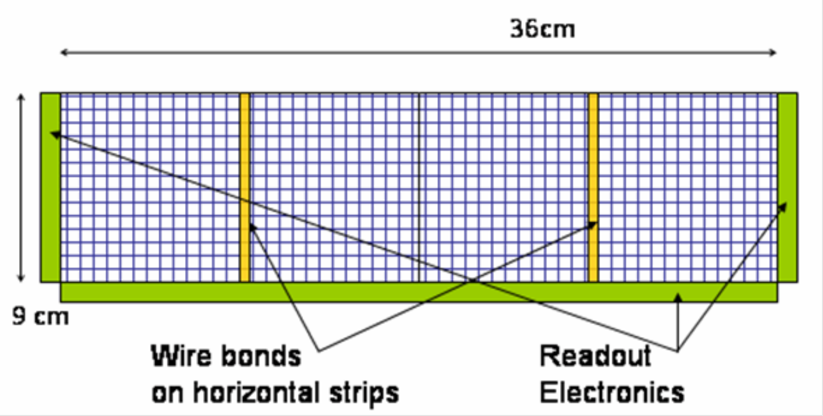
In the past we used **manual cleaving with tweezers – the only manual step!**
The latest tests with automated Dynatex machine are extremely promising:
a) 9-cm long narrow section is removed intact (it broke when being peeled off the blue tape). The removed piece is 680 um wide and 400 um thick!
b) 1.6 x 3.5 cm^2 sensor with slim edges on all 4 sides.

Cut-off from Glast/Fermi production.

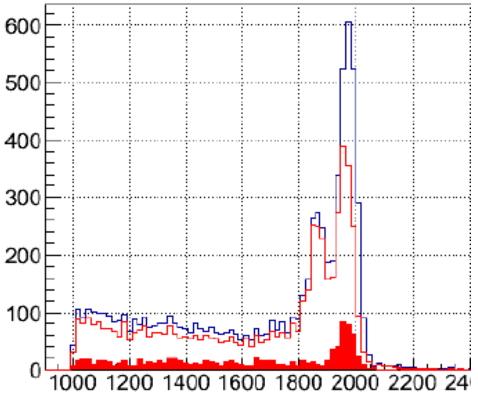


SCP treated SSD in pCT Tracker

Large area coverage requires tiling of 4 sensors,
having ~ 1mm inactive edges which create image artifacts.



Overlapping sensors introduces artifacts requiring additional, non-uniform energy corrections



For Tiling with no Overlap: “Slim Edges”

To make up the required instrumented area “paving” (instead of “shingling” or overlaps), a simplified SCP method will be used to make slim edges on 9x9 cm^2 sensors by post-processing. This development (next 2 slides) was caused by narrow edges on these sensors (they are already cut) before the new cleaving advances.

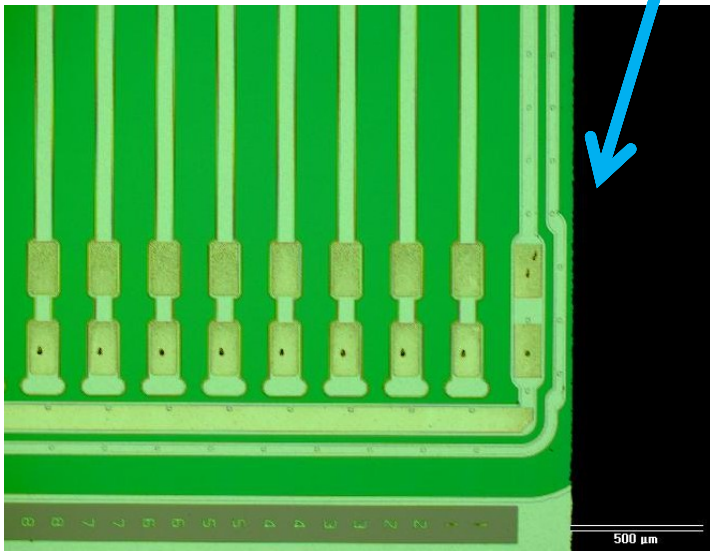
The processing is being done by CNM (Giulio Pellegrini). The example 2 slides later is one of the first trials.

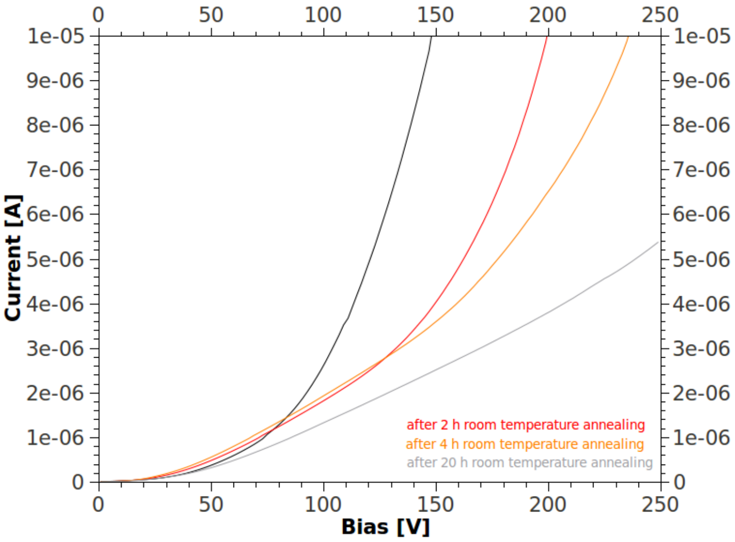
Alternative Wafer Processing

Based on our studies, wafer cleaving provides the best performance due to low defect density on the sidewall. Nonetheless, a process modification is possible:

instead of   Scribe-Cleave-Passivate,
one can do   Cut-DamageRemoval-Passivate.

The cut here can be either laser through-cut or conventional saw cut.
This might insure reliability of the singulation process, at the price of possibly higher currents.
An option for difficult cases, e.g. with wrong lattice orientation.





NB: This process variation works for N-type sensors only, where XeF2 sidewall etch is compatible with passivation.

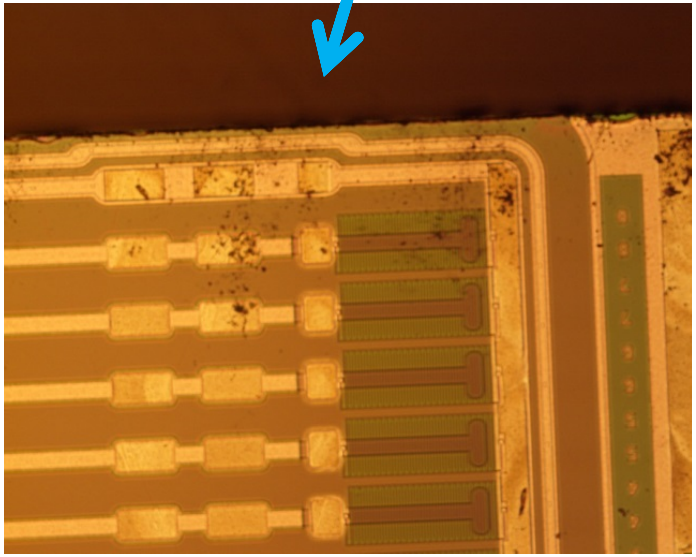
Alternative Wafer Processing: CNM

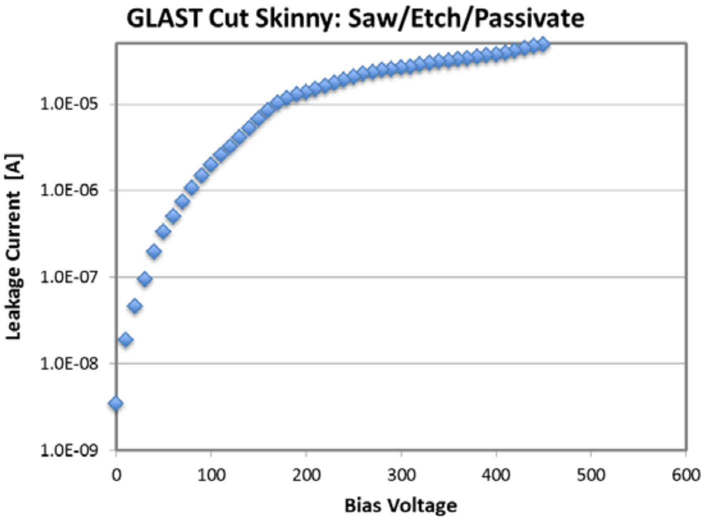
The same idea was tried at CNM, with the following variations:

- A conventional saw cut instead of the laser through-cut.
- Nitride passivation on the side on the horizontal sensor instead of nanostack of SiO2 and alumina.

The performance is similar: not quite as good as in case of cleaving, but it's suitable for many applications.

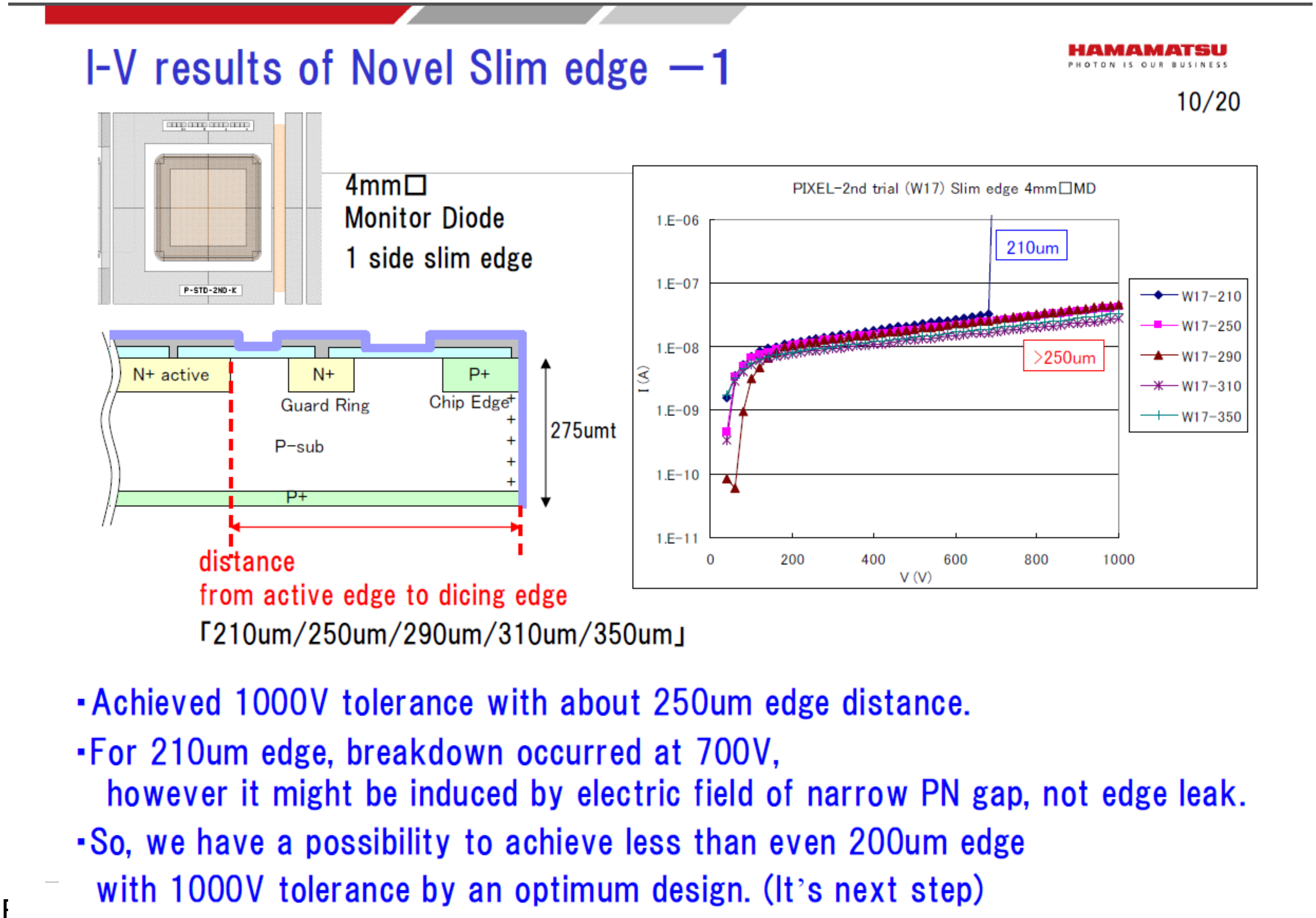
This is what's being used for post-processing sensors for pCT tracker.





SCP Slim edges at HPK

HPK is working on the method as well, for p-type sensors. Their preference is for DRIE with alumina passivation. Achieved very impressive low leakage currents and high Vbd. From presentation by S. Kamada at HSTD-9:



I-V results of Novel Slim edge —1

10/20

4mm□
Monitor Diode
1 side slim edge

distance
from active edge to dicing edge
「210um/250um/290um/310um/350um」

- Achieved 1000V tolerance with about 250um edge distance.
- For 210um edge, breakdown occurred at 700V, however it might be induced by electric field of narrow PN gap, not edge leak.
- So, we have a possibility to achieve less than even 200um edge with 1000V tolerance by an optimum design. (It's next step)

Radiation Hardness

- No issues with radiation hardness of *n-type* sensors with SCP.
- With *p-type* passivated with Alumina (Al_2O_3) see issues in IV tests (charge collection is a separate study, shown in later slides).
- The emerging pattern is:
  - High currents at low ionizing dose: < 1e14 neq/cm^2
  - No significant excess on the edge for high ionizing dose: > 1e14 neq/cm^2
  - No issues for neutron-irradiated samples.
  - The Si-alumina interface is a complicated matter. The possible (simplified!) explanation is that there is a thin layer of Al_xSiO_y forming *between* the Si and Al_2O_3 layers. It forms as a part of ALD application process, during the 1st cycles. The oxide in this layer then behaves like oxide does: gains more of its (positive) interface charge with first few MRad, counteracting the necessary negative oxide from alumina.
  - If this explanation is correct, the effect of the low-dose damage would be process-dependent.
  - Possible solutions include using other materials or deposition methods: HPK seems to see a different dependence on fluence.
- We will verify this understanding with test with dedicated “MAS” structures (MOS-like capacitors). They allow one to measure the interface charges. The structures are produced and verified – this is a project led by J.M. Rafi and G. Pellegrini at CNM. The first samples will go into gamma source ~now (D. Lynn at BNL). Will also irradiate with protons either at Birmingham or Los Alamos.

Charge Collection Testing

Sensor Type	Origin	Edge-Active area Distance [um]	Signal Readout	Beam	Ref
P-type strips	PPS (CIS)	~200	Binary (PTSM)	^{90}Sr	V. Fadeyev *et al* Pixel 2012, NIM A in press
N-type strips	GLAST (HPK)	~200	Analog (ALiBaVa)	^{90}Sr	R. Mori *et al*. 2012 JINST 7 P05002
P-type strips	PPS (CIS)	150	Analog (ALiBaVa)	Focused X-ray	R. Bates *et al*., 2013 JINST 8 P01018
P-type 3D pixels	IBL (CNM)	50	FE-I3 & FE-I4	CERN Test Beam	S. Grinstein *et al*., RESMDD12 G. Pellegrini *et al*., Pixel 2012, NIM A in press
P-type strips	PPS (CIS)		Analog (ALiBaVa)	^{90}Sr	A. Macchiolo
P-type strips n-irradiated	PPS (CIS)	110-220	Single-channel	Laser-TCT	I. Mandic, submitted to NIM
P-type strips n-irradiated	PPS (CIS)	150	Analog (ALiBaVa)	^{90}Sr	A. Macchiolo
P-type strips p-irradiated	PPS (CIS)		Analog (ALiBaVa)	Focused X-ray	A. Blue and R. Bates

In all cases charge collection on the edge was within few % of other electrodes

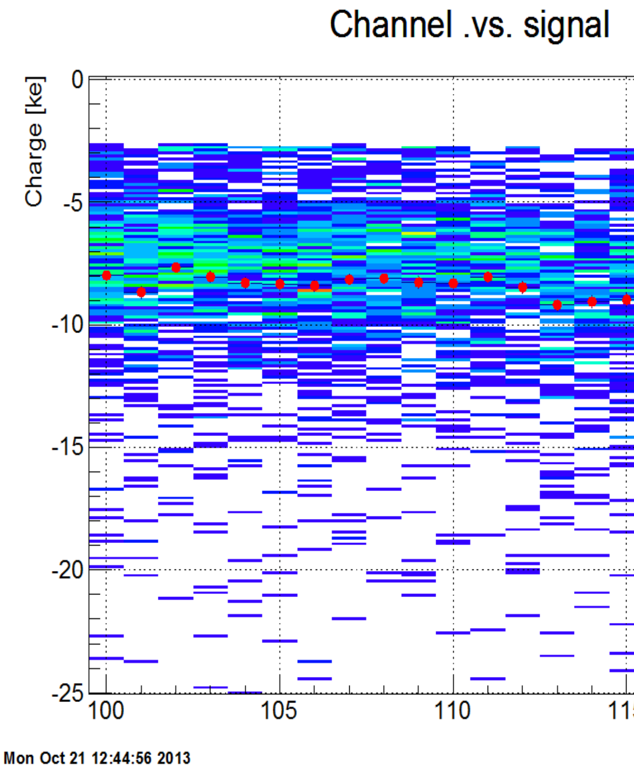
Three last studies are with irradiated devices!

Charge Collection: neutron-irradiated

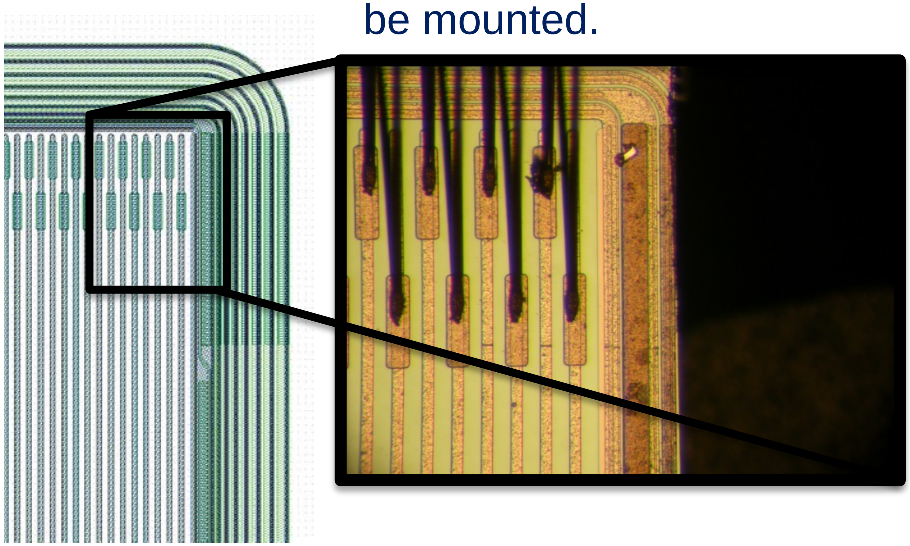
- ❑ n-in-p strip sensor CIS production, 285 mm thick, AC-coupled
- ❑ Treated with SCP method at NRL/UCSC
- ❑ Bias Ring + 1 Guard Ring remaining → 150 mm inactive edge
- ❑ Irradiated with reactor neutrons in Ljubljana at a fluence of 4x10^{15} neq cm^{-2}
- ❑ Biased at 800 V, at -50 C

A. Macchiolo et al (MPI)

Single cluster plot



- ❑ A sensor with fluence of 1x10^{16} neq cm^{-2} is to be mounted.

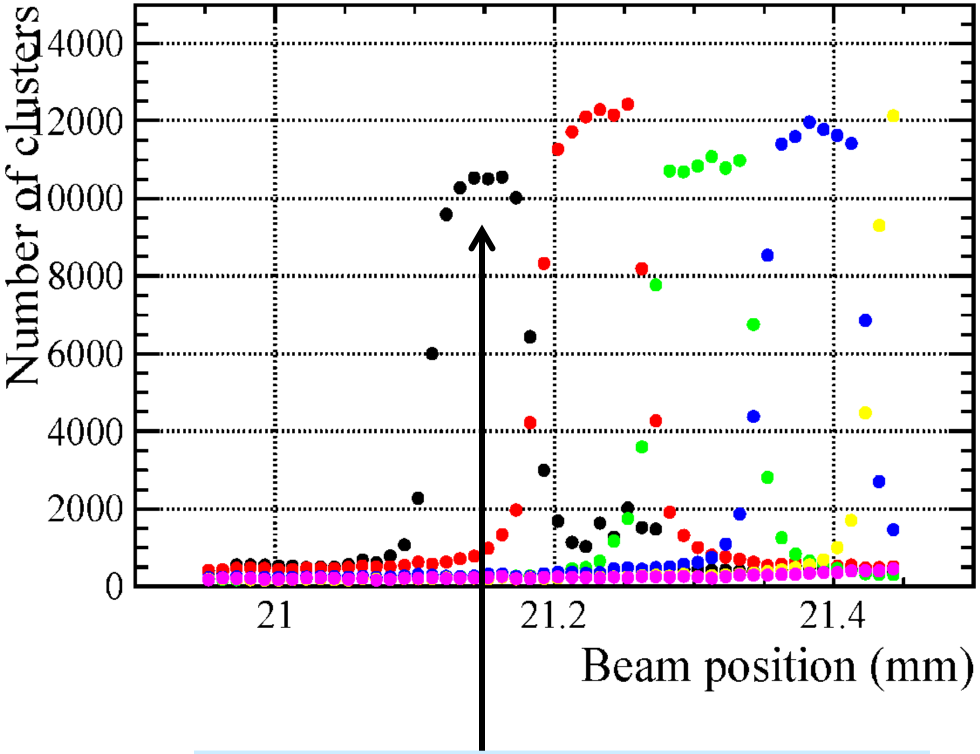


Edge strip properties:
- Similar median charge as for other strips.
- A bit noisier than others.

Charge Collection: proton-irradiated, focused X-rays

A. Blue, R. Bates (Glasgow)

- n-in-p strip sensor CIS production, 285 mm thick, AC-coupled, not irradiated
- Treated with SCP method at NRL/UCSC (“B2P11”)
- 305 mm from the edge to the 1st strip
- Irradiated with protons in Los Alamos, $4.82\text{x}10^{14}$ neq cm^{-2}
- Tested at Diamond X-ray facility:
    - 12 keV beam
    - 2.5 mm FWHM beam
    - 10 mm step size
    - Biased at 500 V, at T = -8 C



Edge strip:

- Similar signal as for other strips.

Conclusions and Future Work

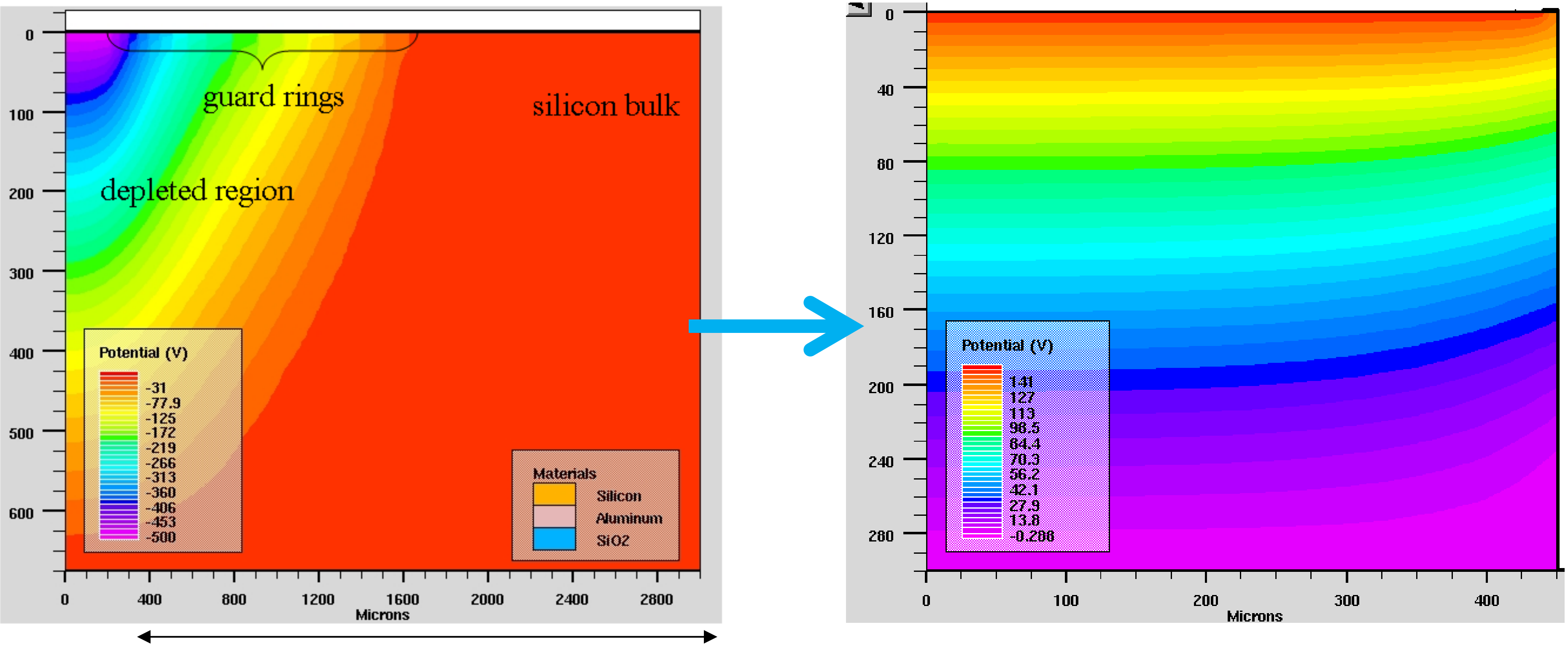
- Technological steps:
  - Cleaving with automated industrial tool works well. This was the only manual steps we used in the past.
  - More popular singulation methods (saw, laser cuts) can be used on n-type devices, at the price of higher leakage currents.
  - HPK has interesting R&D on SCP technology on p-type devices with DRIE.
- Radiation hardness:
  - N-type ok.
  - P-type passivation probably might have an issue we need to overcome. It would be process-specific.
- Sensor sensitivity near the edge:
  - No CC compromise near the edge on un-irradiated sensors.
  - Now this is also confirmed on irradiated sensors:
    - Neutron-irradiated in Ljubljana studies.
    - Neutron-irradiated in MPI studies.
    - Proton-irradiated in U. Glasgow studies.

Back-Up Slides

Slim Edges – Surface Quality

Conventional sensors have the bias voltage gradient in the guard rings region. To implement slim edges, we'd like to have the gradient on the sidewall => similar surface quality and passivation requirements.

Surface imperfections lead to additional current consumption => IV test as a measure of performance.

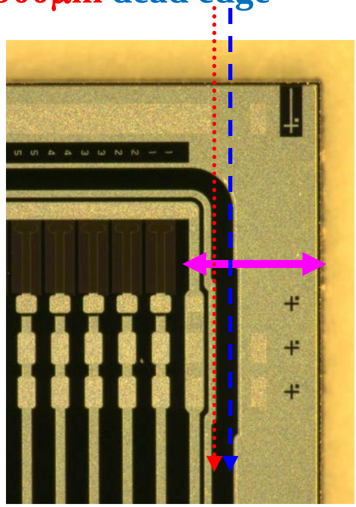


inactive region

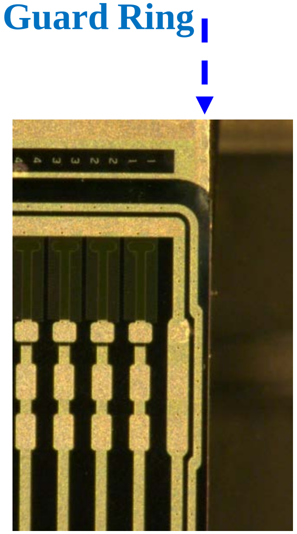
Examples with N-type Sensors

XeF2 scribing + Nitride PECVD

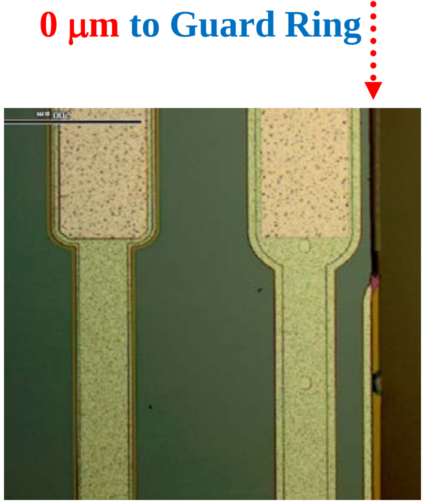
Si SSD with
900μm dead edge

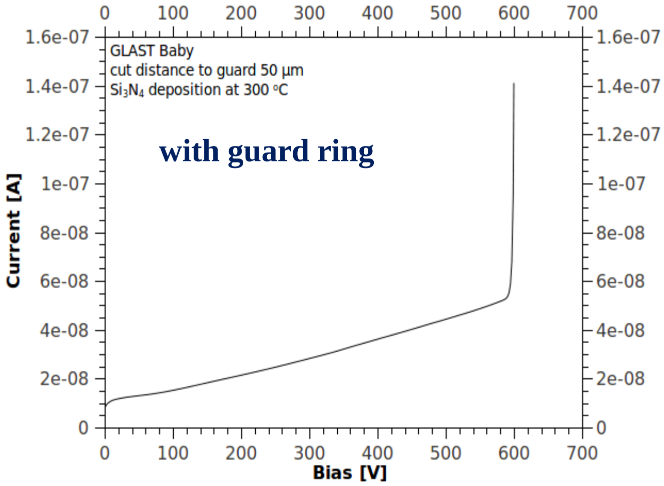


Cut within 50 μm
of Guard Ring

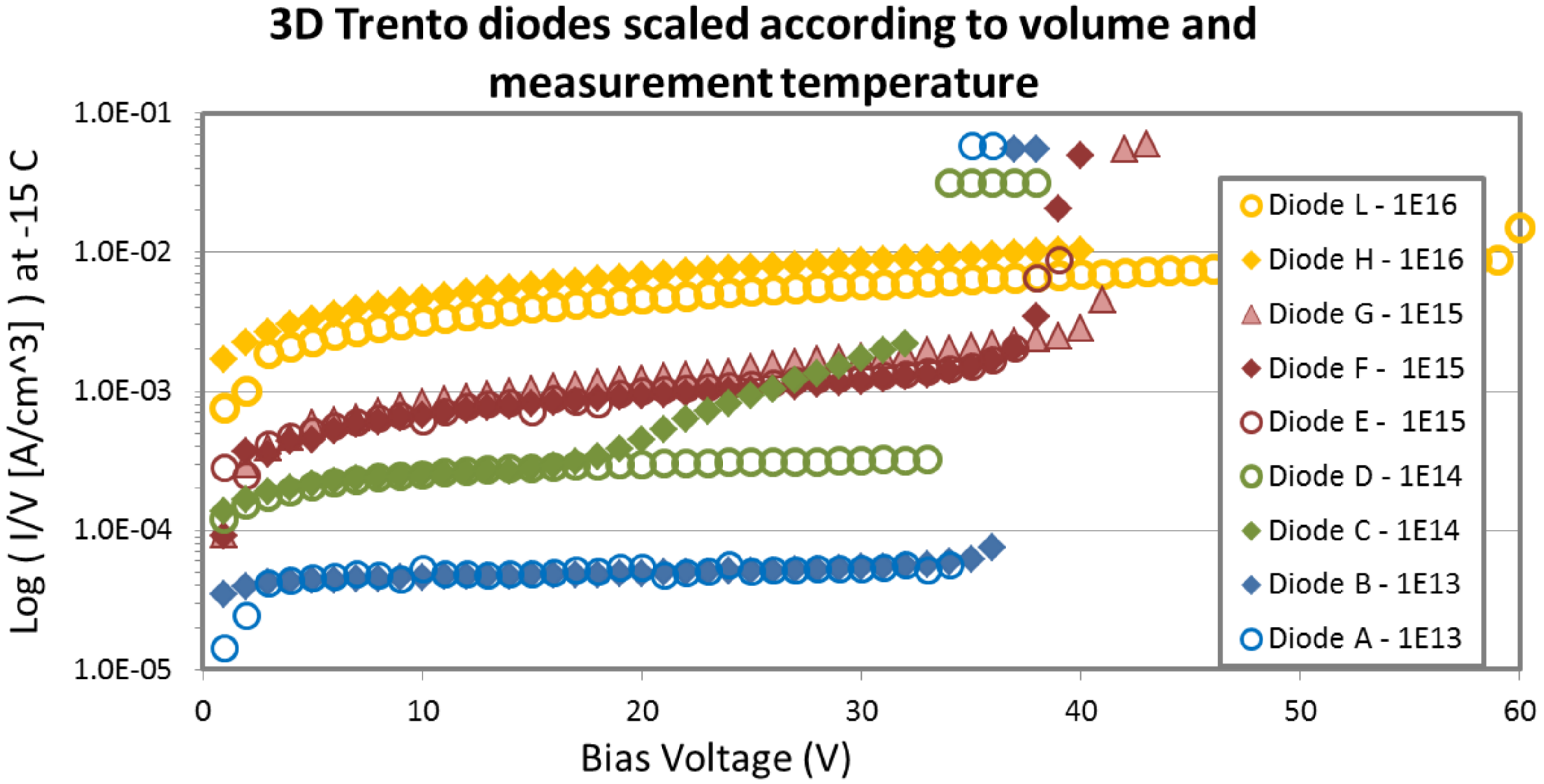


Guard Ring Cut (!)
0 μm to Guard Ring





P-type 3D sensors irradiated at Ljubljana, (PI G.-F. Dalla Betta)

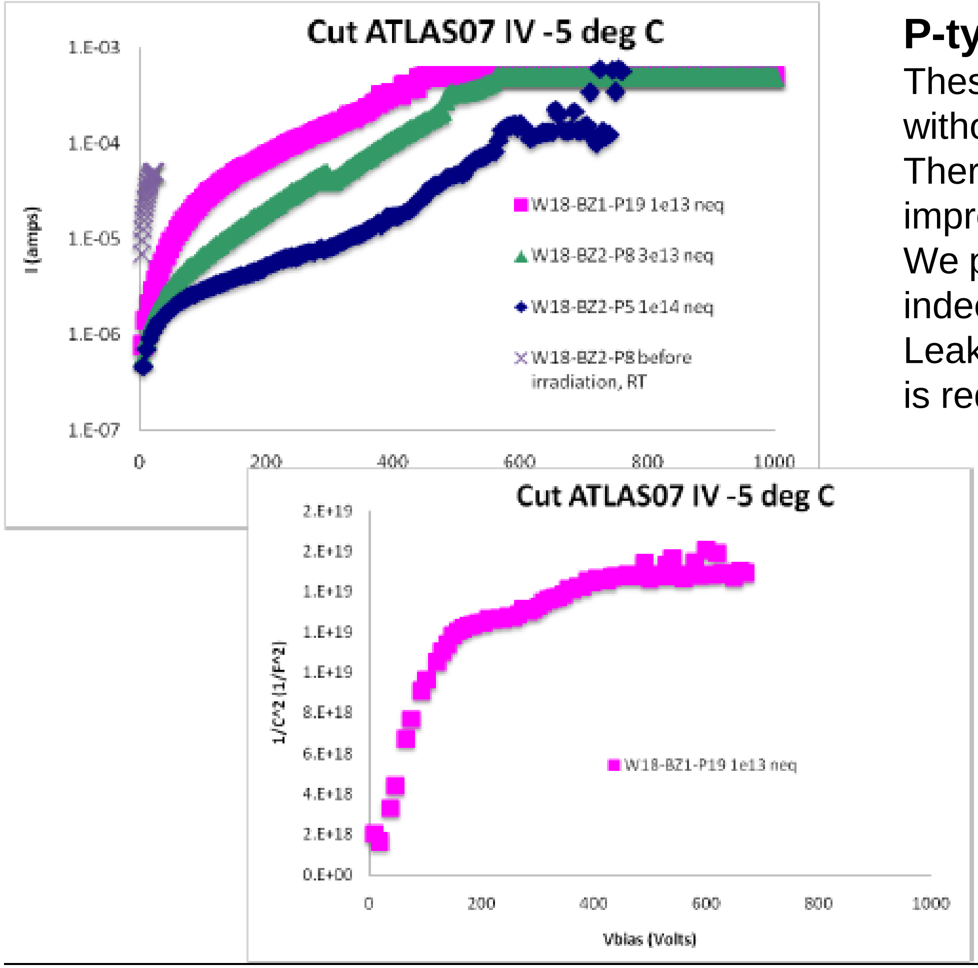


Observation on SCP P-type with neutrons:

3D neutron-irradiate sensors show approximate scaling with fluences:
no high currents for low fluences !
=> See vastly different fluence scaling. Either due to field geometry or non-ionizing dose.

1. 2010 Proton Irradiation Studies @LANL

S-C only: No Passivation



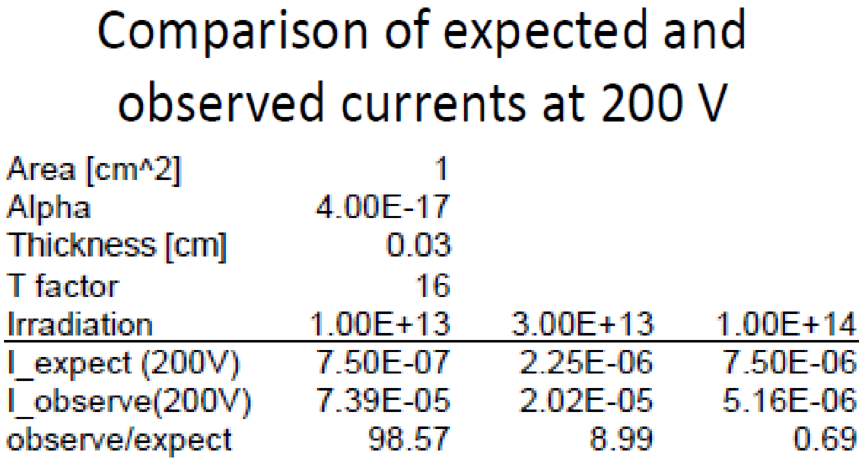
P-type HPK (ATLAS07)

These sensors did not work after cleaving (initial trial without sidewall passivation). Breakdown at ~few Volts.

There is an empirical evidence that the breakdown improves after irradiation.

We put these sensors in proton beam to see if they would indeed improve.

Leakage is initially dominated by the edge current, which is reduced with fluence. At 10^{14} neq, I(edge) < I(bulk).



Comparison of expected and observed currents at 200 V

Area [cm^2]	1		
Alpha	4.00E-17		
Thickness [cm]	0.03		
T factor	16		
Irradiation	1.00E+13	3.00E+13	1.00E+14
I_expect (200V)	7.50E-07	2.25E-06	7.50E-06
I_observe(200V)	7.39E-05	2.02E-05	5.16E-06
observe/expect	98.57	8.99	0.69

Observation #1 on S-C only p-type:

High fluence irradiation -> resistive edge!

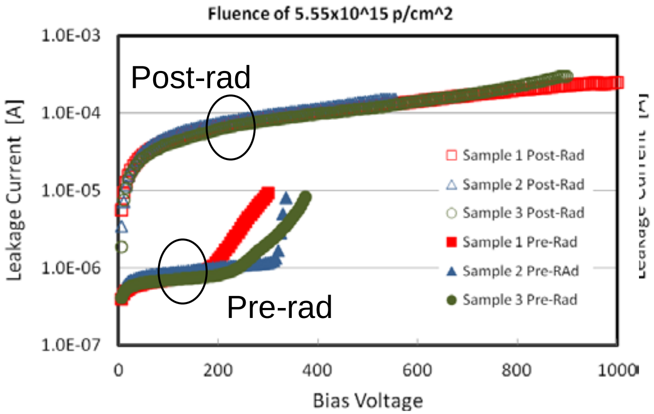
2. 2011 Proton Irradiation @LANL

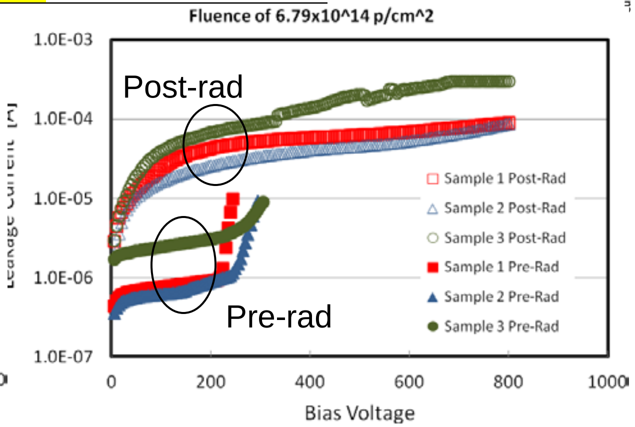
Irradiated 12 SCP processed p-type strip devices (CIS courtesy A. Macchiolo) at LANL (thanks S. Seidel). Results are in-conclusive:

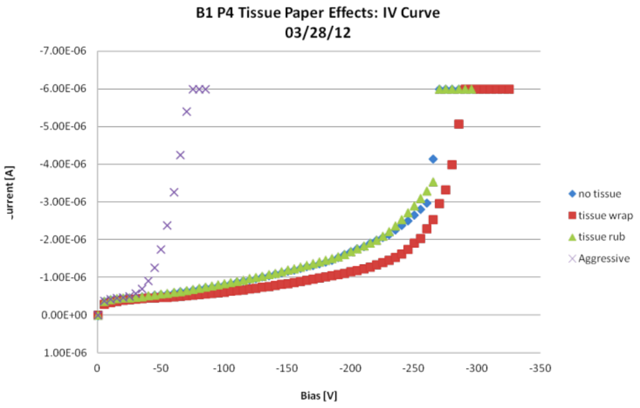
- **+ Breakdown voltages extended post-rad**
- **+ High fluence devices (3/3 for 1e16neq, 3/3 for 1e15neq) show expected post-rad leakage current**
- **- Lower fluence devices (1/3 for 1e13neq and 1/3 for 1e14neq) show earlier breakdown!**

Sensor	**Before Irradiation** V(break) at ~10 uA	**After Irradiation** V(break) at ~100 uA	Fluence	No Guard Rings
B1 P5	30	460	10^13	1
B1 P6	290	165	10^13	1
B2 P1	410	80	10^13	3
B1 P8	15	90	10^14	5
B2 P10	310	80	10^14	5
B2 P6	390	100	10^14	1
B2 P8	300	>800	10^15	4
B2 P9	310	335	10^15	5
B2 P11	250	>800	10^15	2
B2 P2	305	390	10^16	1
B2 P3	340	330	10^16	3
B2 P4	380	425	10^16	3

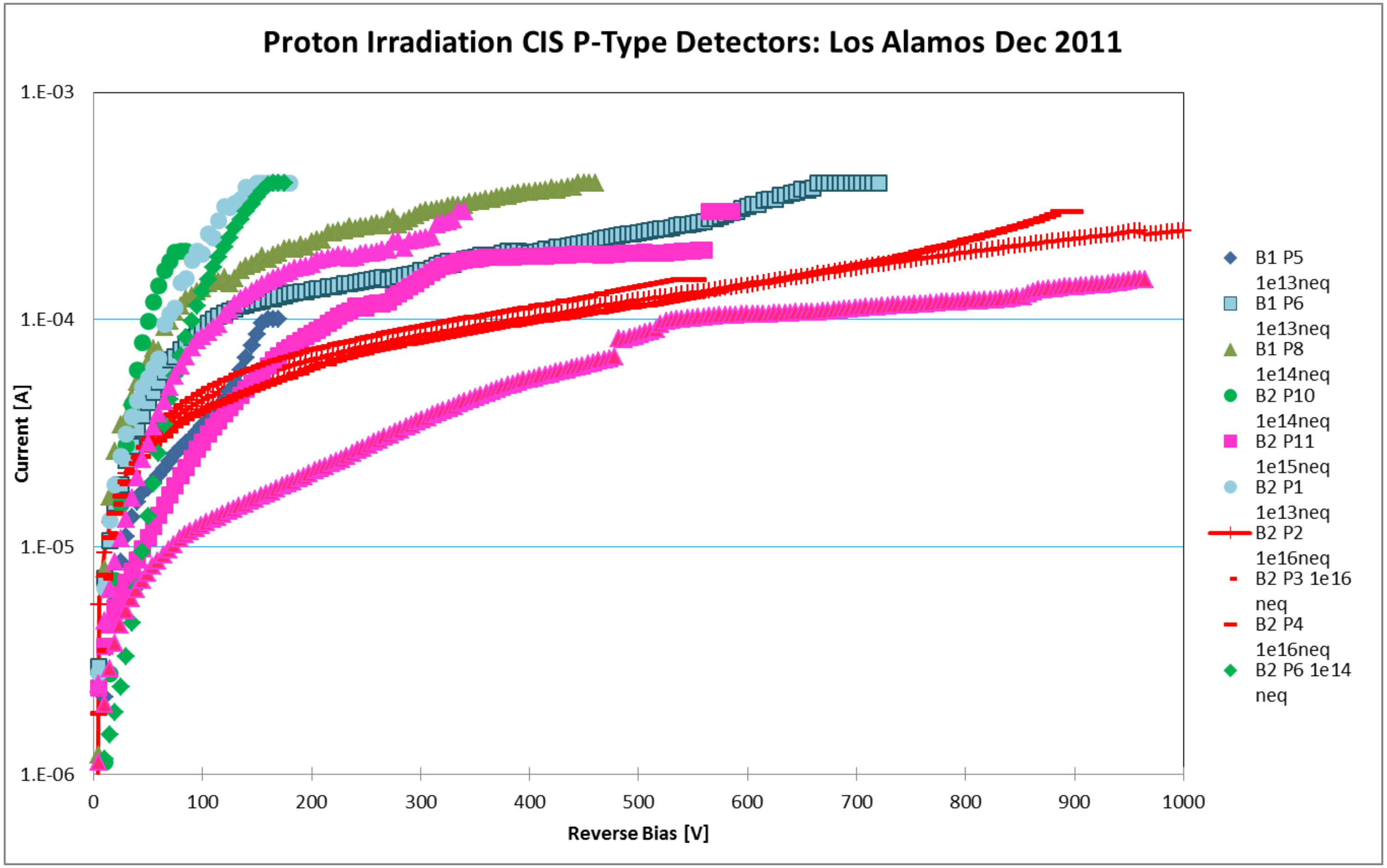
A parallel investigation of the robustness of the passivation layer revealed a possible susceptibility to rough handling. There is no proof that this has skewed the irradiation results.







2. 2011 Proton Irradiation @LANL

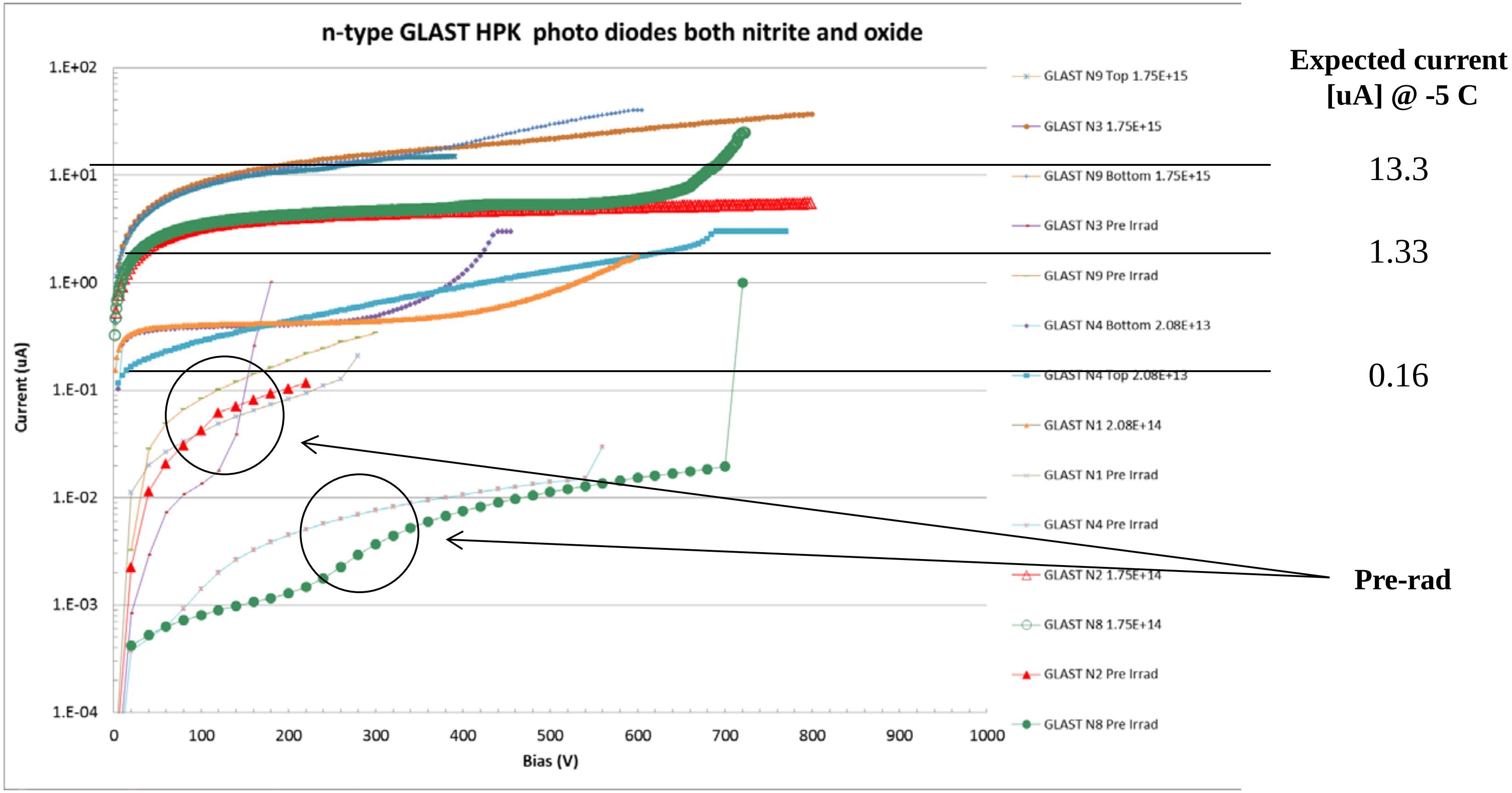


Observation #2 on S-C-P p-type:

Low fluence (<= 1e14): high edge current

High fluence irradiation (>= 1e15): resistive edge!

n-type GLAST HPK Photo Diodes both nitrite and oxide passivation



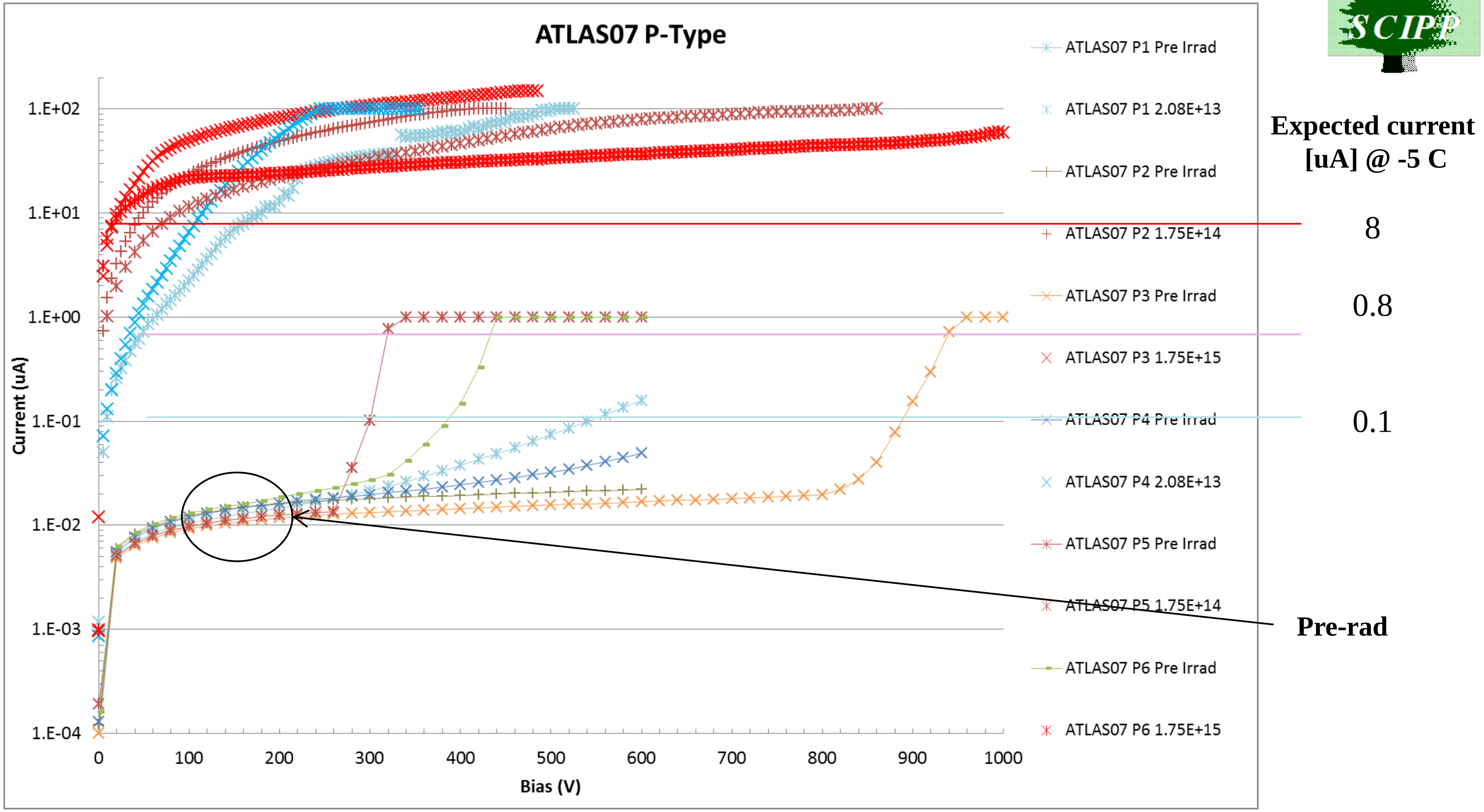
Observation #3 on S-C-P n-type:

low fluence (1e13, < inversion) edge isolation due to passivation (Nitrite/nanostack)

High fluence (>1e14, > inversion): resistive edge

…No dependence on type of passivation, leakage current close to bulk expectation

p-type ATLAS07 HPK Photo Diodes



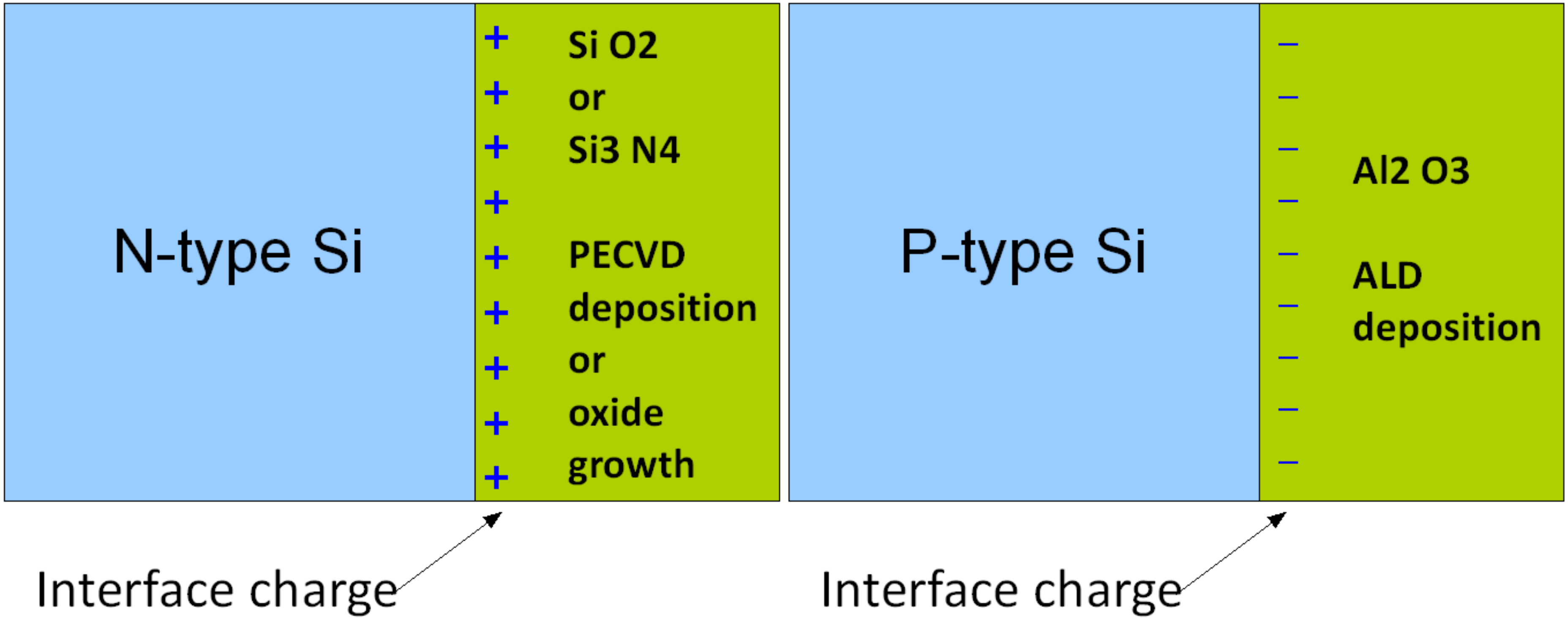
Observation #4 on S-C-P p-type:

Leakage currents do not scale with fluence

low fluence (< 1e14): reduced edge performance

high fluence (>1e14): resistive edge

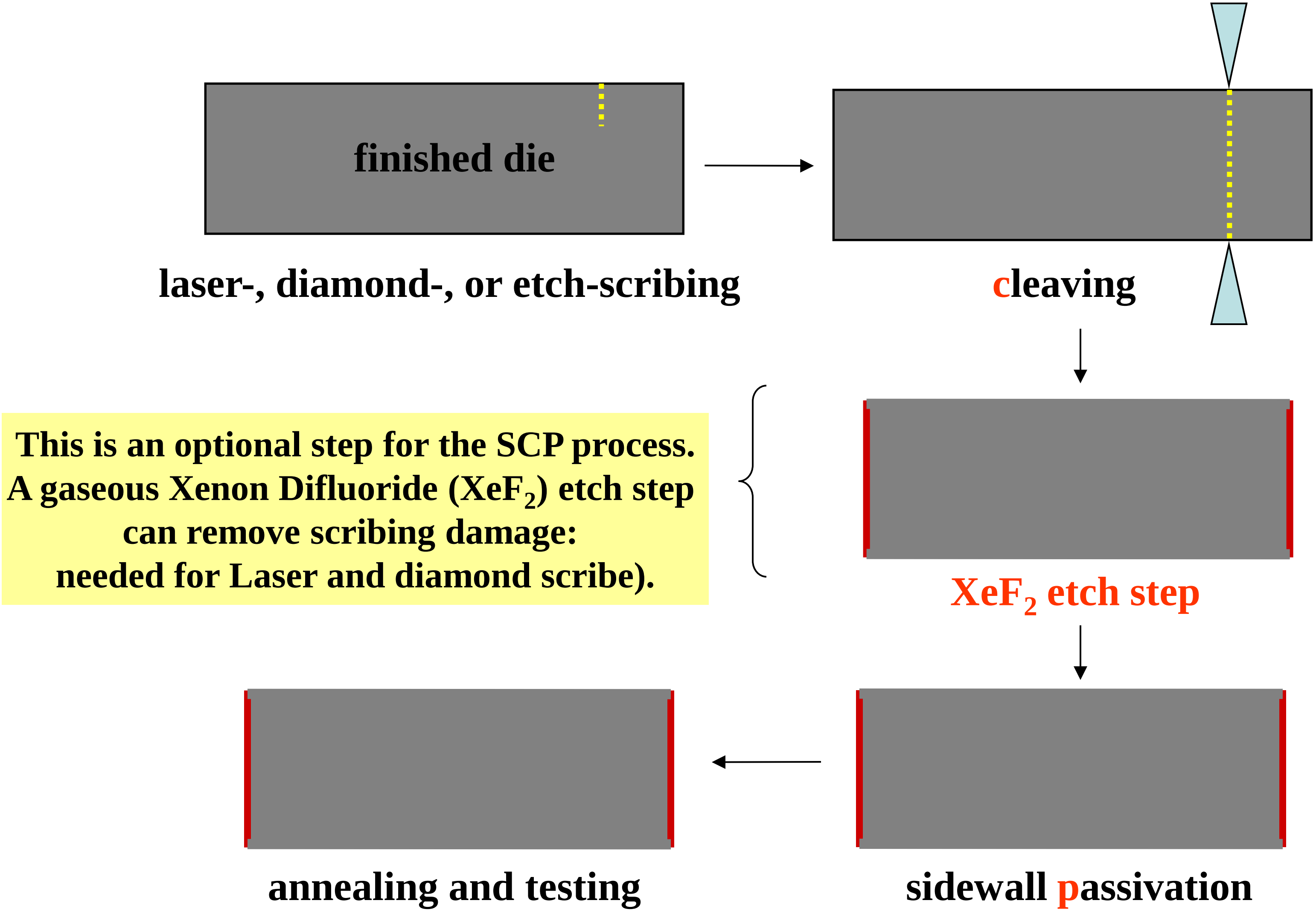
Passivation Options



Surface passivation makes the sidewall resistive. N- and p-type devices require different technologies.

- For n-type devices one needs a passivation with *positive* interface charge. SiO_2 and Si_3N_4 layers works well.
- For p-type material a passivation with negative interface charge is necessary. We found that Al_2O_3 works in this case.

SCP Treatment (Cont)



finished die

laser-, diamond-, or etch-scribing

cleaving

This is an optional step for the SCP process. A gaseous Xenon Difluoride (XeF_2) etch step can remove scribing damage: needed for Laser and diamond scribe).

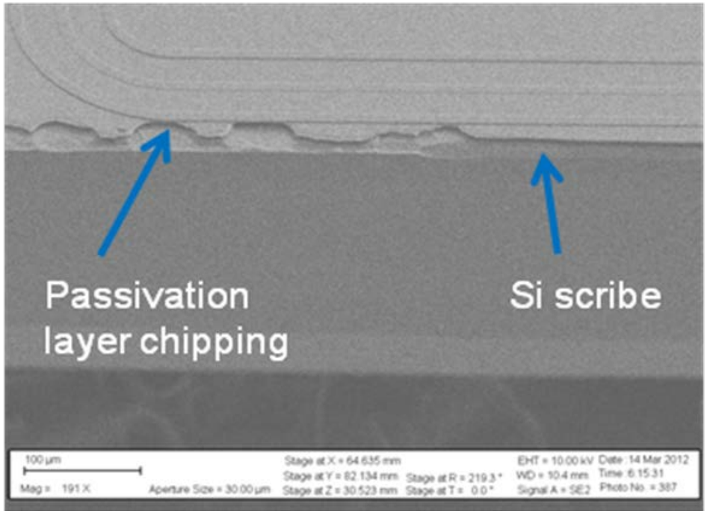
XeF_2 etch step

sidewall passivation

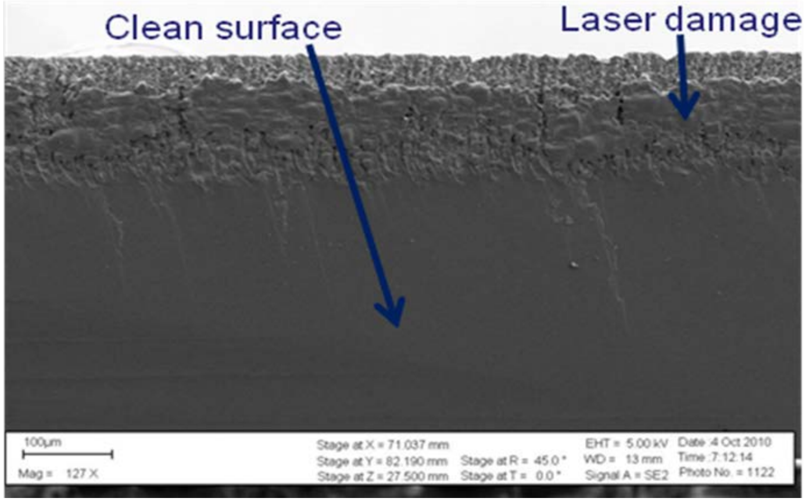
annealing and testing

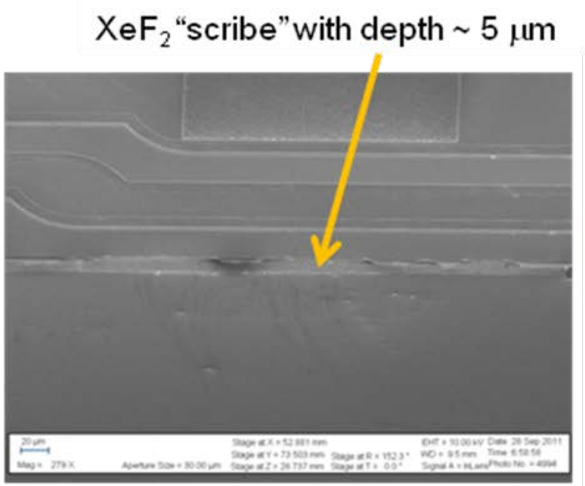
Scribing Technologies: Diamond-, Laser-, and Etch-based

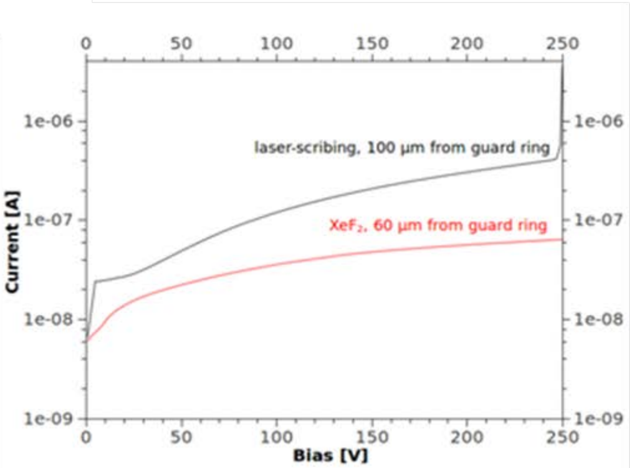
Diamond scribing



Laser scribing



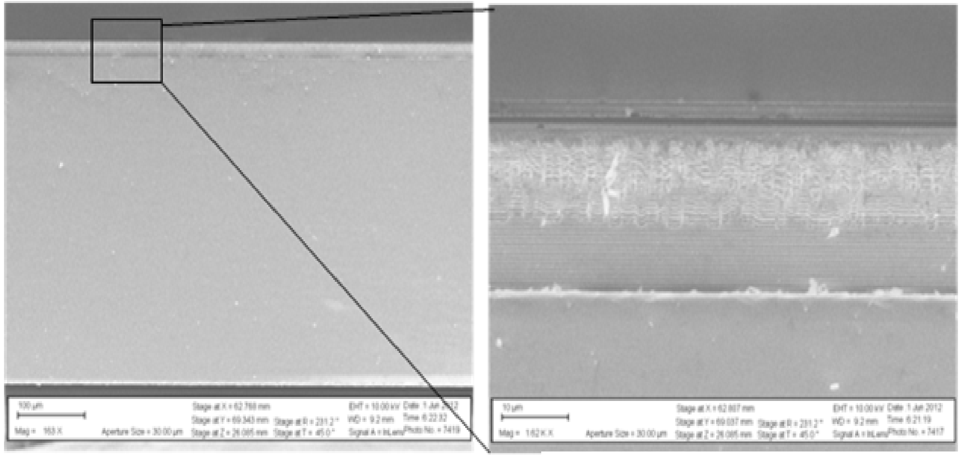


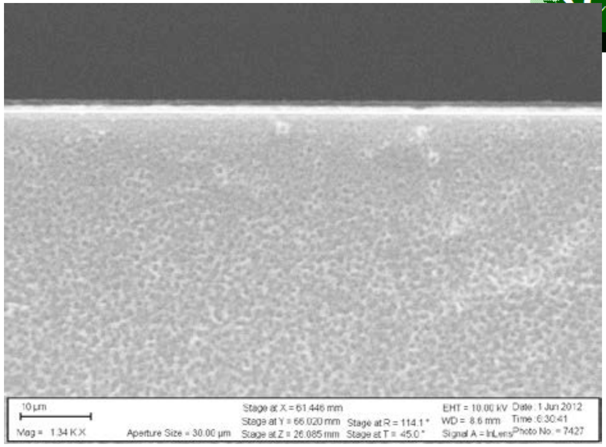


Issues:

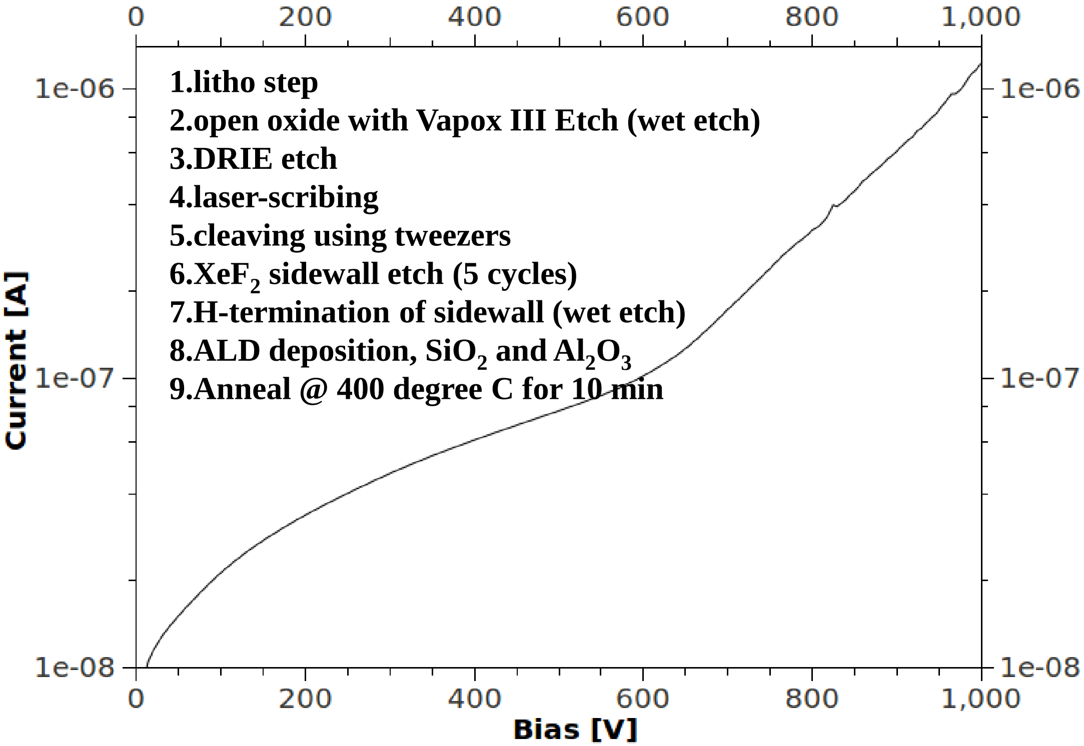
- ➢ Diamond scribing: surface chipping of <u>existing</u> passivation (=> to do again in future runs)
- ➢ Laser scribing: some degree of damage due to affected region of the sidewall
- ➢ XeF2 etching: cleaving by industrial machines is difficult

Scribing Technologies: DRIE



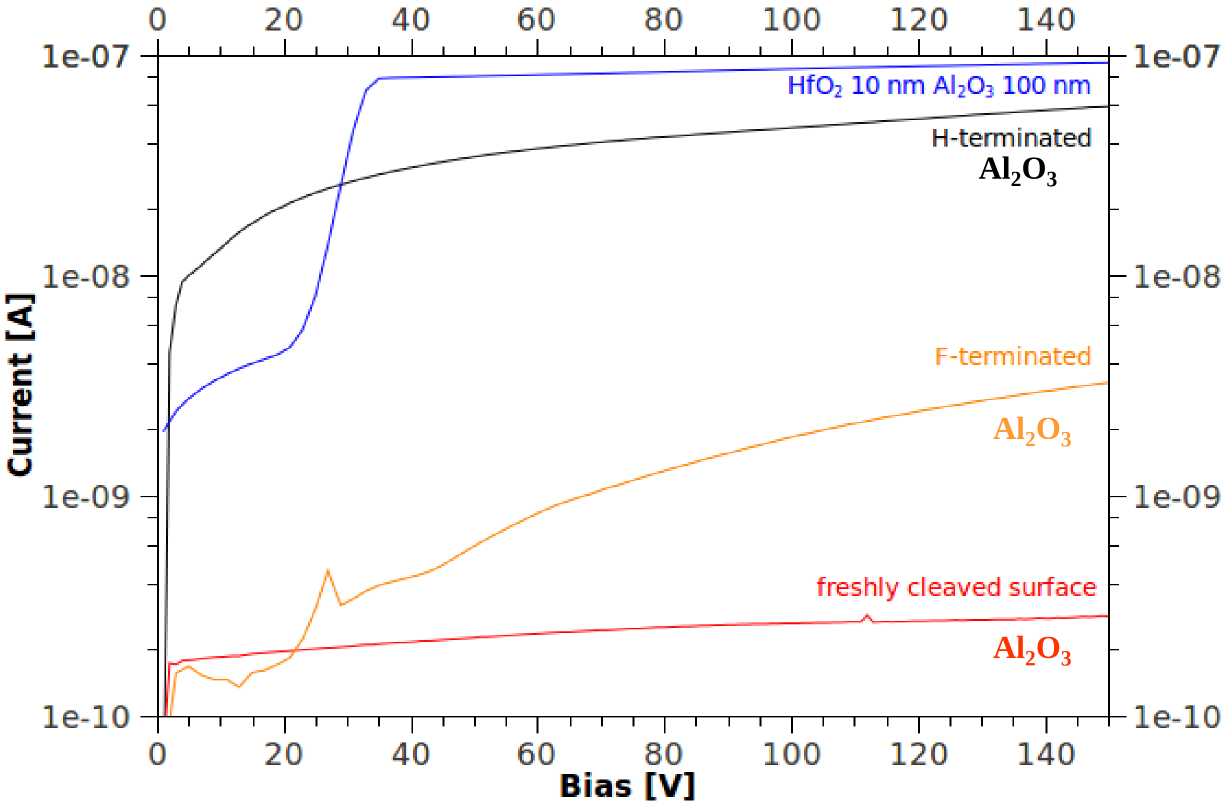


DRIE-based trenching as scribing has a promised of being a “universal” production solution without shortcomings of the other methods.



1. litho step
2. open oxide with Vapox III Etch (wet etch)
3. DRIE etch
4. laser-scribing
5. cleaving using tweezers
6. XeF_2 sidewall etch (5 cycles)
7. H-termination of sidewall (wet etch)
8. ALD deposition, SiO_2 and Al_2O_3
9. Anneal @ 400 degree C for 10 min

Effect of Surface Termination – P-Type Si

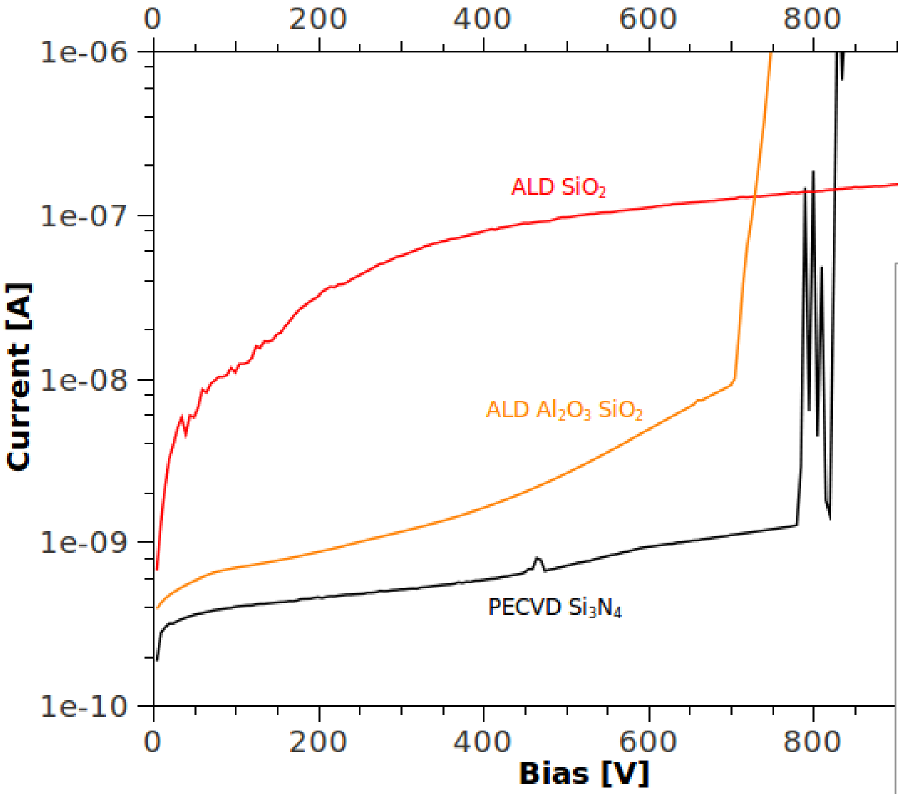


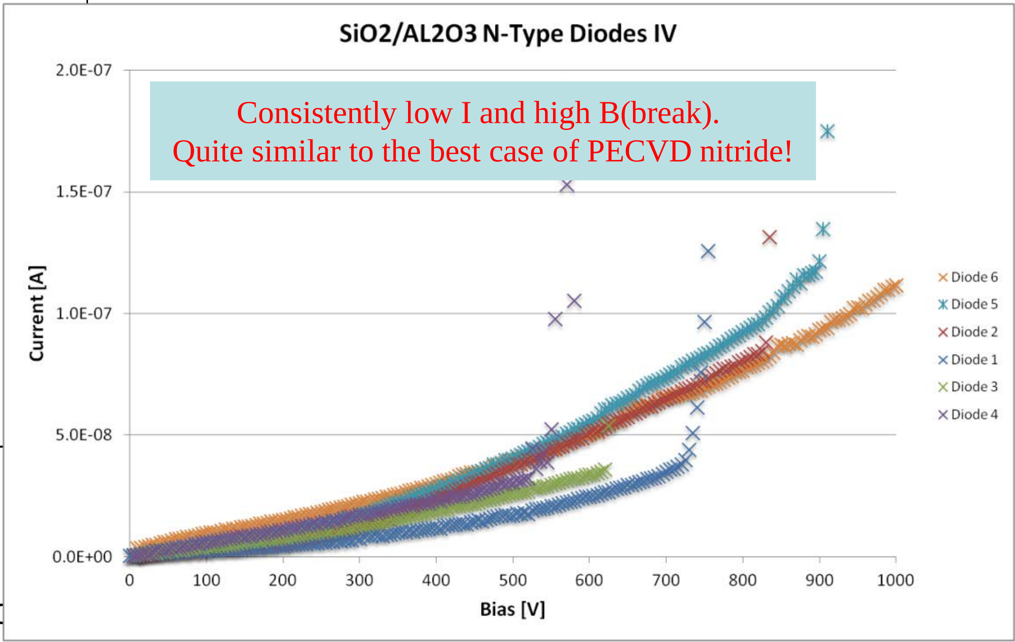
- After all the handling, we need to remove a native oxide. That is done w/ HF and leads to the “H-termination”, which can’t be passivated with alumina Al_2O_3.
- Need to covert the H-termination into F-termination which in combination with alumina ALD should work. Know they chemistry!
- The hunt for on ideal surface termination for p-type Si is still on.

Progress with Passivation (N-type Diodes)

PECVD process has been developed by industry as a wafer process => Small height of the chamber in a typical machine.
This worked well for small size samples, that could be positioned vertically, or slanted. For large sensors this is not quite applicable => replace by ALD method.

Study with HPK Fermi/GLAST diodes. The plain ALD SiO2 is worse than the best case of PECVD Si3N4.
But a “nanostack” of ALD SiO2 (10 nm) and Al2O3 (50 nm) works well.
Parameters are from G. Dingemans et al, J. Appl. Phys. 110, 093715 (2011); doi: 10.1063/1.3658246





Consistently low I and high B(break).
Quite similar to the best case of PECVD nitride!