Centre Nacional de Microelectrònica IMB

SCIPP
SANTA CRUZ INSTITUTE FOR PARTICLE PHYSICS

First measurements of new p-type strips and pad detectors with LGAD in epitaxial wafers

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1)Thin p-type epitaxial substrates

Detector proposed by Hartmut Sadrozinski and Abe Seiden (UCSC), Ultra-Fast Silicon Detectors (UFSD).

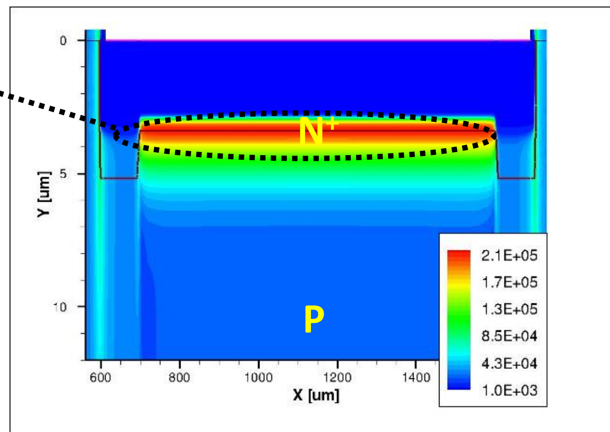
- Provide in the same detector and readout chain:
  - Ultra-fast timing resolution [10's of ps]
  - Precision location information [10's of µm]
- We propose to achieve high electric field using thin p-type epitaxyal substrates grown on thick support wafers, p+ type doped, that acts as the backside ohmic contact. Different thicknesses will be used to study the multiplication effect induced by the high electric field at the collecting electrodes, depending on availability we propose to use: 10, 50, 75um. **Need very fast pixel readout.**

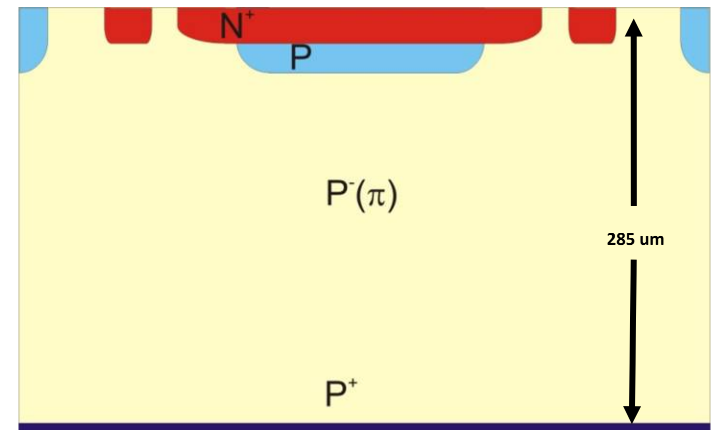
H. Sadrozinski, "Exploring charge multiplication for fast timing with silicon sensors" 20th RD50 Workshop, Bari 2012

2)Low gain avalanche detectors (LGAD)

Creating an n++/p+/p- junction along the center of the electrodes. Under reverse bias conditions, a high electric field region is created at this localized region, which can lead to a multiplication mechanism.

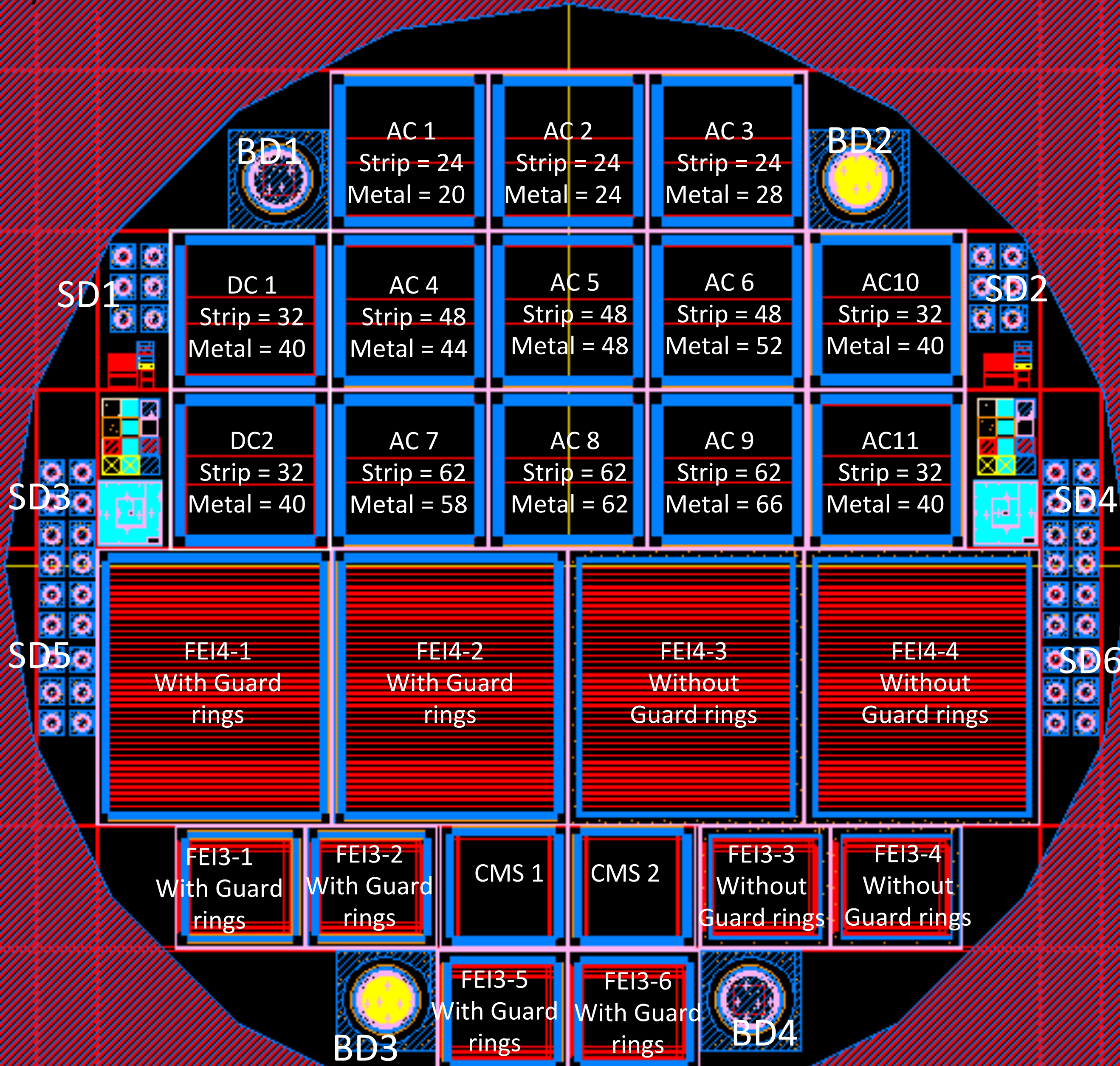
High Electric Field region leading to multiplication





P. Fernandez et al, "Simulation of new p-type strip detectors with trench to enhance the charge multiplication effect in the n-type electrodes" , Nuclear InstrumentsandMethodsinPhysicsResearchA658(2011) 98–102.

Mask layout



Fabrication

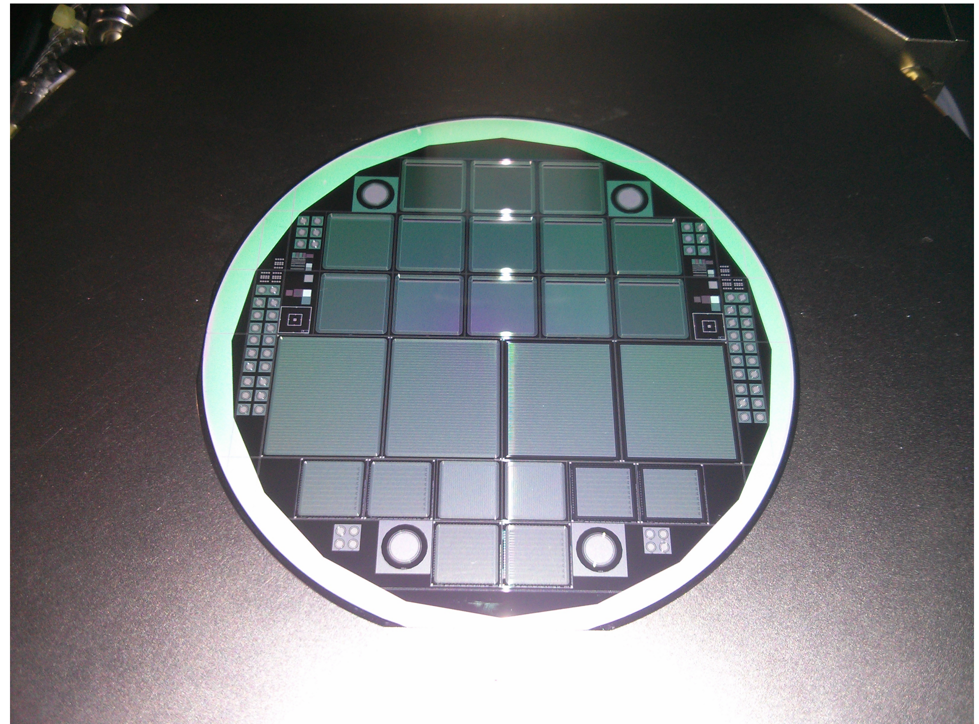
In June fabrication finished in CNM Barcelona

- Epitaxial 10um
- Epitaxial 50um
- Epitaxial 75um
- Float Zone

- Fabrication of 2 runs
  - 14 wafers with LGAD
  - 14 wafers without LGAD

4 wafers are diced and half of them are in Santa Cruz

24 wafers are in CNM



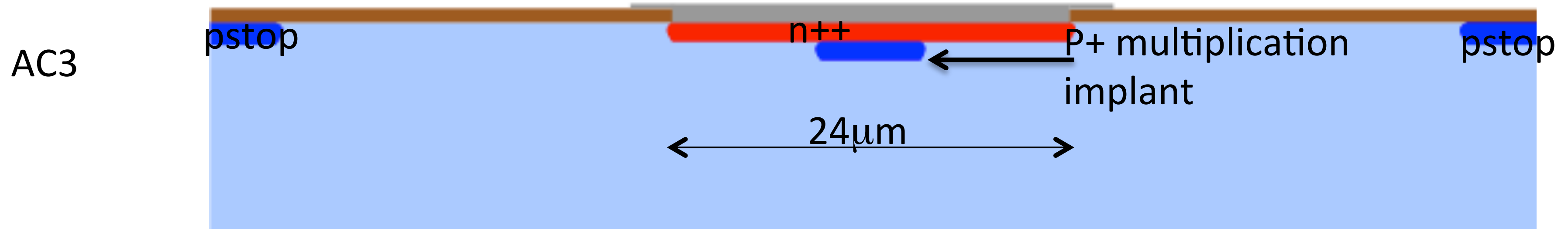
Strip detectors

Pitch p=80 μm

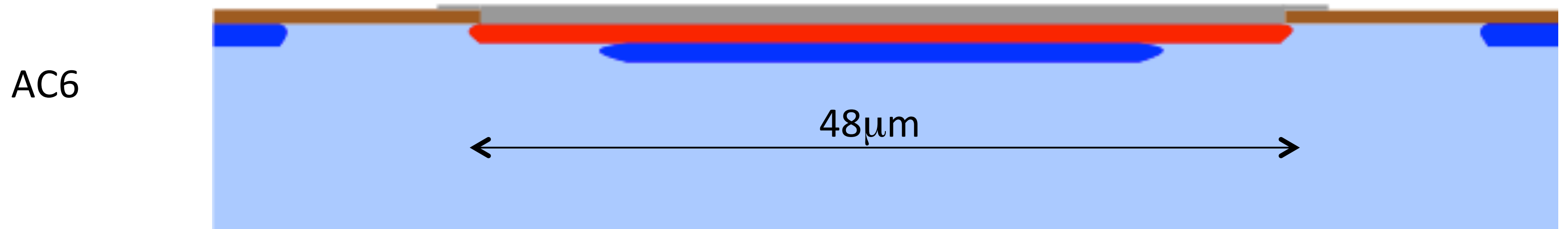
	Strip width [μm]	Metal [μm]	P-implant [μm]	w/p	P-implant/ pitch
AC1	24	20	6	0.3	7.5%
AC2	24	24	6	0.3	7.5%
AC3	24	28	6	0.3	7.5%
AC4	48	44	30	0.6	37.5%
AC5	48	48	30	0.6	37.5%
AC6	48	52	30	0.6	37.5%
AC7	62	58	44	0.775	55%
AC8	62	62	44	0.775	55%
AC9	62	66	44	0.775	55%
AC10/AC11/ DC	32	40	14	0.4	17.5%

Strip cros-section: Pitch 80um

AC3



AC6



AC9

Wafers

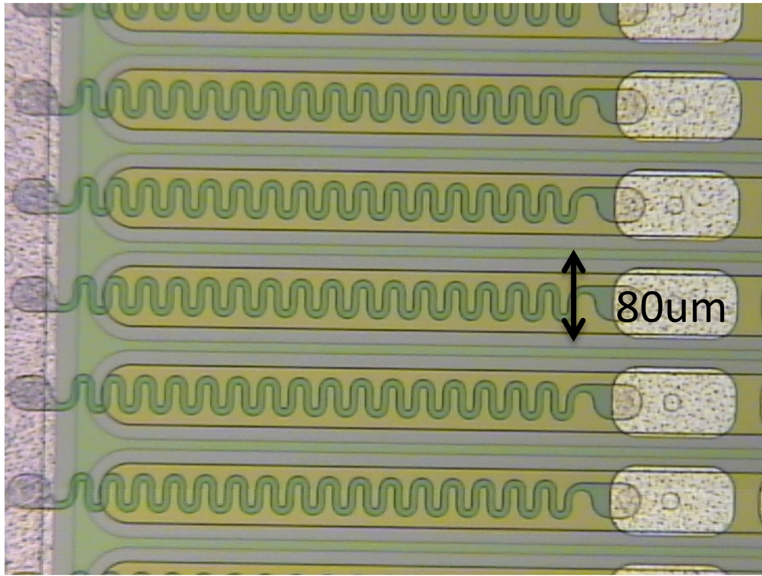
# of Wafers	Thickness (um)	Substrate thickness (um)	Resistivity (Ohms·cm)	Substrate resistivity (Ohms·cm)
4	9.8 Epitaxial	525	110.5	0.006
4	50.4 Epitaxial	525	96.7	0.006
3	75.2 Epitaxial	525	104.6	0.006
3	285 (FZ)		12000+-7000	

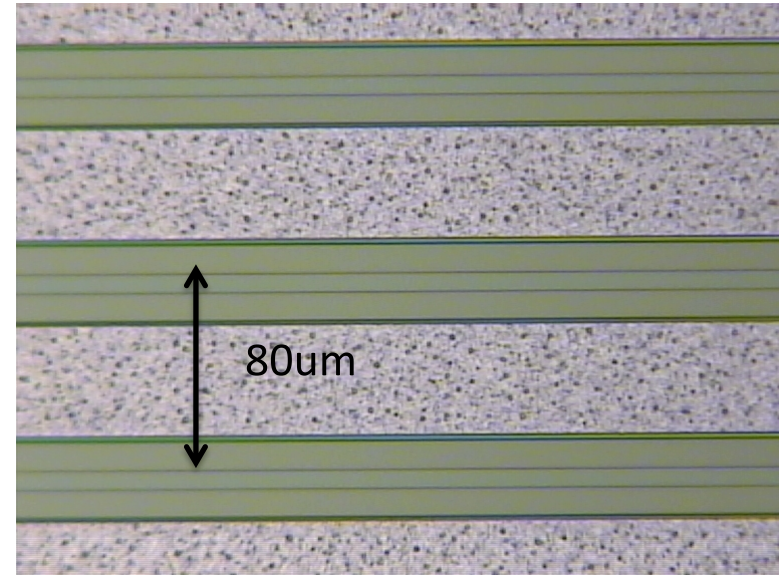
Annealing

	Time	Temperature [ºC]
Shallow	20s	950
Standard	51min	1000
Deep	51min	1100

Fabrication LGAD with epitaxis

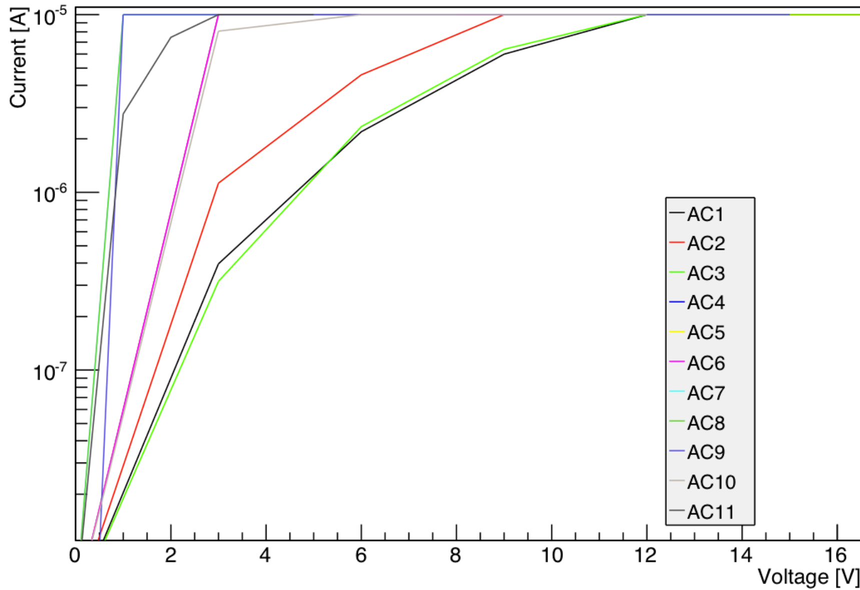
# wafer	Wafer	P-stop	Drive in	Annealing
1-2	Epitaxial 10		No	Shallow
3	Epitaxial 10	no	No	Standard
4	Epitaxial 10		No	Standard
5	Epitaxial 50			Shallow
6	Epitaxial 50			Standard
7	Epitaxial 50	no		Standard
8	Epitaxial 50			Deep
9	Epitaxial 75			Shallow
10	Epitaxial 75			Standard
11	Epitaxial 75			Deep
12	FZ			Shallow
13	FZ			Standard
14	FZ			Deep

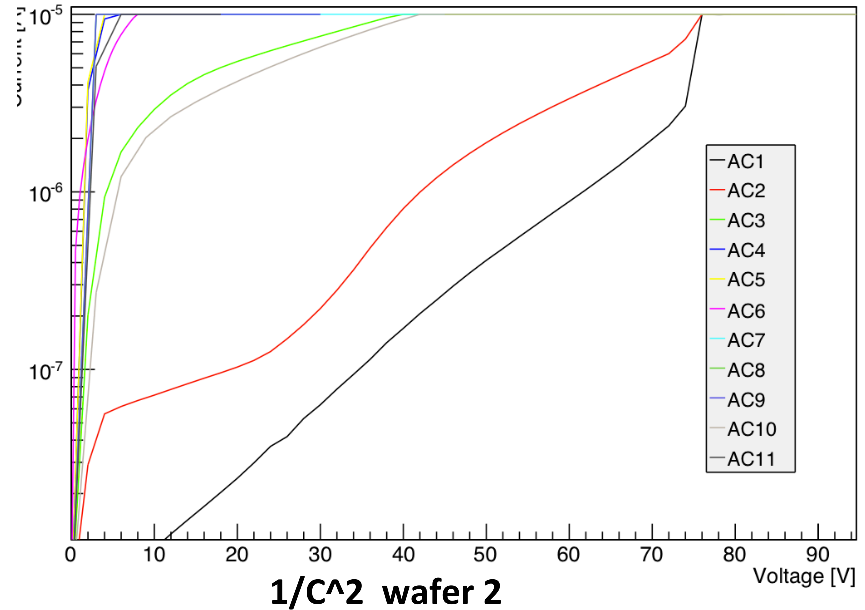




STRIPS:
ELECTRICAL CHARACTERIZATION

Epitaxial 10um wafers: IV and CV

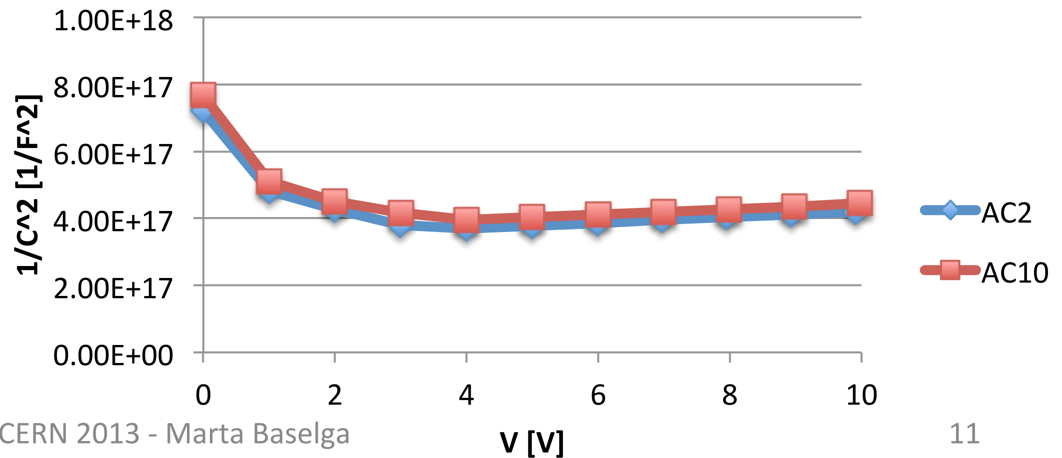




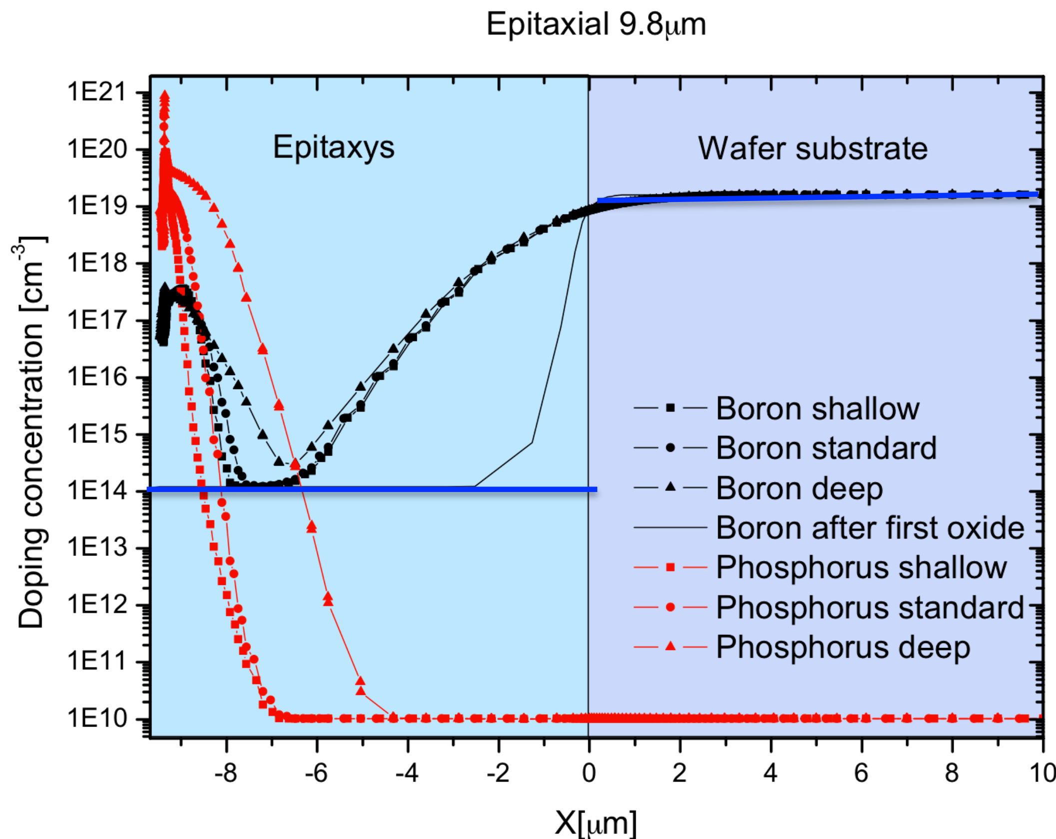
Wafer 1, 2, and 3 break down voltage before 12V

Some break down voltage for wafer 4 is up to 70V

Wafer 2 - C very high! Resistance very low



Epitaxial 10um: Doping simulation*



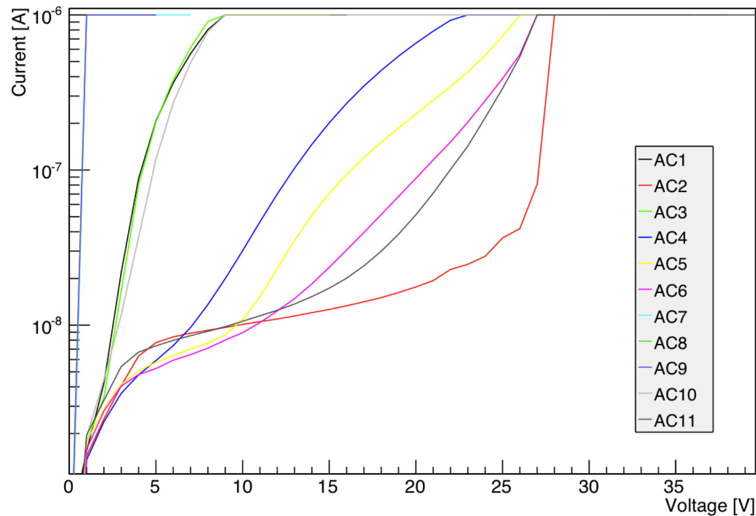
Deep annealing was not performed in 10um epitaxial wafers

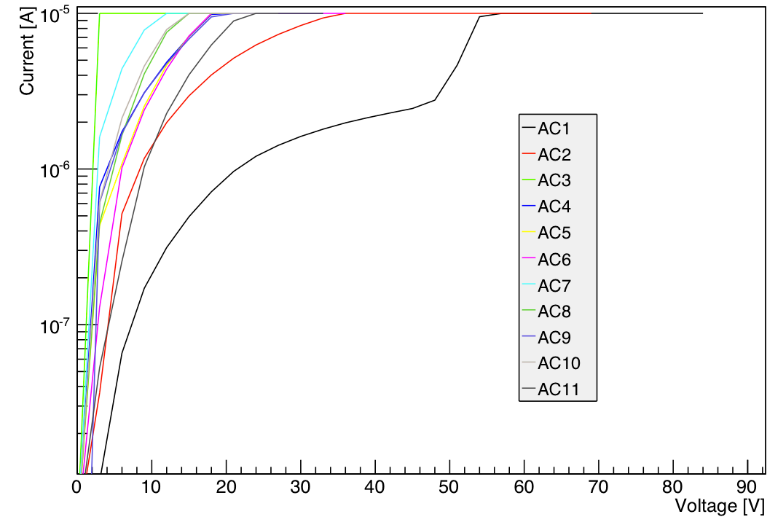
We are concerned that after all the fabrication process the boron (p+ implant) had diffused to the substrate wafer (high boron doped wafer)

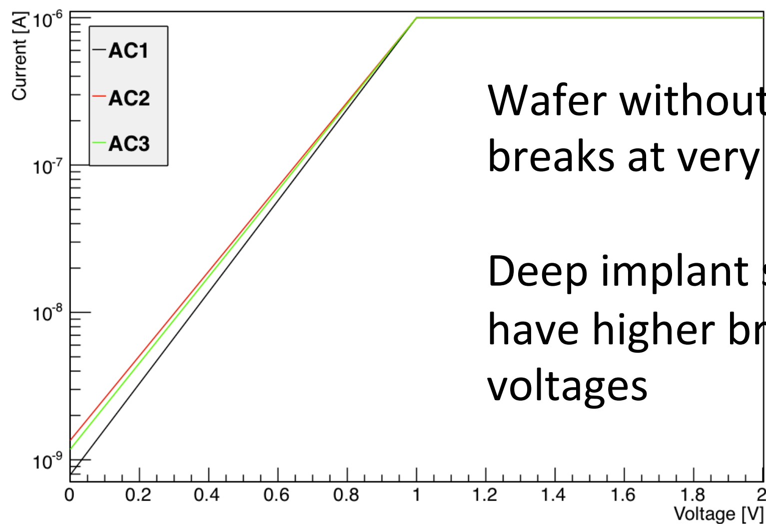
Initial boron profile

*Sentaurus TCAD

Epitaxial 50um IV curves

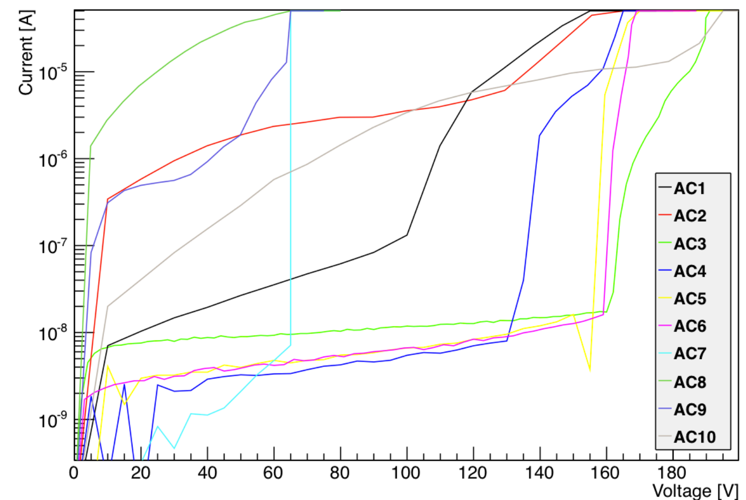




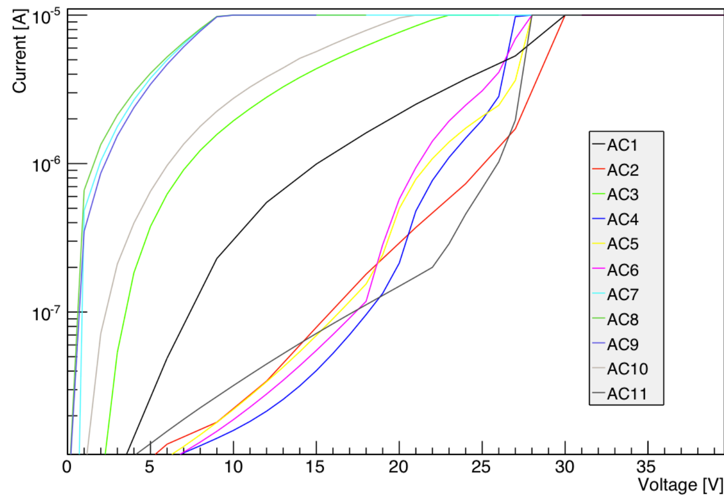


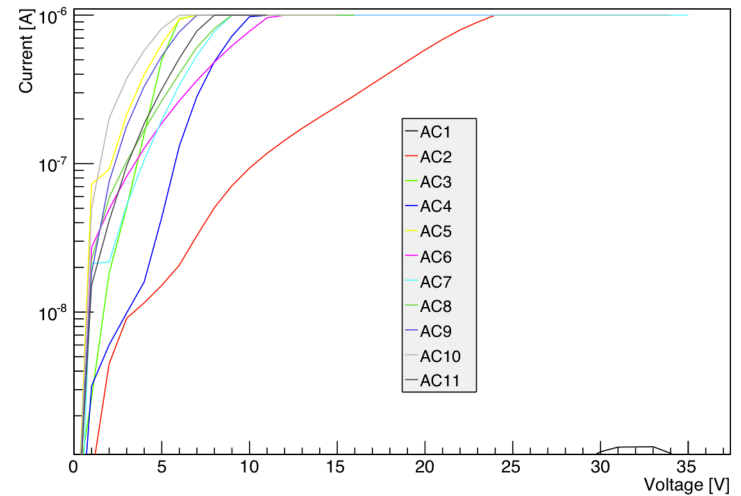
Wafer without p-stop breaks at very low voltage

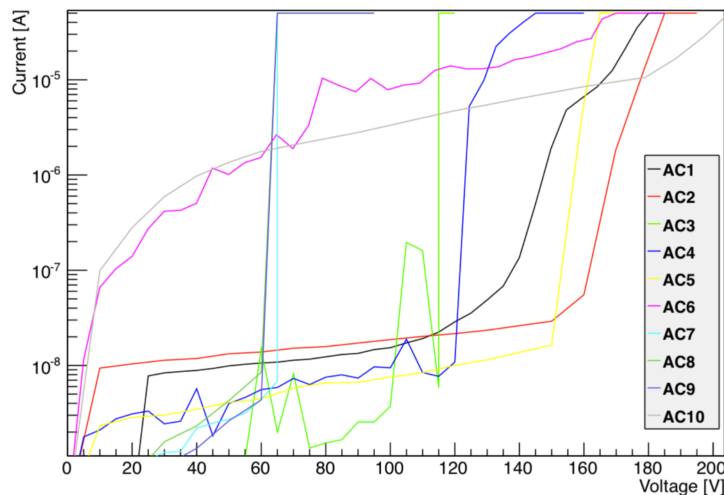
Deep implant seems to have higher break down voltages



Epitaxial 75um: IV curves



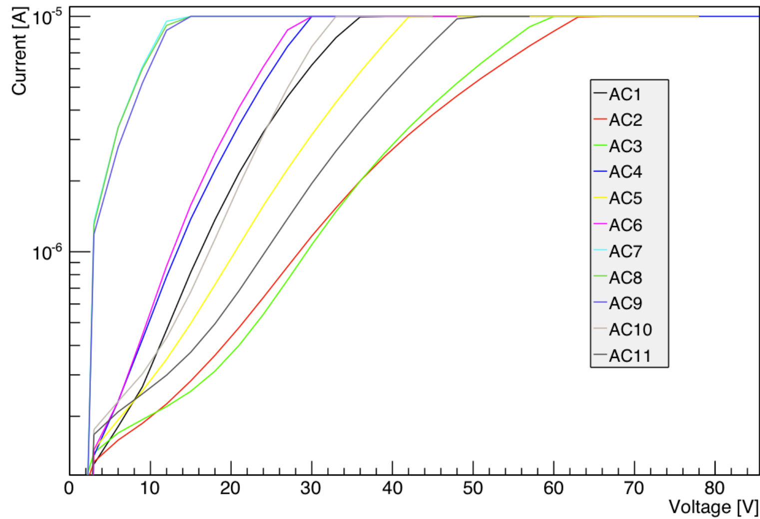


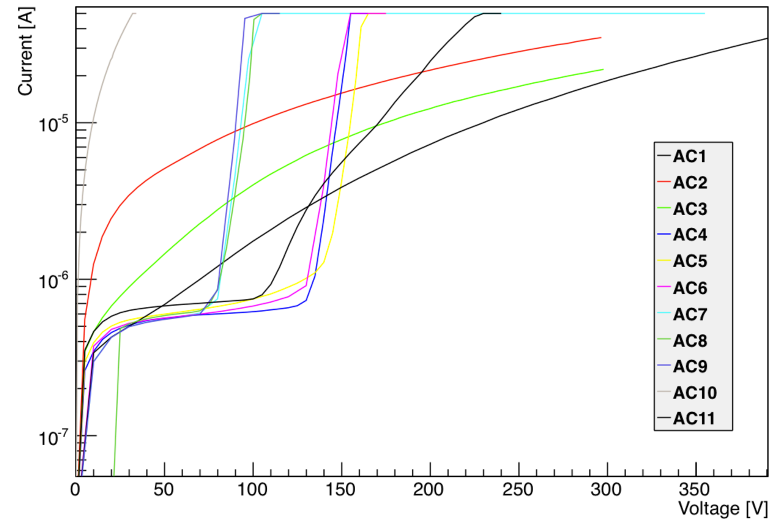


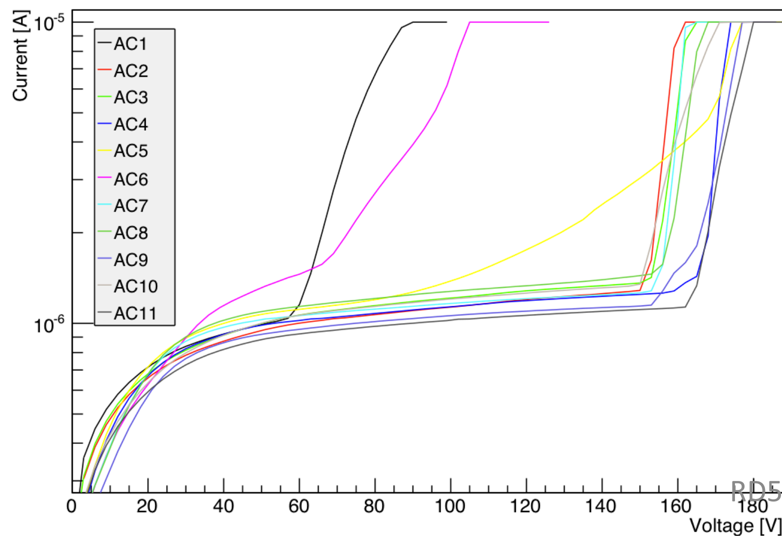
Deep annealing seems to have higher break down voltages and lower leakage current

First detectors to break down are the ones with wider strip

Float zone: IV curves

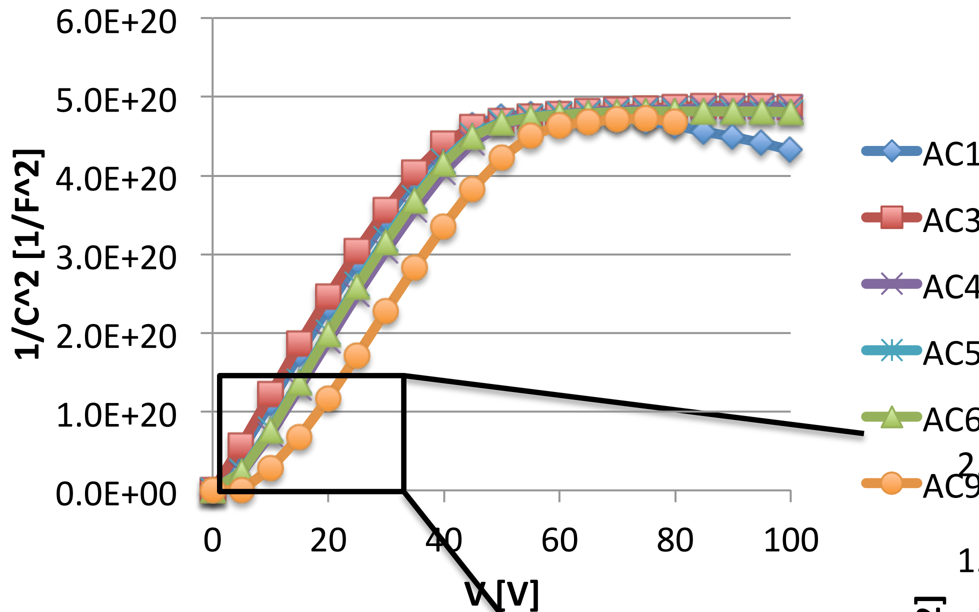




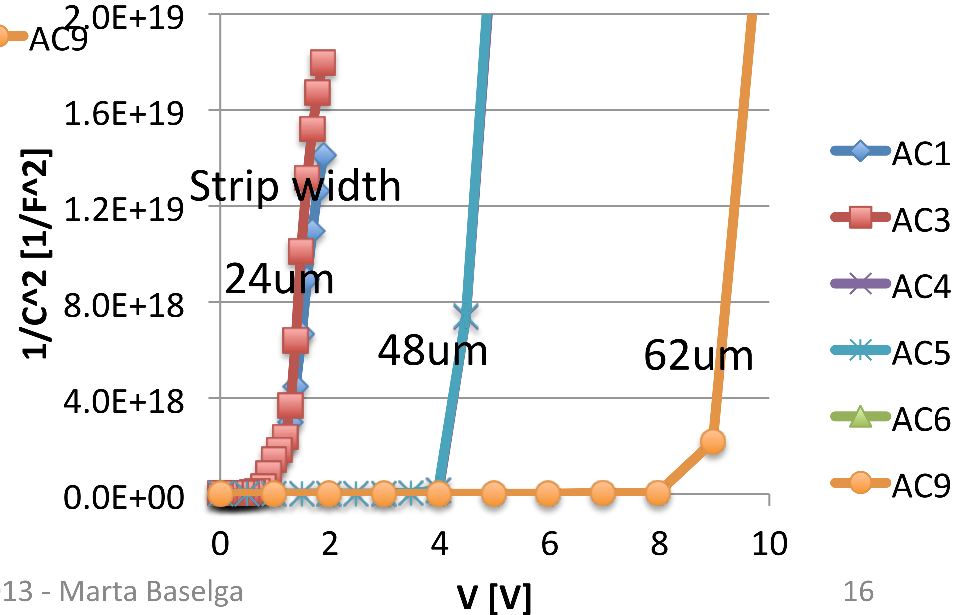


Deep annealing have the higher break down voltage

Float Zone: W13 (standard annealing) CV



The wider the p+ implant the longer the foot



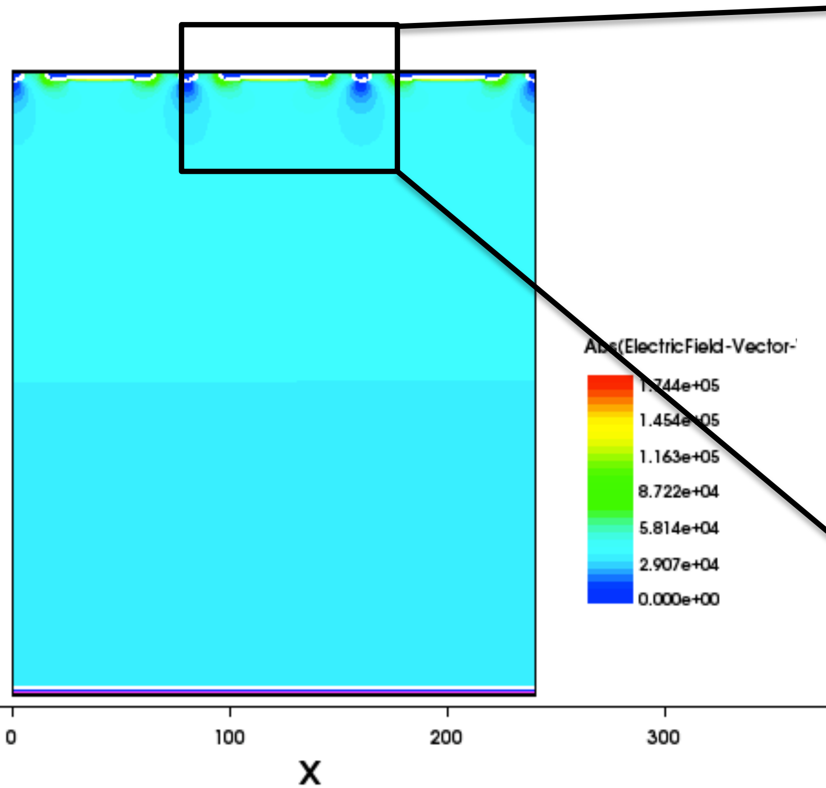
Full depletion voltage @50V

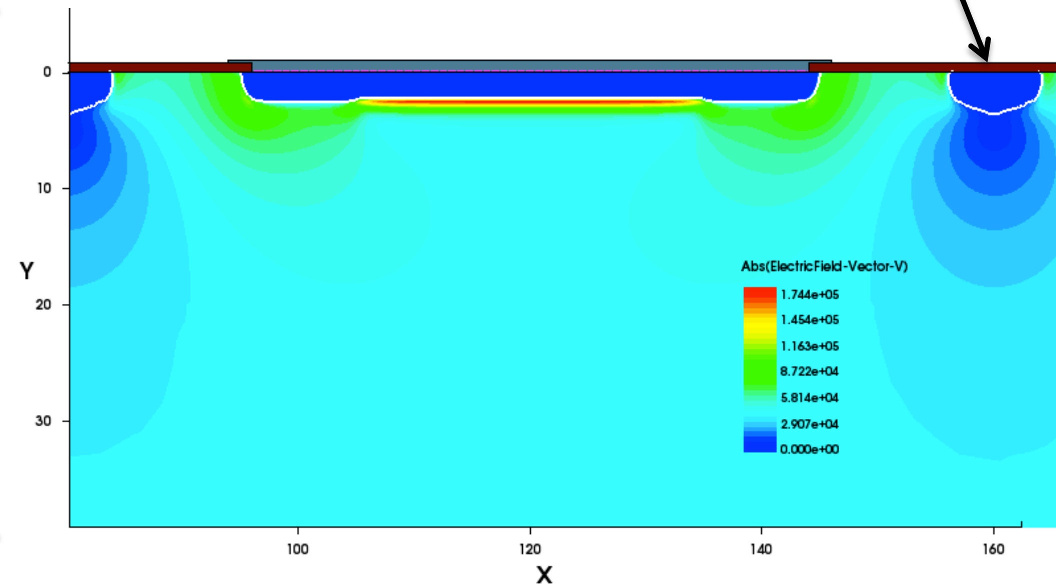
Strip detectors

Pitch p=80 μm

	Strip width [μm]	Metal [μm]	P-implant [μm]	w/p	P-implant/ pitch
AC1	24	20	6	0.3	7.5%
AC2	24	24	6	0.3	7.5%
AC3	24	28	6	0.3	7.5%
AC4	48	44	30	0.6	37.5%
AC5	48	48	30	0.6	37.5%
AC6	48	52	30	0.6	37.5%
AC7	62	58	44	0.775	55%
AC8	62	62	44	0.775	55%
AC9	62	66	44	0.775	55%
AC10/AC11/ DC	32	40	14	0.4	17.5%

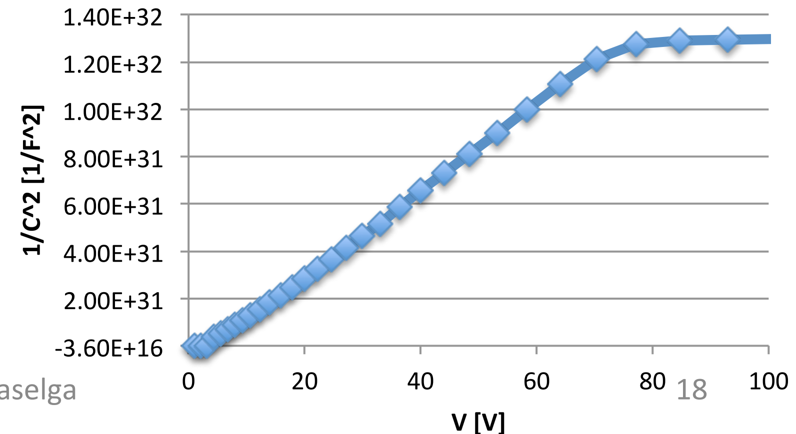
Simulation of strips @1000V AC6 (strip width 48um) FZ Deep annealing



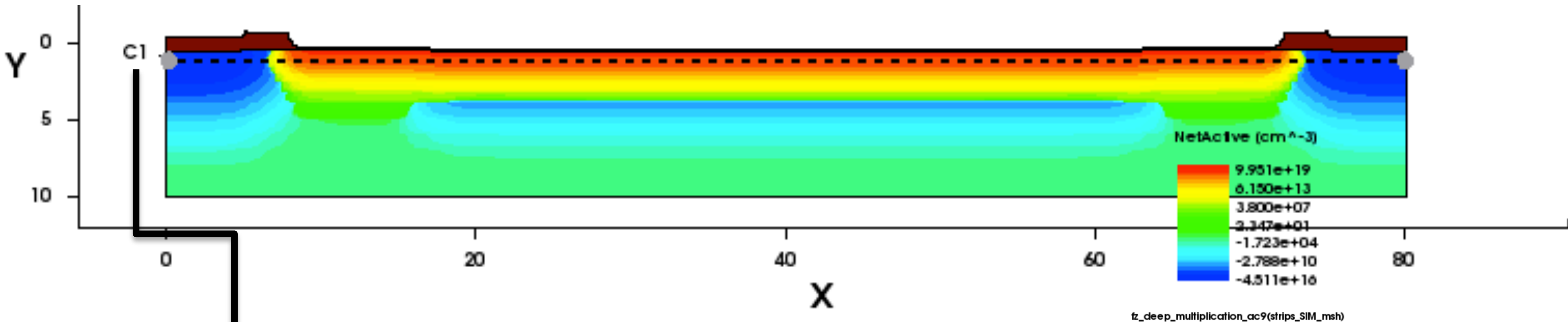


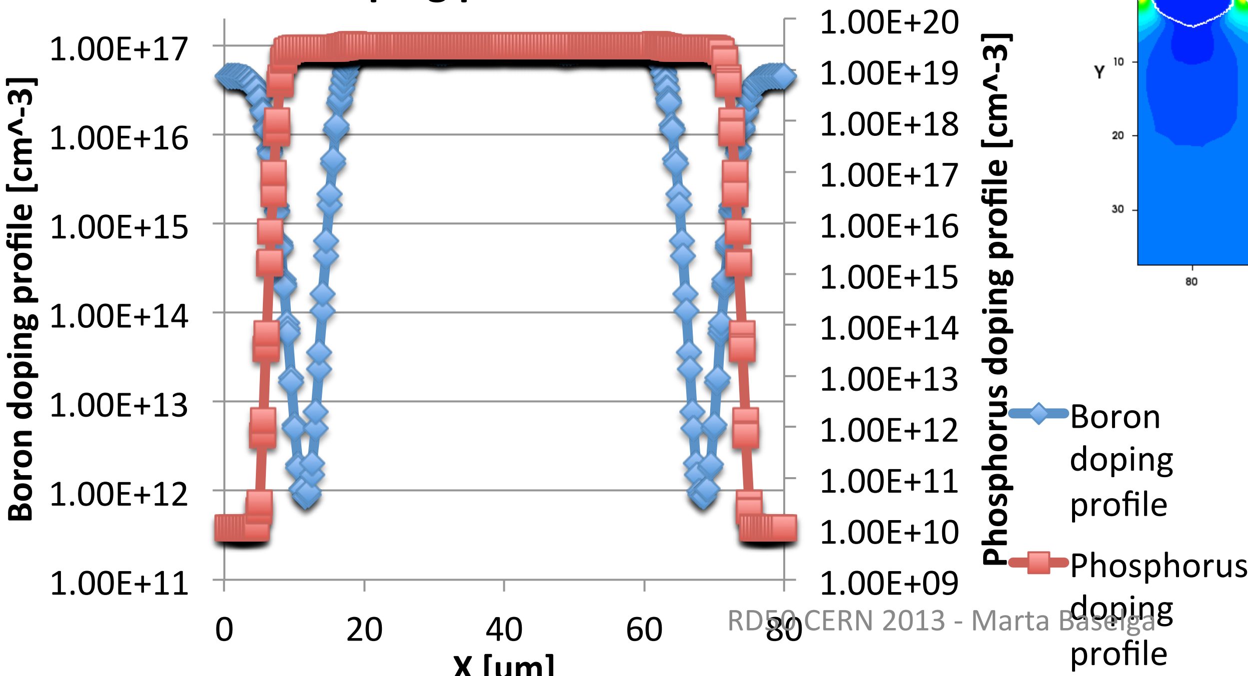
Electric field simulations show that the electric field is higher down the strip

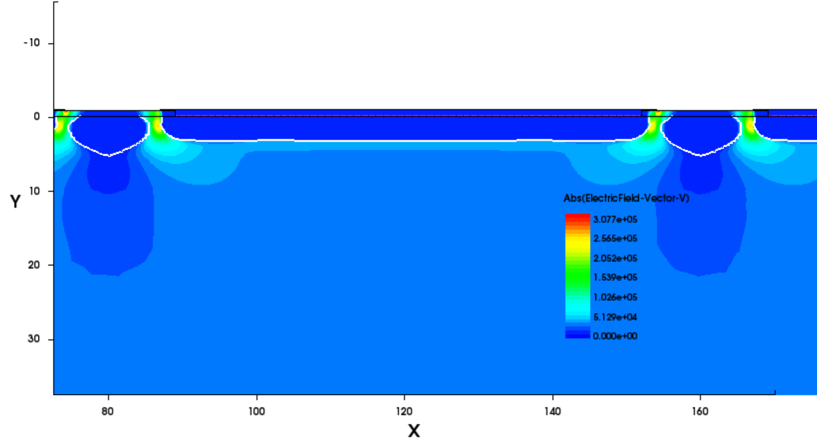
CV curves shows a foot of 6V



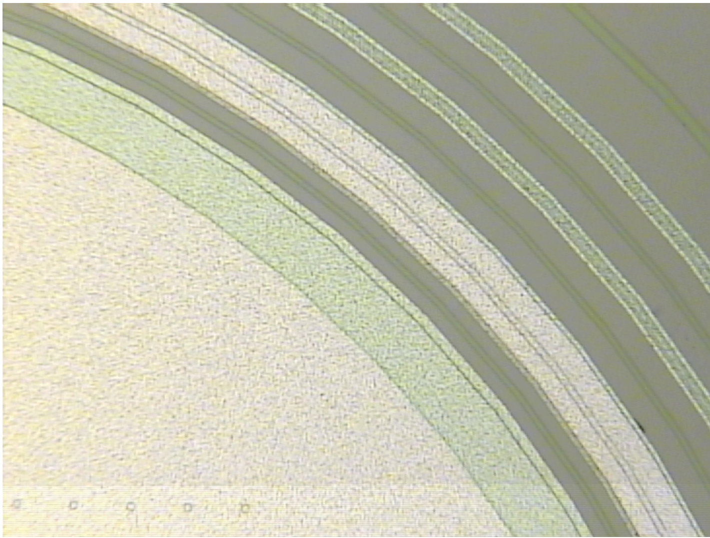
Simulation for AC9 (strip width 62um)

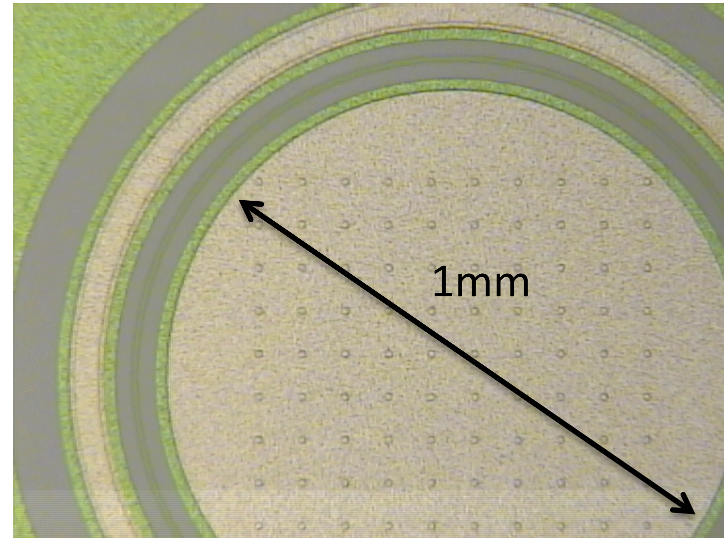






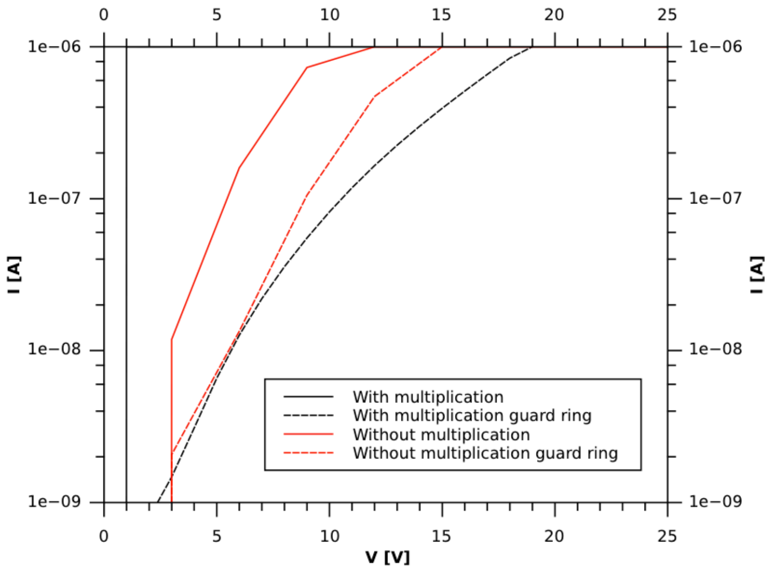
Electric field simulation
High electric field between the strip and the pstop at 600V

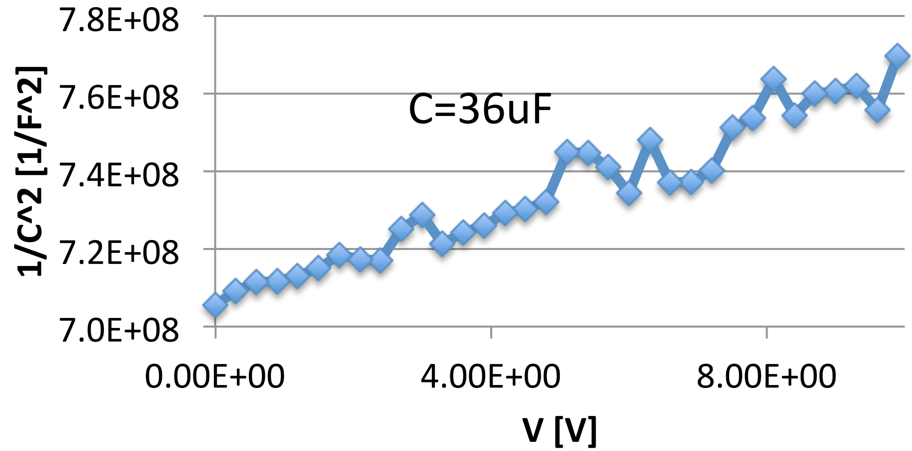




PAD DETECTORS

Epitaxial 10 um

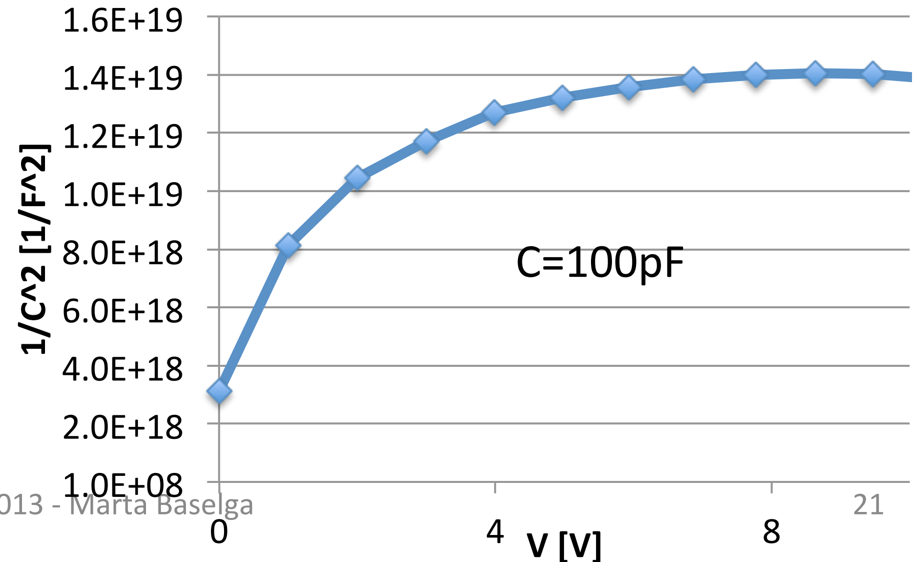




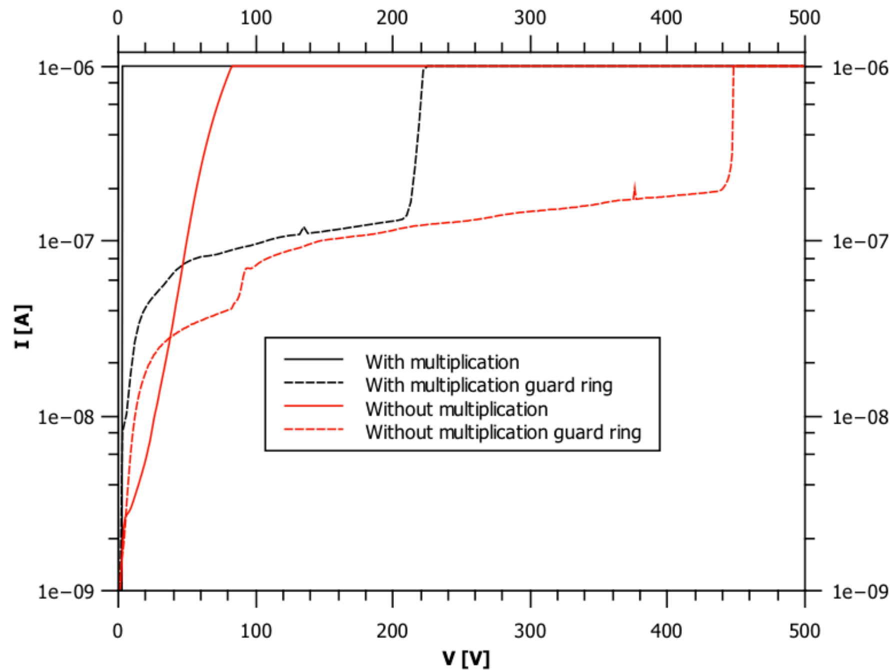
Diodes without multiplication seems to be working

Diodes with multiplication breaks at very low voltages

CV curve for diodes without multiplication has low full depletion voltage 6V

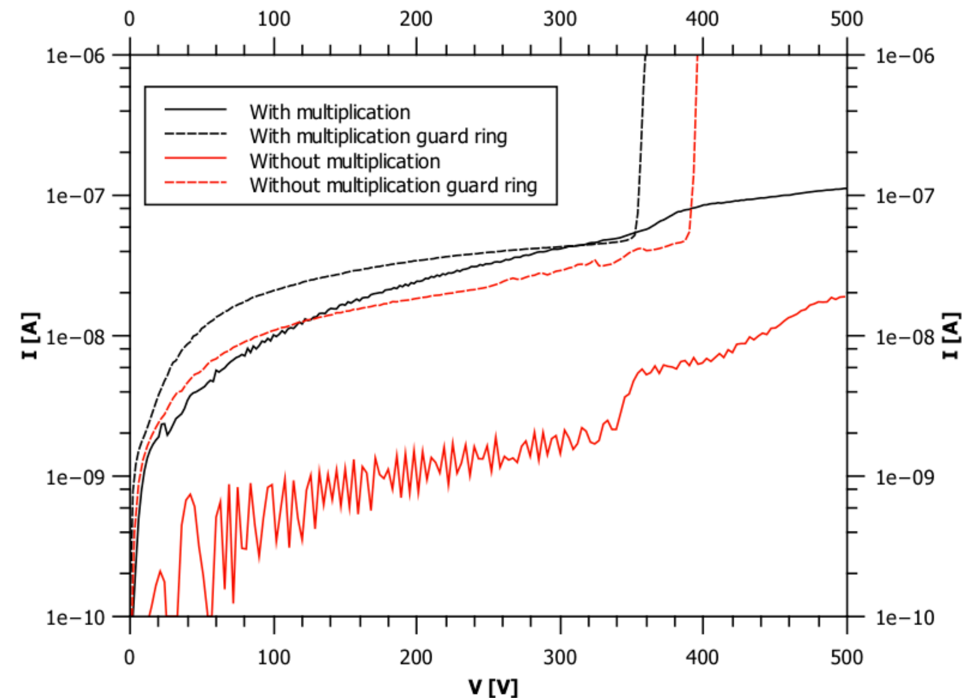


Epitaxial 50um: IV

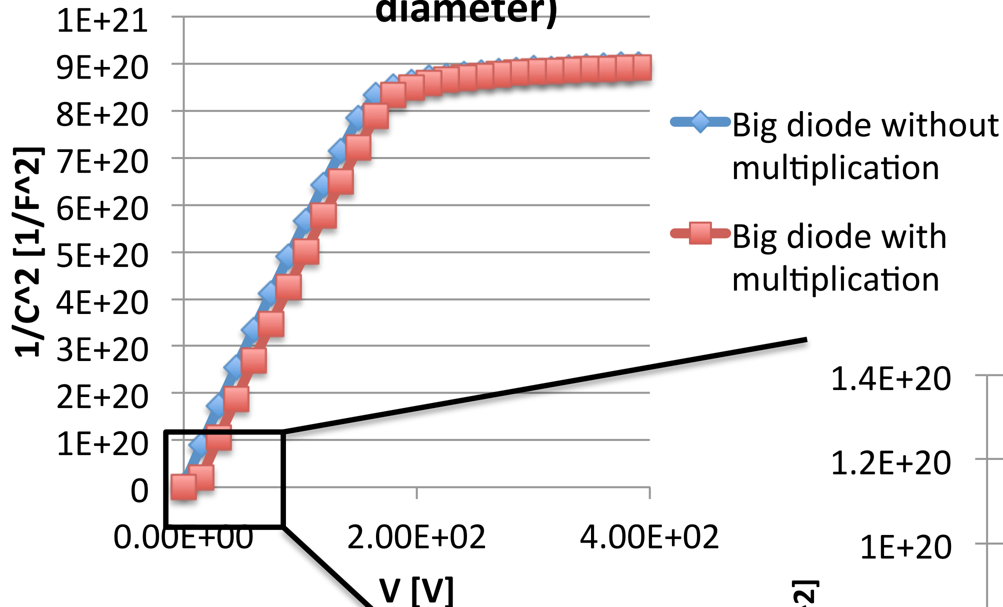


Break down voltage of diodes with gain has lower values than the diodes without gain

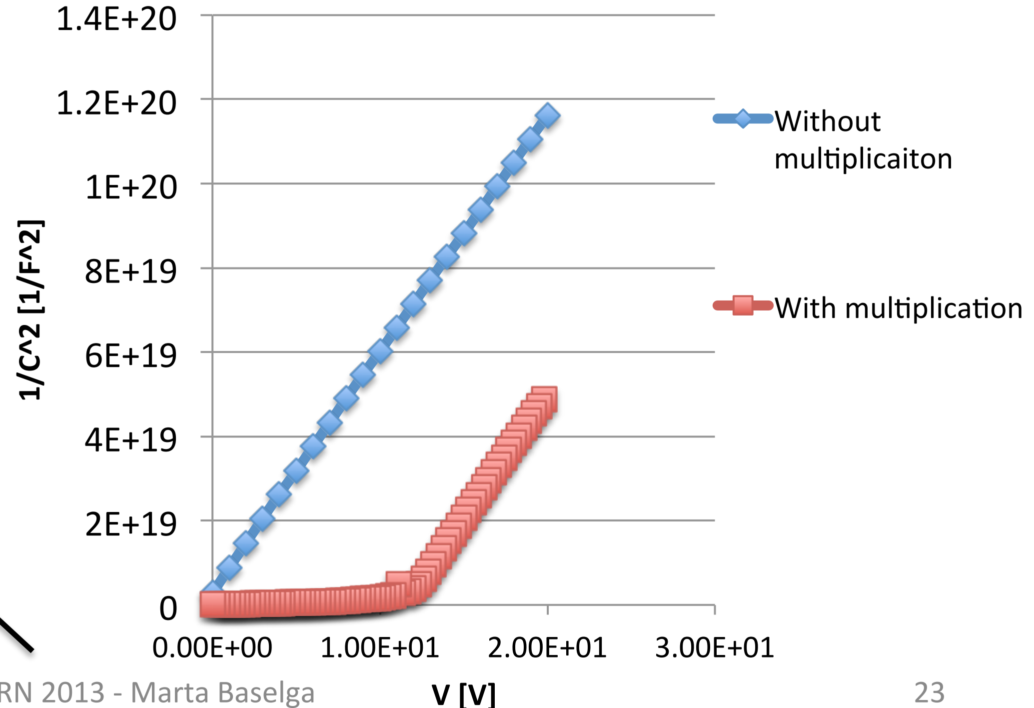
Wafer with deep annealing



Epitaxial 50um: CV

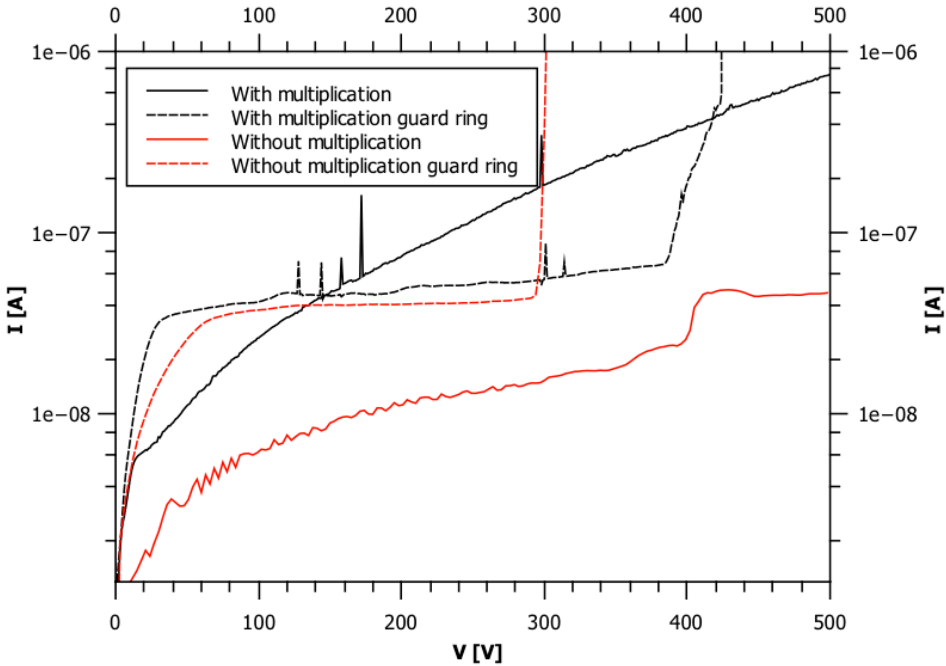


Full depletion voltage @175 V
Gain sensor has a foot of 12 V

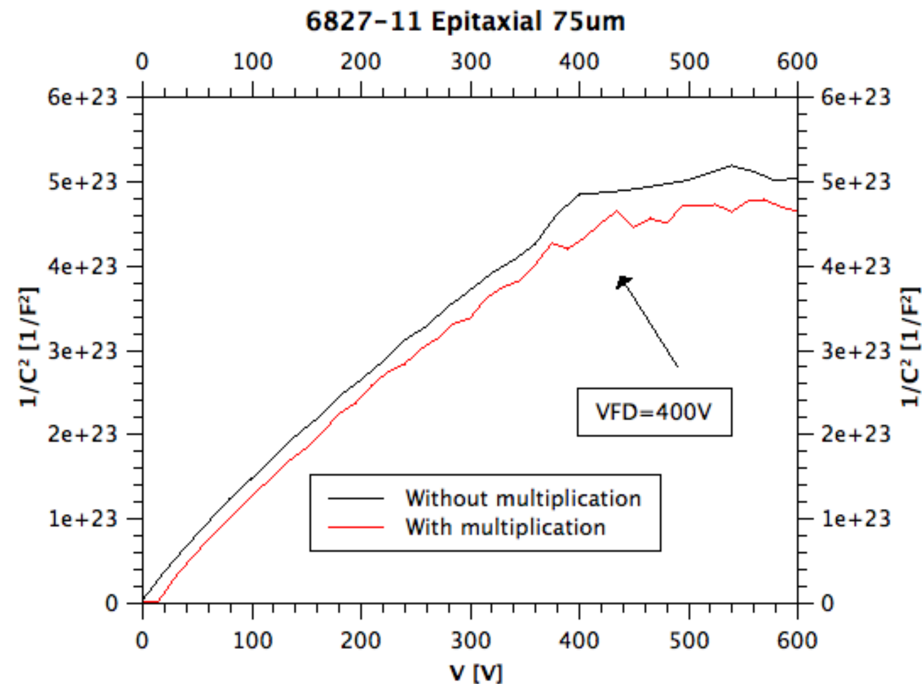


Some TCT measurements in Hartmut Sadrozinski presentation

Epitaxial 75um: IV and CV

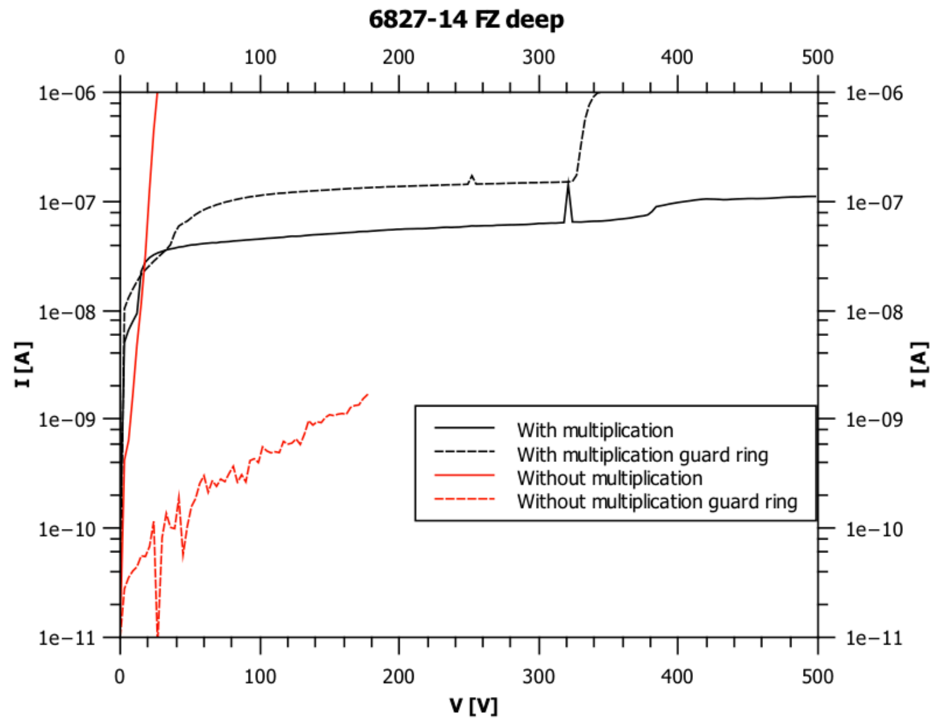


Break down voltage are high for deep annealing



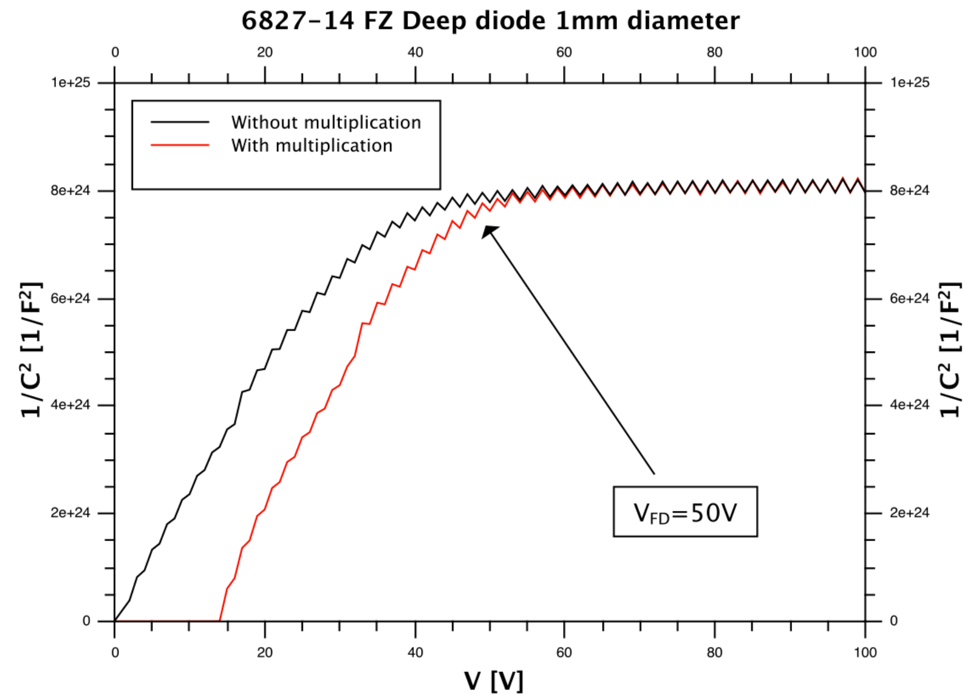
Full depletion voltage @400V

Float zone wafers



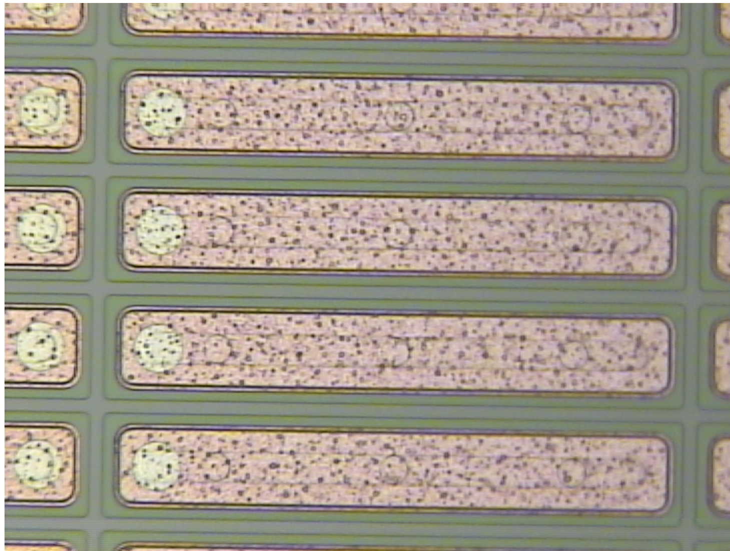
High break down voltage for deep annealing

Foot around 14V

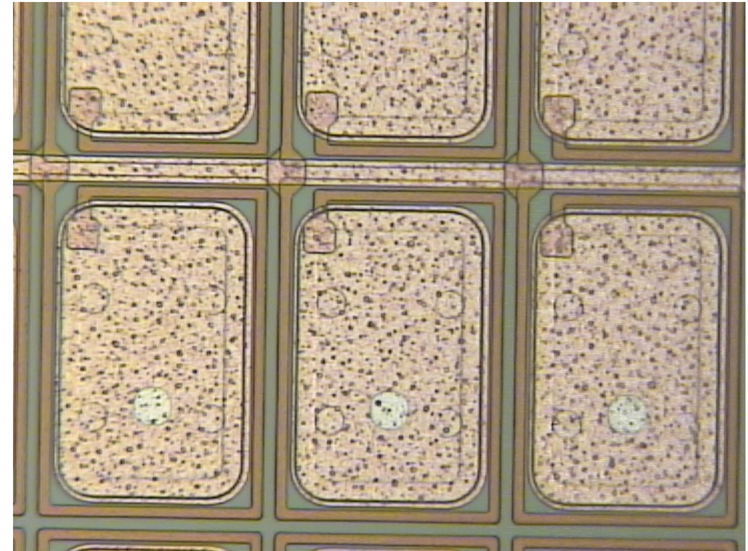


Full depletion voltage @50V

FEI4 pixel

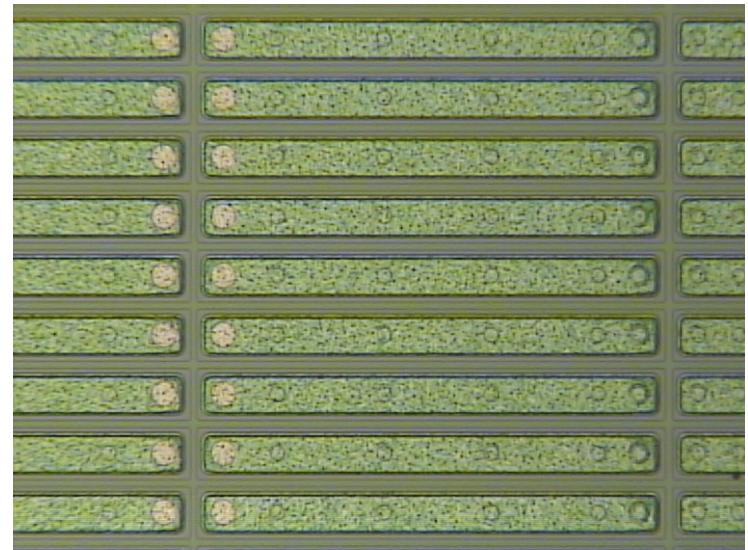


CMS

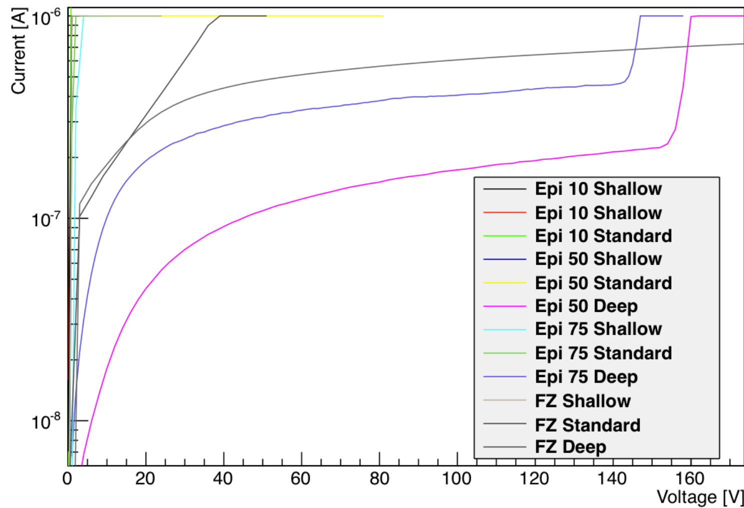


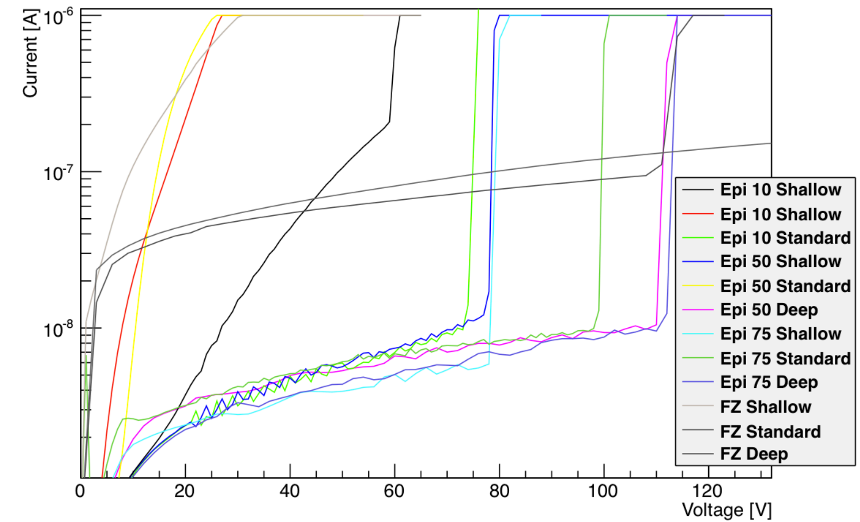
OTHER DETECTORS

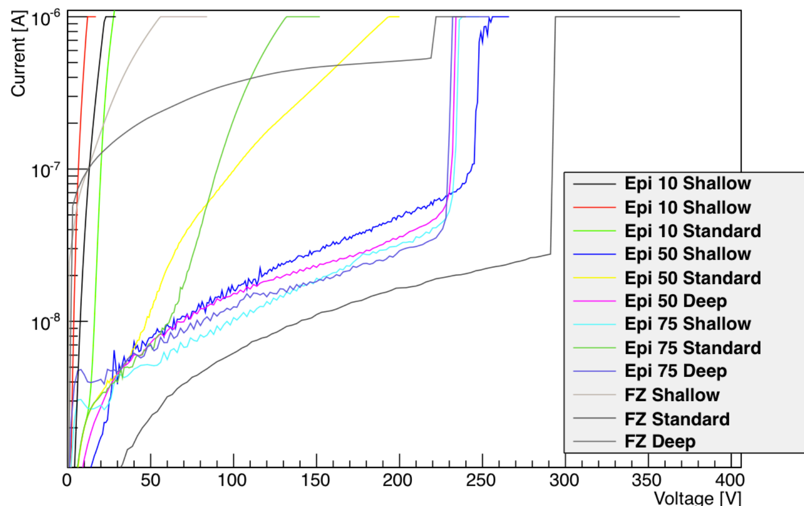
FEI3 pixels



Measurements for the guard ring and bias grid (CMS)







FEI3 and FEI4 measurements are for the guard ring

Deep annealing have higher break down voltage

Conclusions

- Detectors were successfully fabricated in CNM Barcelona
- P-implant and substrate of epitaxial 10um wafers seem to have diffused too much
- CV curves for strip detectors present a foot depending on the p-implant width
- For epitaxial wafers, alphas have to be put from the front of the sensor due to the 525um substrate wafer
- More results on TCT measurements in Hartmut Sadrozinski presentation

THANKS FOR YOUR ATTENTION.
ANY QUESTIONS?