Planar Pixel Detectors for the ATLAS Pixel Detector upgrade

Gianluigi Casse

UNIVERSITY OF LIVERPOOL

Acknowledgements: PPS Collaboration Members

PPS's participating members:

- CERN
- AS CR, Prague (Czech Rep.)
- LAL Orsay (France)
- LPNHE (France)
- University of Bonn (Germany)
- HU Berlin (Germany)
- DESY (Germany)
- TU Dortmund (Germany)
- University of Göttingen (Germany)
- University of Geneva (CH)
- MPP & HLL Munich (Germany)
- Università degli Studi di Udine – INFN (Italy)
- KEK (Japan)
- Tokyo Inst. Tech. (Japan)
- IFAE-CNM, Barcelona (Spain)
- University of Liverpool (UK)
- UC Berkeley/LBNL (USA)
- UNM, Albuquerque (USA)
- UCSC, Santa Cruz (USA)

ATLAS Planar Pixel Sensor Project

GOALS

- Prove Planar Technology for all radii of HL-LHC with rad-hard geometries (n-in-n, n-in-p)
- Geometry optimization: Slim/Active edges for improved tiling
- Cost reduction

TOOLS

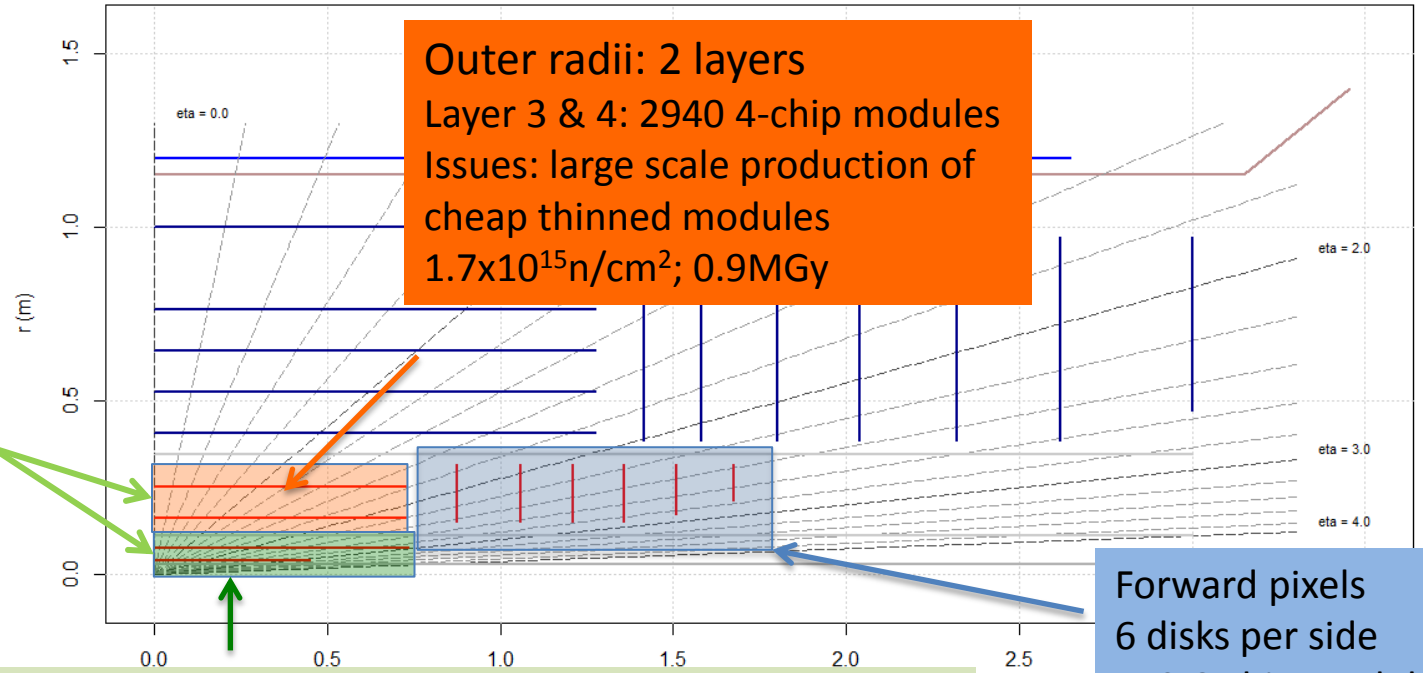
- Productions
  CiS, MPI-HLL, MICRON, HPK, VTT
- Irradiations
  Reactor neutrons (Ljubljana)
  26 MeV protons (Karlsruhe)
  800 MeV protons (Los Alamos)
  24 GeV protons (CERN)
  70 MeV protons (CYRIC)
- Advanced simulations
  TCAD packages with radiation parameters
- Lab and test beam measurements
  Radioactive sources
  120 GeV π (CERN)
  4 GeV e^- (Desy)
  Eudet telescope

ATLAS Planar Pixel Sensor Project

Silicon Planar technology for ATLAS upgrade pixels?? Have you seen the requirements?

Simone Martini (c. 1284 – 1344)

Phase-II Upgrade Pixel Detector

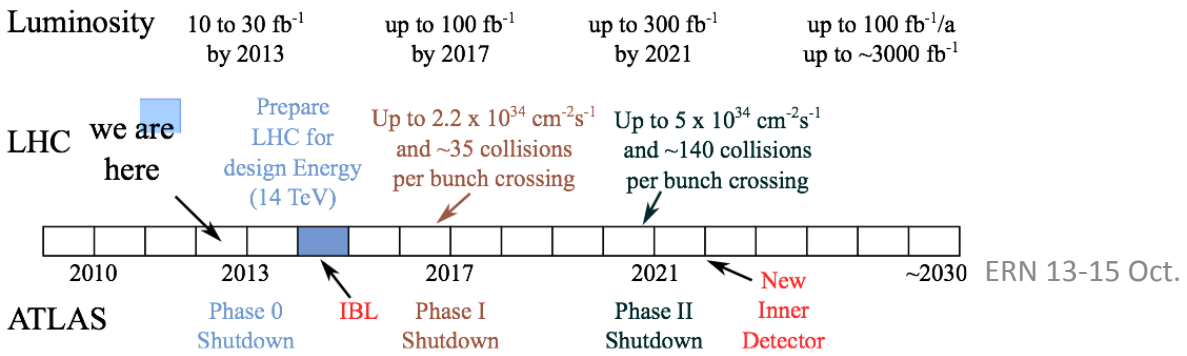


Outer radii: 2 layers
Layer 3 & 4: 2940 4-chip modules
Issues: large scale production of cheap thinned modules
1.7×10^{15}n/cm^2; 0.9MGy

Barrel pixels: 5.1 m^2 silicon area

Inner radii: 2 layers
Layer 1: 352 2-chip modules
Layer 2: 576 4-chip modules
Issues: radiation damage & small pixels 1.4×10^{16}n/cm^2; 7.7MGy

Forward pixels
6 disks per side
552 6-chip modules
280 4-chip modules
3.1 m^2 silicon area
Issues: large scale production of cheap thinned modules
1.8×10^{15}n/cm^2; 0.9MGy



ERN 13-15 Oct.

Requirements

- 2 Inner Barrel layers
  - Sensors
    - All sensor materials possible
    - 150 µm silicon or thinner
  - Pixel size 25 µm x 150 µm
  - ROIC thickness 150 µm
  - ToT = 0-8 bits
  - 2x1 and 2x2 chip modules
  - Data rate as high as 2 Gbit/s per module

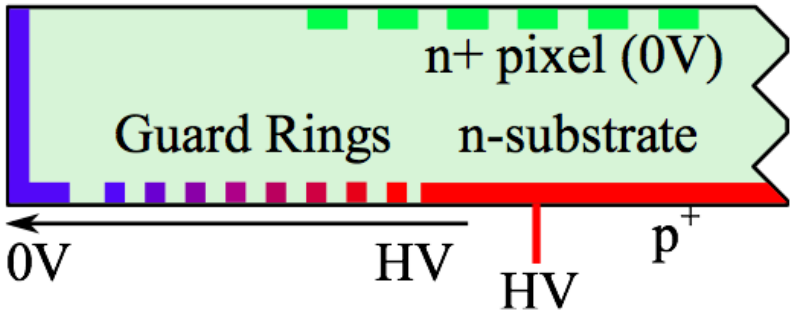
- 2 outer Barrel layers / Disks
  - Sensor planar n-in-p
  - Pixel size 50 µm x 250 µm
  - 150 µm thicknesss
  - ROIC FE-I4X; 2x2cm^2 thickness 150 µm
  - ToT = 4 bits
  - *2x2 FE-I4 (Quad) ~4x4cm^2*
  - Data rates of 640 Mbit/s per module

Current ATLAS

Phase-II upgrade ATLAS

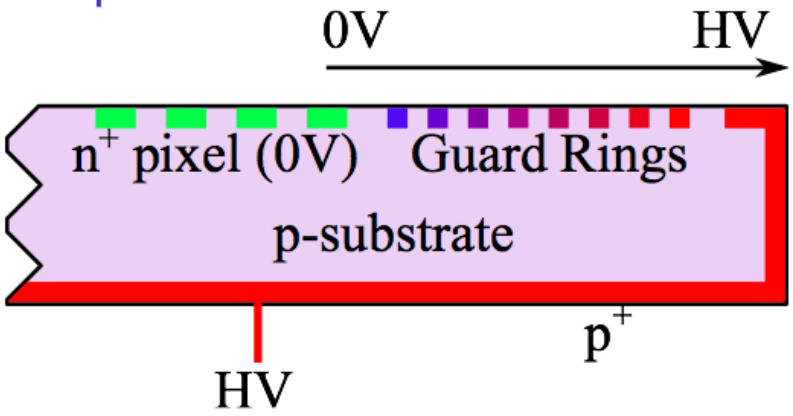
N-in-N vs N-in-P

n-in-n



- Double sided process (more expensive, up to 40%)
- Pixel can be shifted below guard-rings
- Used already widely (ATLAS, CMS, ...)

n-in-p



- Single sided process
- No backside-alignment needed

More foundries available Easier handling/testing, due to lack of patterned back-side implant

- Cost-effective
- Danger of sparks between chip and sensor ?

Issues to compare:

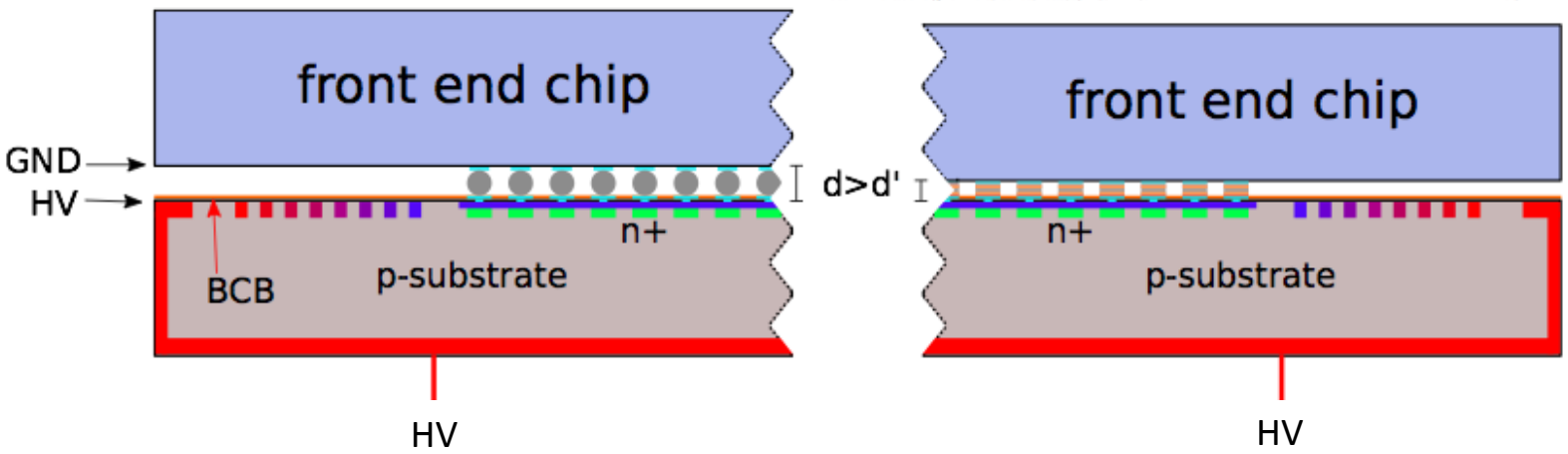
Radiation hardness

Prevention of edge sparks

Edge

Cost and handling

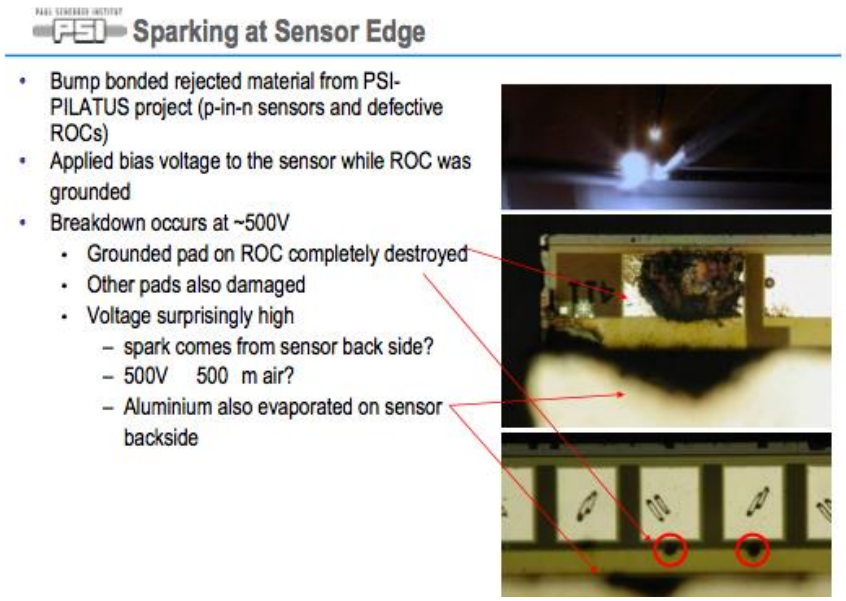
Edge sparking issue



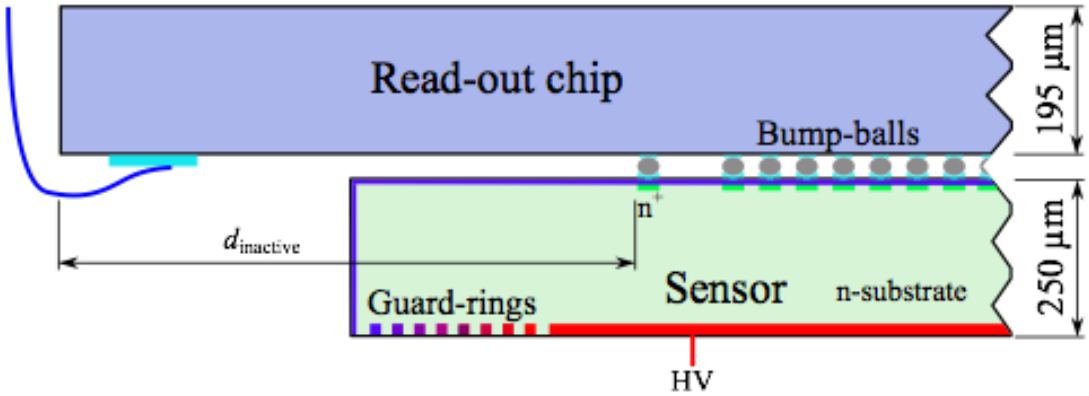
At Pixel 2010 T. Rohe reported about observed discharges between sensor and read-out chip.

- BCB: No Discharges observed up to 1000 V
- Parylene: Tested up to 700 V, no sparks [1]. (Later, other samples, 1000 V)
- Silicon adhesive: No discharges observed up to 1000 V

Y. Unno et al., "Development of novel n+-in-p Silicon Planar Pixel Sensors for HL-LHC", http://dx.doi.org/10.1016/j.nima.2012.04.061



Current ATLAS Pixel Detector

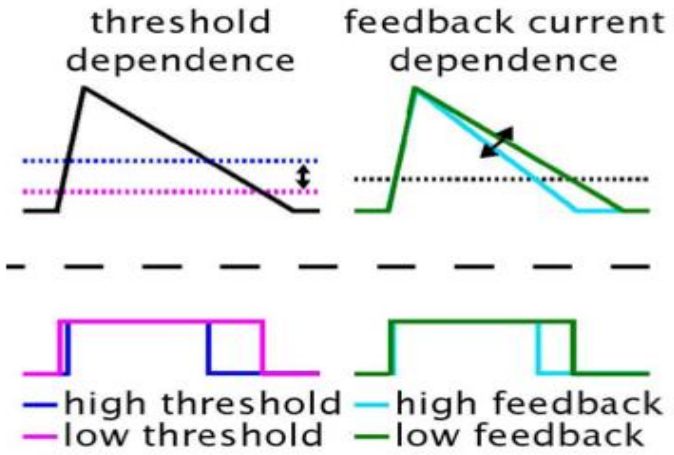


Sensor design

- DOFZ Si n-substrate, 250µm thick
- Read-out chip planar n+-in-n pixels, 400x50µm^2
- 16 guard rings on p side to shape HV step
- 1.1 mm inactive edge incl. safety margin

Read-out and interconnection

- FE-I3: 2880 channels
- DC coupled and bump bonding
- Shaper + Amplifier + Discriminator
- ToT ∝ Charge



Radiation hardness and thickness

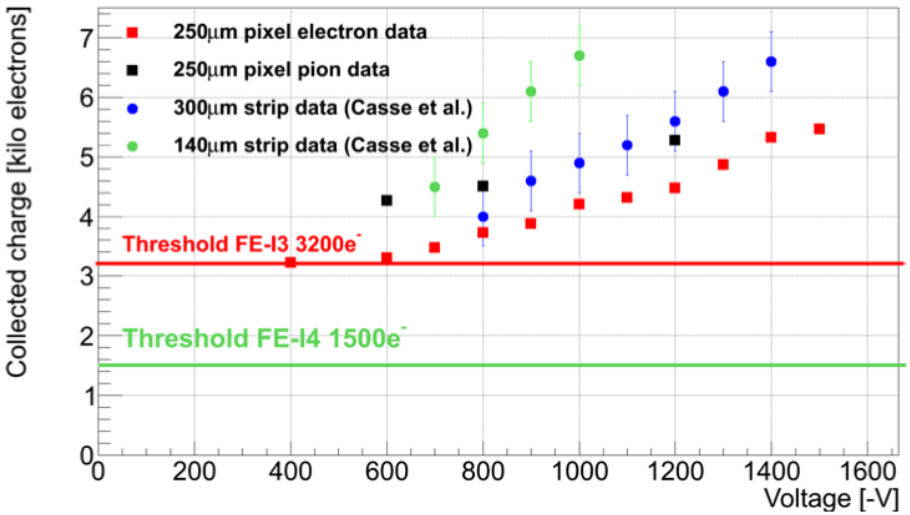
It is well documented that radiation hardness is improved (after high fluences) by thinning the sensors. Good for reducing the material. Radiation hardness of n- and p-type substrates and optimal thickness for the pixel layers is investigated.

n-in-n Sensors with FE-I3

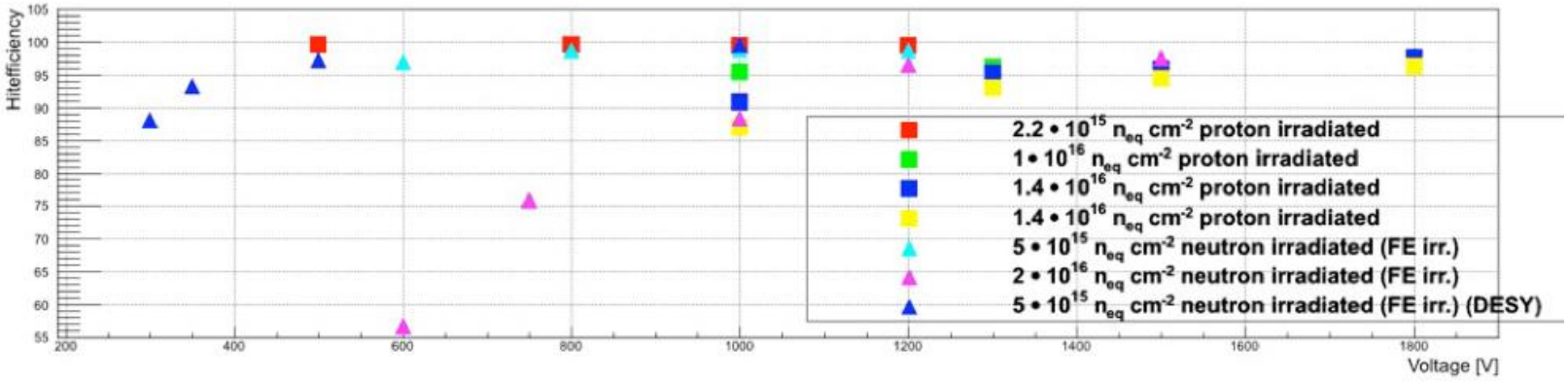
Performance of n-in-n sensors at the inner layer fluences

Combined results from MPP and TU Dortmund

- Produced at CiS with d=(250-285)µm
- Irradiated up to 2 · 10^{16} n_{eq}/cm^2 Charge as high as 4.2 ke at 1 kV
- FE-I4 chip allows for low thresholds of (1-1.5) ke
- Hit efficiency fully recoverable by increasing bias voltage
- Main loss in bias dot region



T. Wittig, "Radiation hardness and slim edge studies of planar n+-in-n ATLAS pixel sensors for HL-LHC", PIXEL2012



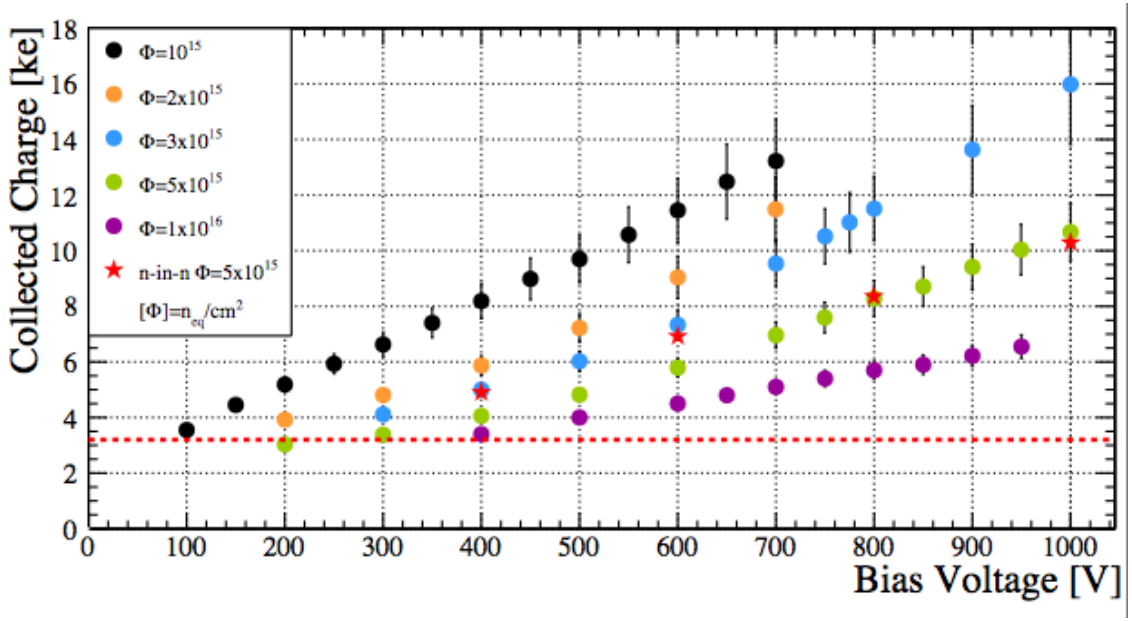
CC's for n-in-p Sensors with FE-I3 chip

MPP/HLL design produced by CiS on 285 µm FZ. n-irradiated up to 10^{16} n_{eq}/cm^2

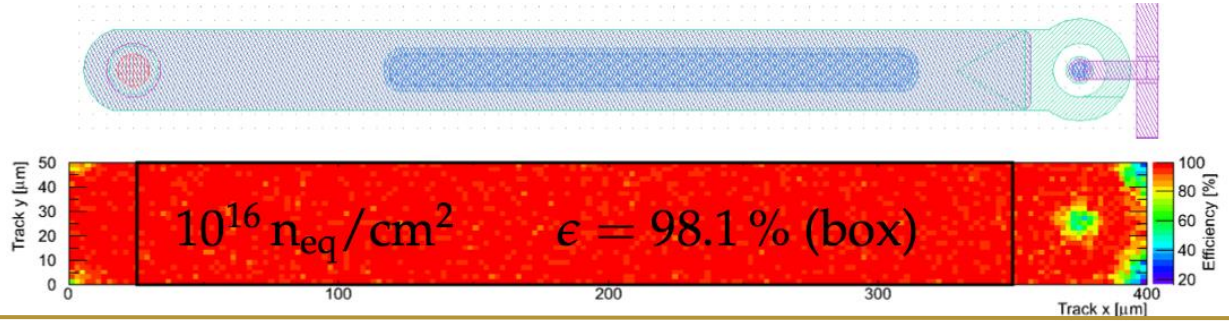
- Charge exceeds threshold by a factor 2
- Testbeam with Eudet telescope

Hit efficiency of 97.2 % at highest fluence, 600 V and threshold of 2ke

(98.1 % in central region)
Main losses in punch through and corners for ⊥ tracks



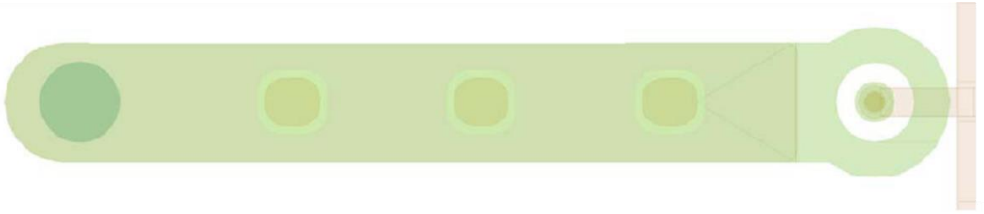
C. Gallrapp et al., "Performance of novel silicon n-in-p planar Pixel Sensors ", Nucl. Instrum. Meth. A679 (2012) 29



FE-I4 Module Hit Efficiencies

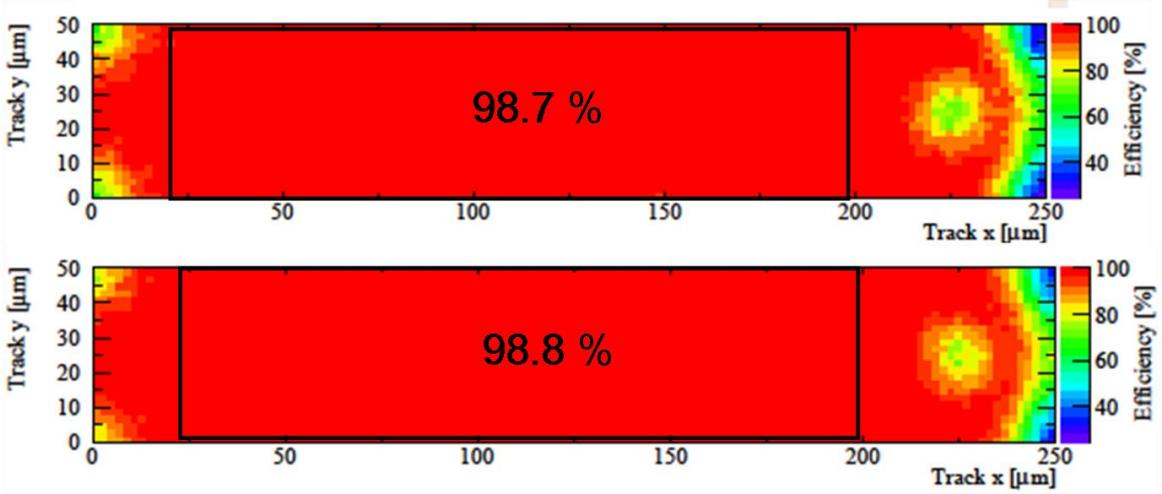
Hit efficiency of the module projected in one single pixel cell, Eudet telescope, 120 GeV pions at CERN-SPS

Design of the
FE-I4 pixel



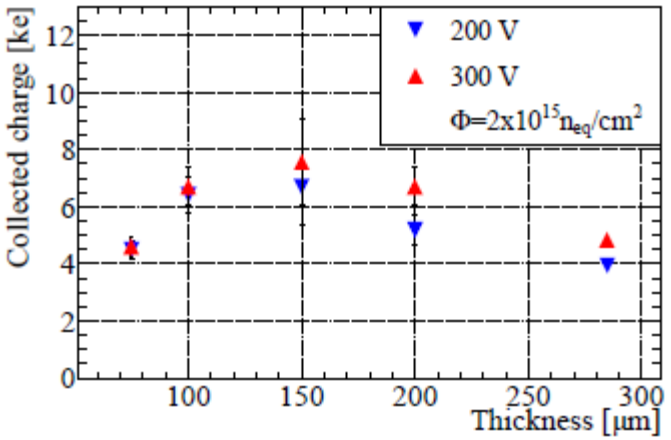
$\Phi=4x10^{15}\ n_{eq}\ cm^{-2}$
400 V
Global eff.= 96.5%

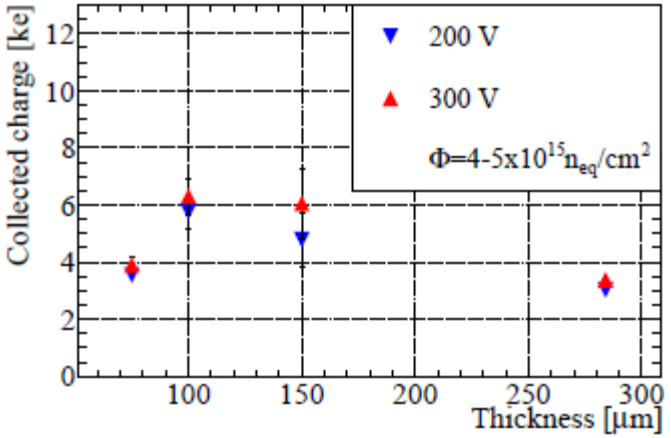
$\Phi=4x10^{15}\ n_{eq}\ cm^{-2}$
500V
Global eff.= 96.9%



- Main loss of efficiency in the bias dot and in the bias rail → problem is relevant only for perpendicular tracks, as in this case

A. Macchiolo, "Thin n-in-p pixel sensors and the SLID-ICV vertical integration technology for the ATLAS upgrade at HL-LHC", PIXEL2012


Collected charge [ke]
Thickness [μm]
200 V
300 V
Φ=2x10^15 n_eq/cm^2


Collected charge [ke]
Thickness [μm]
200 V
300 V
Φ=4-5x10^15 n_eq/cm^2

Test beam results

Phase II Requirements: Inner Layers

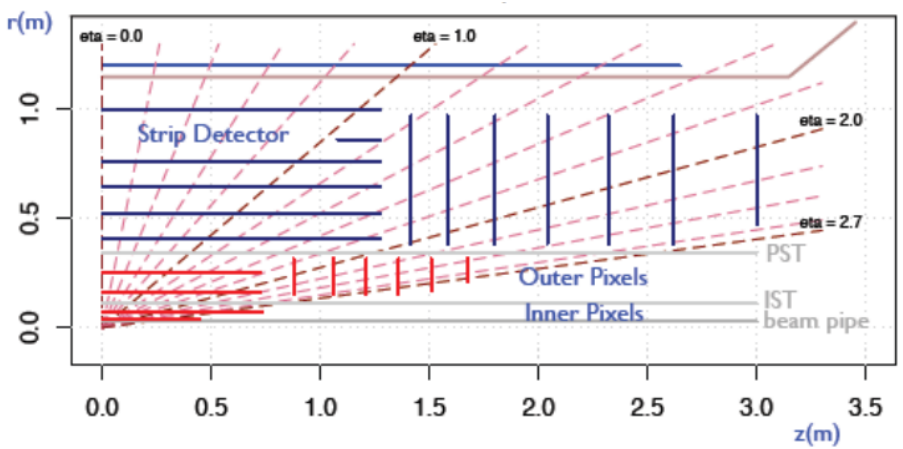
The phase II upgrade of ATLAS foresees a new Inner detector
4 pixel layers, up to r = 25 cm are planned.
Large area ≈ 8 m^2

Cost effective modules are mandatory

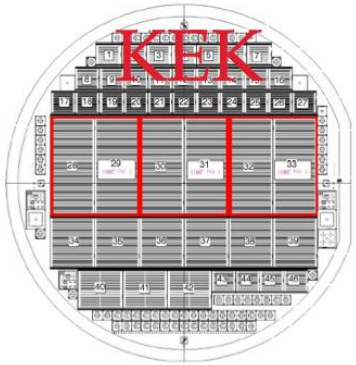
N-in-P sensors are foreseen for such large areas

Reduce inter-connection cost: connect one large sensor to four (quad) or even six (hex) FE-I4 chips (2x2 cm, developed or the IBL)

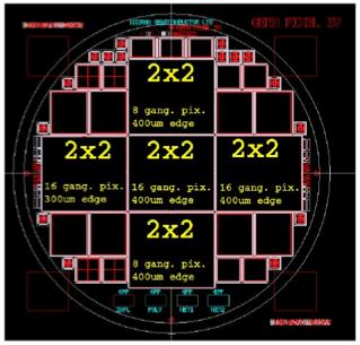
- KEK/HPK
- Liverpool/Micron
- MPP/HLL

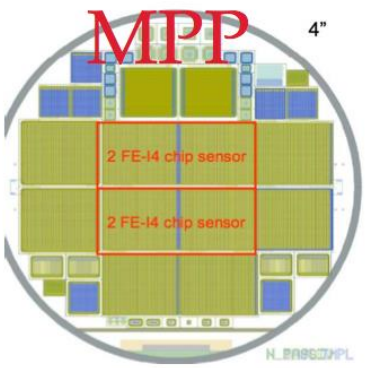


P, Allport, "ATLAS upgrades update", LHC Detector Upgrade Review



Liverpool

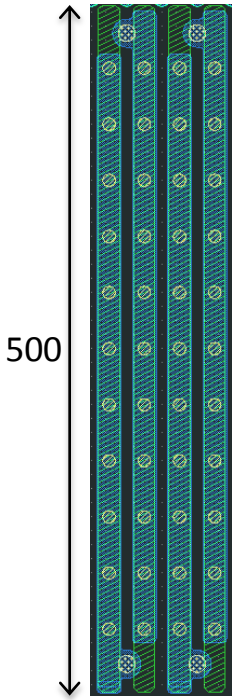


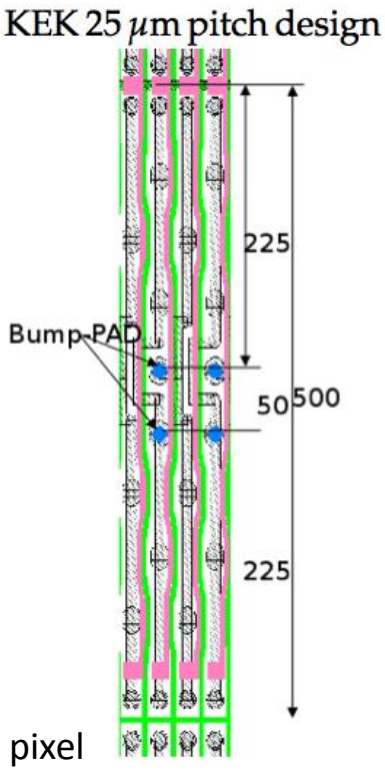


Phase II Requirements: Inner Layers

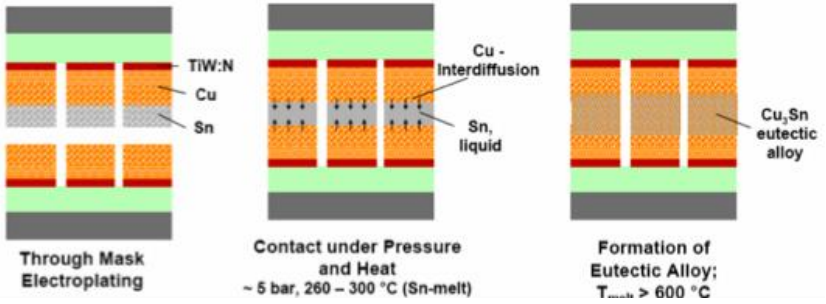
For the inner layers the requirements are:

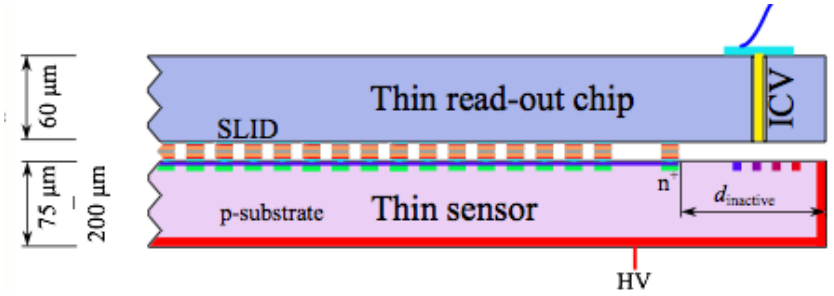
- Best achievable resolution:
  - Reduce Rφ-pitch to 25 μm, for sensor and chip
  - New/improved interconnection technique, e.g. SLID (below)
  - New Liverpool pixel design (right), still using present chip (FE-I4)
  - New KEK pixel design (right), still using present chip (FE-I4)
  - Smallest achievable radius → no overlap → Minimize inactive edge
  - Thin sensors and chips to reduce multiple scattering, PPS uses (75 − 150)μm
  - KEK 25 μm pitch design
- Radiation hardness: $2 \cdot 10^{16}$ n_{eq}/cm^2



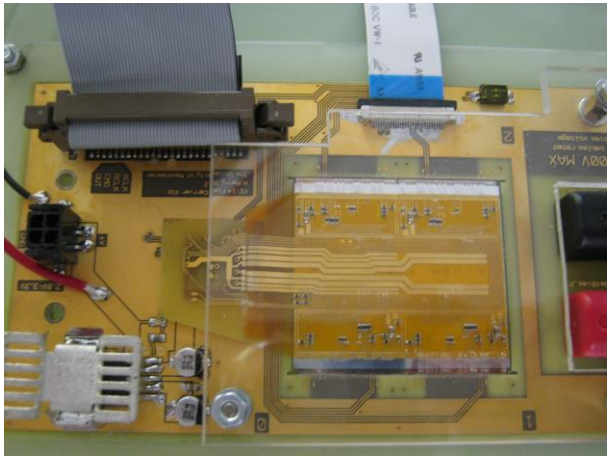


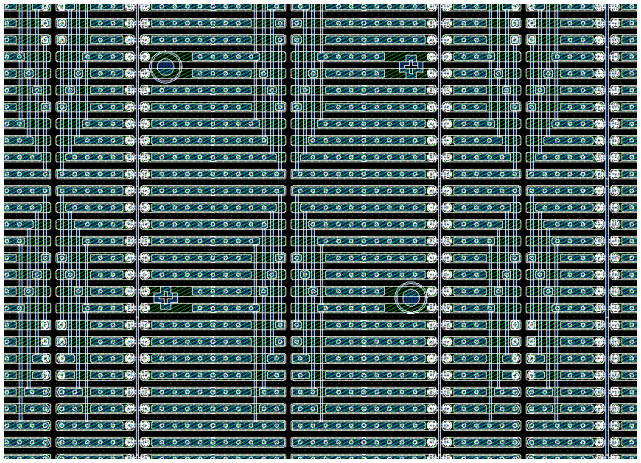
Liverpool 500x25um pixel

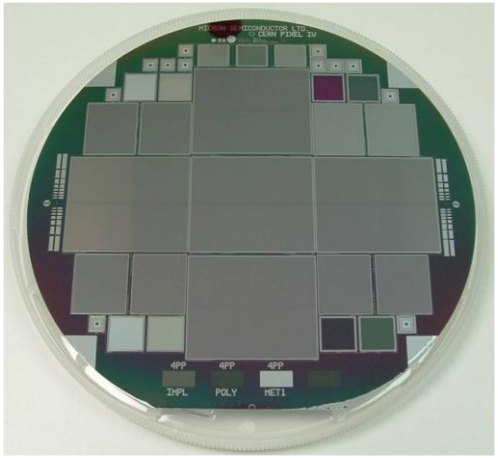


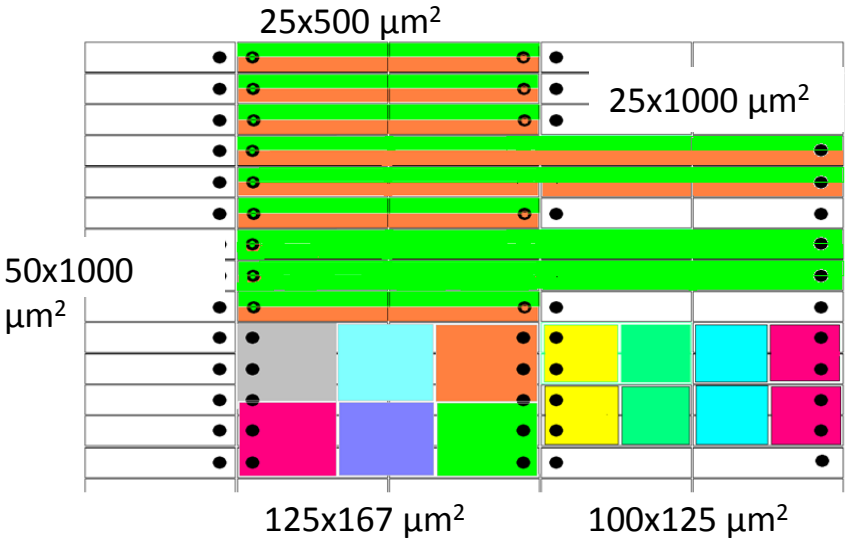


Phase II Requirements: Designing for the Future









UK pixel upgrade groups (Liverpool, Glasgow, Manchester, RAL)

- Working Quad module, (can only be read out 1 FE at a time)
- Quad Module Flex's and Multiplexing
- Working with layout simulation groups to determine, best pixel structures for Barrel Wheels etc.. including "Stixel" structures for intermediate layers between Pixel an Strip layers

KEK:

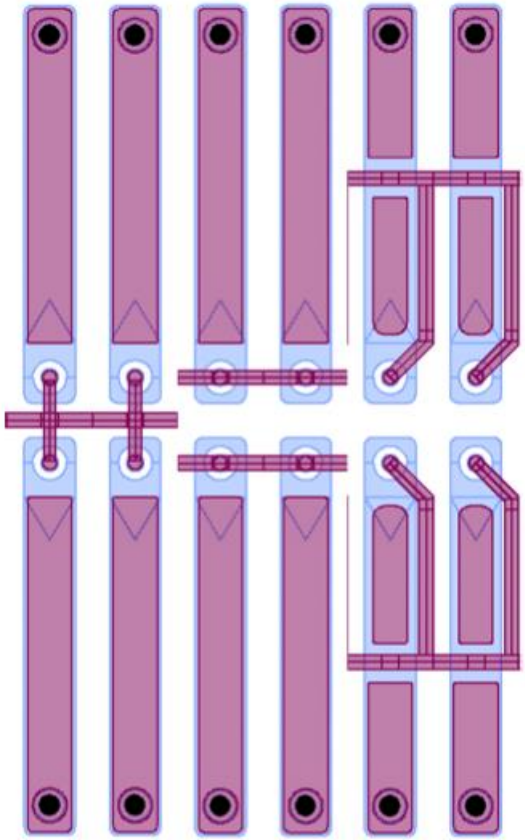
Working on Single chip card design's for quad Modules

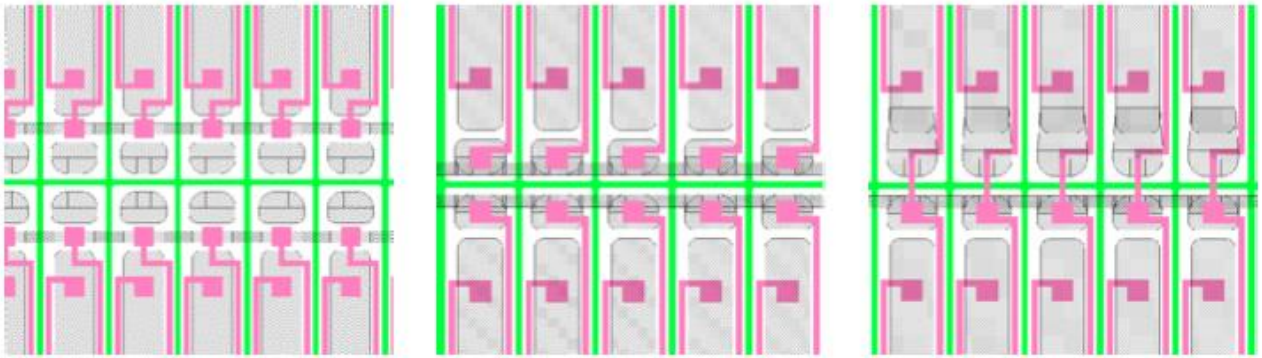
Bias Grid Design

To overcome the efficiency loses in the punch through structure for perpendicular tracks, different designs are under investigation: “Bias rail” is a metal over insulator, no implant underneath

Dortmund (right)
Bias rail routed differently 2 alternative designs

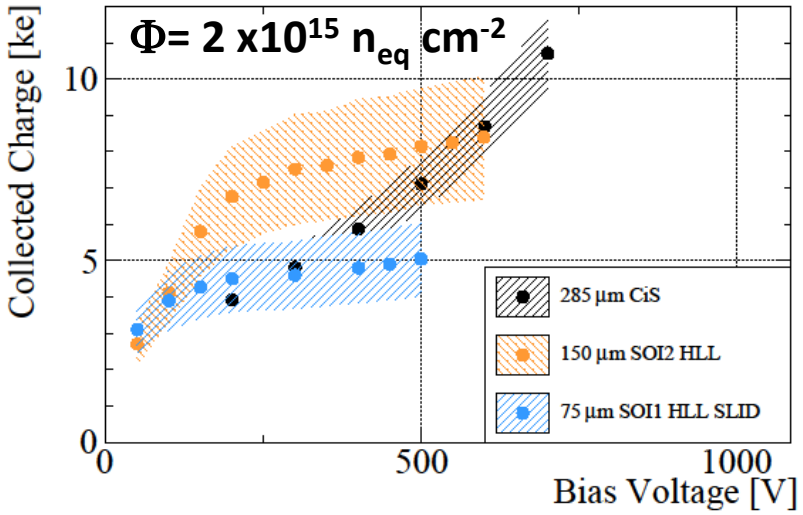
KEK (below)
PolySilicon resistor (encircling pixel implant) 3 different designs

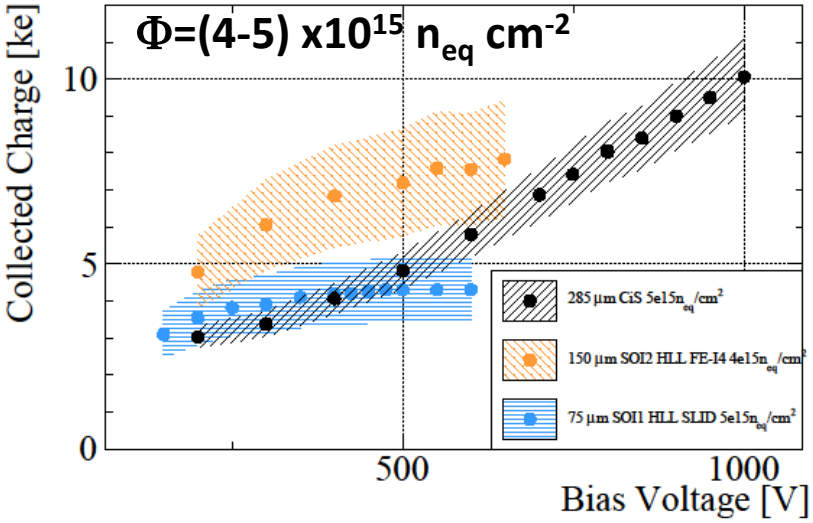


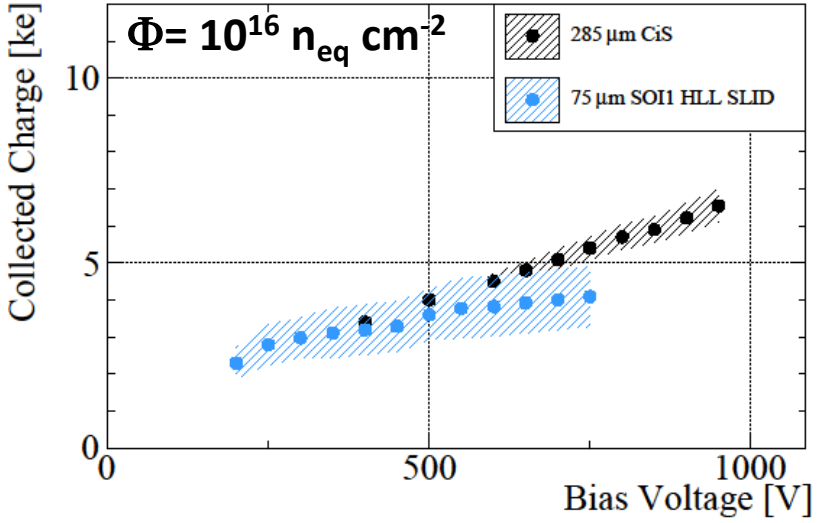


CC's for n-in-p pixels of different thickness

MPP modules and results







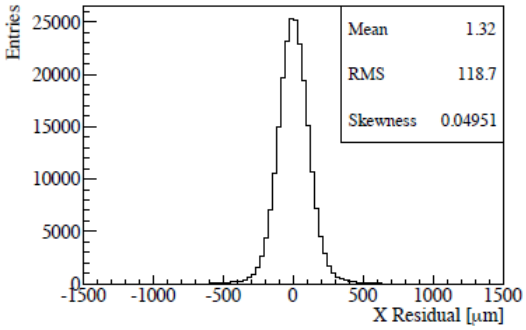
Higher charge with 150 mm thick sensors up to a fluence of Φ=(4-5)x10^{15} n_{eq} cm^{-2}

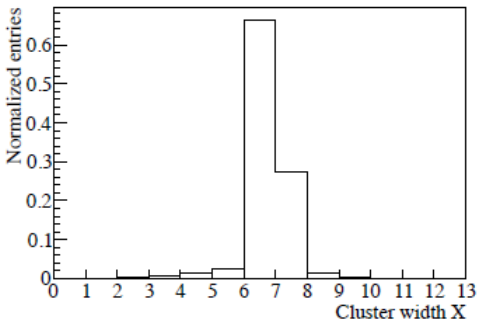
At higher fluences the charge of thin and thicker sensors tend to equalize

A. Macchiolo, "Thin n-in-p pixel sensors and the SLID-ICV vertical integration technology for the ATLAS upgrade at HL-LHC", PIXEL2012

Inclined tracks. (High eta).

- **FE-I4 150 μm thick, irradiated to $4\times10^{15}\,n_{eq}/cm^2$ in Los Alamos**
- ϑ=85° track incidence ($\eta\sim3.1$)
- bias voltage: 500 V
- threshold: 1.6 ke

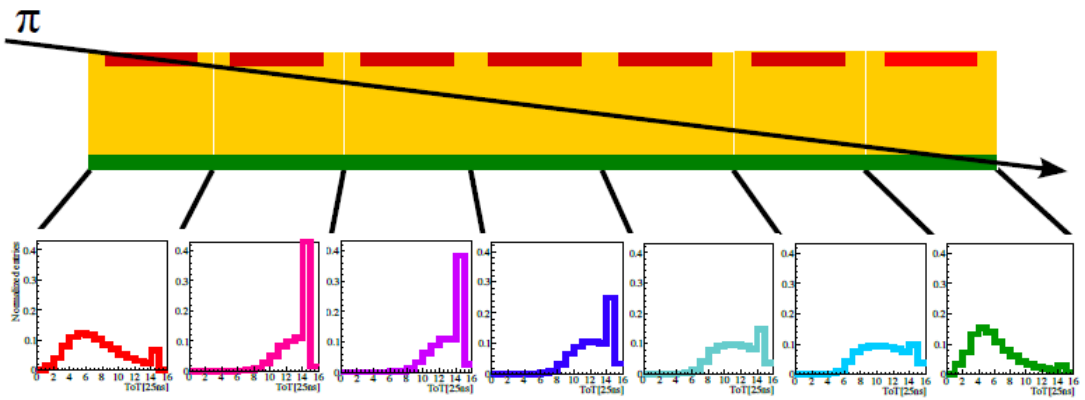




S. Terzo et al., PPS meeting, Paris, 30-09-2013.

High-eta collected charge

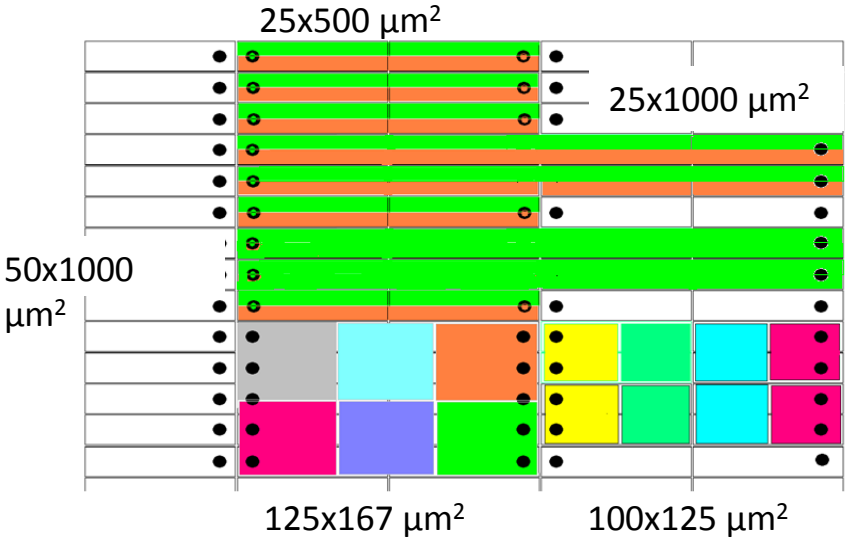
- overflow peak due to the calibration (10ToT @10 ke) at the edge of the ToT range (1-14) for a particle crossing 250 μm (~12 ke)
- observed higher charge collected near the n-implant

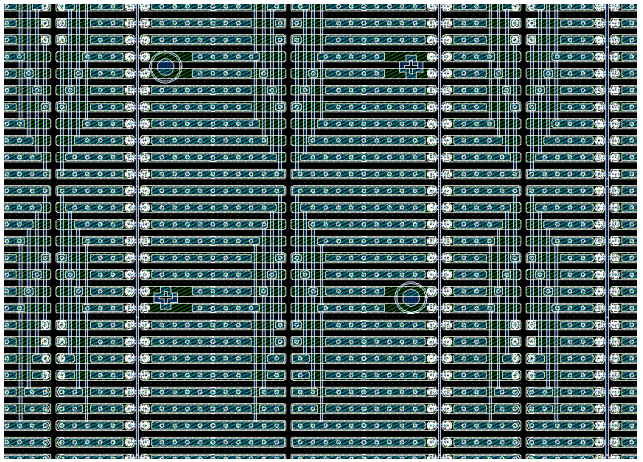


ToT distribution inside clusters of width X=7 along the wide pixel side

Geometry optimisation: *adaptive* pixel size

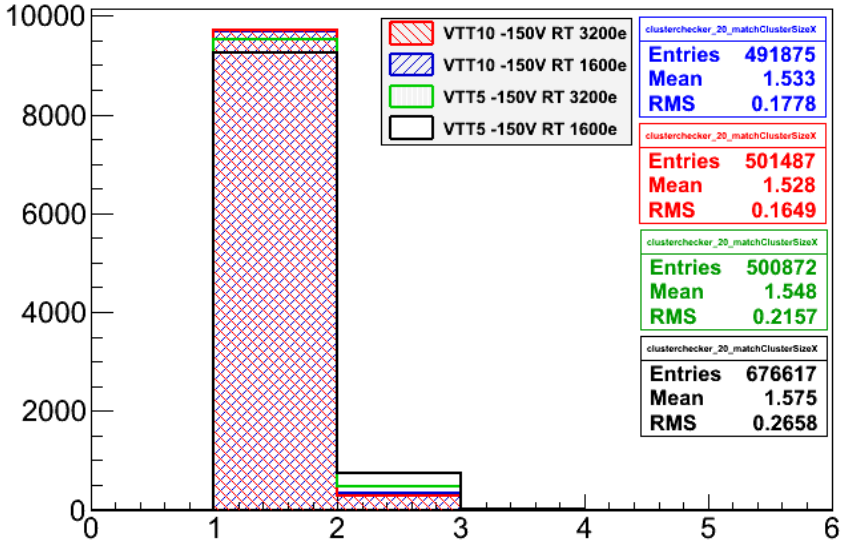
- Compatible with the FE-I4 floor-plan
- Better suited to particular z-regions of the barrel or forward disk/wedges regions
- R&D towards strixel solutions



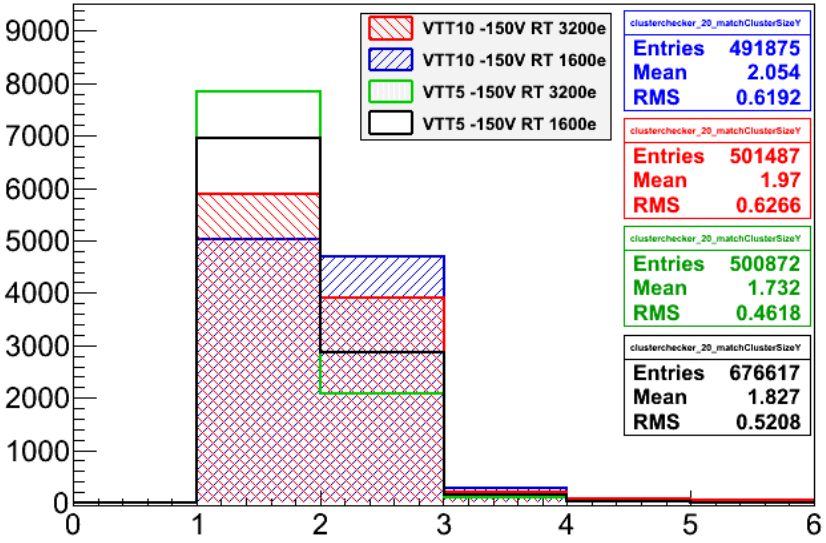


Various pixel sizes, AC and DC coupled, Liverpool

Testbeam results: cluster sizes



Cluster Size X



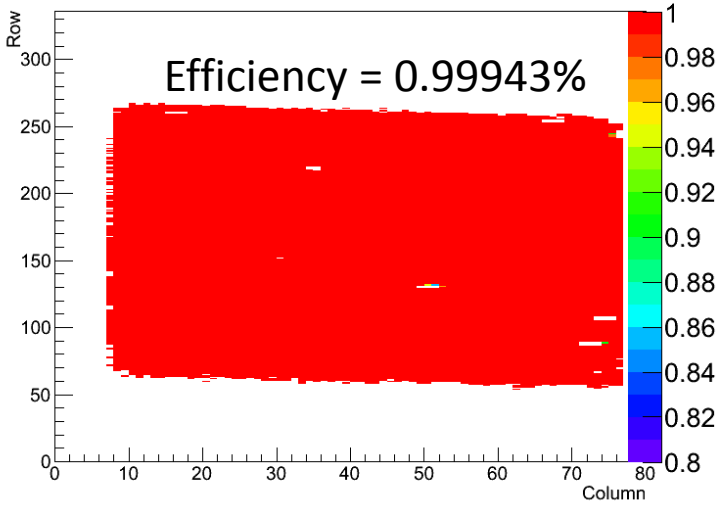
Cluster Size Y

As expected :

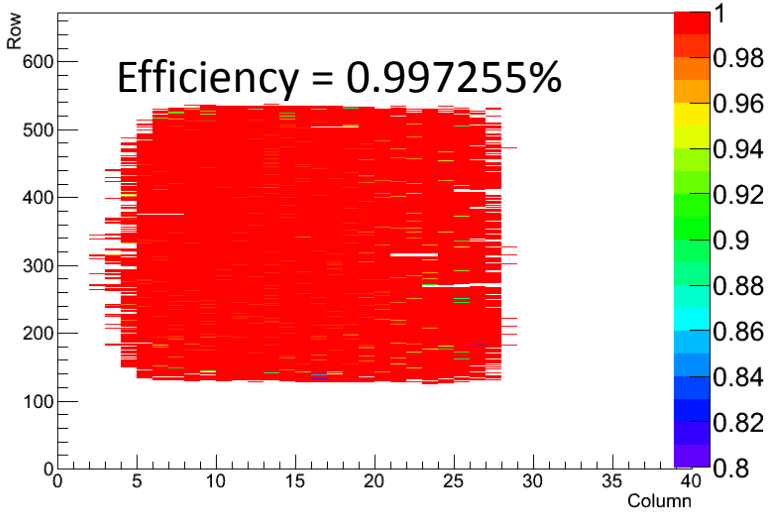
- greater number of 2 hit clusters along Y in 500x25(VTT10)
  - Increased charge sharing
- Minimal change in cluster size in x-direction
  - (500x25 cluster size is slightly more skewed to 1 than 250x50(VTT5))

Sensor Efficiency – 250x50 (VTT5) vs 500x25 (VTT10)

VTT5 3200e



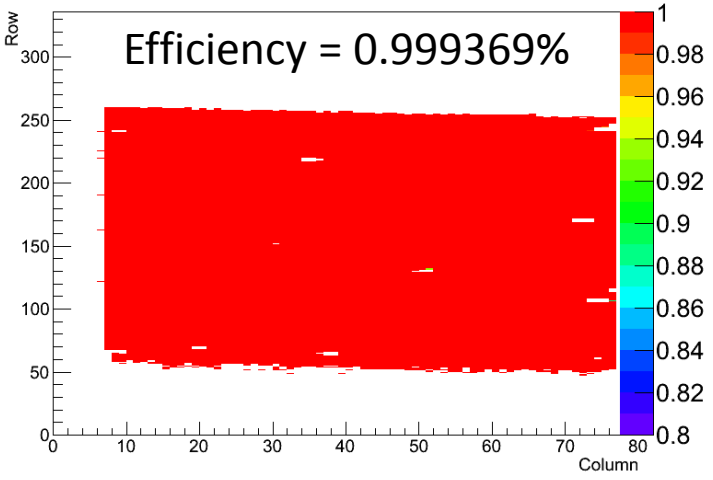
VTT10 3200e



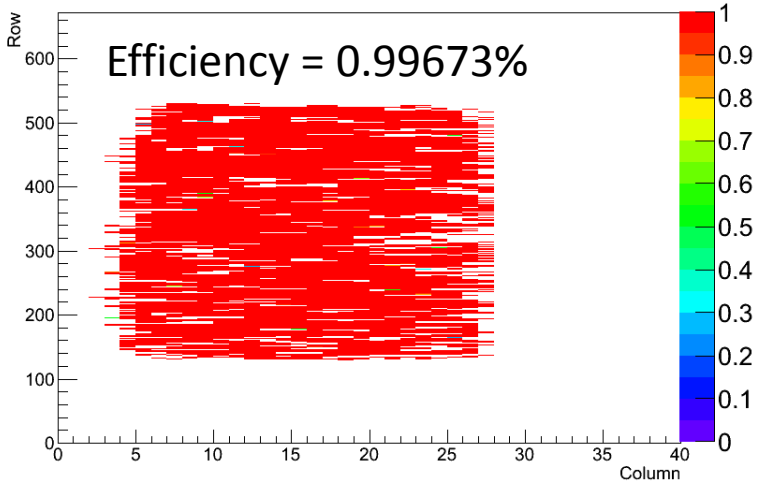
VTT10 show same high efficiency performance as VTT5

(small degradation due to quality of tuning).

VTT5 1600e



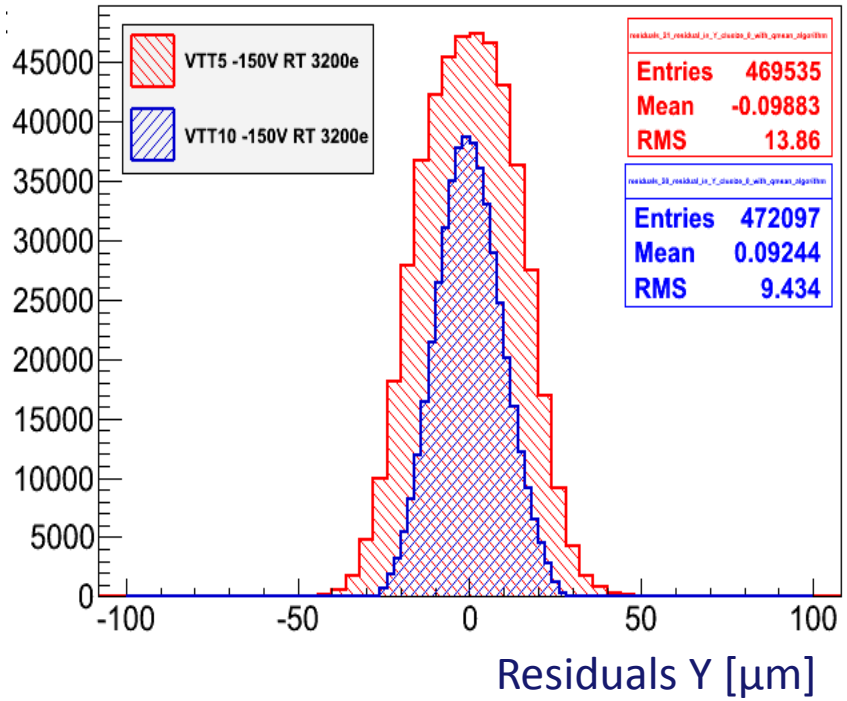
VTT10 1600e

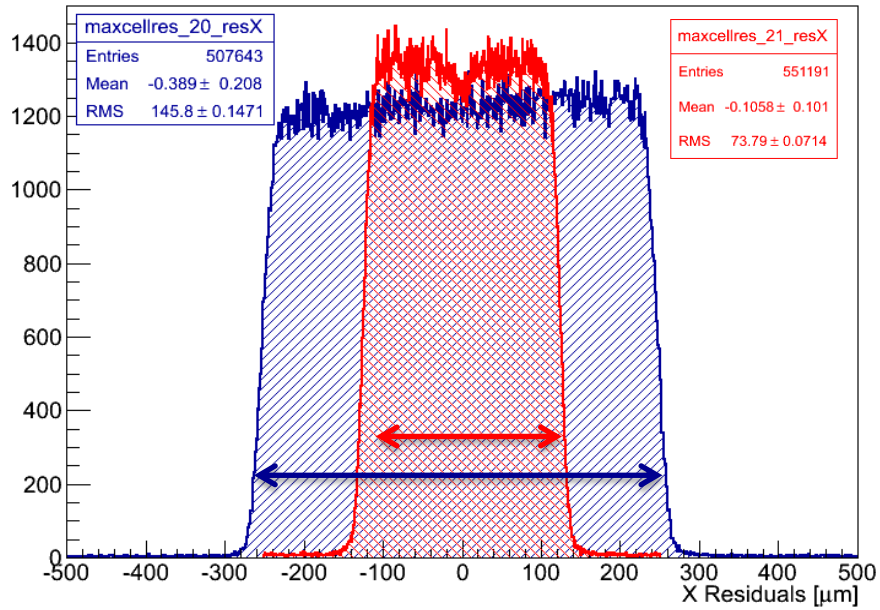


Residual X and resolution – 250x50 vs 500x25

RMS values are approximately what is expected for pitch/root(12):
500x25 : 500/√12 = 144.3
250x50 : 250/√12 = 72.17

Width of distribution
500 for 500x25 and about 250 for 250x50





500x25 : 25/√12 = 7.217
250x50 : 50/√12 = 14.43

Geometry optimisation: *other design variations*

- Reduce need for overlap or inactive gaps (depending on geometry and location)

Geometry optimisation: *slim* or *active* edges

- Reduce need for overlap or inactive gaps (depending on geometry and location)

Slim or Active Edges: Introduction

Slim edges can be achieved by guard ring design or by active edges.

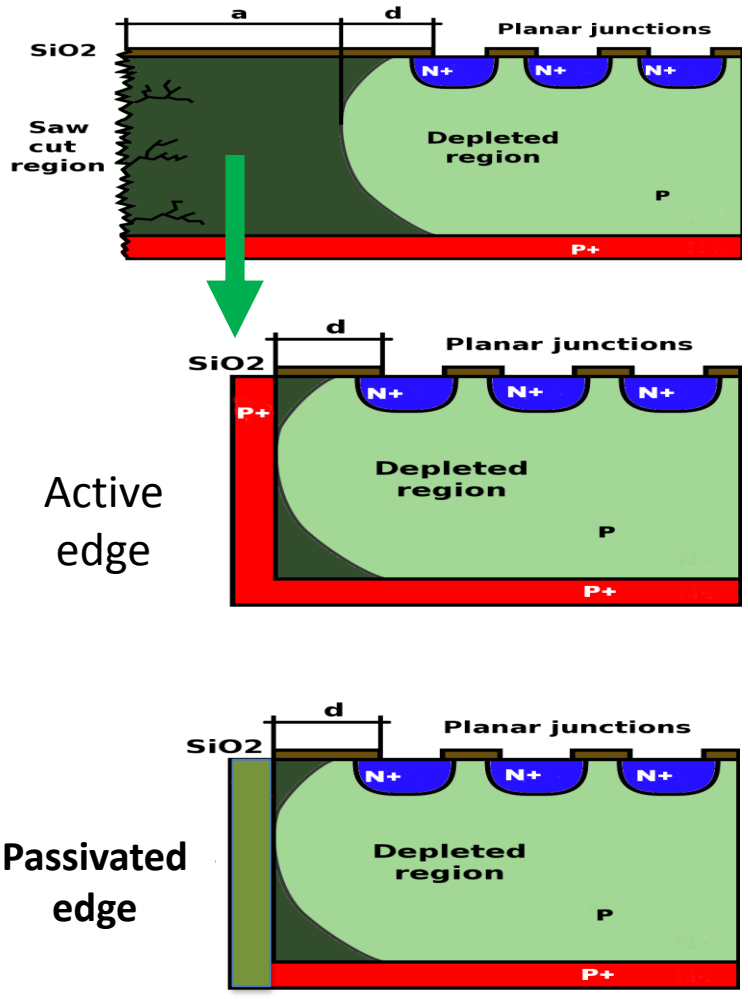
For Phase-II decrease the inactive edge further:

- Two approaches for active edges

  DRIE (Deep Reactive Ion Etching) and side implantation
  DRIE trenching, filling and doping by diffusion

- Two approaches (with several variants) to edge isolation

  SCP: Scribe-Cleave-Passivate Technology
  Backplane Guard-Rings (n-in-n only)



Slim or Active Edges: Introduction

Slim edges can be achieved by guard ring design or by active edges.

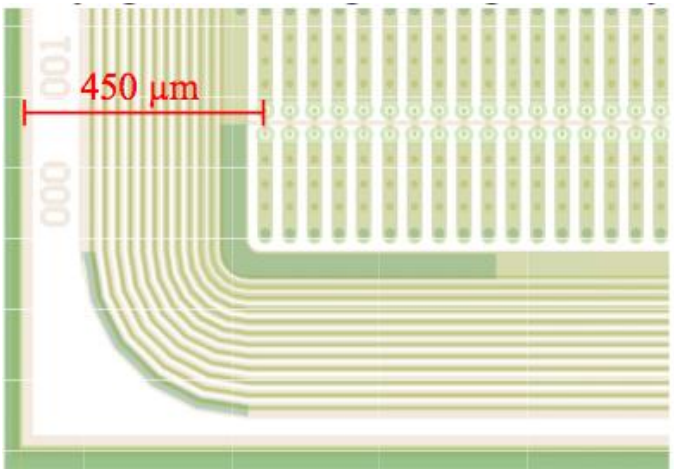
For Phase-II decrease the inactive edge further:

- Two approaches for active edges

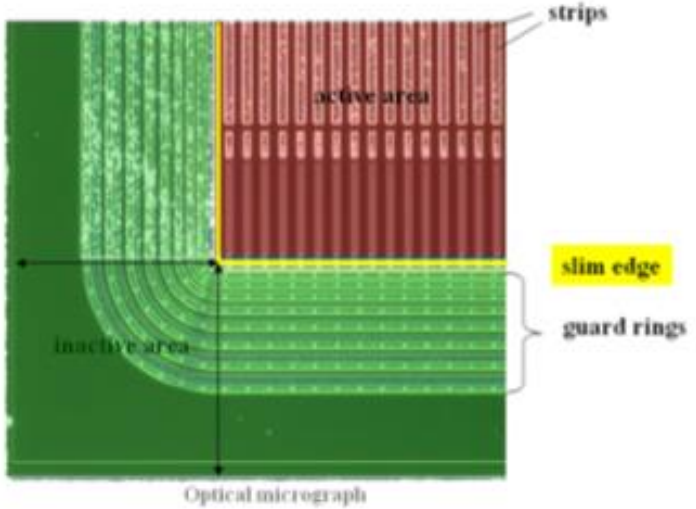
  DRIE (Deep Reactive Ion Etching) and side implantation
  DRIE trenching, filling and doping by diffusion

- Two approaches (with several variants) to edge isolation

  SCP: Scribe-Cleave-Passivate Technology
  Backplane Guard-Rings (n-in-n only)

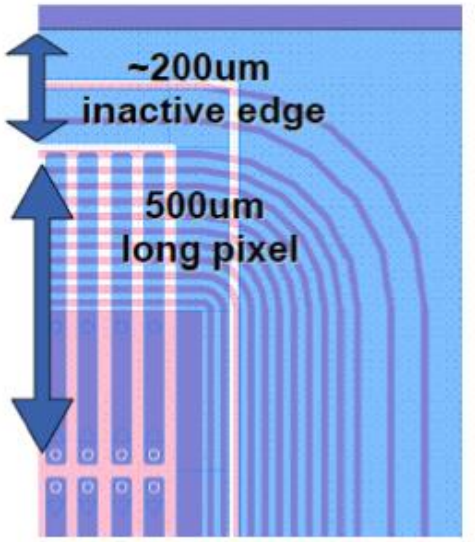


Micron/Liverpool n-in-p prototypes down to $d_{inactive}$ = (250 − 300)µm



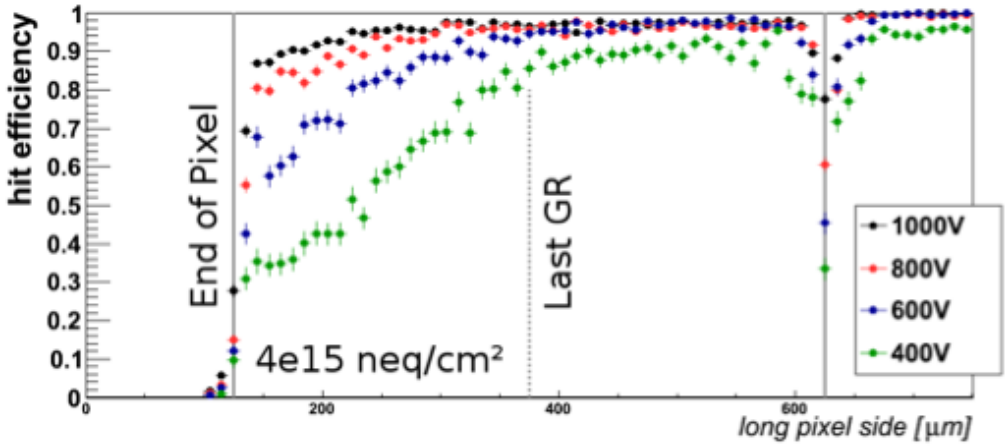
Slim Edges: n-in-n Design Approach

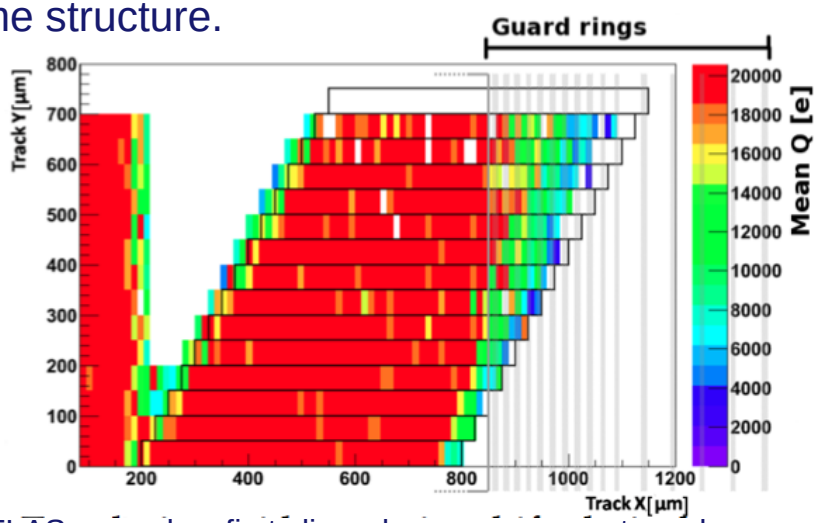
Project by TU Dortmund



- Guard Rings are shifted beneath the outermost pixels
- Least possible inactive edge ~ 200µm
- Less homogeneous electric field, but charge collection dominated by region directly beneath the pixel implant
- Approach adopted in IBL

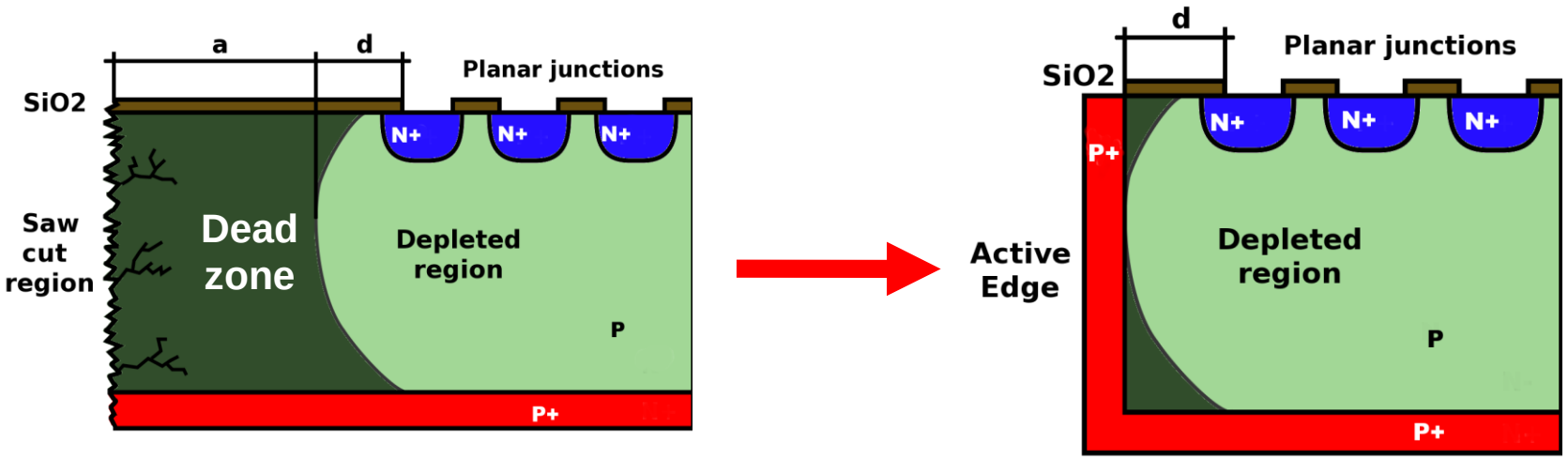
Bottom right: Test design with stepwise shifted pixels, this shows how collected charge is affected due to a less homogeneous electric field when pixels are shifted under the GR's, bottom left: shows the effect on efficiency for same structure.





A. Rummler, Silicon n-in-n pixel detectors: Sensor productions for the ATLAS upgrades, first slim-edge measurements and experiences with detectors irradiated up to SLHC fluences, 6Th Trento Workshop on Advanced Radiation Detectors

The Active Edge project



- Joint project FBK-LPNHE
- Goal: make the rim zone equipotential
- How: DRIE as for 3D process
- Trench doped by diffusion

- Aiming at: HL-LHC ATLAS intermediate pixel layer
- n-in-p production
- 200 μm thick sensors
- Pixel-to-trench distance as low as 100 μm

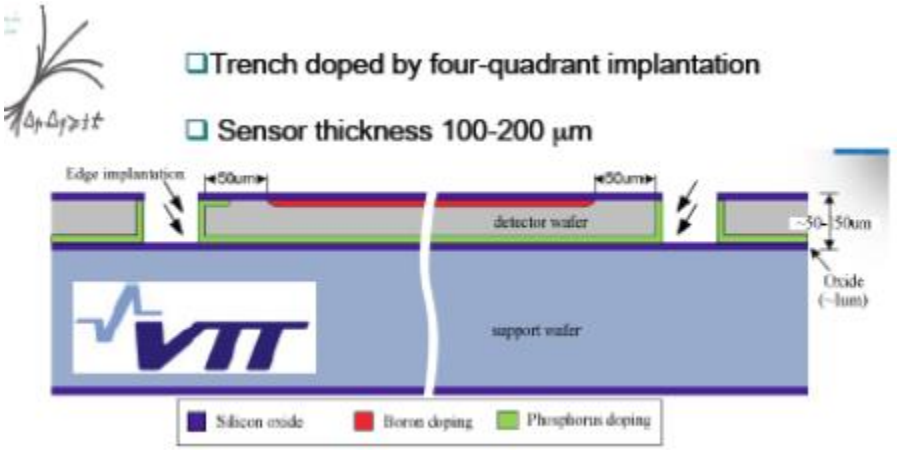
See " Novel Silicon n-in-p Edgeless Planar Pixel Sensors for the ATLAS upgrade" talk Friday afternoon

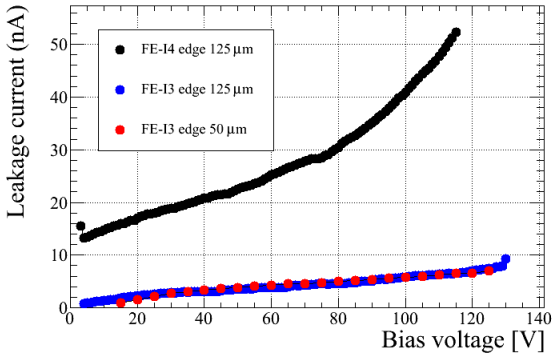
Active edges with planar n-in-p sensors

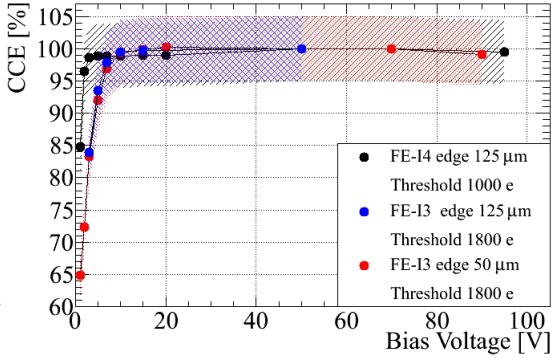
- MPP joint project

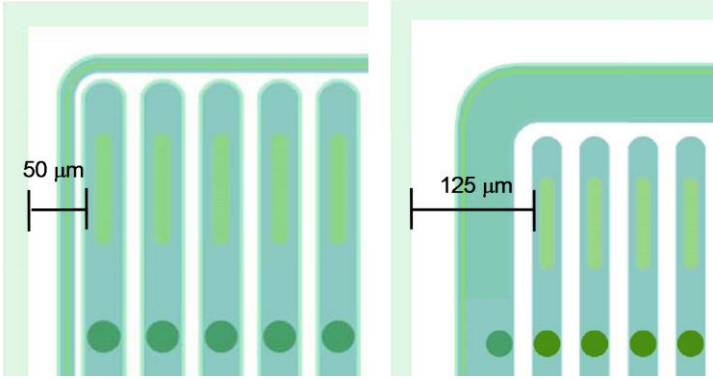
n-in-p pixels at VTT: active edge process with back-side implantation extended to the edges

100µm thickness
V_{break}~120V
V_{depl} ~7-10 V
Charge ~ 6±1 ke





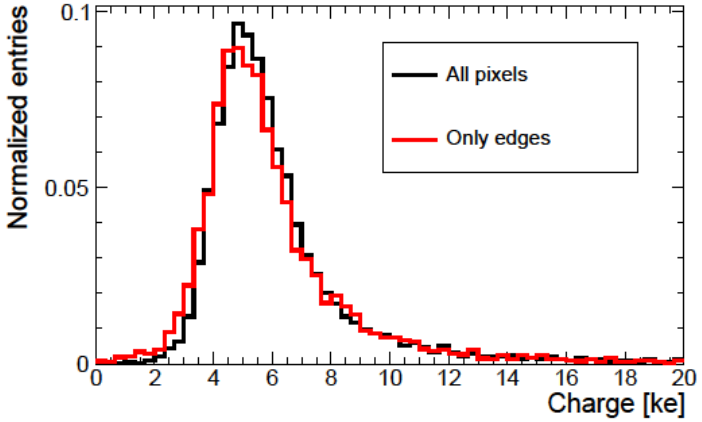


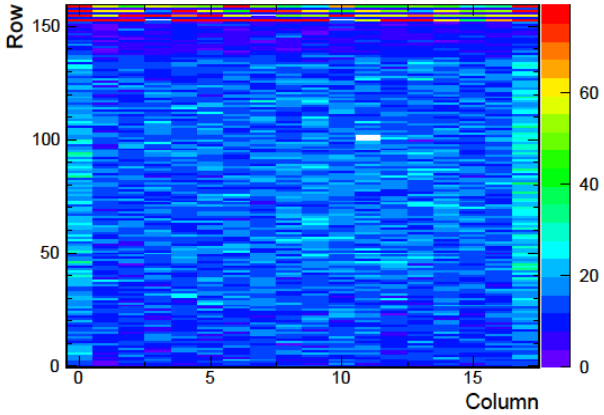


A. Macchiolo, "Thin n-in-p pixel sensors and the SLID-ICV vertical integration technology for the ATLAS upgrade at HL-LHC", PIXEL2012

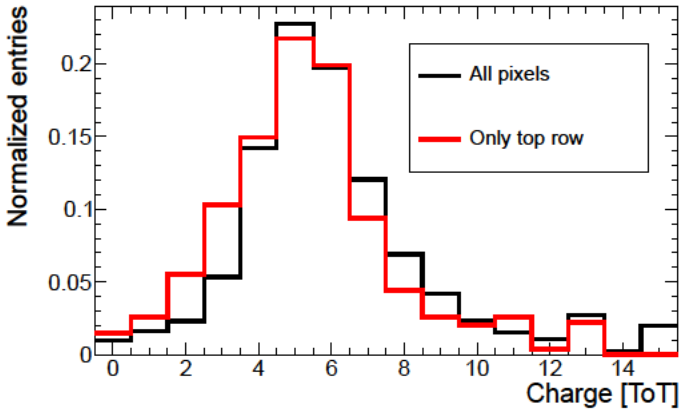
CCE with ^{90}Sr scans

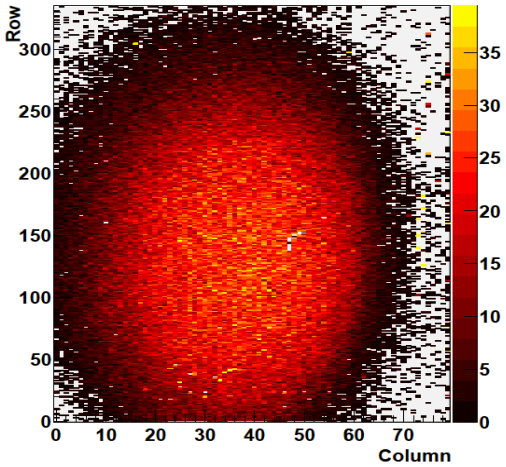
Active edges with planar n-in-p sensors





FE-I3
MPP - 50 µm
edge sensor
V_{bias}=15 V

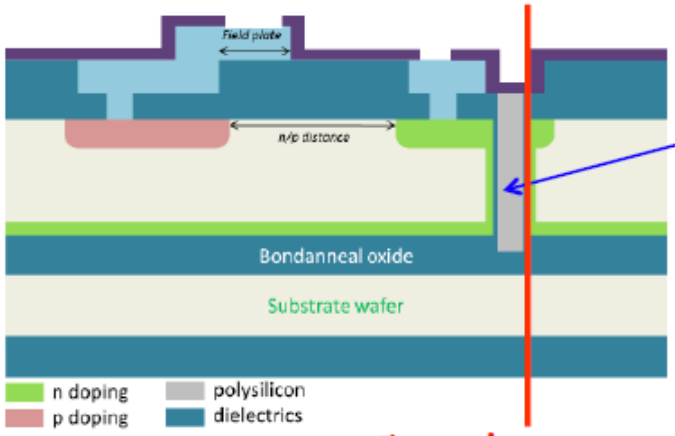




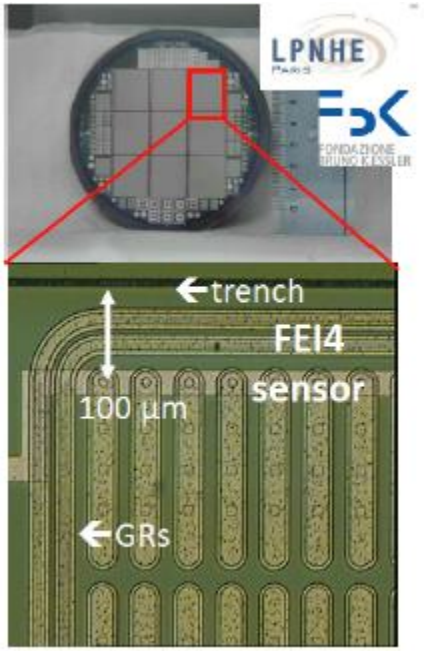
FE-I4
MPP - 125 µm
edge sensor
V_{bias}=15 V

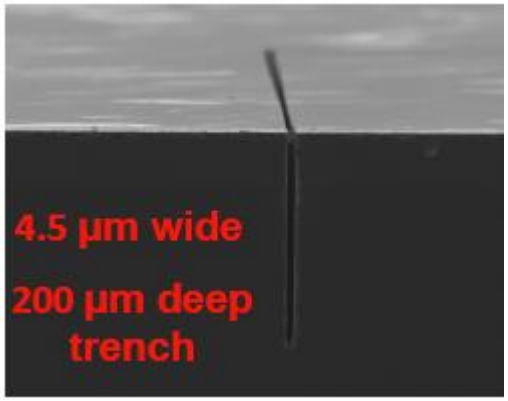
- Edge pixels show the same charge collection properties as the central ones
- Plan to study the hit reconstruction efficiency at the edges with test-beam before and after irradiation

A. Macchiolo, "Thin n-in-p pixel sensors and the SLID-ICV vertical integration technology for the ATLAS upgrade at HL-LHC", PIXEL2012



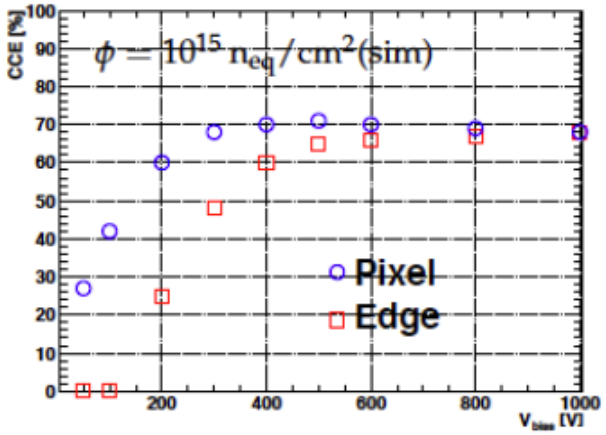
Deep trench diffusion
(electric field stabilisation)
10 μm width
220 μm depth
Polysilicon filling





G.Calderini

HSTD9 - Hiroshima, 1-5 September 2013



- FE-I3/I4 designs by LPNHE/FBK
- Thickness 200um n-in-p
- Different edge/GR configurations (typically 100-200um)
- Simulations indicate good CCE close to edge after 10^{15} n_{eq}/cm^2
- Modules expected in Autumn

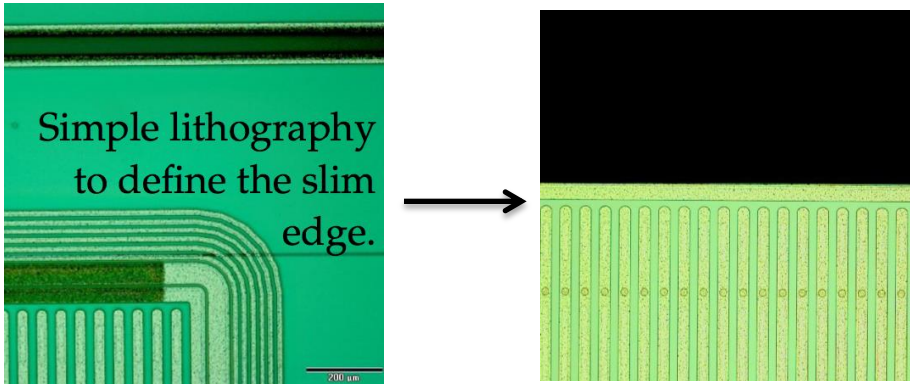
Slim Edges: SCP

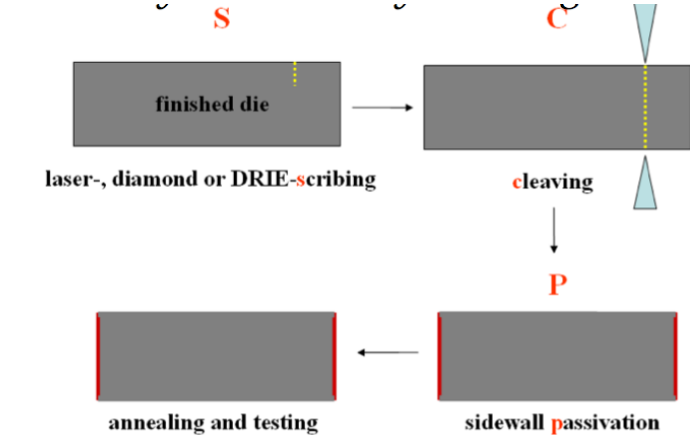
- Project by SCIPP (UCSC) and NRL Post-Processing approach
- SCP: Scribe-Cleave-Passivate
- For n-in-p: ALD deposition of alumina

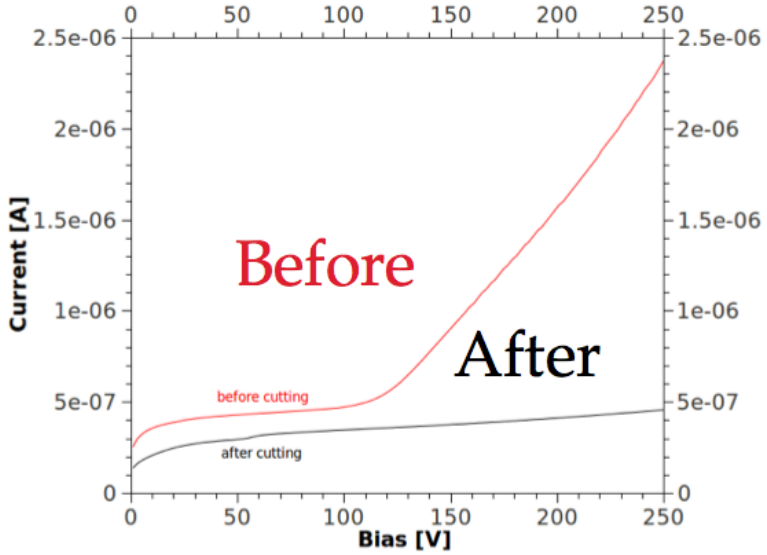
- Relies on:

  Low damaged sidewall due to cleaving.

  Controlled potential drop along sidewall due to fixed interface charge from passivation.

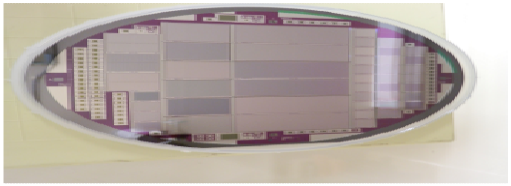


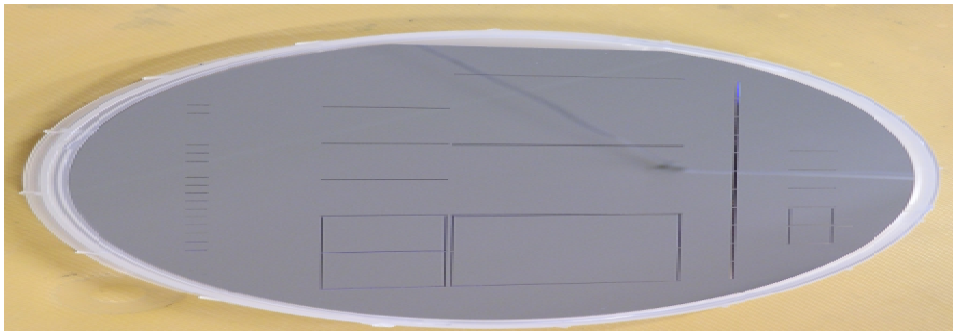




P. Weigell, "Recent Results of the ATLAS Upgrade Planar Pixel Sensors R&D Project", PIXEL2012

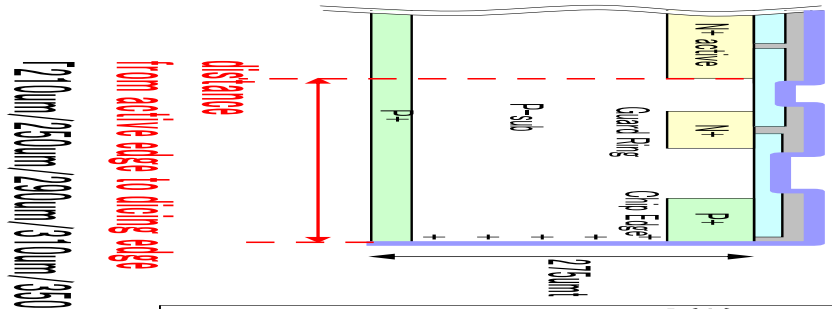
Dry Etch and Alumina Process

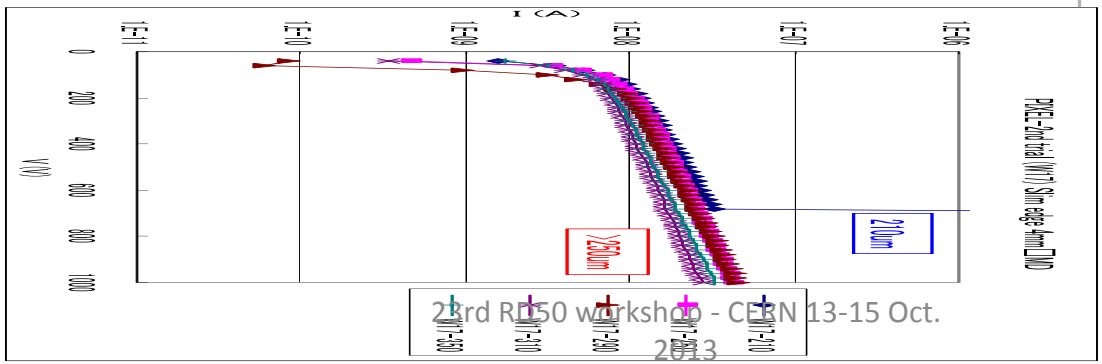




Y. Unno, 2013/10/01 PPS meeting at Paris

Similar process developed
By HPK





Summary

- We are studying different pixel geometries that could be part of the ATLAS ITK
- We are starting with basic measurements at 0degrees, for unradiated 25x500µm^2 modules
  - The CERN pixel V has improved electrical characteristics
  - Basic characteristics such as efficiency and residuals are looking sensible
  - Cluster Size
    - Minimal difference in x
    - Increased charge sharing in y
- We can now progress to studying :
  - Radiated pixel studies
  - High Eta studies
    - Data available, but not yet reconstructed
  - 125x500
    - Data available, but not yet reconstructed

BACKUP

Conclusion

Planar Pixel Sensors

- are understood and well established technology exhibit excellent performance in ATLAS and CMS.
- these latest PPS results imply good performance also after high irradiation levels
- have cost effective processing

and are thus well suited for coming detector upgrades towards the HL-LHC.

Especially

- Sufficient hit efficiency after HL-LHC inner layer fluences for high bias voltages
- Hit efficiency above 97 % at 10^{16} n_{eq}/cm^2 for standard thickness at 600 V
- Different productions with active edges are finishing at the moment and exhibit good performance

Choosing a device thickness

Thinner devices retain, a greater fraction of Collected Charge (CC) than thicker devices after irradiation

Graphs show the CC vs received fluence for strip devices at 600V and 1000V

Low threshold operation of FE-I4 enables thin devices to be used.