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ATLAS EXPERIMENT http://atlas.ch

IOP Institute of Physics

ATLAS PIXEL DETECTOR UPGRADE for HIGH LUMINOSITY LHC

Institute of Physics Conference

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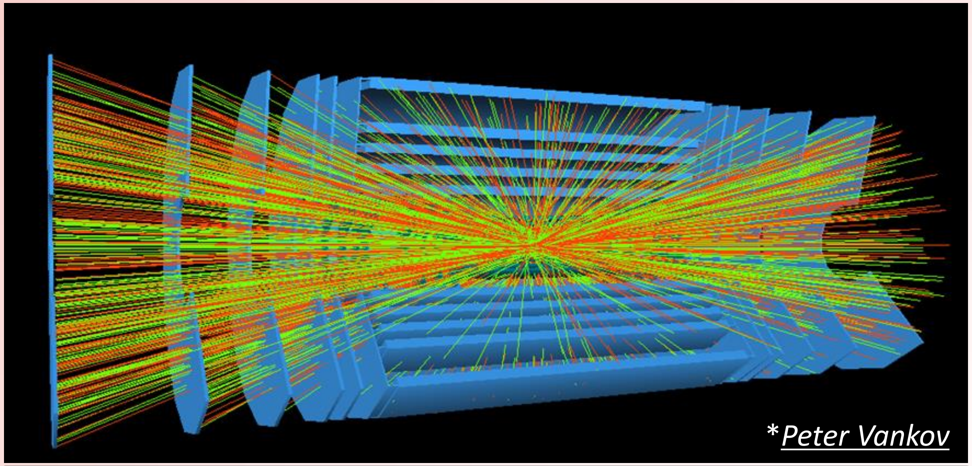
Royal Holloway University of London

Kate Doonan

*In collaboration with University of Edinburgh, **University of Glasgow**, University of Liverpool, University of Manchester & Rutherford Appleton Laboratory*

Outline

- Reasons for Pixel Upgrade
- The FE-I4
- Sensors
- Tuning in Laboratory
- Bump-Yield Studies
- Test Beam Activity
- Reconstruction of Test Beam Data

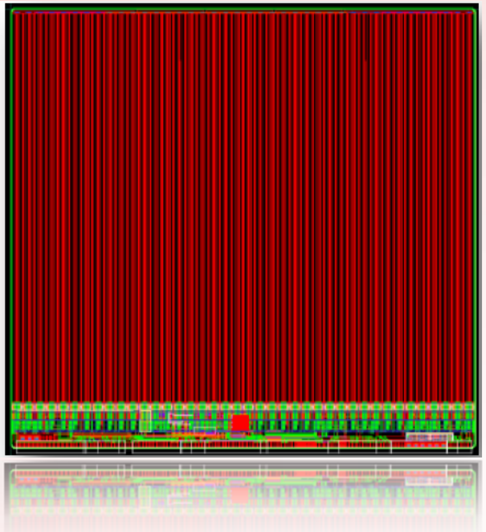


Introduction

- Why is an upgrade to the Pixel Detector necessary?
  - Higher multiplicity → harsh radiation environment → radiation tolerance from detectors
  - High instantaneous luminosity → increased pile-up → higher bandwidth
  - High occupancy → higher granularity in *z* →resolve individual vertices and provide pattern recognition
- What does a pixel upgrade entail?
  - Development of new Front-End chips and sensor technology to deal with pile-up and increased radiation fluences
- What is being done to make the upgrade a success?
  - Characterisation in Lab and Test Beams

The Front-End I4 – FE-I4

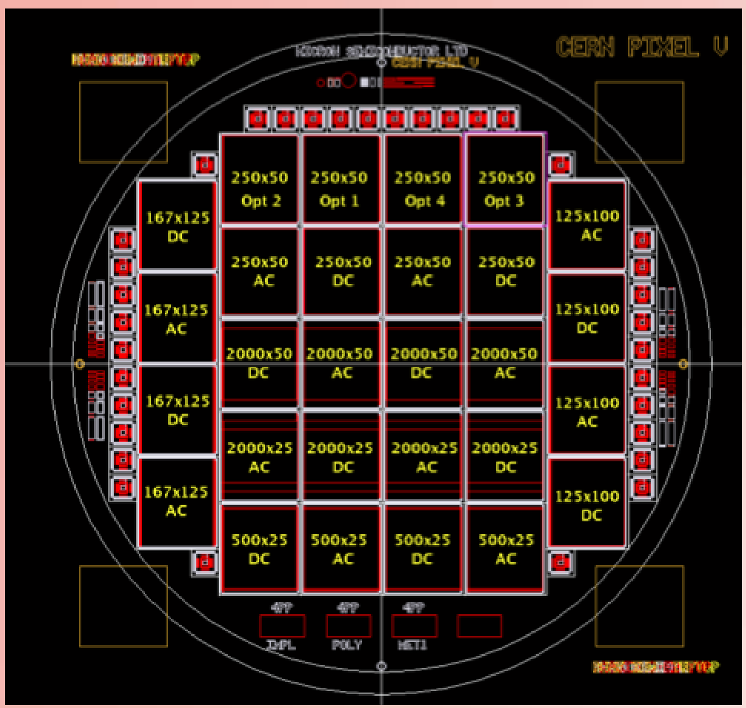
- New Front-End read out chip developed for Insertible *b*-Layer (IBL): FE-I4
- Correct pixel size for outer barrel layers and forward disks
- Made to fit largest reticle in 130nm IBM CMOS process
- Starting point for Front-End to be used for HL-LHC Upgrade
  - 40MHz readout, large area, high active fraction, radiation tolerant to 5 x 10^{15} n. eq. for IBL, high granularity
  - single Chip assemblies and Quad modules with possibility to include multiplexing for 4-chip readout



Pixel Size	250µm x 50µm
Pixel Array	80 columns x 336 rows
Chip Size	20.2mm x 19mm
Active Fraction	89%

Single Chip Sensors

CERN Pixel V



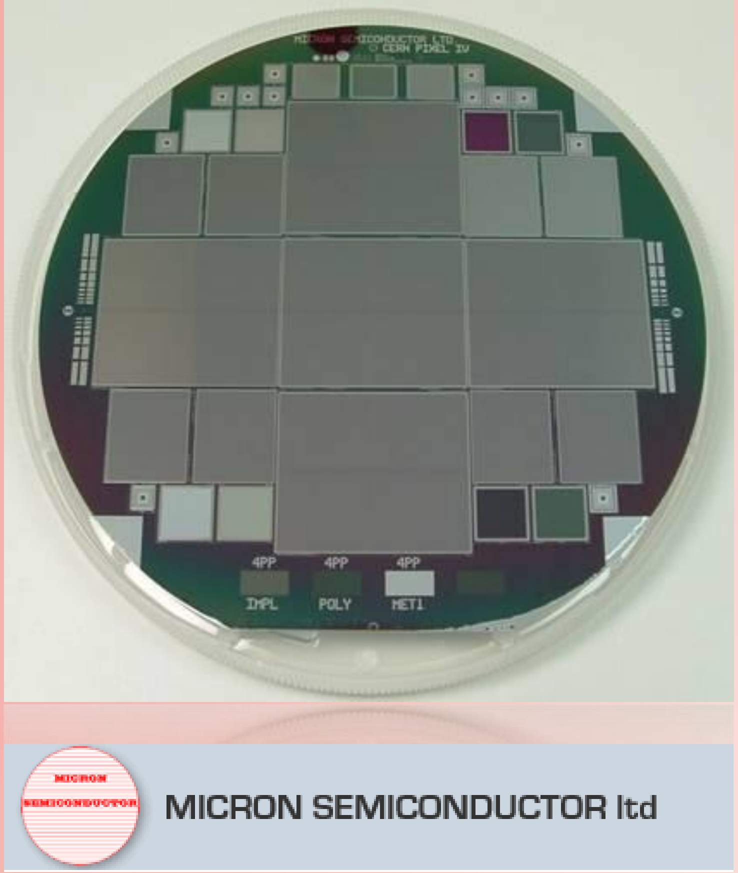
Variety of sensor geometries

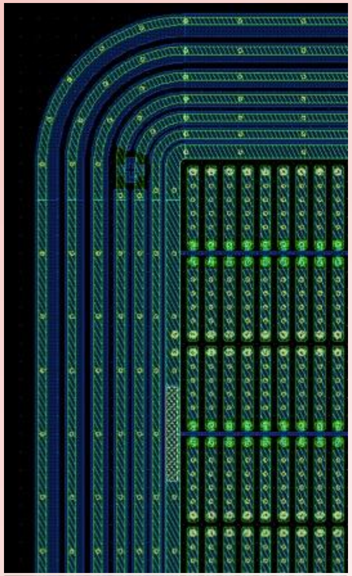
125µm x 100µm, 167µm x 125µm — Pixel Endcap capabilities

250µm x 50µm, 500µm x 25µm — Outer Barrel Layers

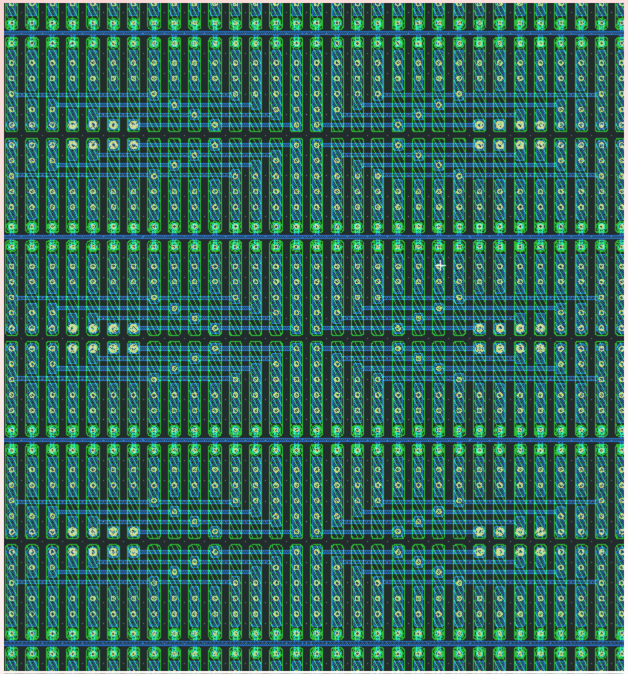
2000µm x 25µm, 2000µm x 50µm — Potential for use in 5th Pixel Layer

Quad Sensors





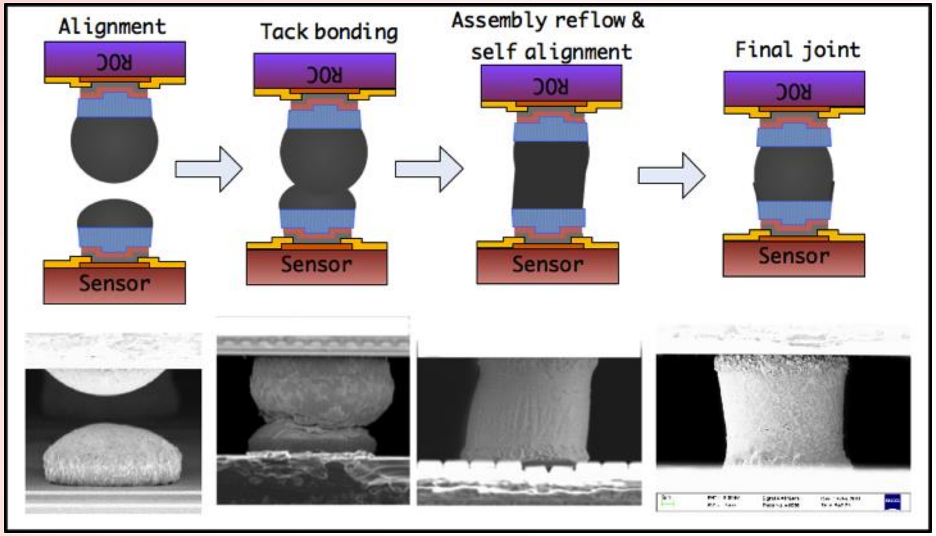
- Long pixels (250→500µm) are used to keep sensor area active from chip-side to chip-side



- Ganged pixels (multiple pixels per channel) used to connect chip-bottom to chip-bottom

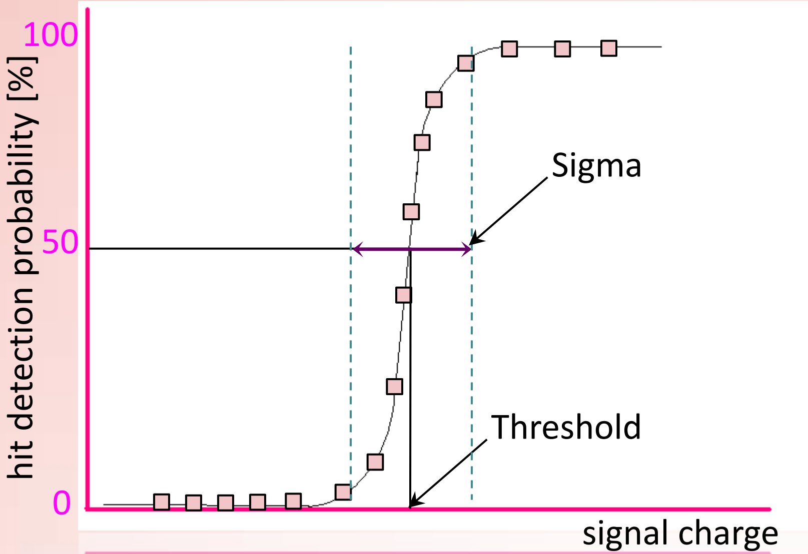
Making A Module

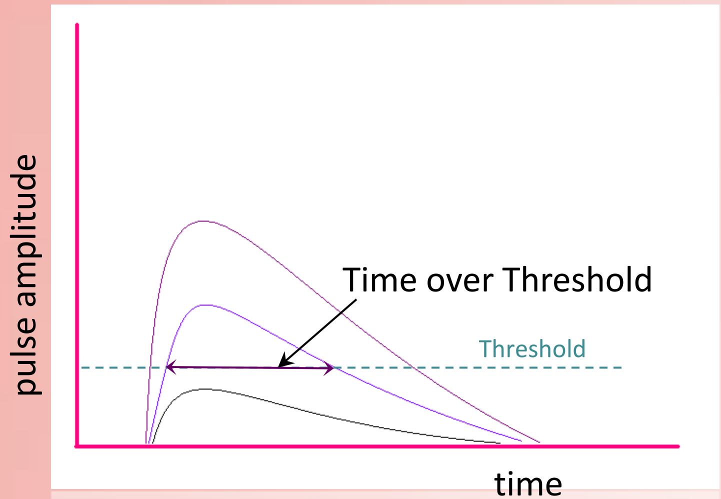
- Sensor attached to Front-End chip (or read-out chip, ROC) via bump-bonding
- One example of the bump-bonding process at VTT, Helsinki using SnPb (solder) bumps:
  - Deposit under-bump metallisation (UBM) and bumps
  - Flip-chip bond to sensor
  - Re-flow bumps at 260ºC



Characterising a Front-End Assembly

- Threshold tuning
- ToT Tuning
- Bump-Yield studies
- Source Scans





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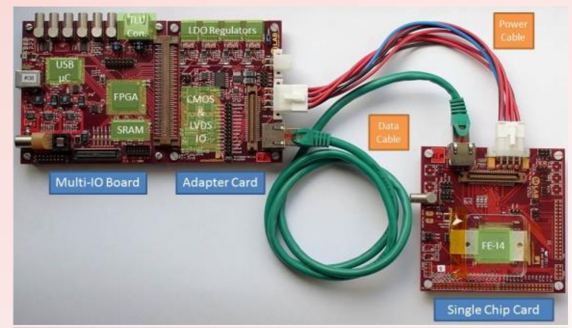
Characterising a Front-End Assembly

- What do we require from assemblies?
  - Uniform Threshold and Time-over-Threshold (ToT) values
  - Low noise at operation threshold
    - **3000e, (1500e after irradiation) threshold, 9 ToT @ 16ke for IBL**
  - All pixels must be capable of readout
    - **Bump-bonding must be of high quality (99.8%)**
  - Still in working order post-irradiation to fluences expected
  - Efficiency high over all sensor
  - Require minimum dead area –
    - **use ganged and long pixels over quad sensors**
    - **investigation of slim edges**

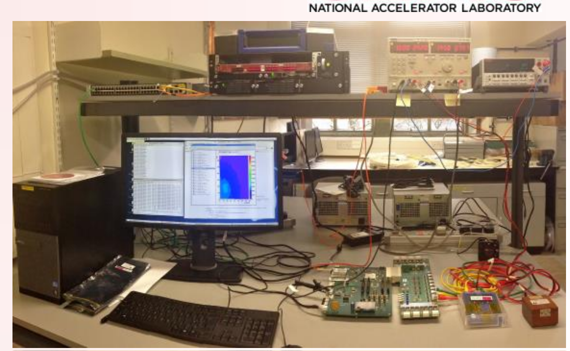
Characterising a Front-End Assembly

- Characterisation in the lab requires a read-out system and control software
  - USBPix & STControl (Bonn)
  - RCE system & CalibGui (SLAC)
- To explore efficiency and resolution, we need high-energy particles and a telescope
  - Test Beams at DESY (Hamburg), SPS (CERN) and SLAC (California) with EUDET Telescope

USBPix universitätbonn



RCE system SLAC NATIONAL ACCELERATOR LABORATORY



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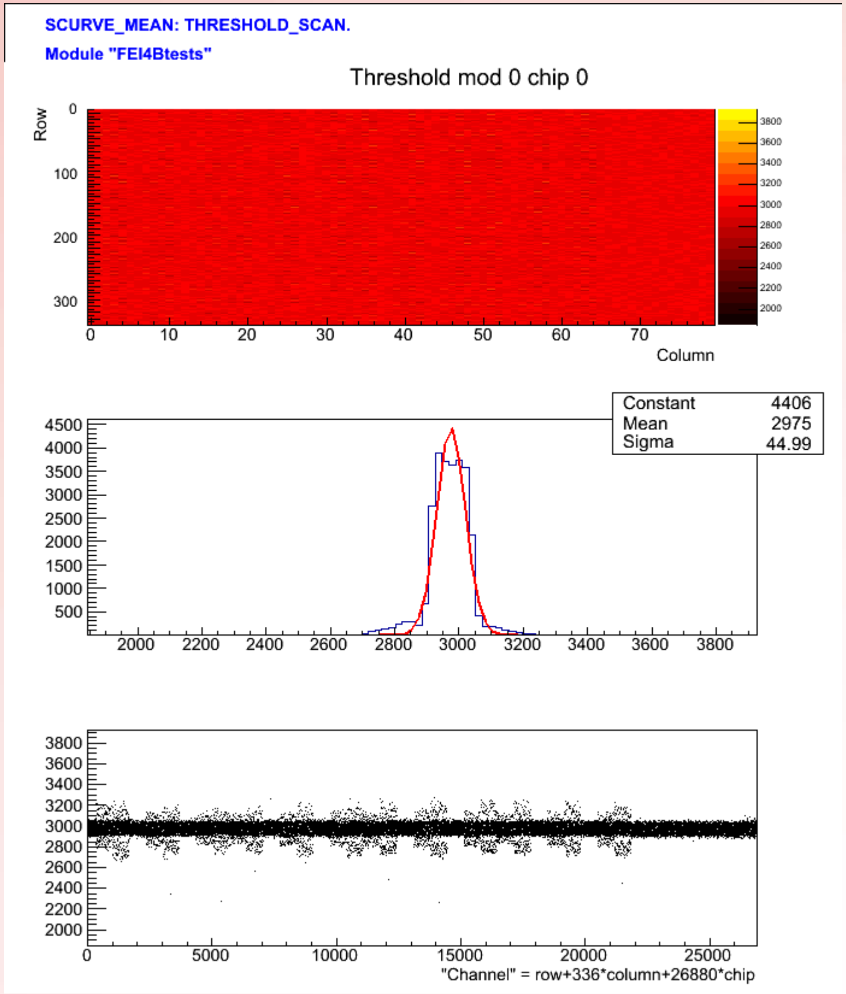
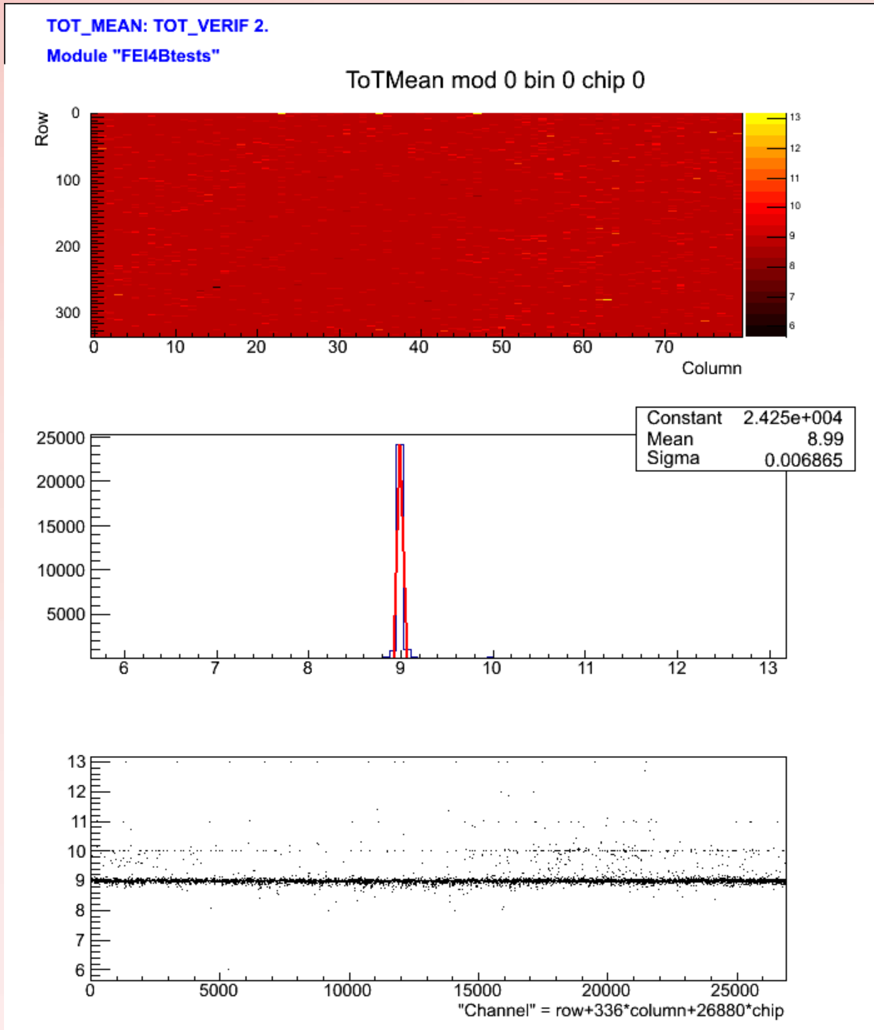
Characterisation in Laboratory

- Threshold tuning
  - Tune by changing local pixel threshold voltage, TDAC, over whole pixel matrix until threshold is uniform
  - Check uniformity: inject each pixel with incremented amount of charge until charge is high enough to register as being a signal – i.e. being over threshold
  - Tuned threshold dispersion must be <100e (IBL TDR)



Characterisation in Laboratory

- ToT Tuning
  - 80 e-h pairs per µm of Si created by a MIP
  - i.e. a MIP passing through 250µm of Si creates 20k e-h pairs
  - Tune time 20ke spends over threshold to be 9 by altering FDAC value pixel-by-pixel until matrix ToT is uniform
  - 20ke spends 9 x 25ns bunch crossings above threshold



Characterisation in Laboratory

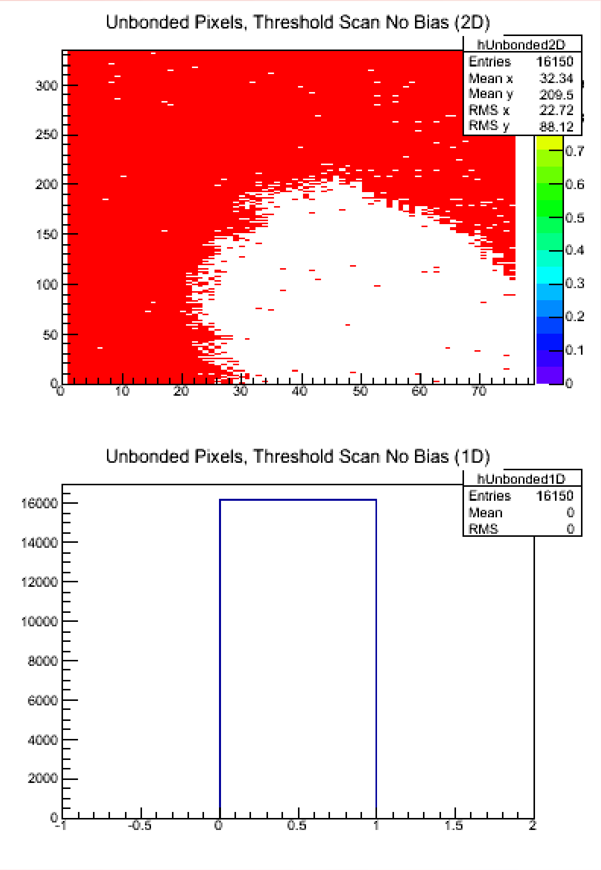
- Bump-Yield studies
  - Assessing quality of different vendors for ATLAS Phase-II Upgrade has lead to interesting studies in bump-bond yields
  - Eventually want thin modules: 150µm chip and 150µm sensor
  - Bowing effect due to CTE mismatch in the CMOS stack in the FE-I4
  - Problem can be rectified by providing back-side compensation to the wafer to prevent lifting and breaking of bump-bonds during re-flow

How to assess bump-yield:

- Perform Threshold Scan at 0V
- Look at sigma on threshold
- Large sigma ~400e due to bulk of silicon as it is undepleted
- Sigma ~120e is due to noise inherent in FE electronics i.e. these pixels are unbonded
- Perform Crosstalk Scan at high voltage
- Look at occupancy
- If pixel exhibits crosstalk under bias, it is merged

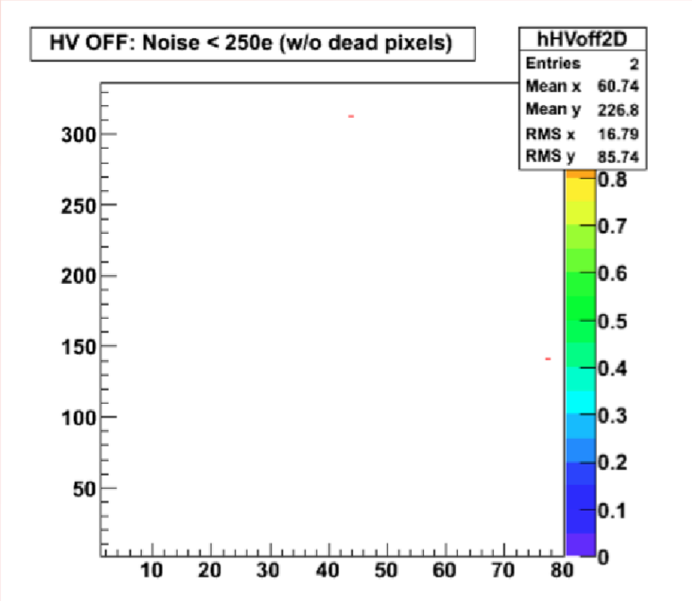
Characterisation in Laboratory

- Thinned VTT module with poor bump yield.
- 16150 disconnected pixels due to bowing at high temperature during re-flow
- Bump-yield: 39.9%



Characterisation in Laboratory

- Advacam bump-bonded module shows vastly improved results
- 2 disconnected pixels gives bump-yield of 99.99%

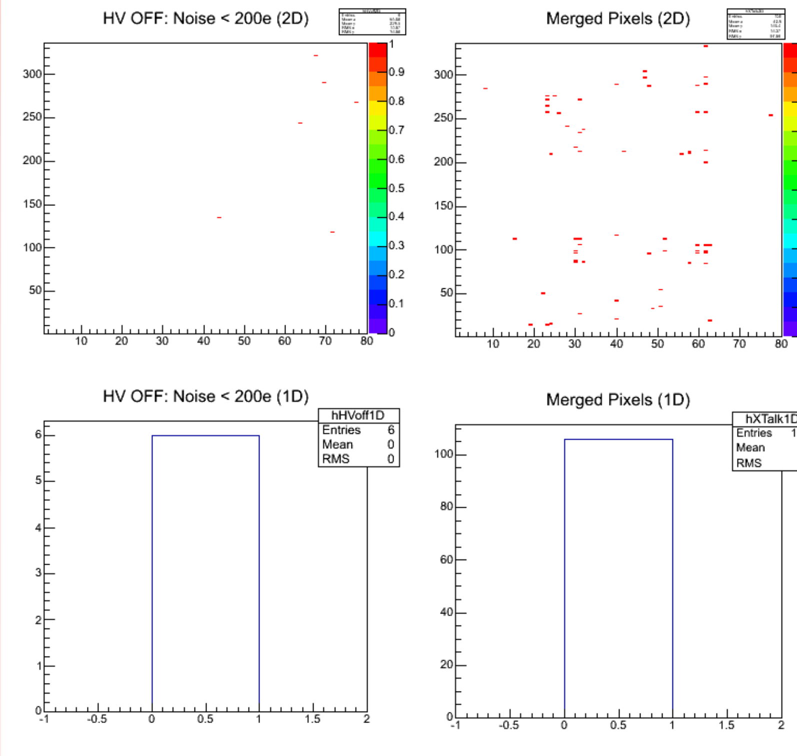


*Marko Milovanovic

Characterisation in Laboratory

- Bump yield study on Indium-bumped module by John Lipp at RAL (full thickness but work on thinned modules starting)
  - Bonding performed at 30ºC
- Disconnected pixels: 6/26880
  - (criteria: Sigma > 0e and < 200e)
- Merged bumps: 106/26880
  - (criteria: Crosstalk occurs at 100V)
- Total Bump-Yield: 26768/26880

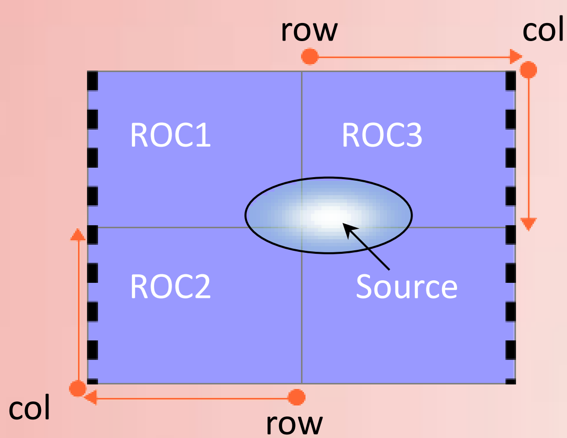
99.6%

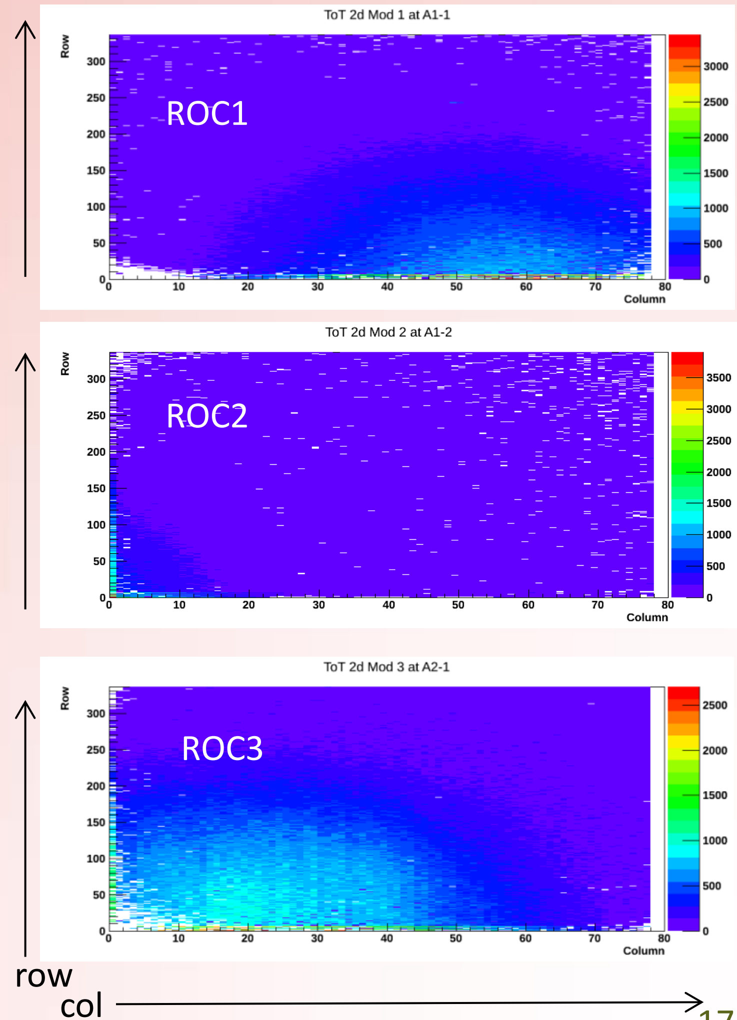


IBL TDR accepted bump-yield 99.8% (57 disconnected pixels)

Characterisation in Laboratory

- Source Scan on Quad Module
  - Use Americium-241 and self-trigger mode in RCE
  - Decays by α-emission with a by-product of γ-rays
  - Plots show 3 chips of quad with Am-241 source

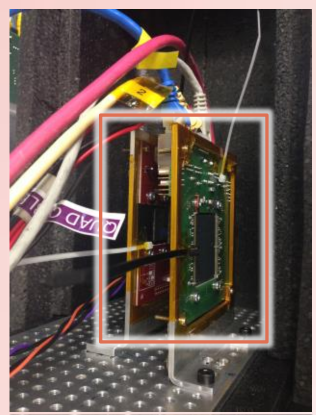


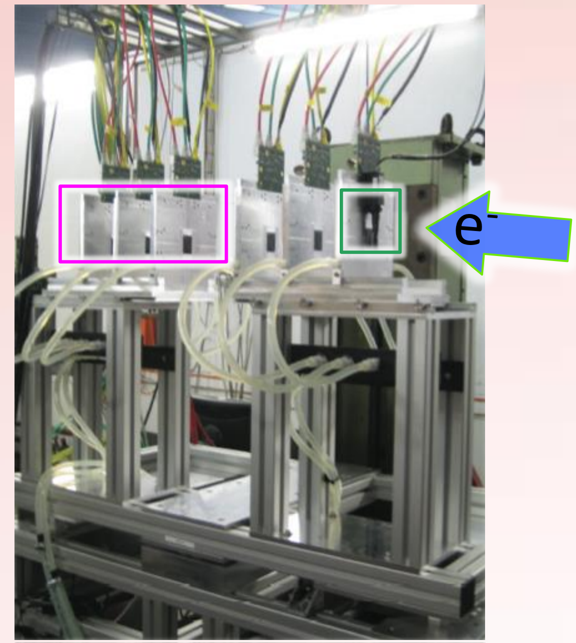


Characterisation at Test Beams

Eudet Telescope

- 3 Mimosa planes in each telescope arm
- Overlapped scintillators (2cm x 1cm) act as trigger
- Devices under test (DUTs) placed between arms
- 4GeV electrons
- Read out data with RCE system or USBPix





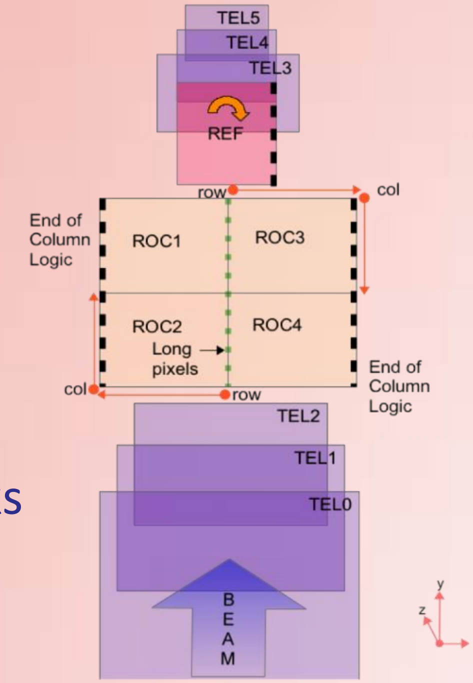
Reconstruction of Test Beam data

RECONSTRUCTION

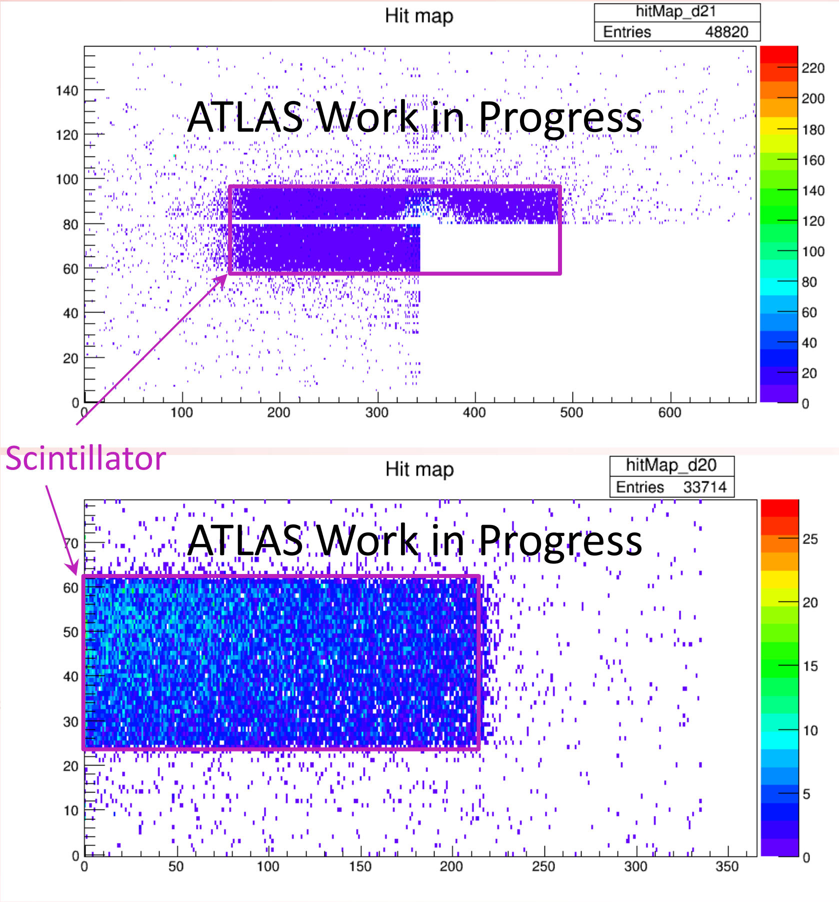
- Converter
- Clustering
- Hitmaker
- Align
- Fitter
  - Outputs TBTracks

ANALYSIS

- Efficiency
- Resolution
  - Multiple scattering studies



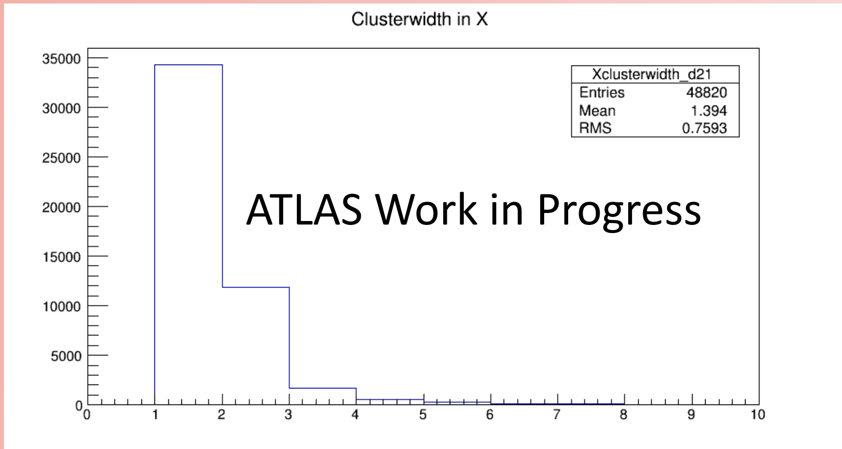
Quad Module



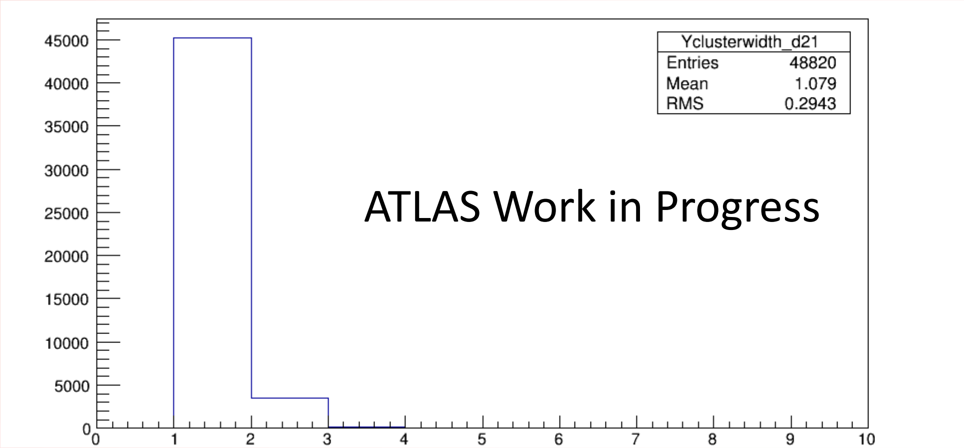
Reference sensor

Reconstruction of Test Beam data

- Cluster size in X
  - More cluster size 2 & 3 as expected due to smaller pixel pitch (50μm)



- Cluster size in Y
  - More cluster size 1 as expected due to larger pixel pitch (250μm)



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Conclusions

- Detailed work underway for HL-LHC Upgrade of ATLAS Pixel Detector
  - Use of FE-I4 as read-out chip
  - Development of sensor technology

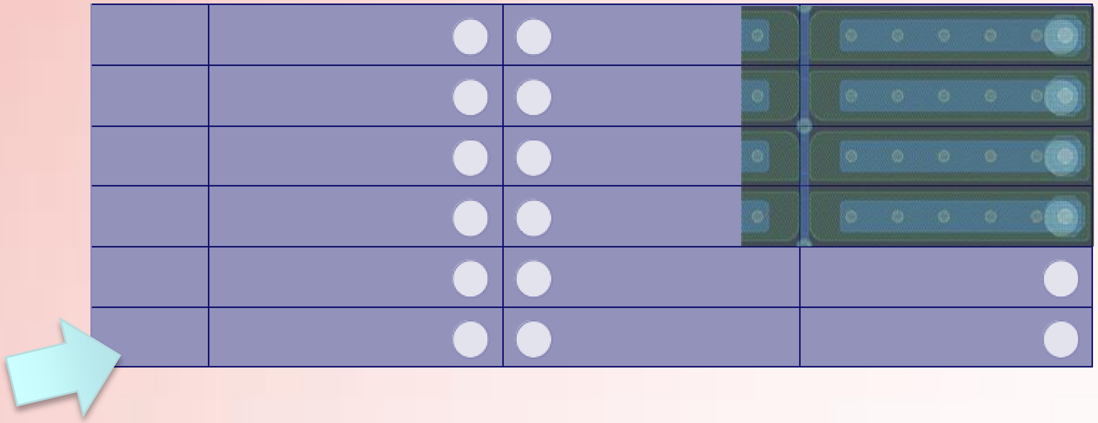
- Characterisation of both Front-End chips and Sensors
  - Tuning and exploration of FE-I4 characteristics
  - Bump Yield studies
  - Test Beams

Thank you for your attention!

BACKUP

CERN Pixel V – Sensor Geometries

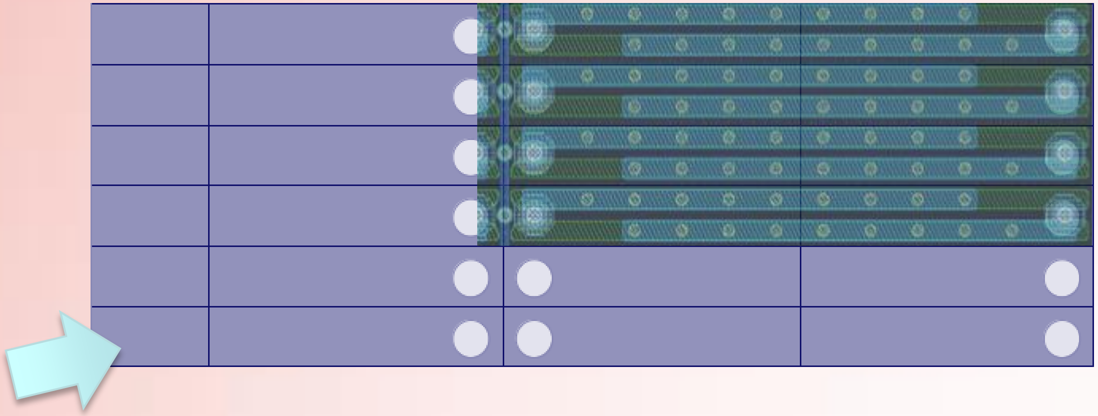
ROIC Pixel Matrix
250µm x 50µm



250µm x 50µm

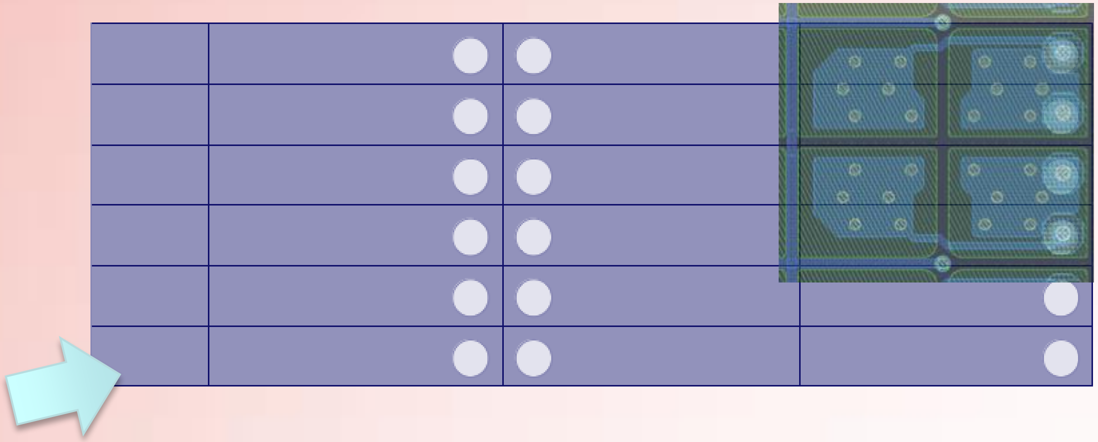
CERN Pixel V – Sensor Geometries

ROIC Pixel Matrix
250µm x 50µm



500µm x 25µm

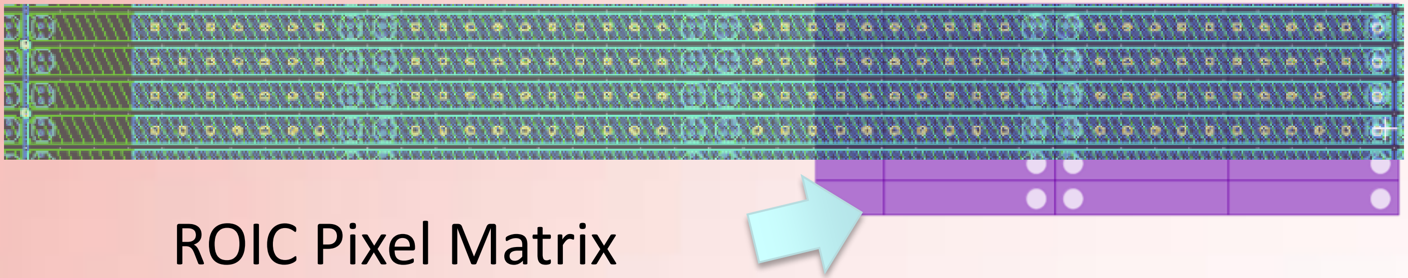
CERN Pixel V – Sensor Geometries



ROIC Pixel Matrix
250µm x 50µm

125µm x 100µm

CERN Pixel V – Sensor Geometries



ROIC Pixel Matrix
250µm x 50µm

2000µm x 25µm

Characterisation in Laboratory

FDAC structure

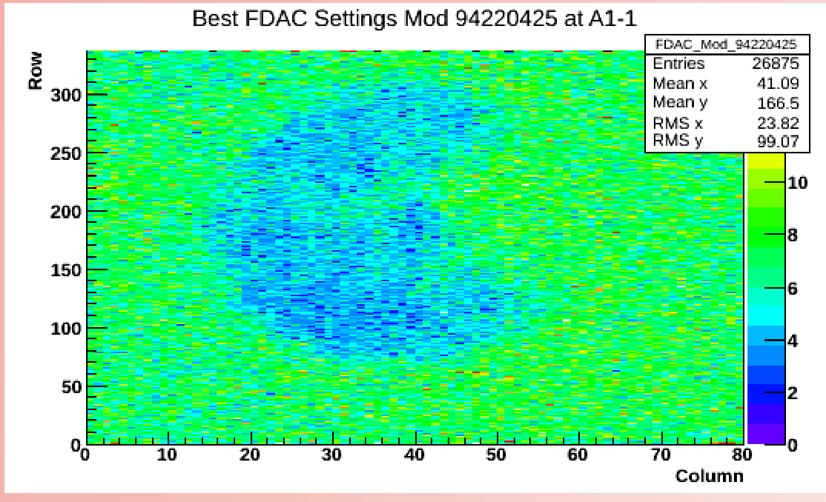
- Structure in FDAC maps was discovered during tuning ToT of modules *and* bare ROC using USBPix and RCE system
- Not seen in TDAC map so is **not** physical damage to module
- Improvement when using IBL tuning parameters but structure still evident
- Scope for exploring parameter space of scans in both USBPix and RCE
  - May be a powering issue
  - Investigation on-going

Characterisation in Laboratory

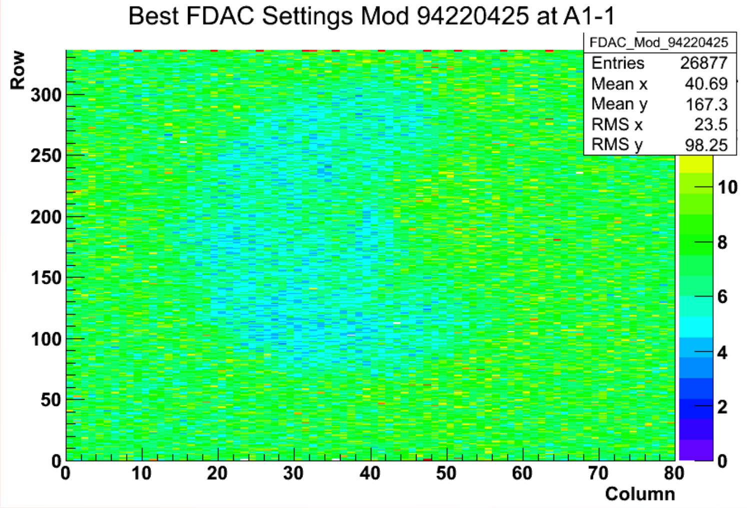
FDAC structure

SC 3072-4-8

250μm x 50μm



Original tuning



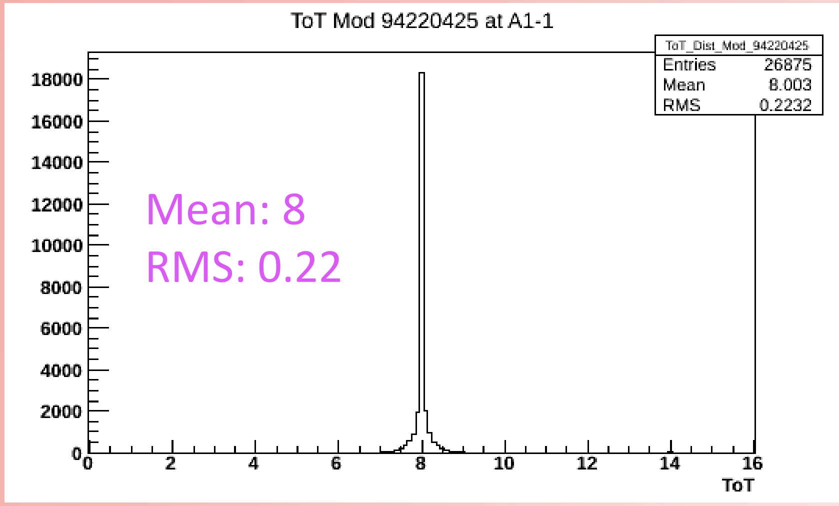
Using IBL tuning scheme

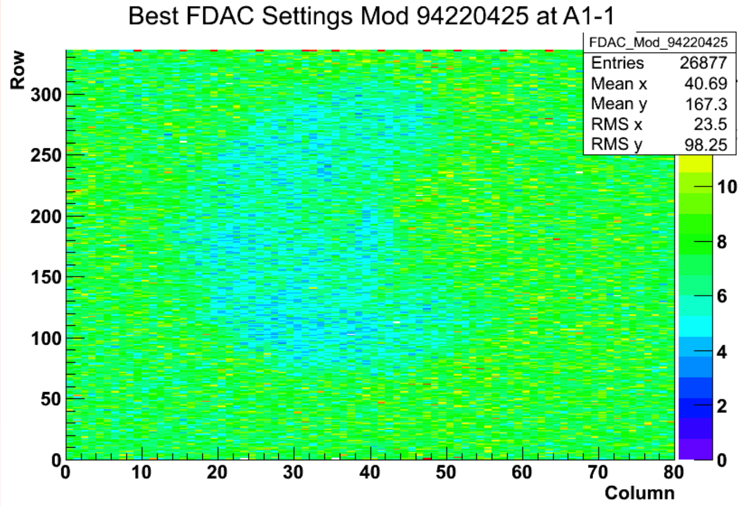
Characterisation in Laboratory

FDAC structure

SC 3072-4-8

250µm x 50µm





FDAC map corresponds to well-tuned ToT

Using IBL tuning scheme