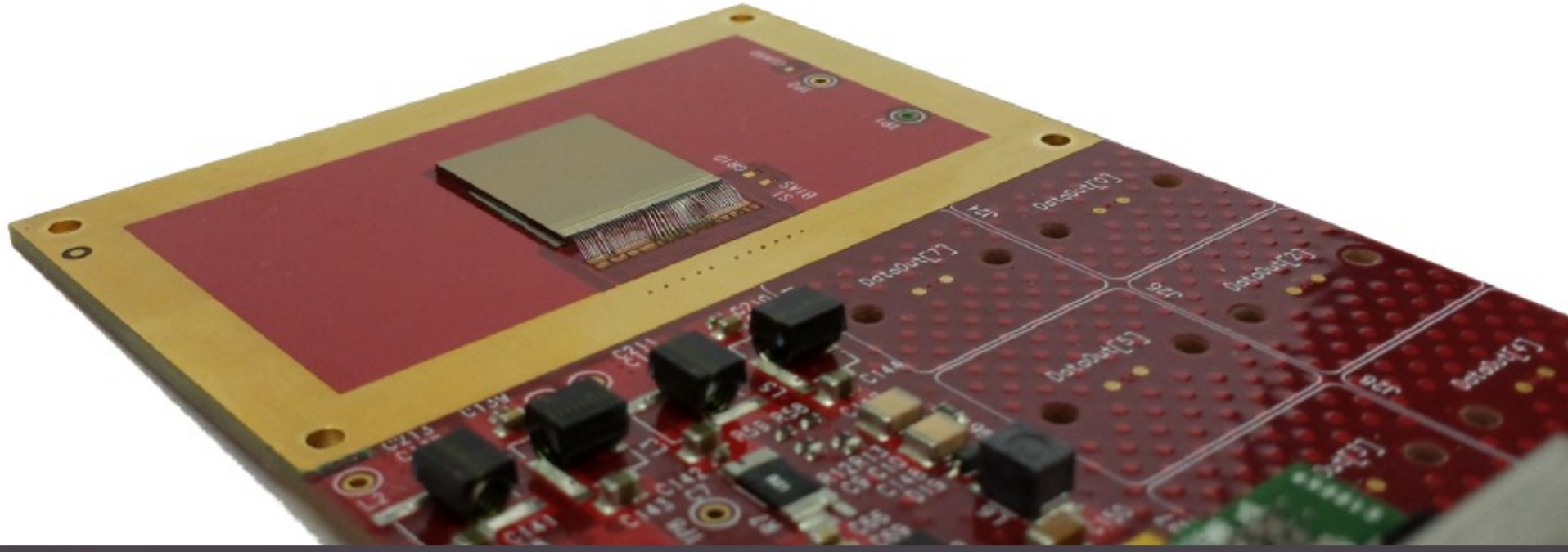


Timepix3 and readout status

Szymon Kulis (CERN)
on behalf of the
CLIC detector and physics study
and **Medipix3 Collaboration**

CLIC Detector and Physics Collaboration Meeting
Geneva, 1-2 October 2013

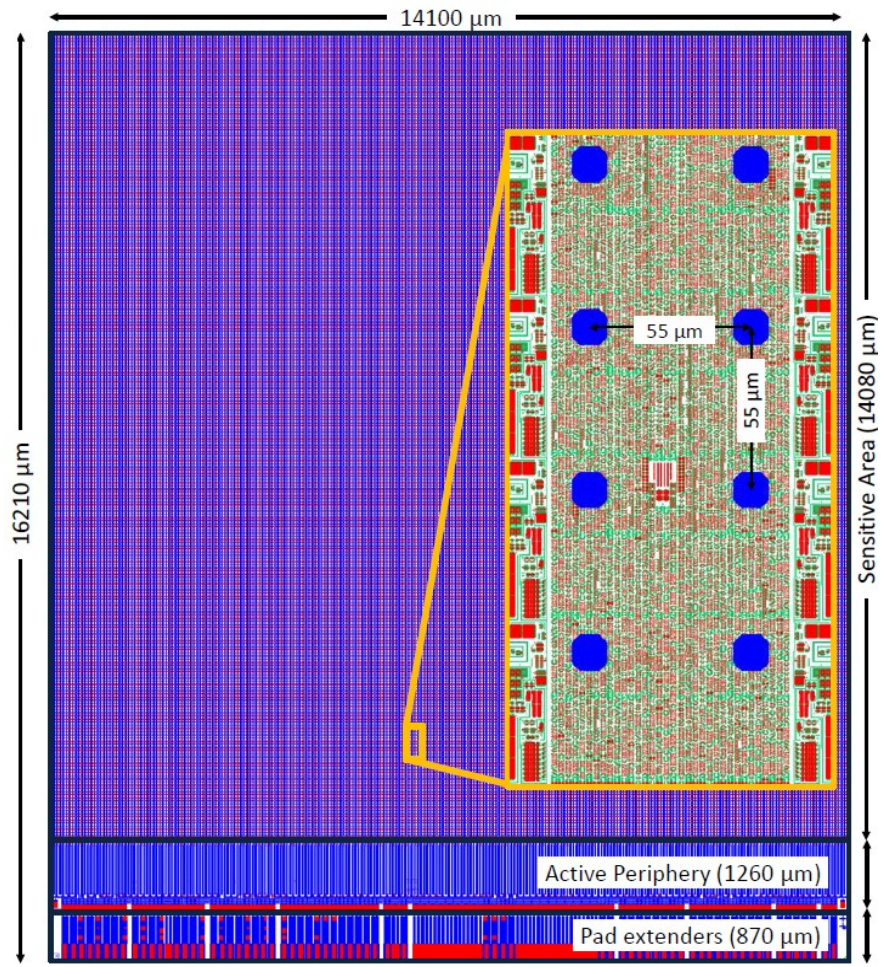
Agenda

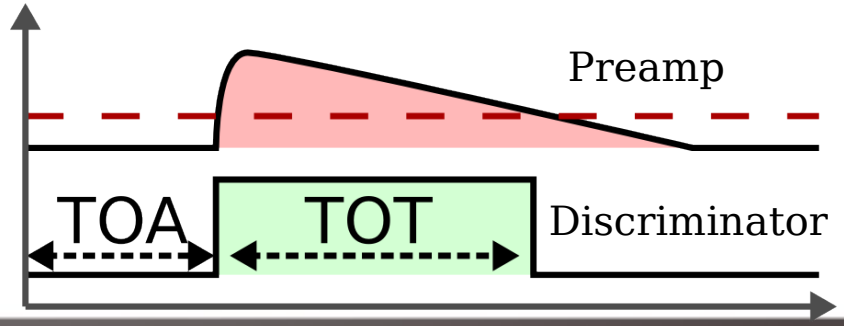
- Timepix3 readout chip
  - General features
  - Front-end architecture
  - Digital Concepts
- Data Acquisition system
  - Architecture
  - Firmware
- Timepix3 preliminary results

Timepix3 Chip

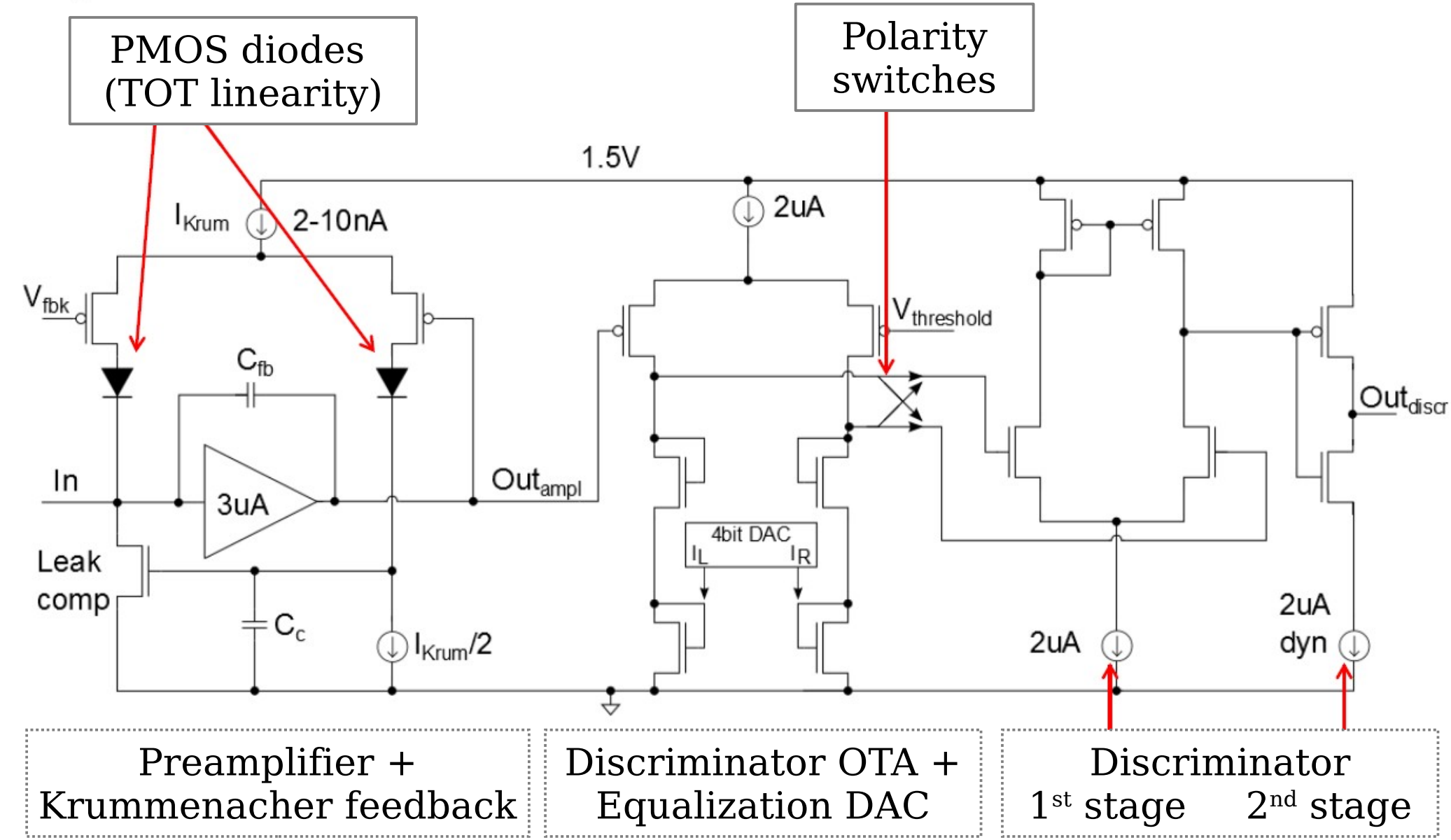
General features:

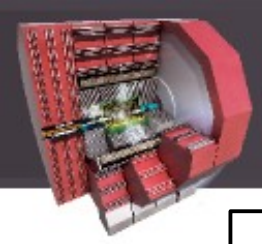
- Pixels count: **256x256**
- Pixel size: **55µmx55µm**
- **2 main measurement modes:**
  - simultaneous **TOT** (10 bit) and **ToA** (18 bit)
  - **event counting** (10 bit) and **integral TOT** (14 bit)
- **Adjustable input dynamic range (TOT)**
- **Fast ToA for time stamping** *with a precision of **1.56ns***
- **Data-driven readout** *dead-time free for a maximum hit rate of 40Mhits/s/cm²*
  - *8 sLVS fast data lines (8 x 640Mbps → 5.12 Gbps)*
  - *8/10 bit encoding*
  - *Built-in PLL*
- **Shutdown/wake-up features**





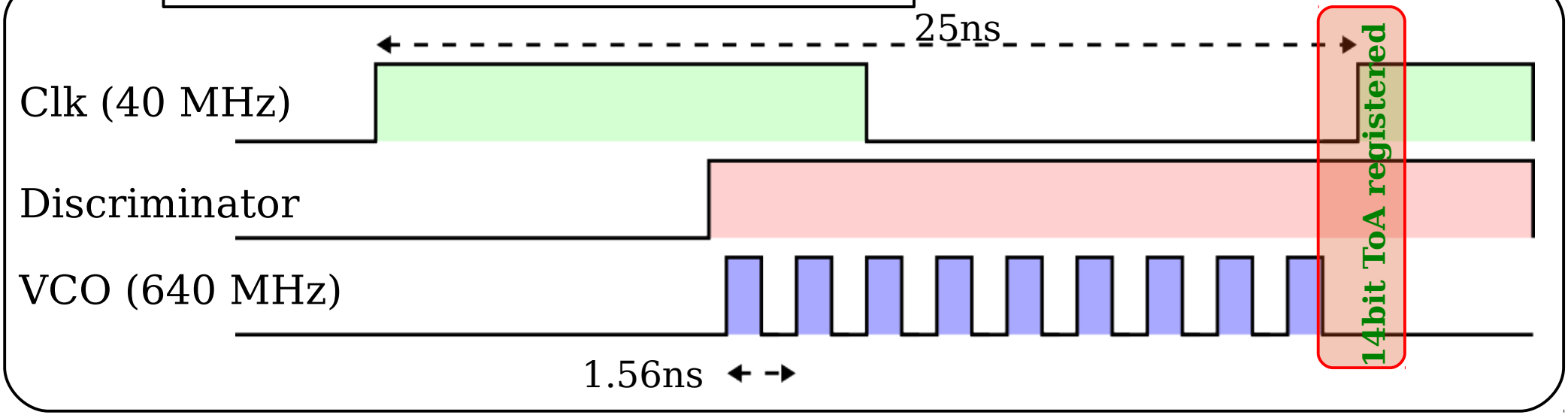
Timepix3 – Front end



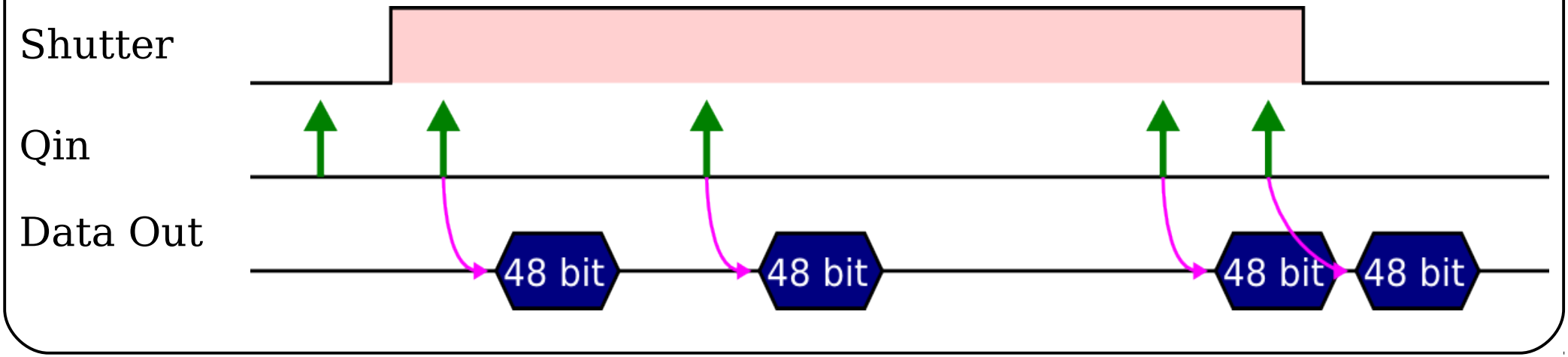


Timepix3 – Digital Concepts

Precise ToA measurement



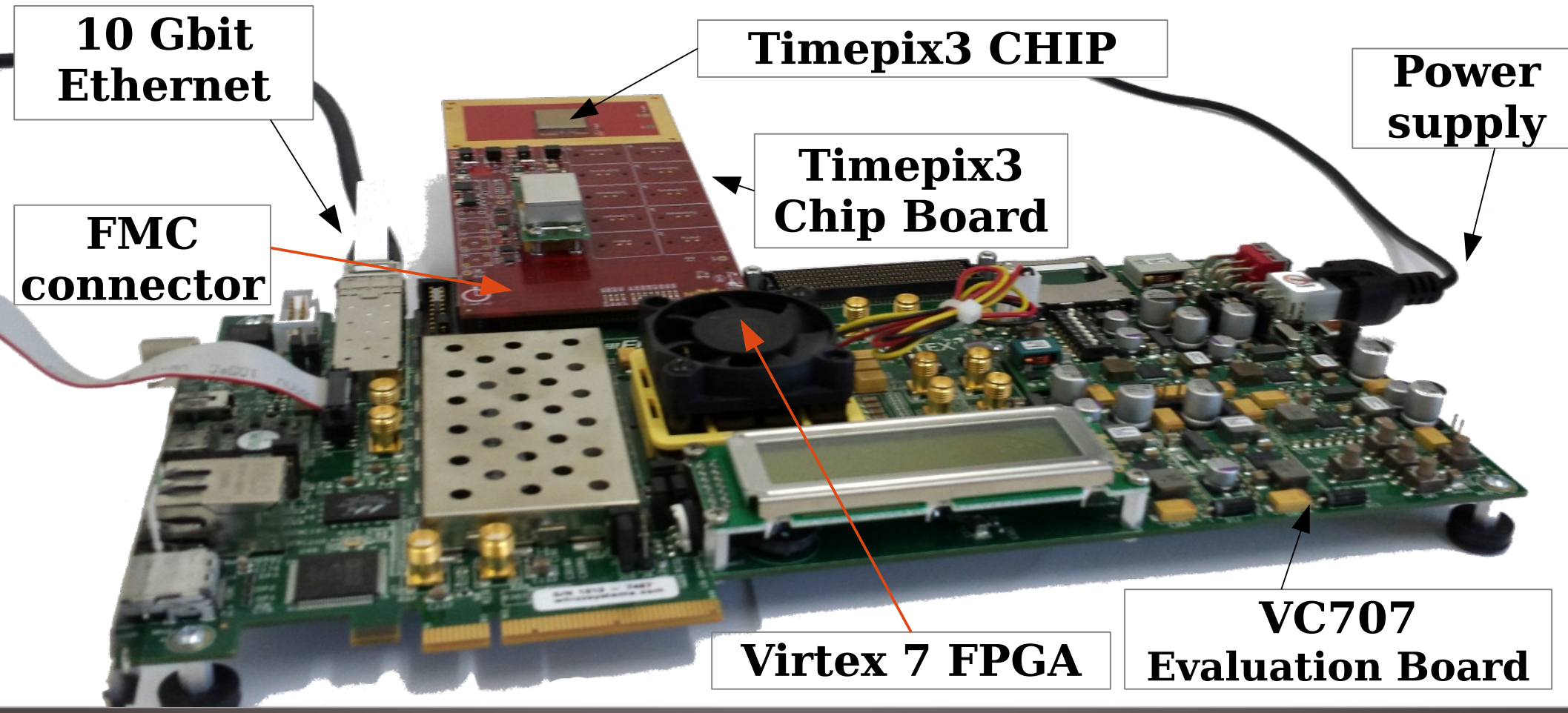
Data-driven readout mode



Timepix3 Readout System

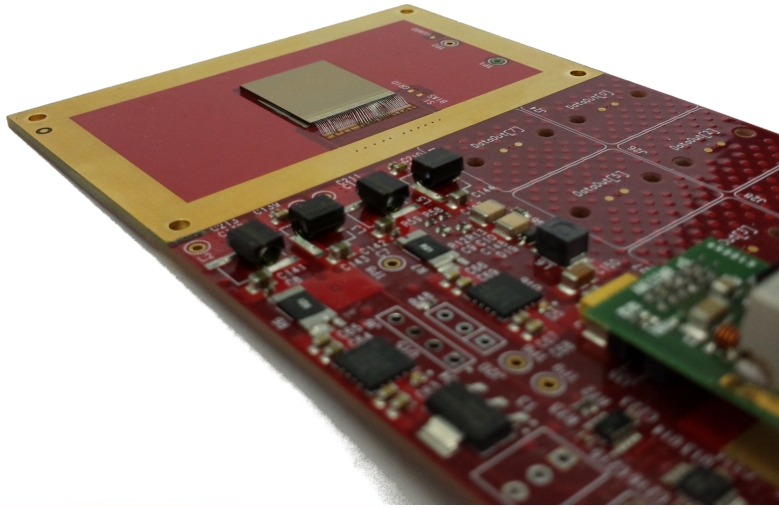
Speedy PIxel Detector Readout (SPIDR)

Aim to read out 1 Timepix3 at full speed (5.1 Gbps),
or multiple Timepix3 chips at lower speed (fewer links per TimePix3)



Timepix3 Chip Board

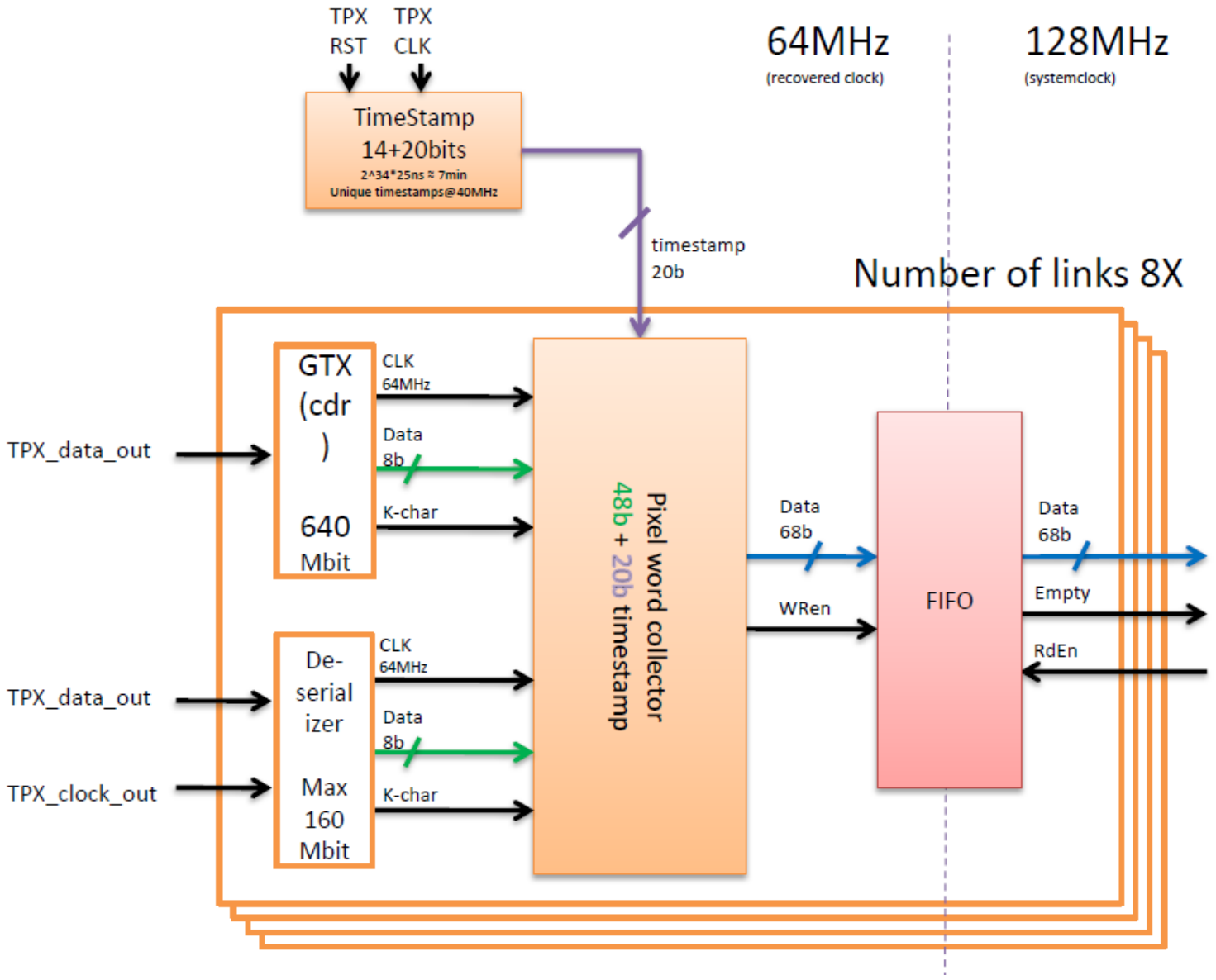
- **FMC connector** (high pin count 8 gbt's)
- MUX for selecting between RocketIO (gigabit transceiver) and regular IO pins on FPGA
- **ADC & DAC I²C**
- **Voltage regulators + Voltage and Current monitors**
- CERN AMIS5 **DC/DC converter** (rad hard and magnetic field tolerant)
- **Flash** for storing pixel matrix configuration
- **High Voltage generator** for Si sensor (12-100V) + extra pads for HV bias
- **Lemo connectors** (trig/clk/busy)
- **Temperature sensor behind chip**
- No (important) routing behind chip (allows removing/thinning of PCB for beamtest)
- **Probing fixtures** for fast data lines



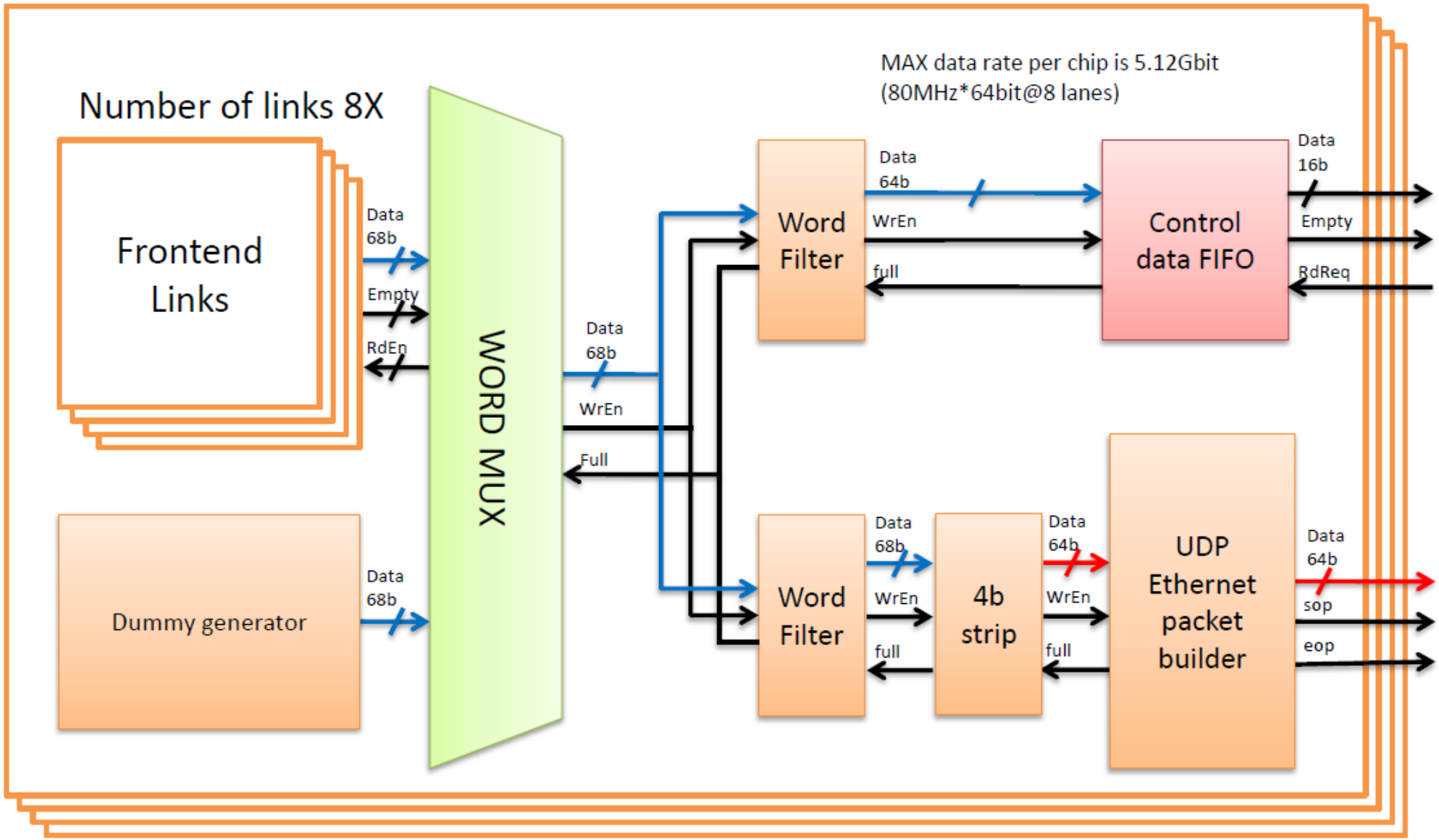
FPGA Firmware

- Modular firmware architecture (EASE HDL entry)
- Platform independent components:
  - Leon3 - softcore CPU
  - Verilog coded MAC
- Configuration options
  - Number of links
  - Number of chips
  - Frontend link type (GTX/Serial)
  - Ethernet type (1Gb / 10Gb XAUI / 10Gb PCS)
- Simulation of firmware in combination with Timepix3 Verilog models available

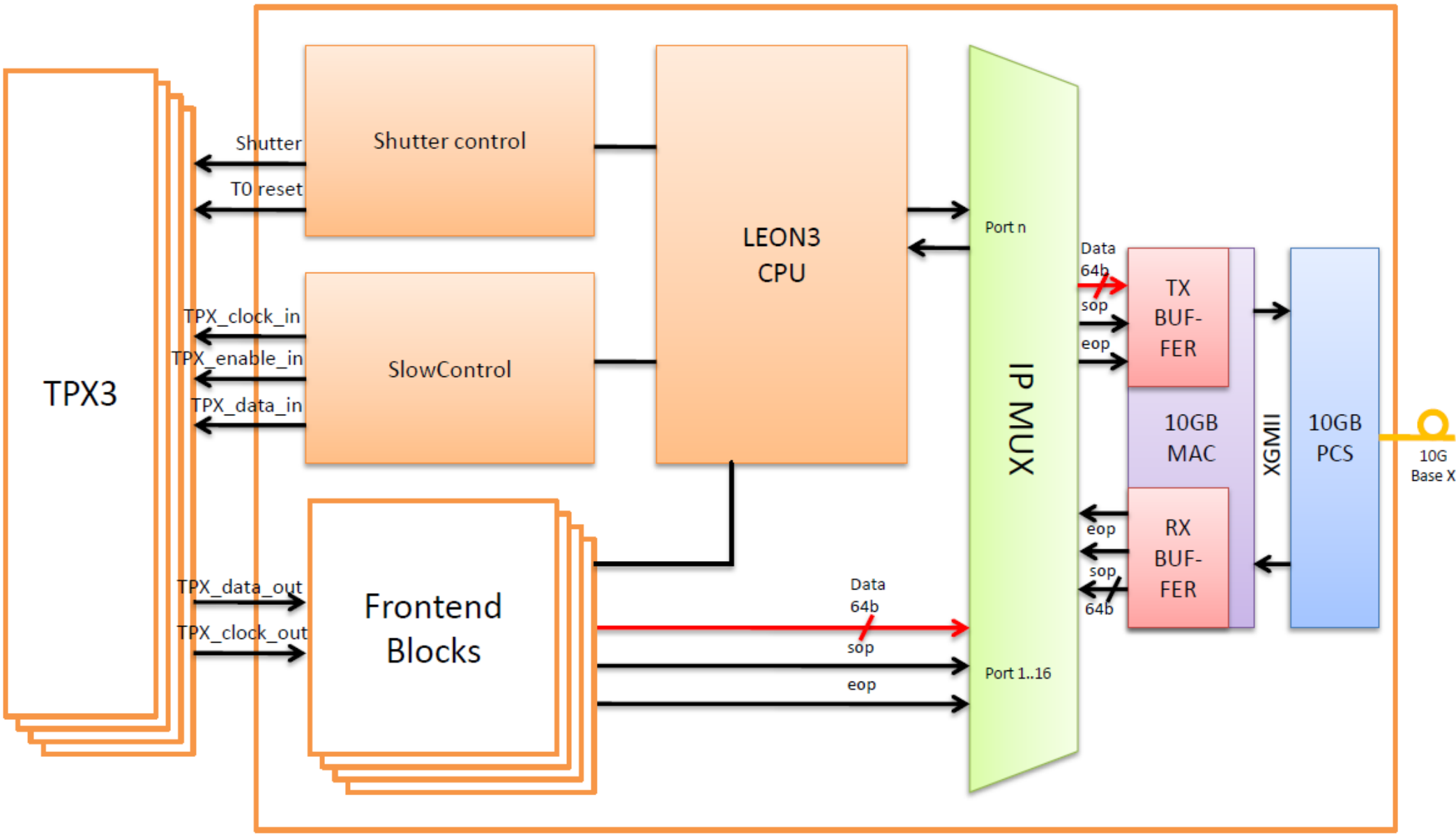
FPGA Data Lines



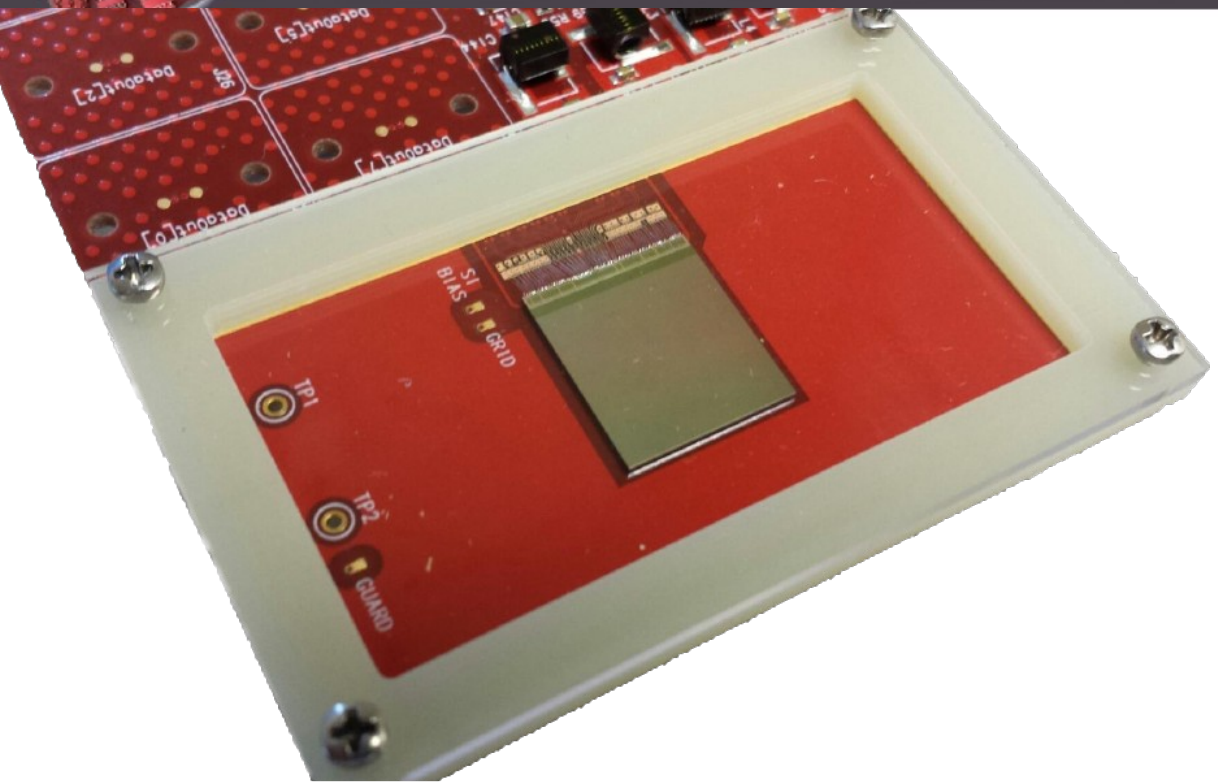
FPGA Word Filter



FPGA Firmware



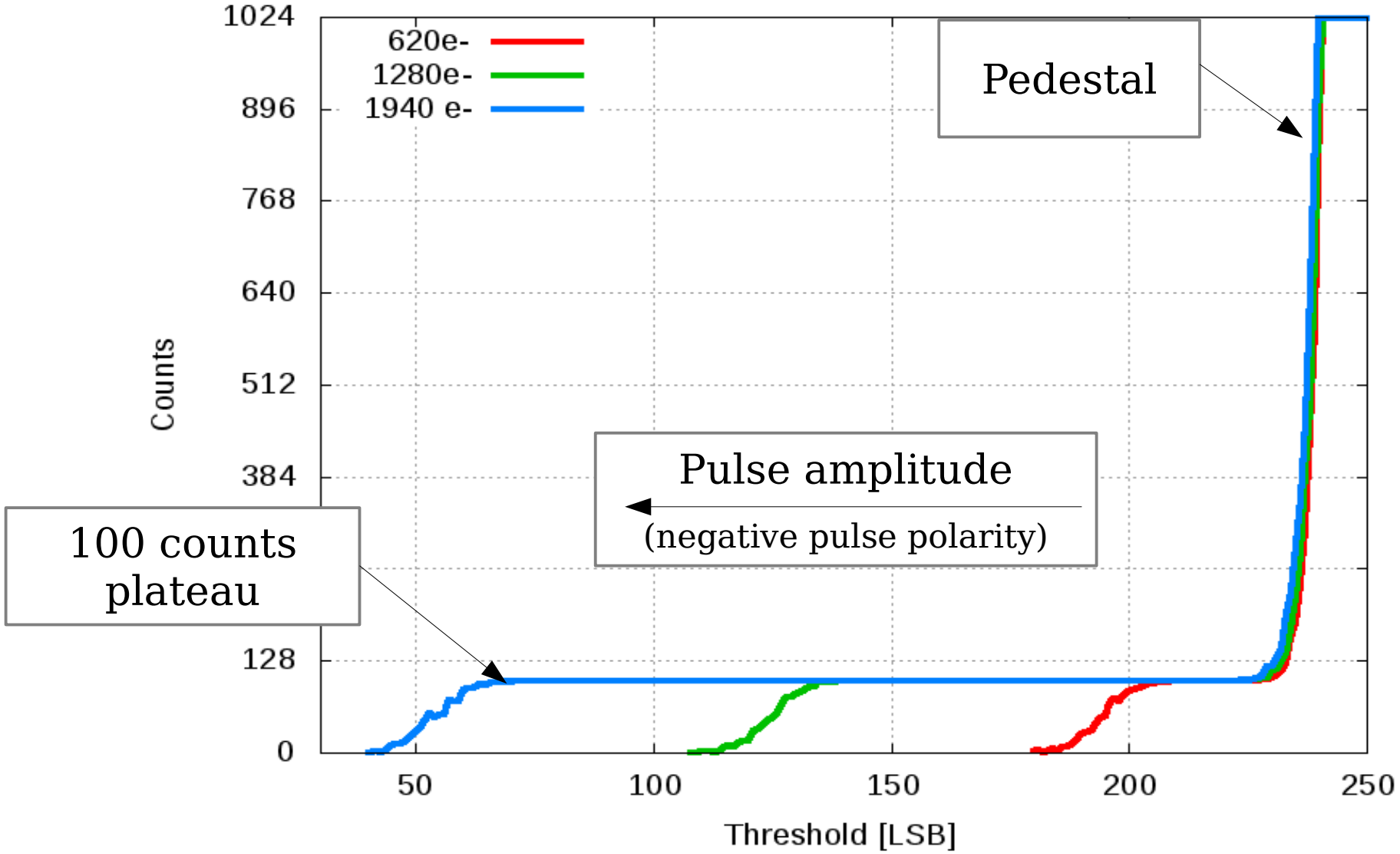
Timepix3 Preliminary Results



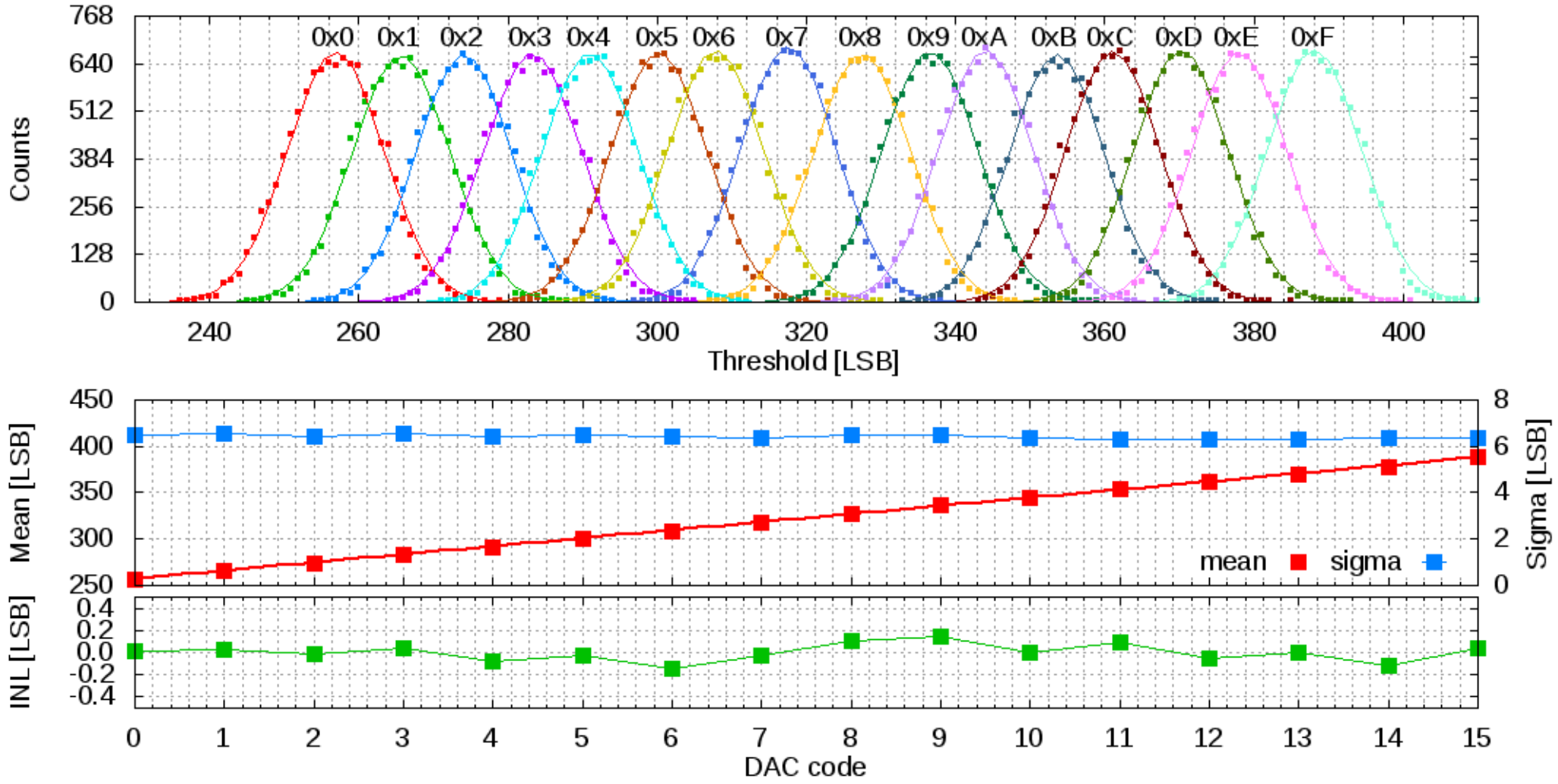
- **2 chips** under test since beginning of September
- Periphery tested at 95%, **no issues detected**
- **Data readout functional** at full speed (640MHz)
- Current consumption:
  - Analog **450mA**
  - Digital **370mA** (in data driven mode and no pulses injected)

Timepix3: S-curves

100 pulses in Photon Counting + integral TOT mode (negative pulse polarity)

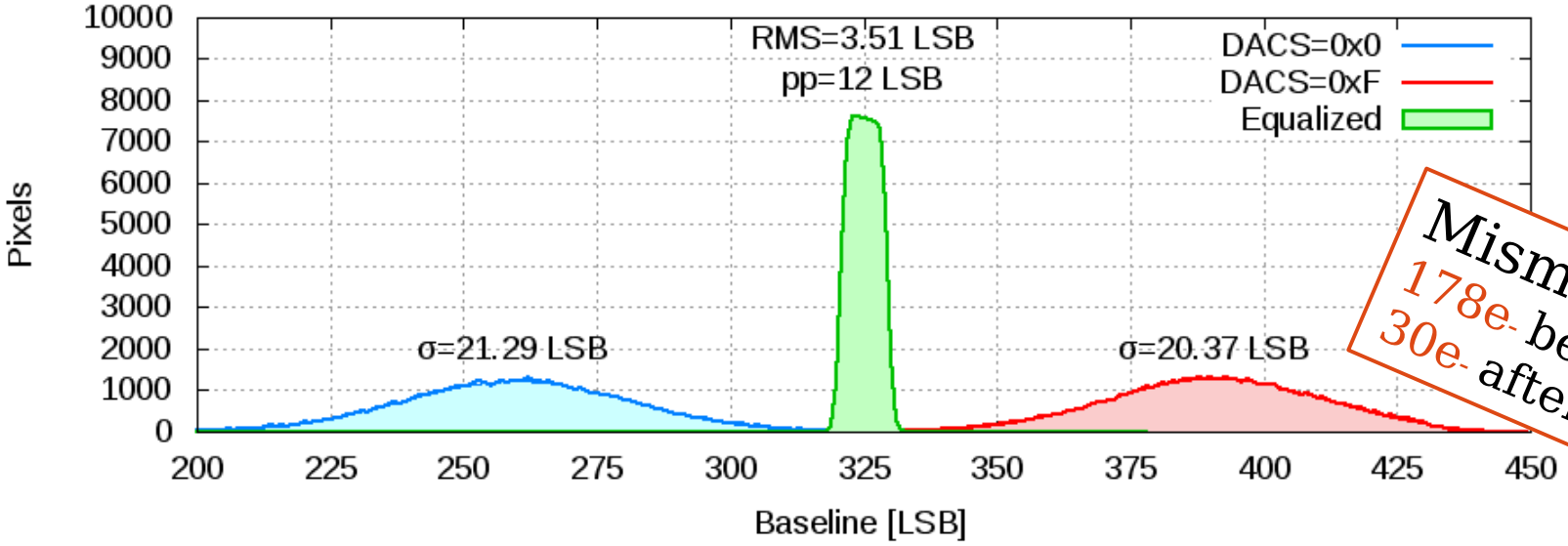


TPX3: Scan of a pixel equalization DAC

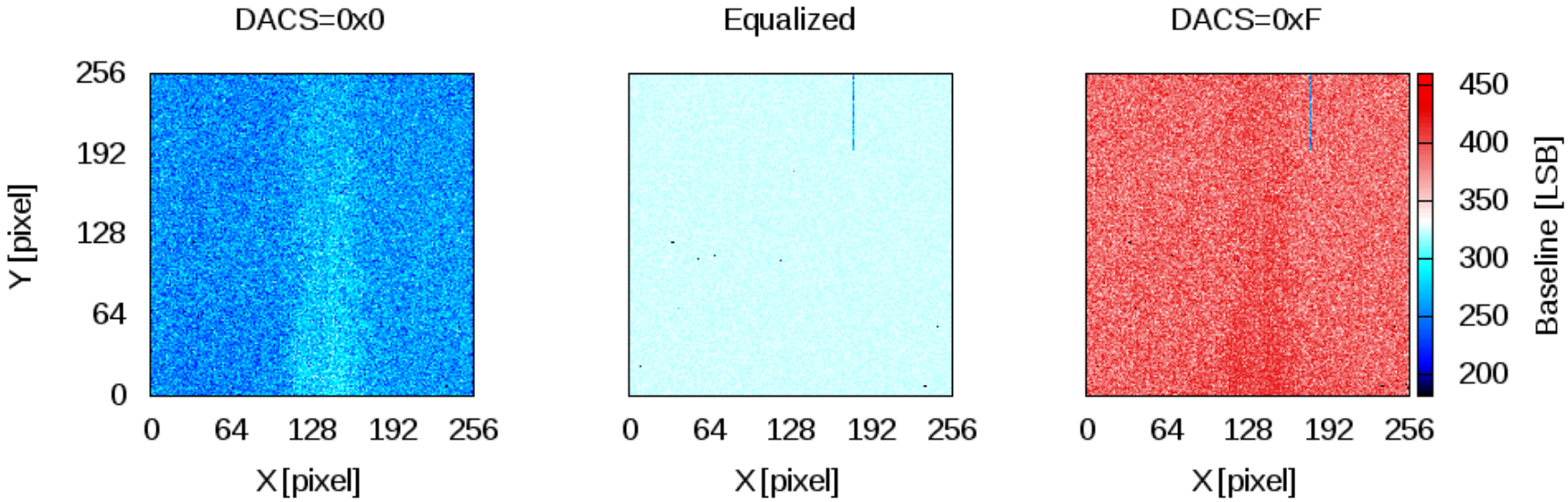


- 4bit equalization DAC shows **very good linearity**, as expected.
- Noise 6.5LSB: **~65e$^-$** (better than 75e$^-$ expected), assuming 50mV/ke- gain.

Timepix3 Equalization



Mismatch:
178e- before equalization
30e- afterwards.



Summary

- **DAQ Status** → firmware is almost done (90%)
  - **Slow Control Block** is working properly.
  - Front-end block + GTX receiver is working at full speed **(8 lanes@640Mbit)**
  - **UDP Ethernet Packet generator** is functional.
  - **Leon3 CPU** is up and running including Ethernet communication (TCP/IP).
  - .. but there are still things left to do: time stamp block, test multiple chips configuration, advanced trigger logic, throttle/busy, 1Gb Ethernet, clustering/sorting, ...
- **Timepix3** → tests recently started. Preliminary results promising:
  - Power consumption as simulated
  - Periphery tested at 95%, no issues detected
  - Equivalent Noise Charge ~ **65 e-**
  - Channels mismatch ~ **30 e-**

  } **~71e-** (minimum threshold around 430e-?)
  - **.. and much more to come !**

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