CLICPIX AND MEDIPIX3-TSV PROJECTS

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Outline

- The CLIC project

- CLICpix design

- CLICpix prototype characterization

- TSV interconnects

- Conclusions

Outline

The CLIC project

The Compact Linear Collider (CLIC) is a study for a high-energy and high-luminosity collider

- □ e^+e^- collider

- □ Can be used to determine standard model parameters with a higher precision than proton colliders

- □ Allows the detection of new particles and the testing of models as supersymmetry and Higgs strong interactions

- □ 3 TeV → 48 km long!
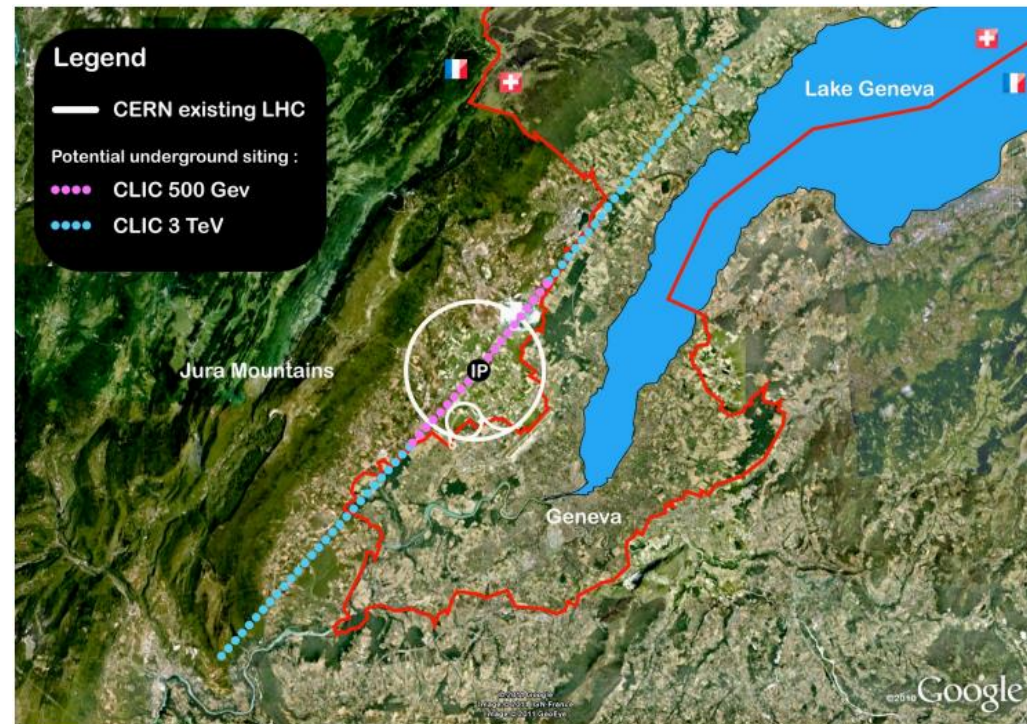
The CLIC beam

- Bunch crossings every 0.5 ns in trains of 156 ns

- Bunch trains every 20 ms → small duty cycle

- Air cooling → low power consumption

- Its vertex detector needs high spatial accuracy → small pixels!

Bunch train

Bunch train

Not to scale

20 ms

t

Vertex detector layers

< 6cm
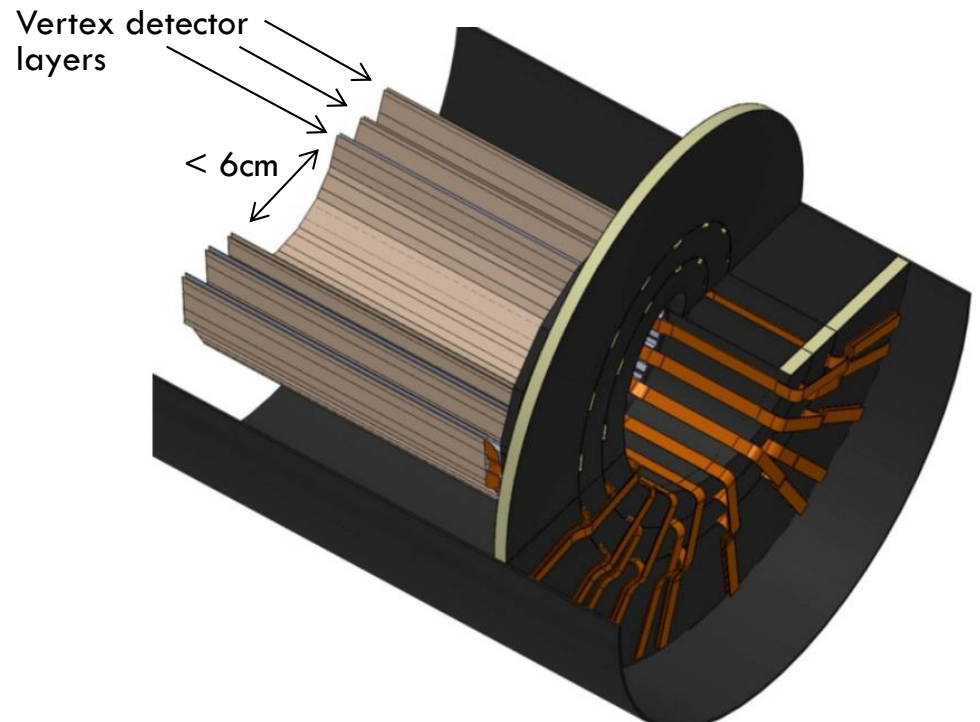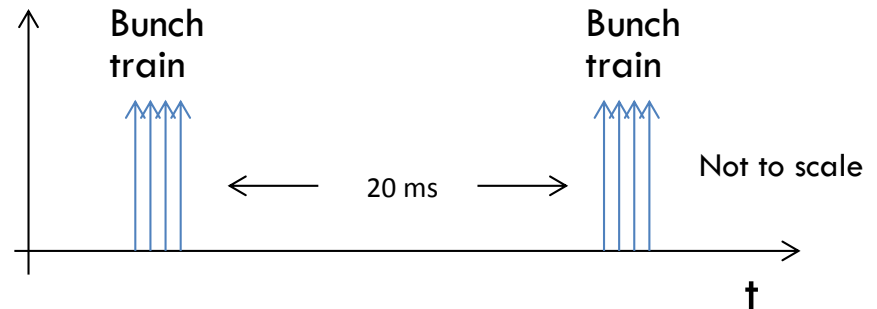
Timing requirements

- 312 bunch crossings in 156 ns and a high background rate→ Event timestamp

- Time of Arrival measurement with 10 ns accuracy is required to discriminate tracks

- High spatial (sub-pixel) resolution → Charge measurement

- At least 4-bit Time-over-Threshold is needed

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CLICpix

- CLICpix is a hybrid pixel detector to be used as the CLIC vertex detector

- Main features:
  - small pixel pitch (25 μm),
  - Simultaneous TOA and TOT measurements
  - Power pulsing
  - Data compression

- A demonstrator of the CLICpix architecture with an array of 64x64 pixels has been submitted using a commercial 65 nm technology and tested

- The technology used for the prototype has been previously characterized and validated for HEP use and radiation hard design[*]
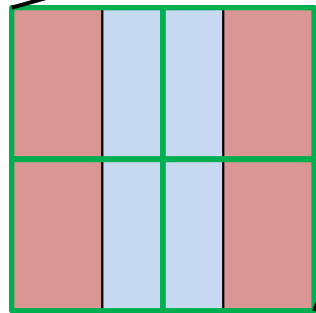
[*]S. Bonacini, P. Valerio et al, *Characterization of a commercial 65 nm CMOS technology for SLHC applications*, Journal of Instrumentation, 7(01):P01015–P01015, January 2012
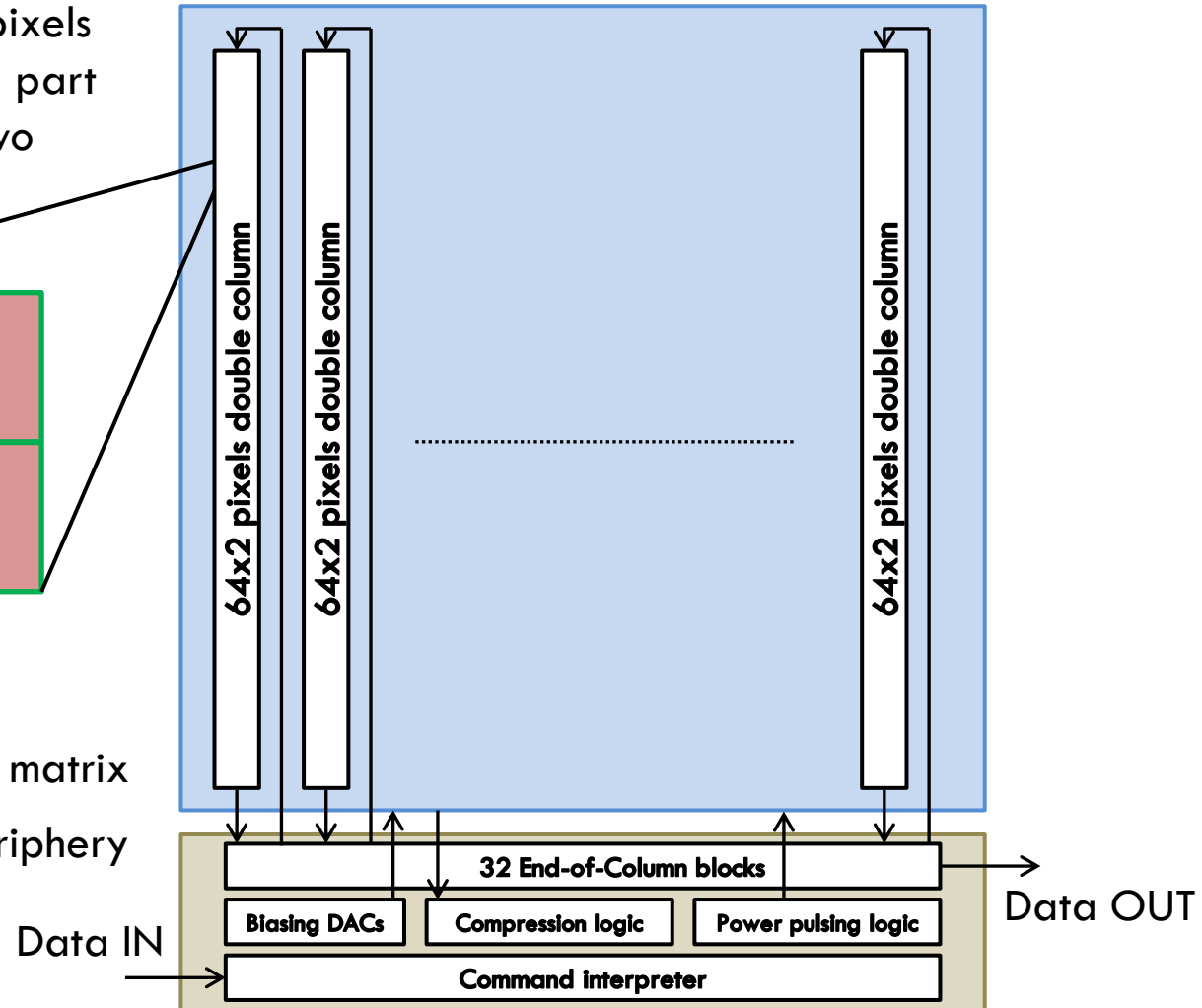

3 mm

1.85 mm
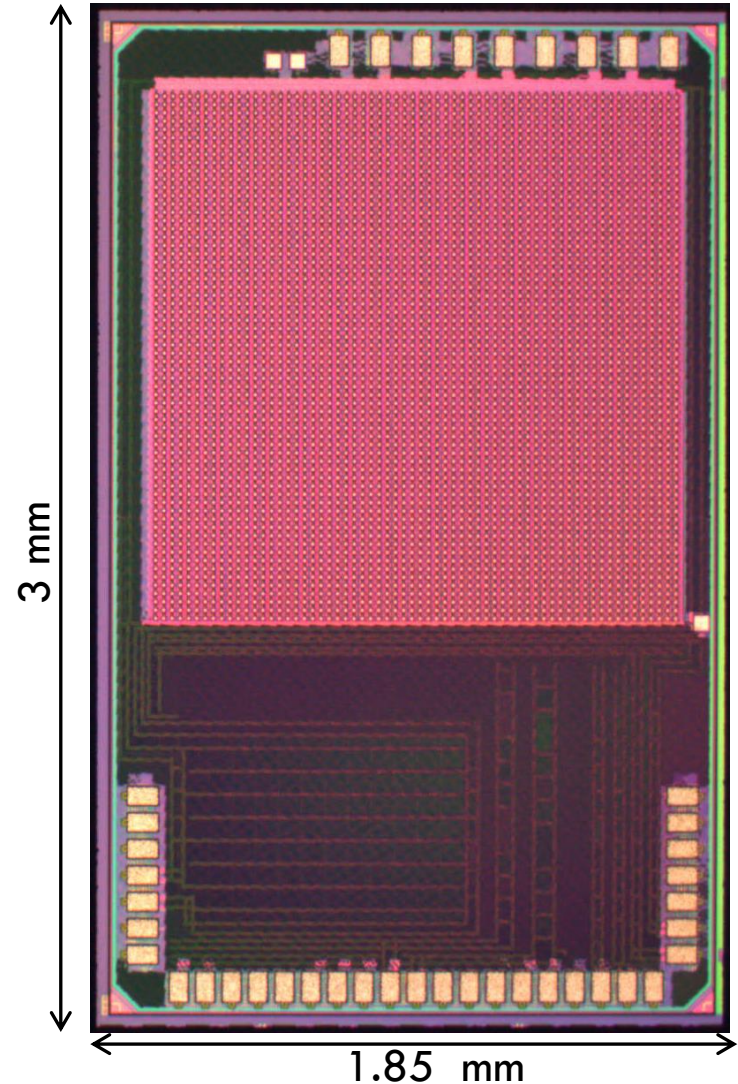
A simple block diagram

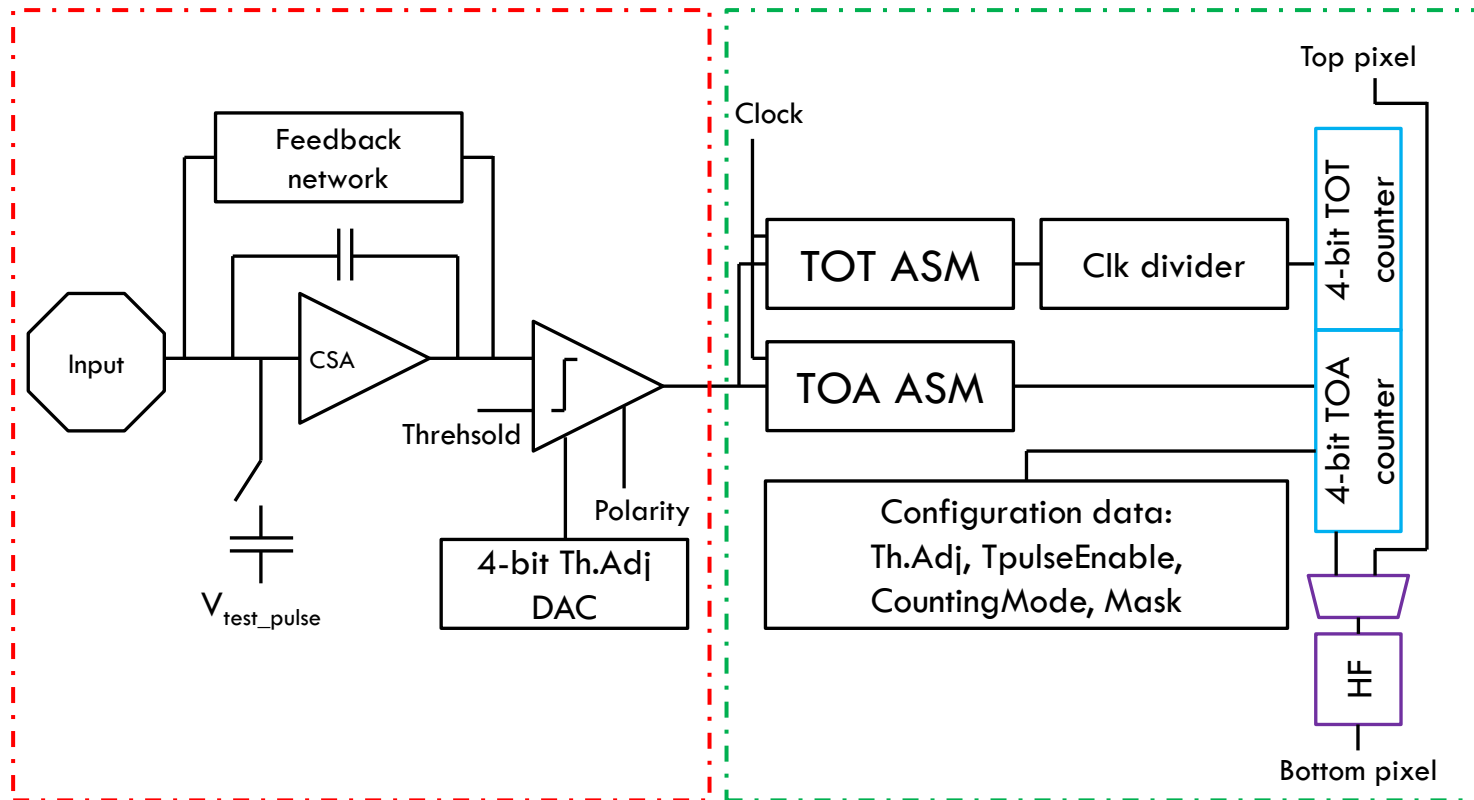Analog part of adjacent pixels share biasing lines. Digital part is shared between each two adjacent pixels

64x64 pixel matrix

Chip periphery

64x2 pixels double column

64x2 pixels double column

64x2 pixels double column

32 End-of-Column blocks

Biasing DACs

Compression logic

Power pulsing logic

Data IN

Command interpreter

Data OUT

Pixel architecture

- The analog front-end shapes photocurrent pulses and compares them to a fixed (configurable) threshold

- Digital circuits simultaneously measure Time-over-Threshold and Time-of-Arrival of events and allow zero-compressed readout

Pixel logic summary

Technology	65 nm (High-Vt Standard Cells), Asynchronous State Machines
Pixel size	25x25 µm - 25x14 µm (Analog) - 25x11 µm (Digital)
Acquired Data	TOT and TOA
Counter Depth (LFSR)	4 bits TOT + 4 bits TOA (or counting, for calibration)
Target Clock Speed	100 MHz (acquisition) 320 MHz (readout)
Data type	Full Frame Zero compression (pixel, super-pixel and column skipping)
Acquisition Type	Non-continuous
Power Saving	Clock gating (digital part), Power gating (analog part)

Super-Pixels

- In CLICpix, pixels are clustered in 2x8 arrays (Super-Pixels)

- Area reduction because some of the electronics can be shared (clock distribution tree, biasing lines)

- Additional compression layer

- The clock is distributed along each column exploiting the delays of buffers to give each pixel a clock signal with a different phase
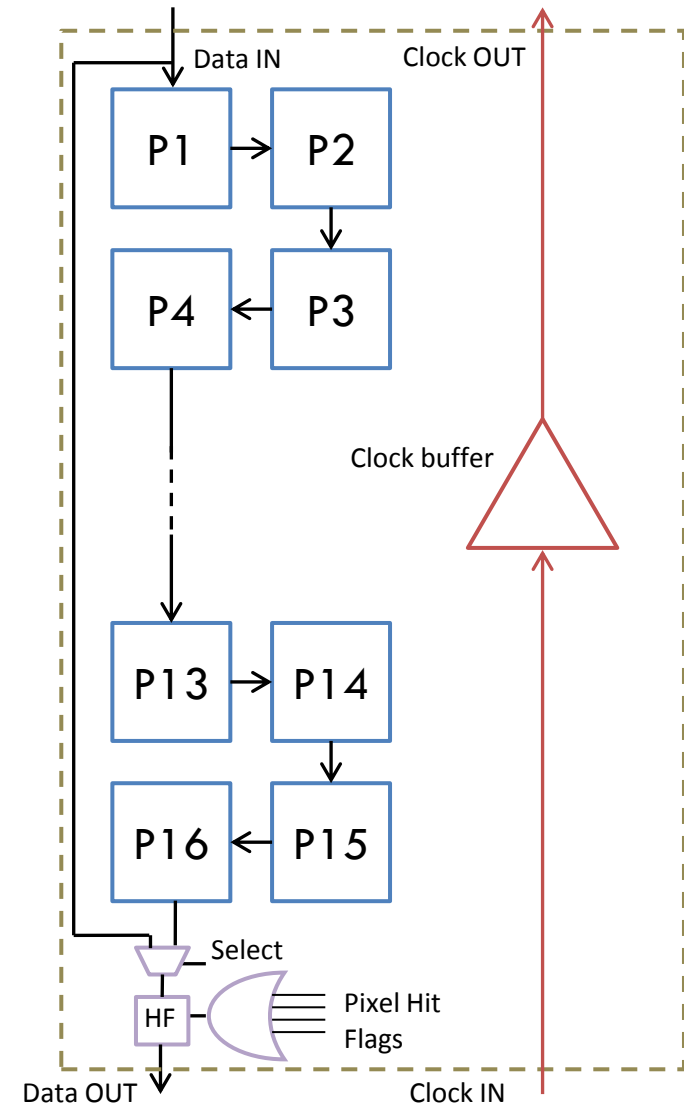
Data compression

- Two different compression schemes were evaluated
- Zero-suppression
  - Only pixels with data are read out
  - Data have an address associated to it
- Zero-compression
  - All pixels are read out
  - Pixels have a "hit-flag" bit allowing to skip data stored in pixels which were not hit
  - Additional compression layers (superpixels, columns) can be added
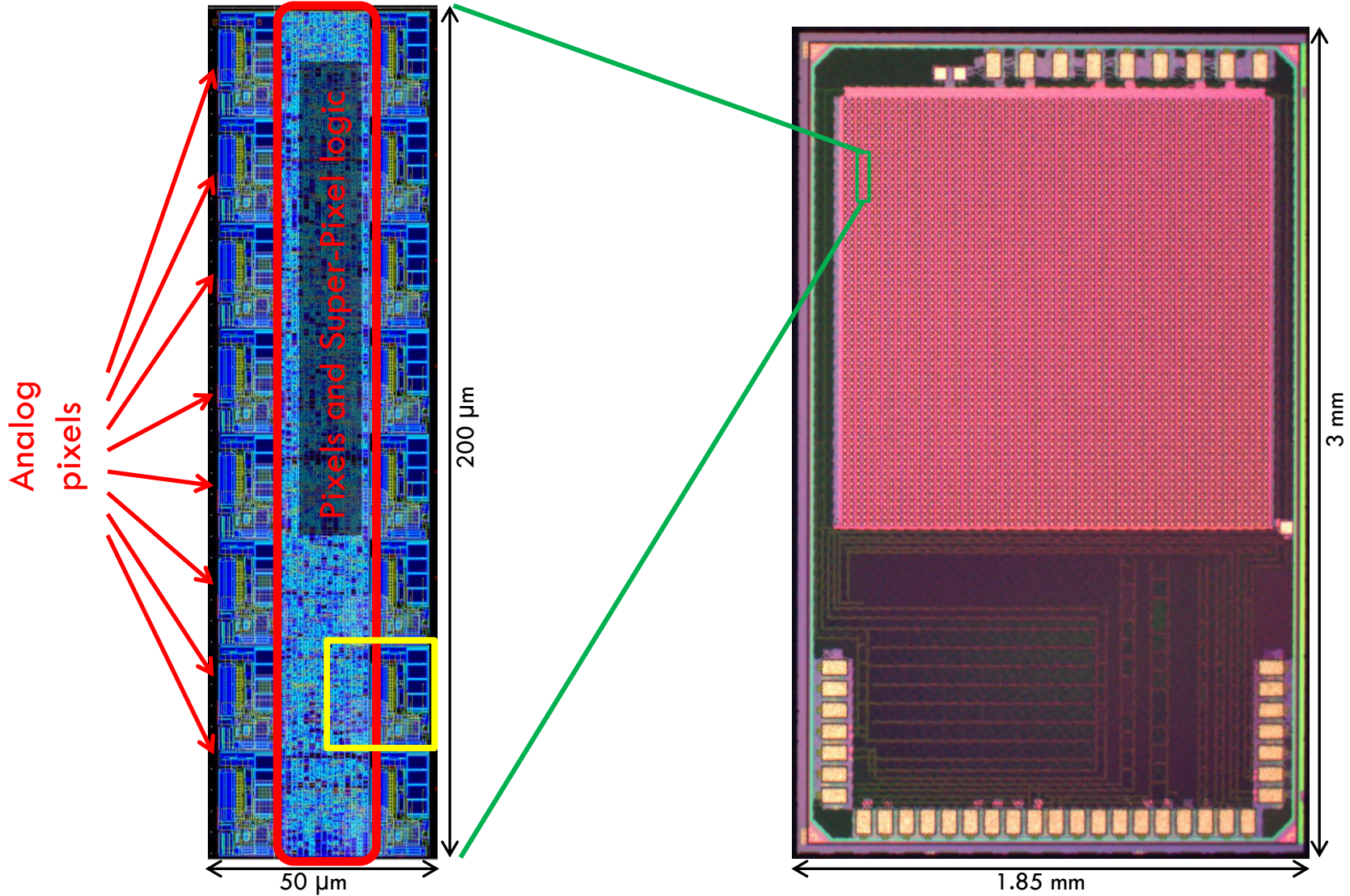
Readout Architecture Comparison

- Readout time for different architectures have been compared.

- 320MHz readout clock (DDR)

- Packet-based readout (red line), zero-compression with pixel, superpixel and column skipping (dotted black line), zero-compression with only pixel skipping (yellow line)
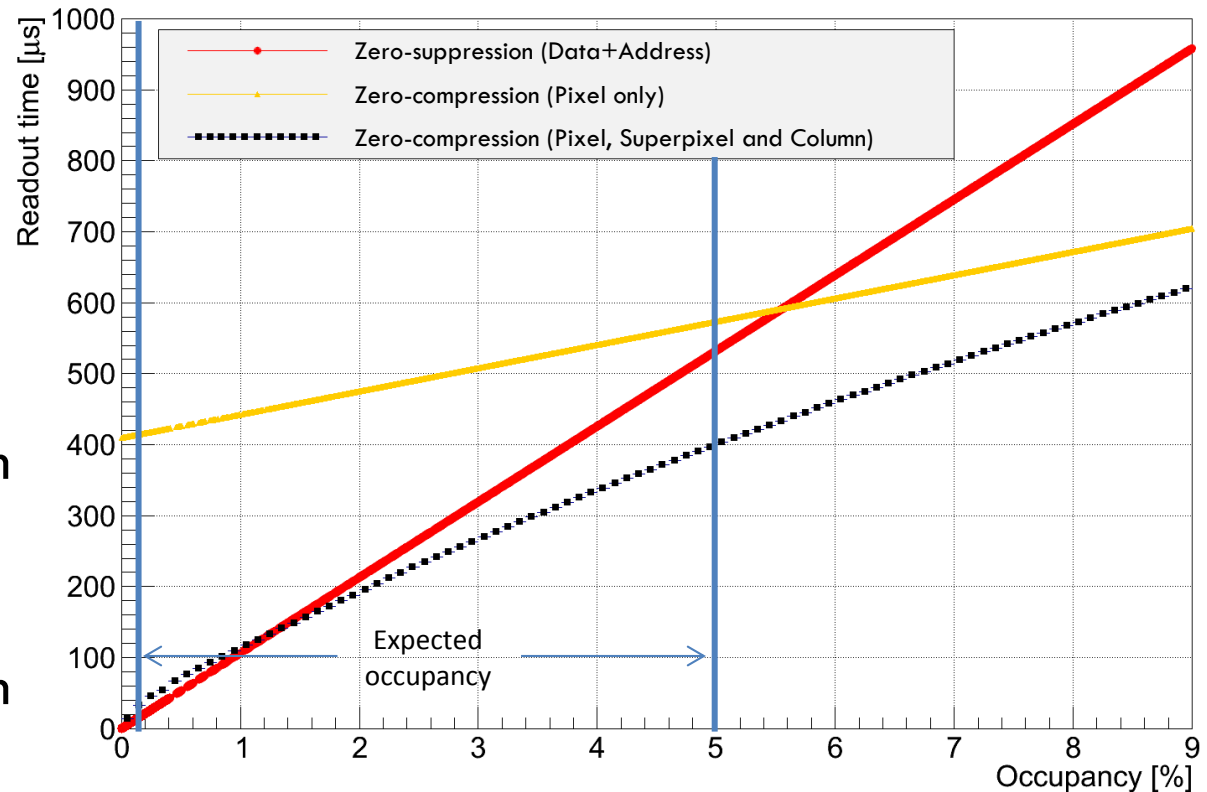
Super-Pixel Layout

Analog pixels

Pixels and Super-Pixel logic

200 μm

50 μm

3 mm

1.85 mm

Outline
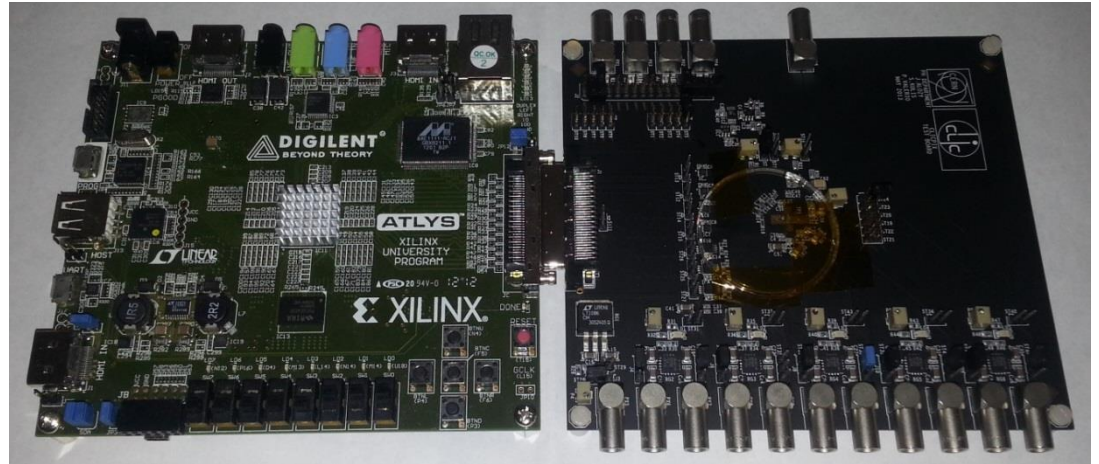
- The CLIC project

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- **CLICpix prototype characterization**

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Functional tests

Using a test setup with an FPGA development board, automated tests could be programmed


- ☐ Configuration data can be sent to the pixel matrix and read back correctly

- ☐ Pixel configuration (calibration DAC code, pixel masking, test pulse injection) works

- ☐ Test pulses can be injected to selected pixels and TOT and TOA counters work

- ☐ Zero compressed acquisition and readout routines produce the expected result and the output stream can be decoded correctly

- ☐ The power pulsing control system works according to specifications reducing the power consumption by more than one order of magnitude

- ☐ The front-end wake-up time is less than 15 µs

TOT measurements

- TOT gain variation is 4.2% r.m.s.
- Tested for nominal feedback current
- Corners have lower TOT gain

Feedback current   0x10 ━ 0x20 ━ 0x30 ━ 0x40 ━ 0x50 ━
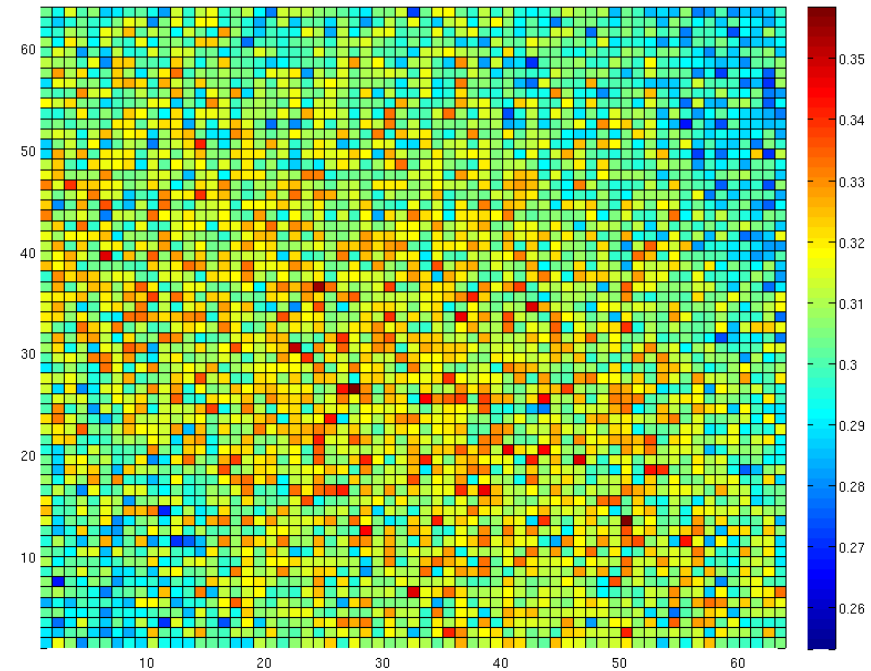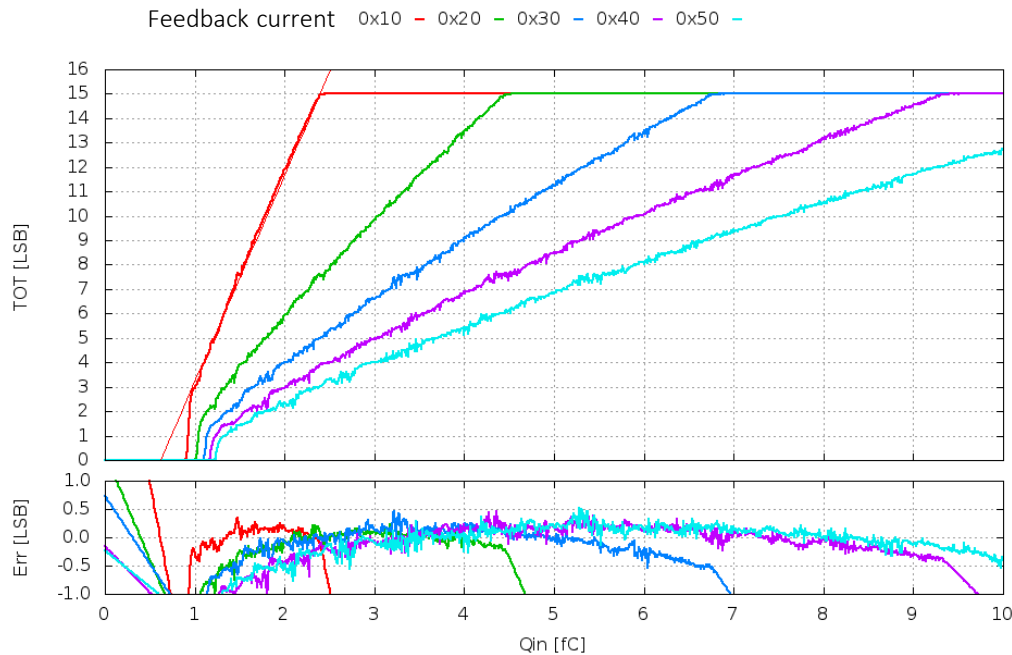
- TOT integral non-linearity for different feedback currents was tested
- TOT dynamic range matches simulations

Threhsold equalization

☐ Routines for equalizing the threshold using the pixel calibration DACs were implemented, finding the noise floor for all pixels

☐ Calibrated spread is 0.89 mV (about 22 e⁻ assuming a 10 fF test capacitance) across the whole matrix
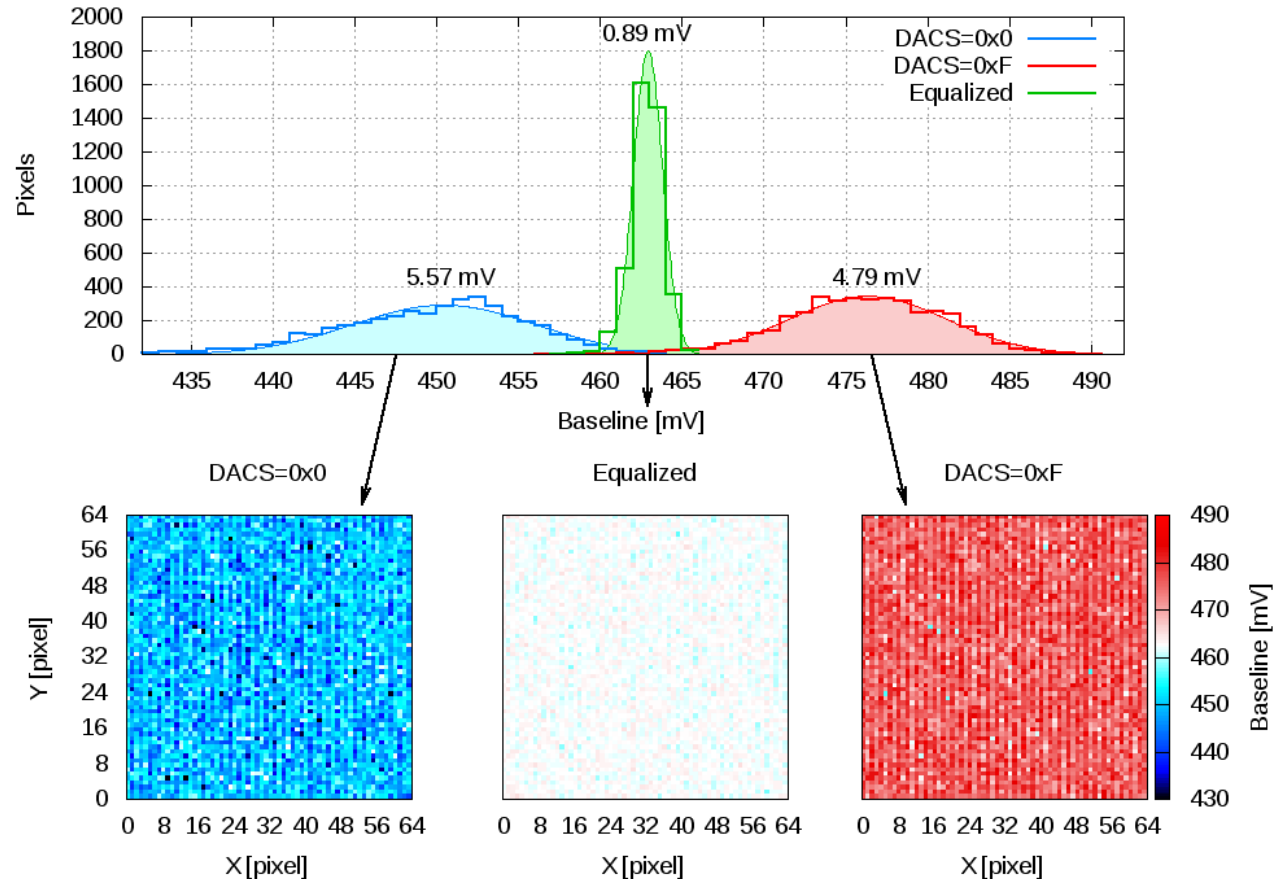
Noise characterization

- ☐ Threshold scans through the baseline voltage were used to calculate the noise floor

- ☐ There is a small pattern effect due to the different routing of pixels in the double columns

- ☐ Average noise is 1.96 mV r.m.s. (about 51 e⁻ assuming a 10 fF test capacitance)
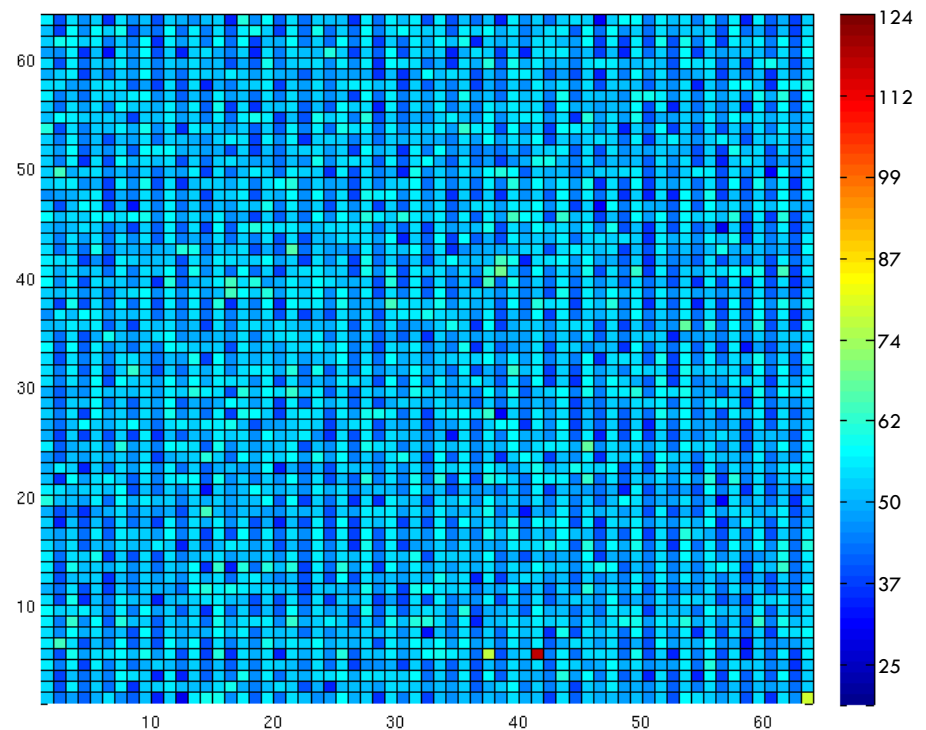
Measurement summary

	Simulations	Measurement
Rise time	50ns	
TOA Accuracy	< 10 ns	< 10 ns
Gain	44 mV/ke$^-$	40 mV/ke$^-$
Dynamic Range	up to 40 ke$^-$ (configurable)	up to 40 ke$^-$ (configurable)
Non-Linearity (TOT)	< 8% at 40 ke$^-$	< 4% at 40 ke$^-$
Equivalent Noise (no sensor capacitance)	~60 e$^-$	~51 e$^-$ (with 10% variation r.m.s.)
DC Spread (uncalibrated)	σ = 160 e$^-$	σ = 128 e$^-$
DC Spread (calibrated)	σ = 24 e$^-$	σ = 22 e$^-$
Analog pixel power consumption (while ON)	6.5 µW	7 µW

Measurements expressed in electrons depend on capacitance values. A nominal value of 10 fF was assumed here for the test capacitor

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Medipix3 TSV project

Objectives :

- Fabrication of a read-out chip with TSV

- Assembly of a particle detector on top of it

- Proof of concept

Project status (January)

- First lot delivered on January 2012 : not in specification

- Third lot delivered on June 2012 : OK

- Dicing & pick out issues @ LETI & VTT

- Dicing solution in october 2012

- CERN tests electrical preliminary testing (14 chips) : OK
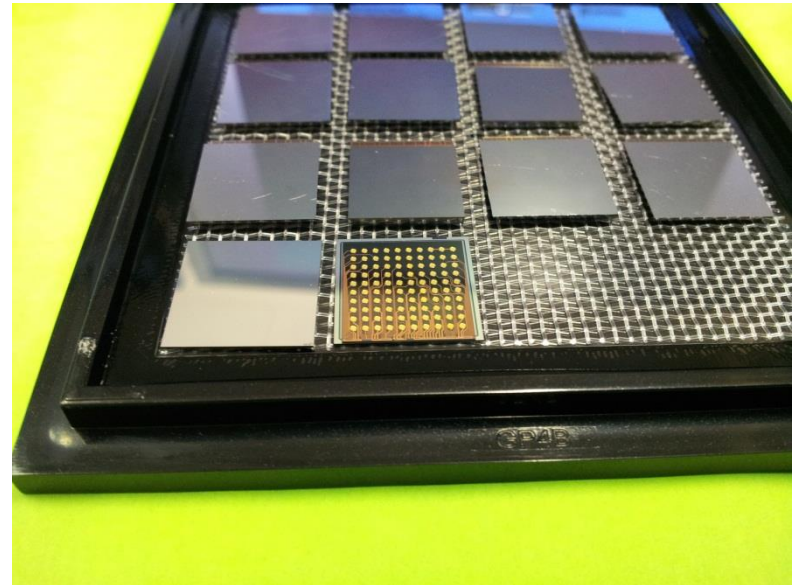
Courtesy of Jerome Alozy

Noise floor comparison

Noise floor comparison: slight difference after the processing

Due to the test setup, the chip temperature was different in the tests

The processed wafers were not chosen among the best ones
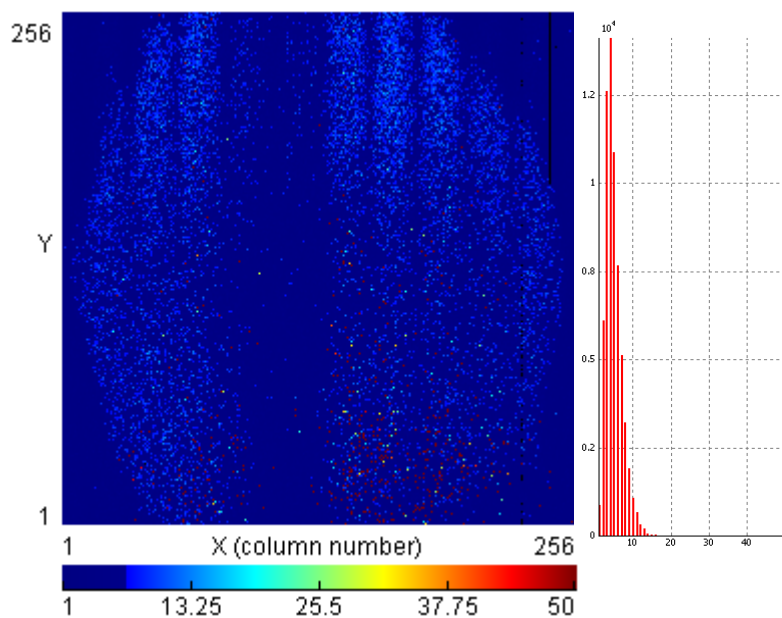

Before TSV
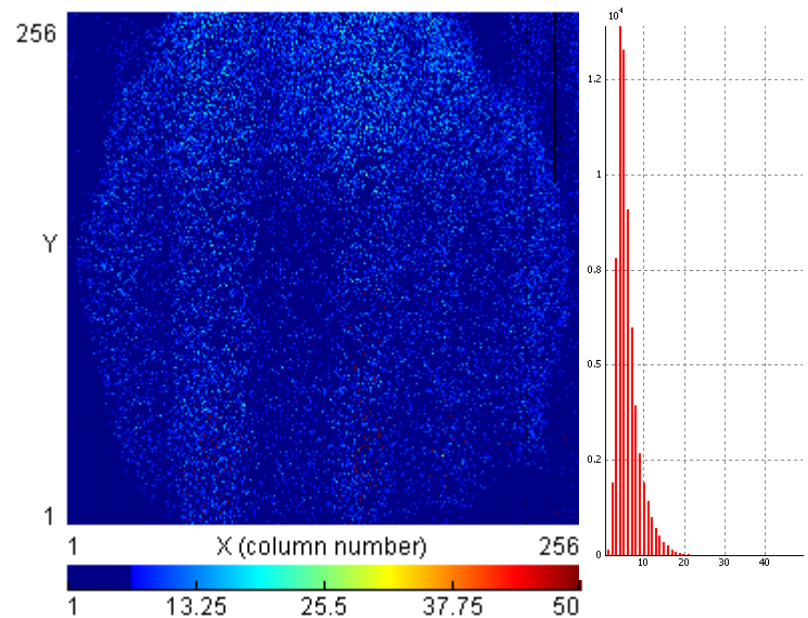
After TSV

MEDIPIX3 TSV (update)

Results are encouraging, but we have a limited number of samples to test.

- New runs of TSV post-process on MEDIPIX3RX wafers instead of MEDIPIX3.0
- 6 tested wafers will be delivered to CEA-LETI in October
- Redistribution layer was just redesigned by CEA-LETI due to TSV layout changes
- "BGA" side footprint will be similar
- Test board will be reused. Test program for Medipix3RX already exist
- Parallel works related to chip on board integration are on-going (soldering the BGA on a PCB)
- PCB temperature profile tests are scheduled this week in CERN assembly workshop to determine the best reflow parameters. Using low temperature fusion Indium balls (this should permit the mounting of MEDIX3RX bump bonded assemblies with sensor – Sn-Pb process)
- 3 more test vehicles PCB will arrive to CERN this week
- TSV assemblies with edgeless sensors currently tested in Advacam, will be delivered to CERN in coming weeks
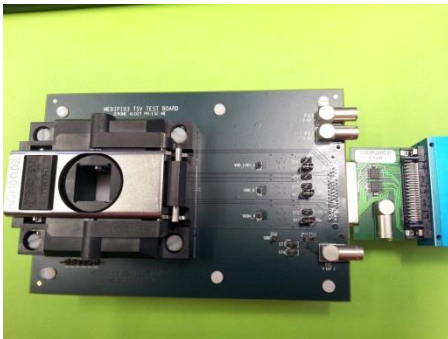
Testboard with socket or chipboard with chip directly mounted on top of it
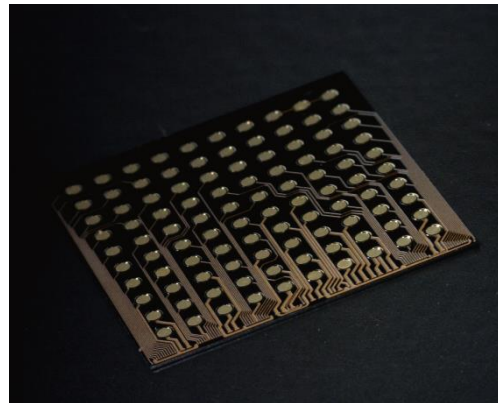
Medipix3.0 TSV processed ("BGA" side)
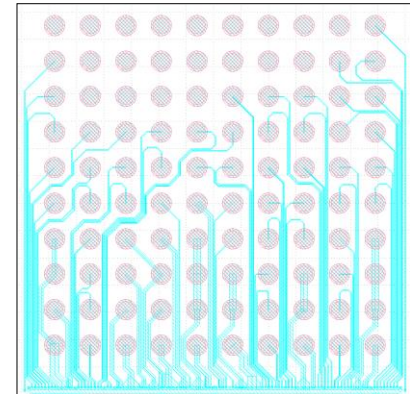
New RDL layer (same pinout)

Outline

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☐ Conclusions

Conclusions

☐ A CLICpix prototype has been designed, fabricated and tested (characterization is still ongoing) using a commercial 65 nm CMOS technology

☐ Main features include 25 μm pixel pitch, simultaneous ToT and ToA measurements and power pulsing capabilities

☐ Measurements closely match simulations
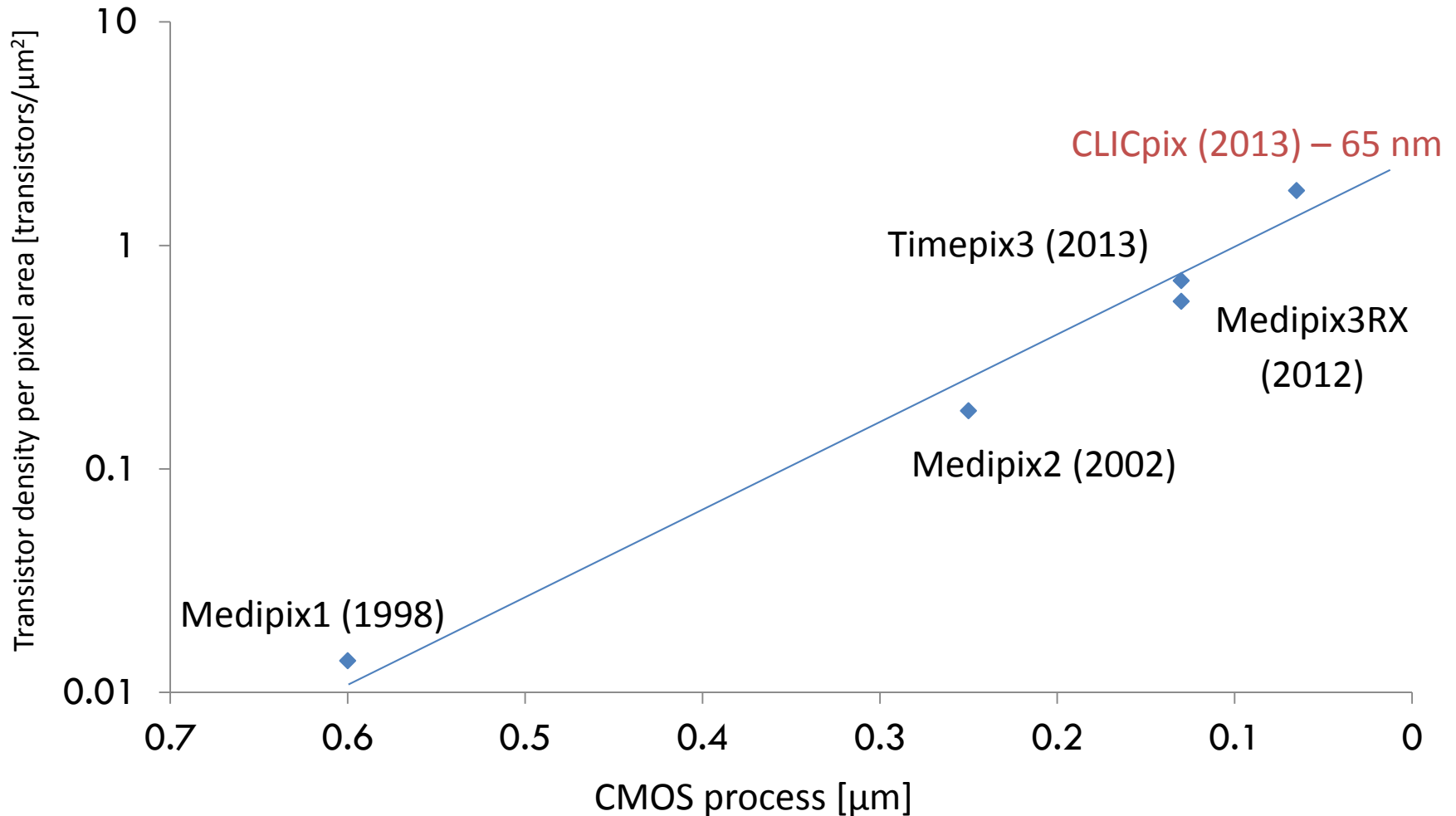
☐ TSV interconnects are being tested for use in existing and future projects

Thanks for your attention

Backup Slides

"Moore's law" for pixel detectors

Analog front-end diagram
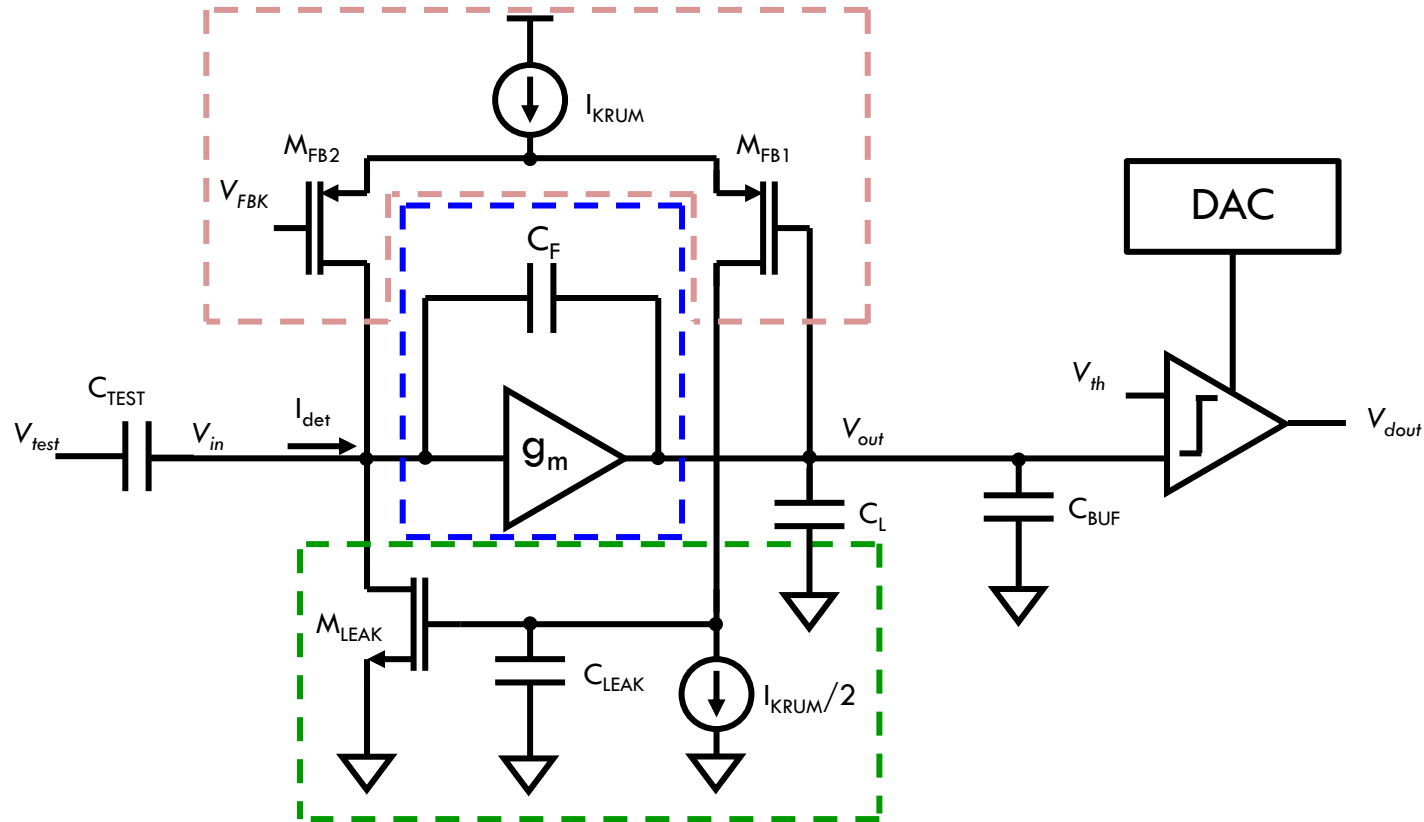
- The front-end uses the Krummenacher architecture, with a single ended preamp, a two-stage discriminator and a binary weighted 4-bit DAC for threshold equalization

- Switches are included to handle pulses of both polarities and to disconnect the test capacitor when it is not used

Timing measurements

- Time over Threshold measures the time the input pulse stays over a fixed threshold
    - It is directly proportional to the amount of charge deposited by a particle and thus its energy

- Time of Arrival measures the relative time in which the pulse was acquired
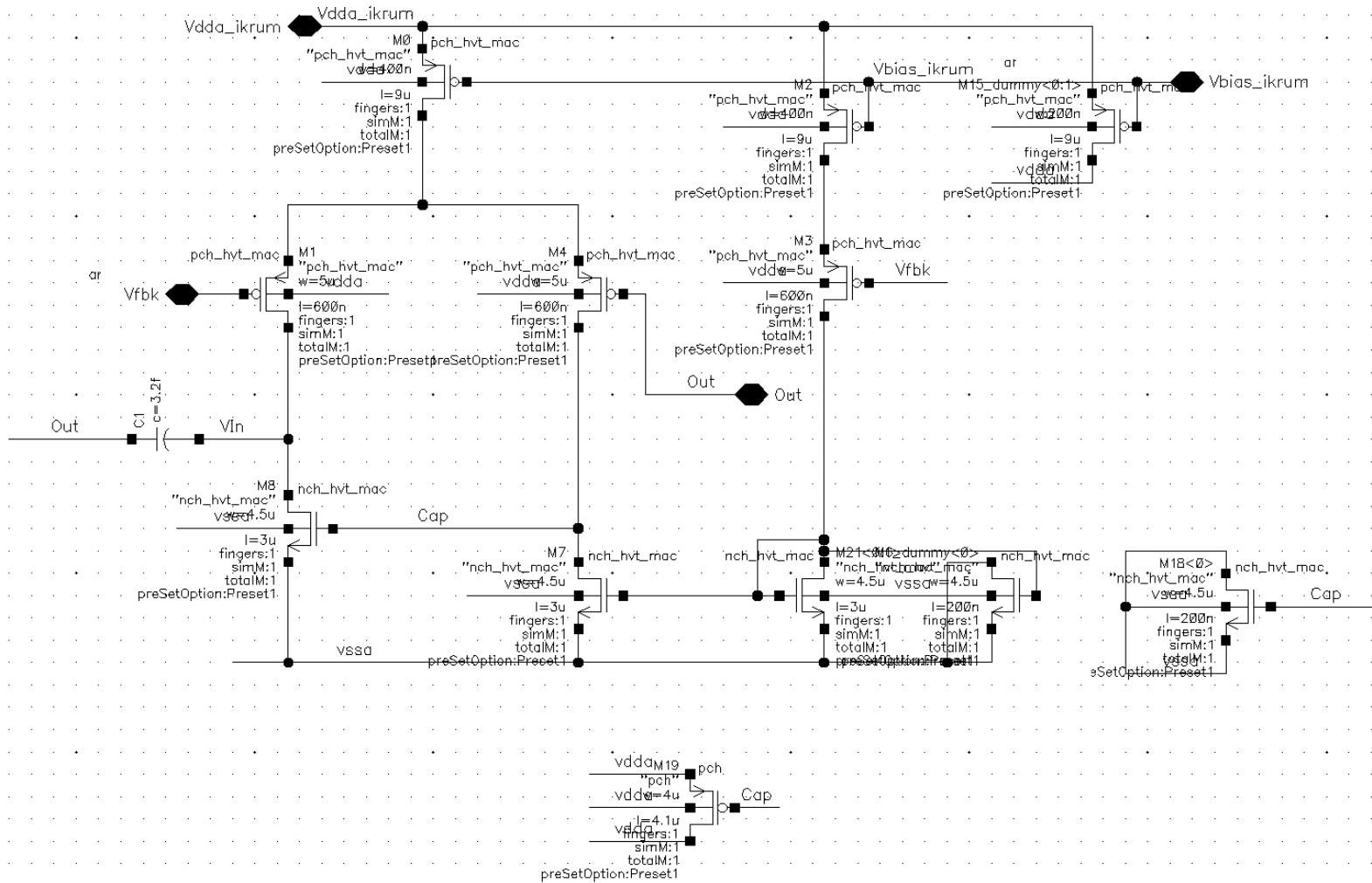   - It is used to identify different particle tracks in a noisy background
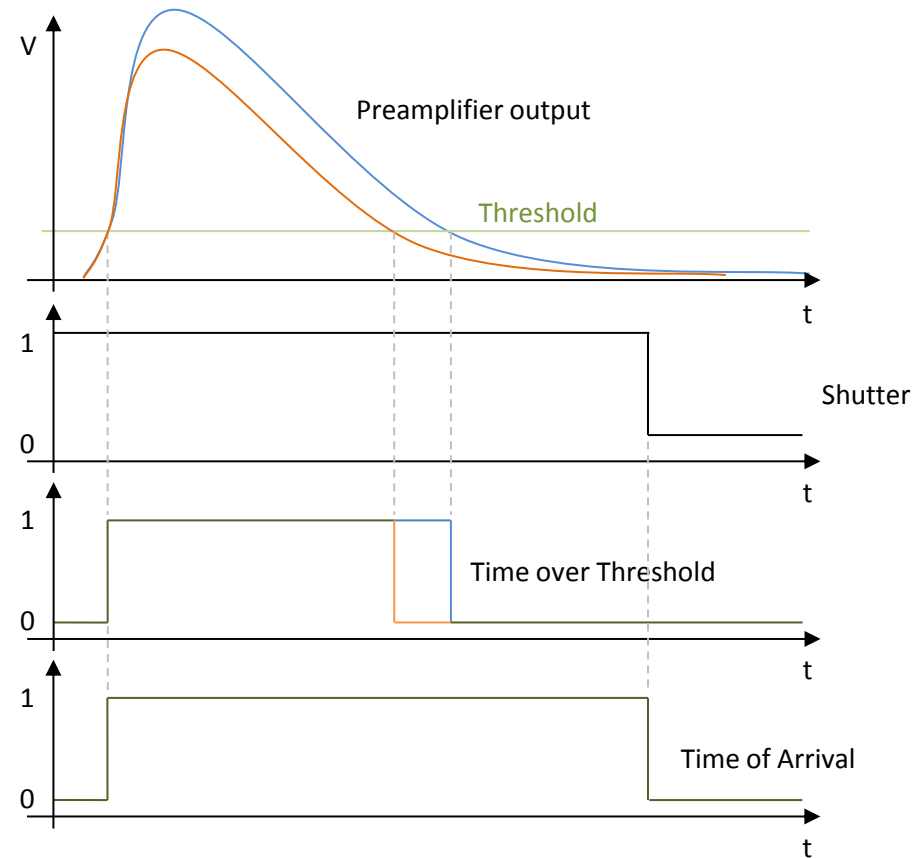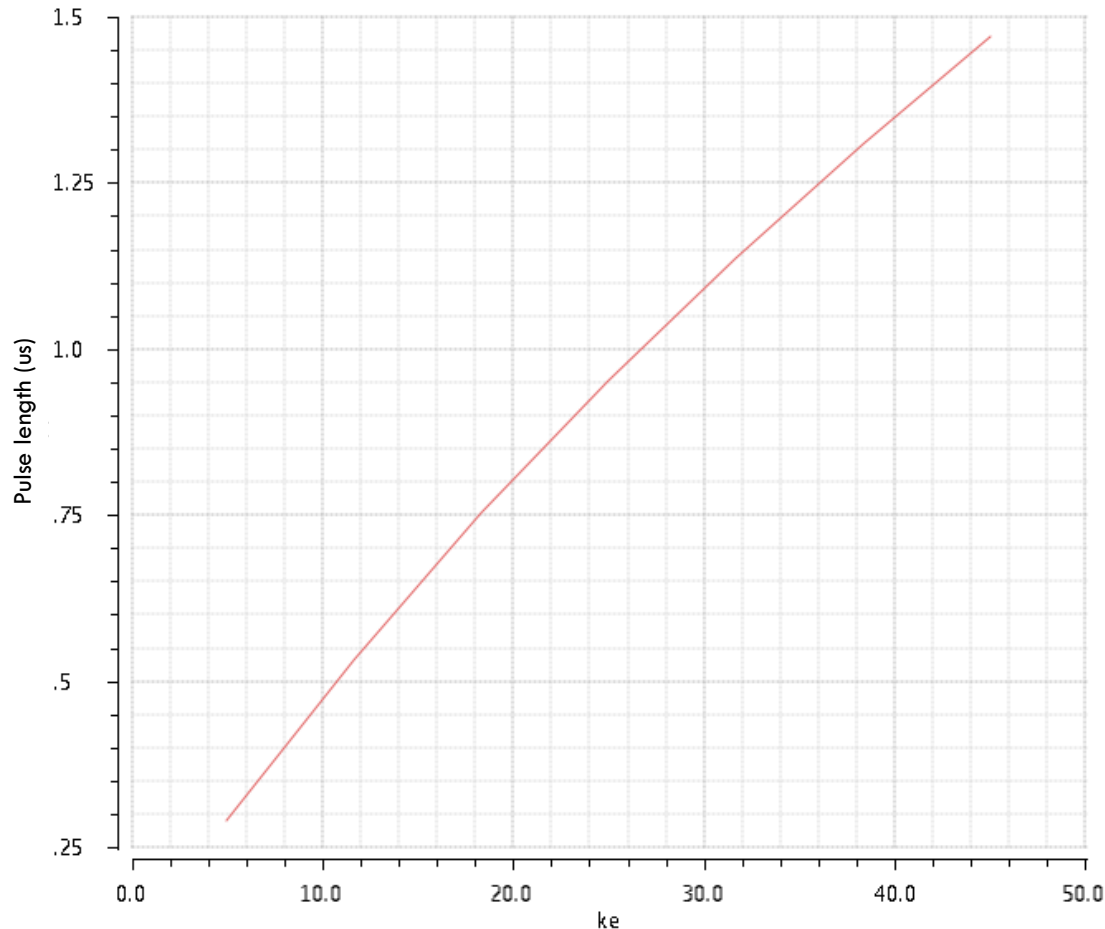
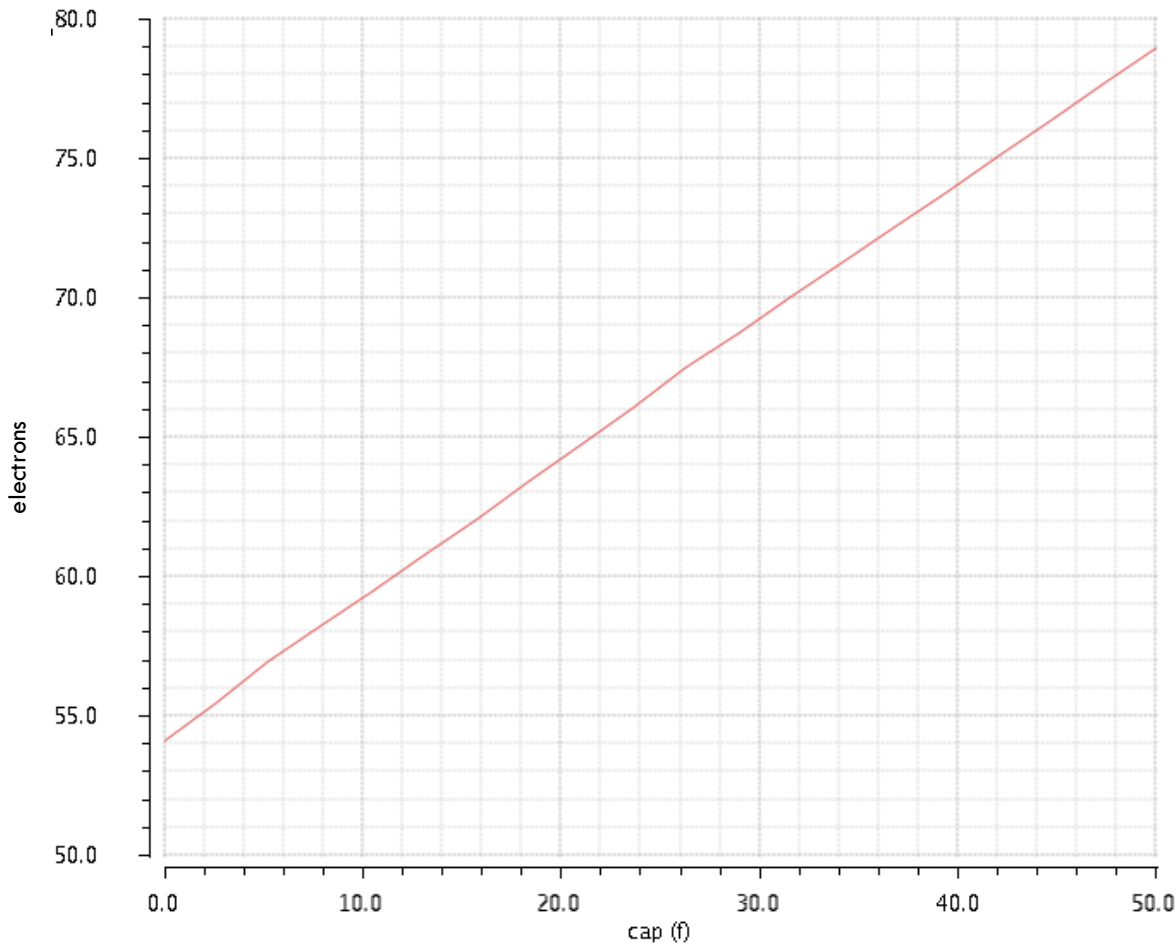# Premplifier schematic
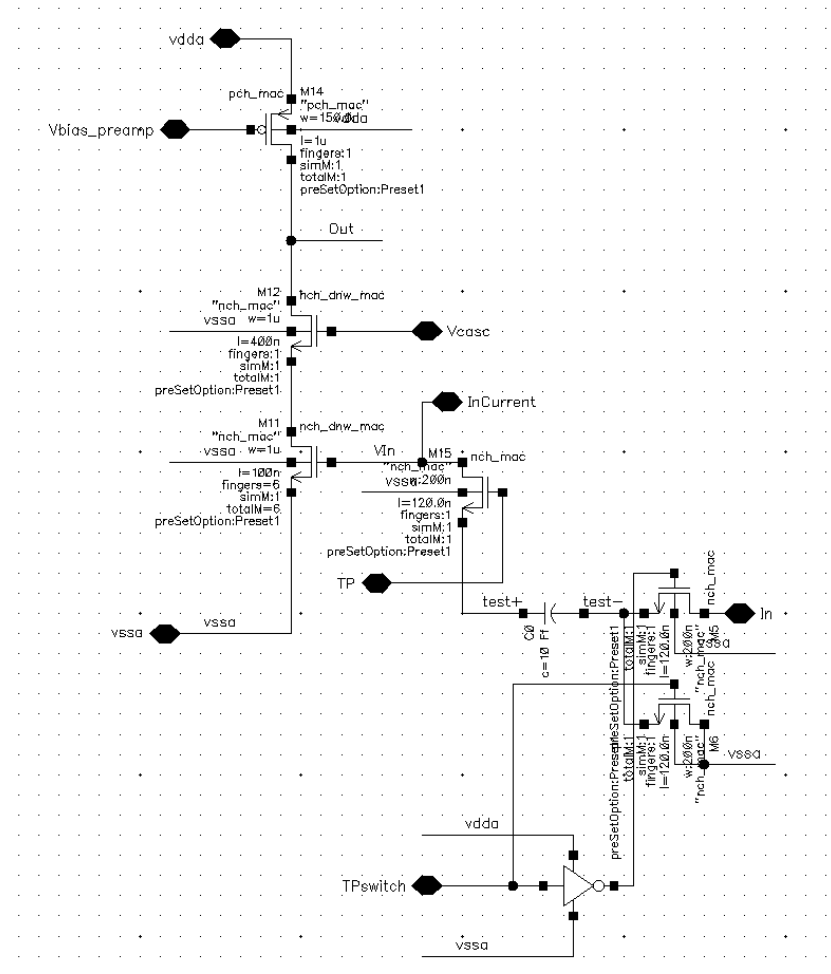
Feedback network schematic

TOT linearity

- The frontend has a linear TOT throughout all its the dynamic range (amplitude saturates with much lower charges)

- Uncertainty in the TOT count (mainly due to mismatch of the Ikrum mirror) is limited to one LSB of the counter
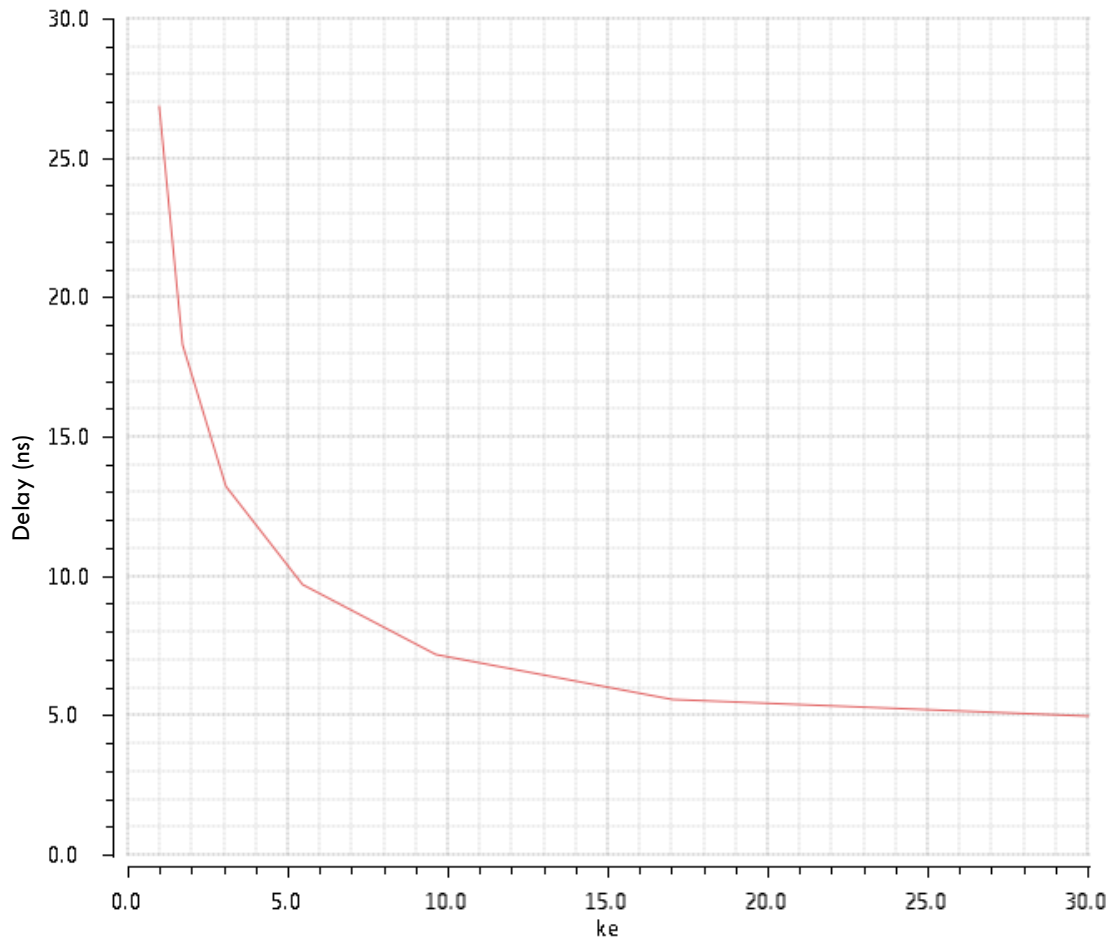
ENC (as a function of input C)

- The capacitances of the pad and the frontend are already included as part of the extracted parasitics

- The frontend show a linear increse of the rms noise by increasing the detector/bonding capacitance
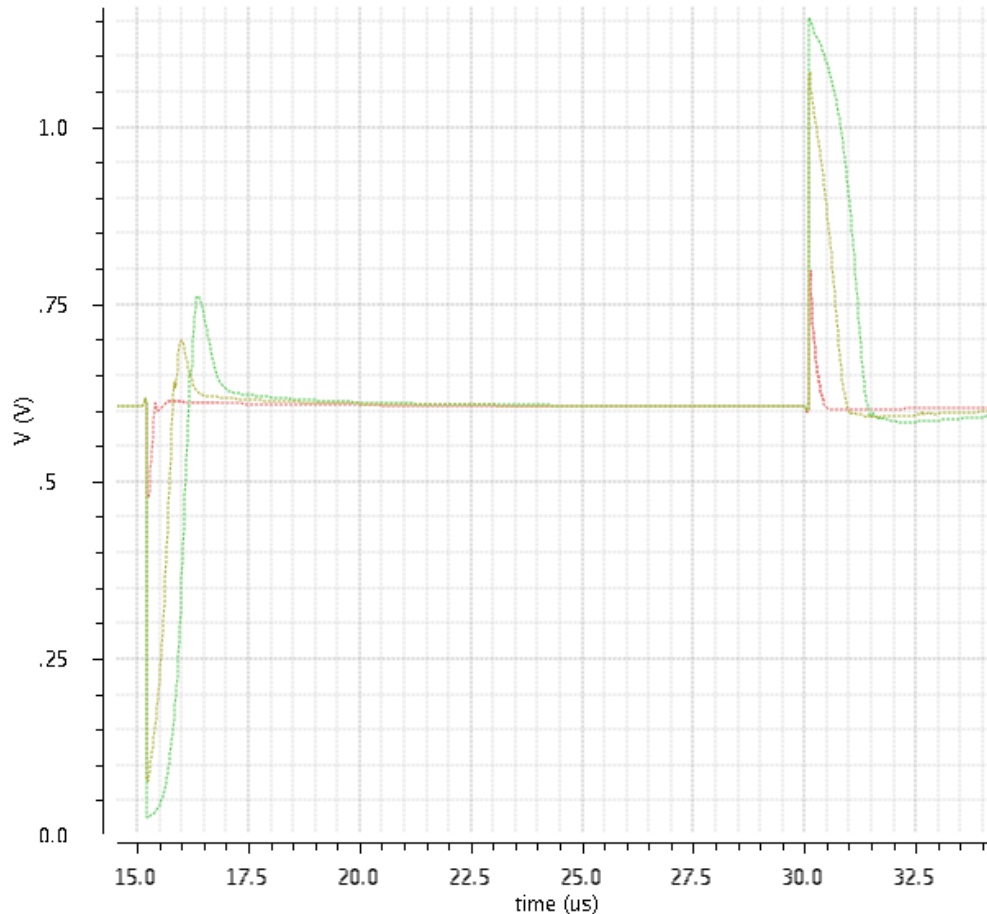
Time walk

- The time walk is reduced for high input charges

- Low charge inputs can produce pulses with a TOT count of 0. The TOT LSB is 2.8 ke$^-$.

- The TOA can be corrected by using the TOT information. Two or three bins are enough to have a 10 ns resolution for all input pulses but those the with a TOT of 0.
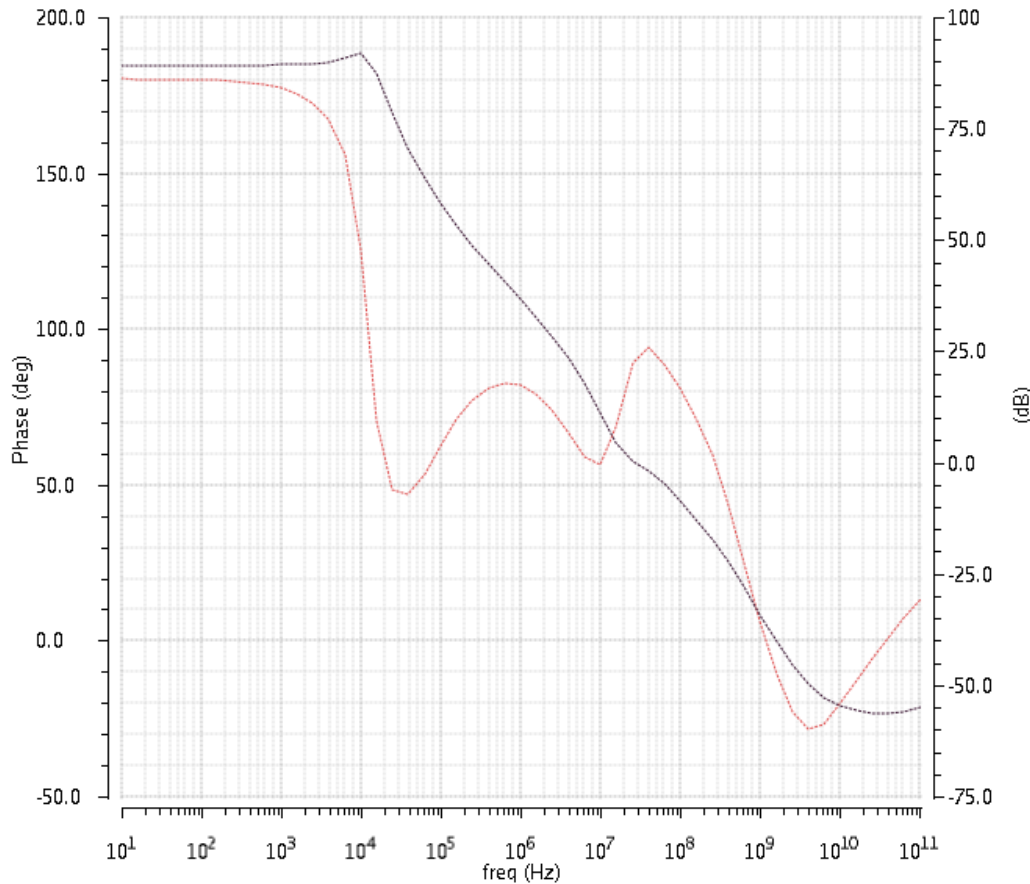
Polarity effect

- The front-end produces pulses with a different shape for different input polarities
- The effect is due to having a small compensation capacitor (for area issues)
- Pulses with different polarities but same energy will give different TOT measurements. This can be compensated by changing the Ikrum value
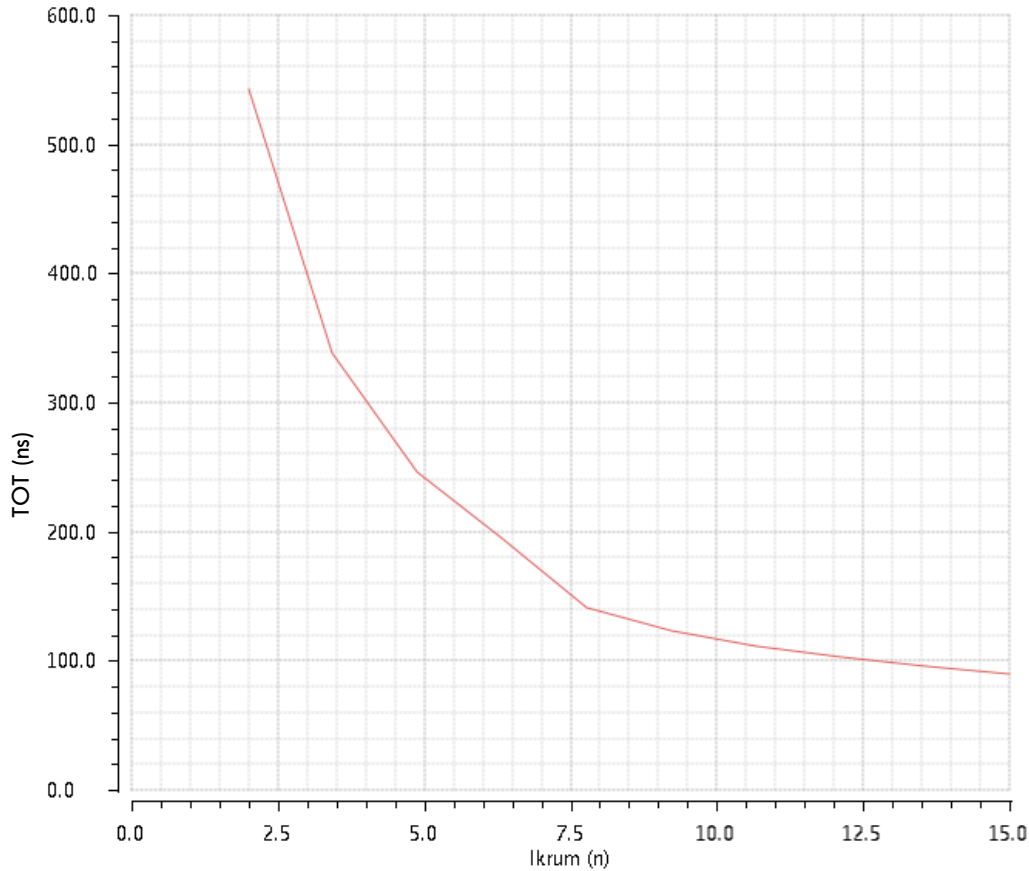
Front-end stability

- Open-loop Bode diagram was simulated (including parasitics) opening the circuit at the input of the preamplifier
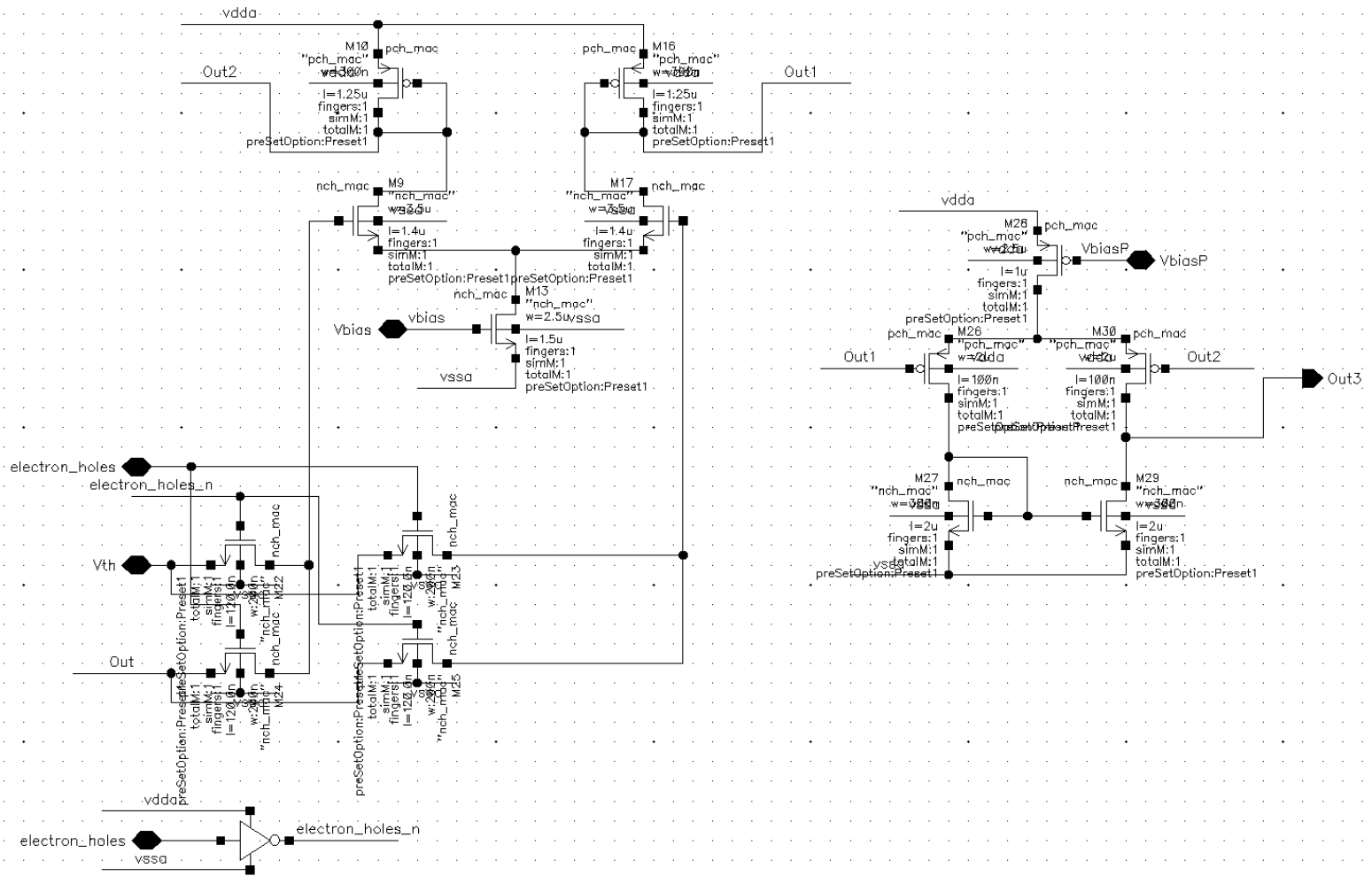- Phase margin is approx. 50 deg

Effect of Ikrum on TOT

- The plot shows the effect of Ikrum on the TOT for a 5 ke$^-$ pulse.
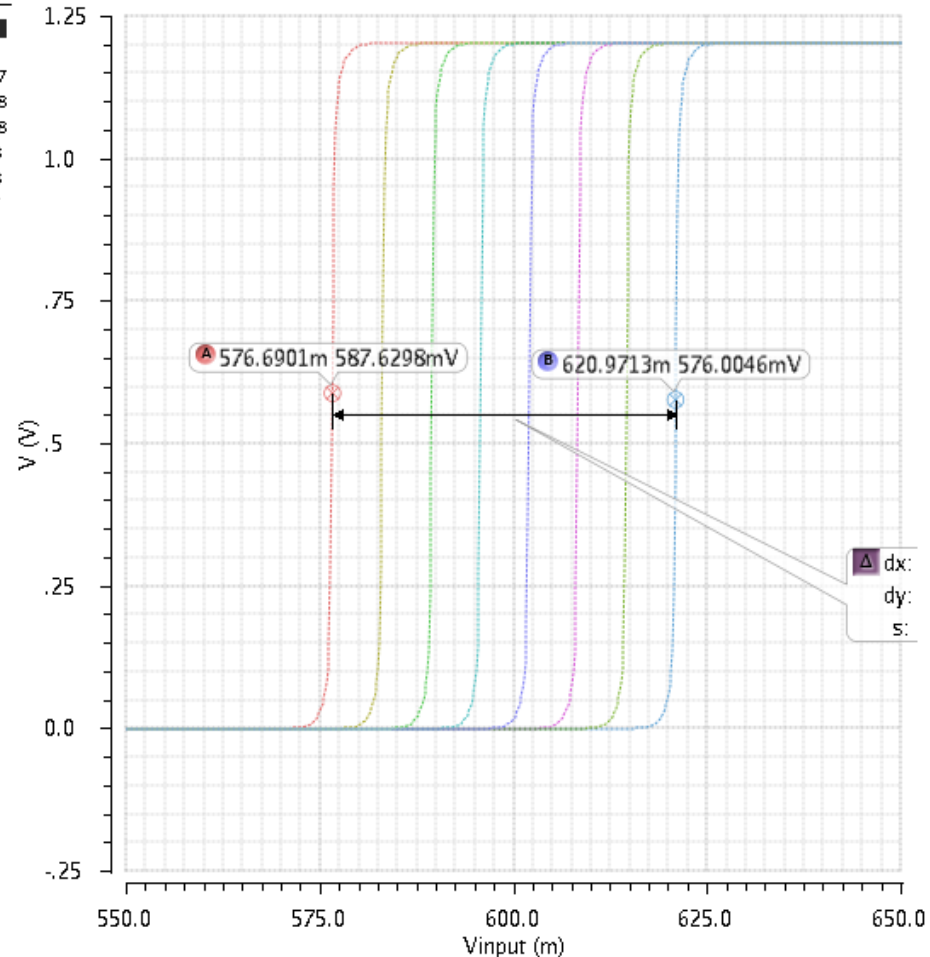
Discriminator schematic

Calibration DAC schematic

Threshold variation due to DAC output

The plot is obtained by making a DC sweep of the discriminator input and checking when its output trips
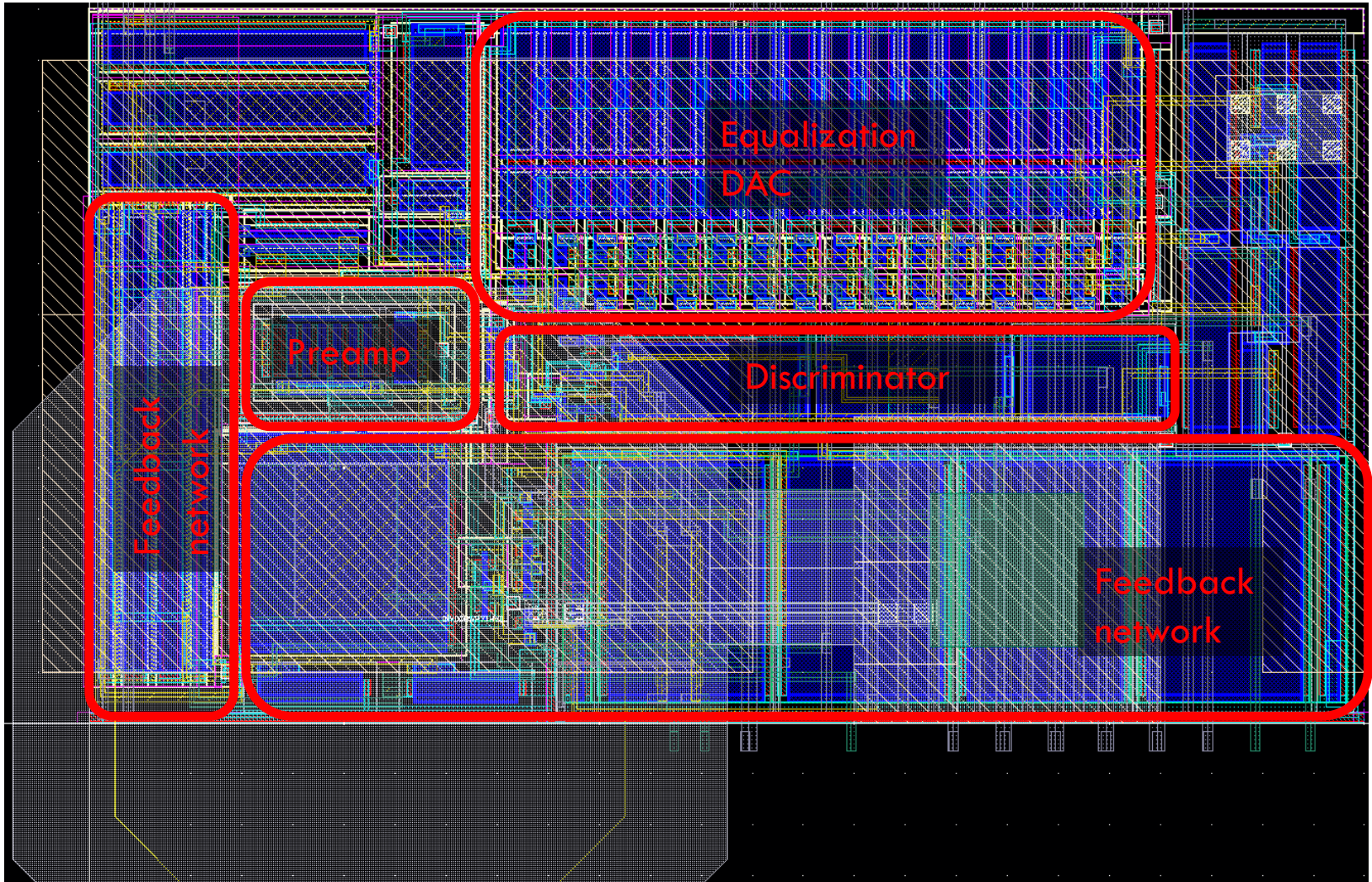
Equalization DAC INL
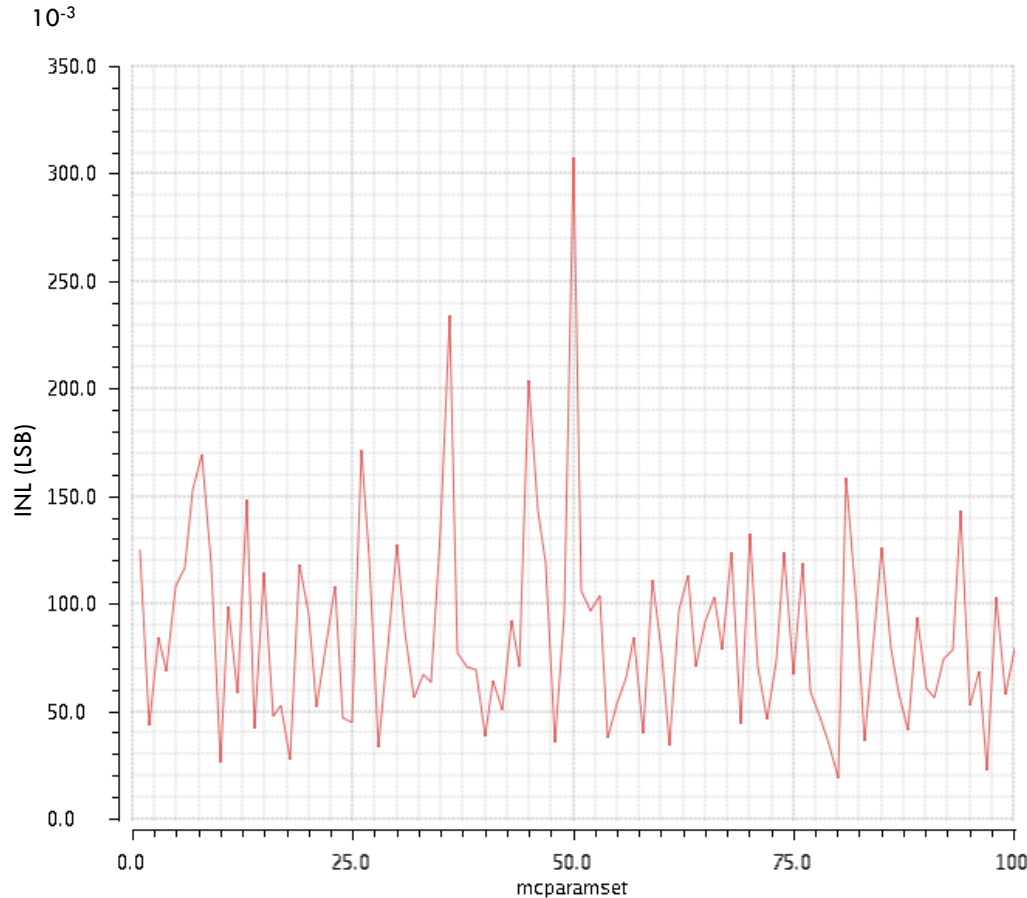
□ INL of the DAC was simulated using Montecarlo simulations with mismatch models (Montecarlo runs with process variations are not possible with TSMC PDK).

Analog Pixel Layout

Power pulsing

- The specific application of the chip requires a very low duty cycle (the chip will acquire data for 156 ns every 20 ms), leaving the possibility to periodically turn off and on parts of the chip

- The main contribution to the power consumption is the analog front-end, which would use $\sim 2W/cm^2$ if run continuously.

- A power pulsing scheme has been implemented allowing to reduce the average power consumption to less than 50 mW/cm^2 (allowing the use of air cooling)

- In order to make the requirements for the power supply more relaxed, each column can be turned on at a different time to gradually turn on and off the chip

- Power pulsing is activated by an external signal and it switches the biasing of the structures which use the most power to a low-power state. During this power saving state the analog power can be switched off entirely

Power pulsing

- The specific application of the chip requires a very little duty cycle (the chip will acquire data for 156 ns every 20 ms), leaving the possibility to periodically turn off and on parts of the chip

- The analog part of the pixel uses too much power by itself. It's necessary to implement a controlled power down when the chip is not acquiring data

- In order to make the requirements for the power supply more relaxed, each column can be turned on at a different time to gradually turn on each chip

Power

20 μs   ~15 μs

Bunch crossing

t
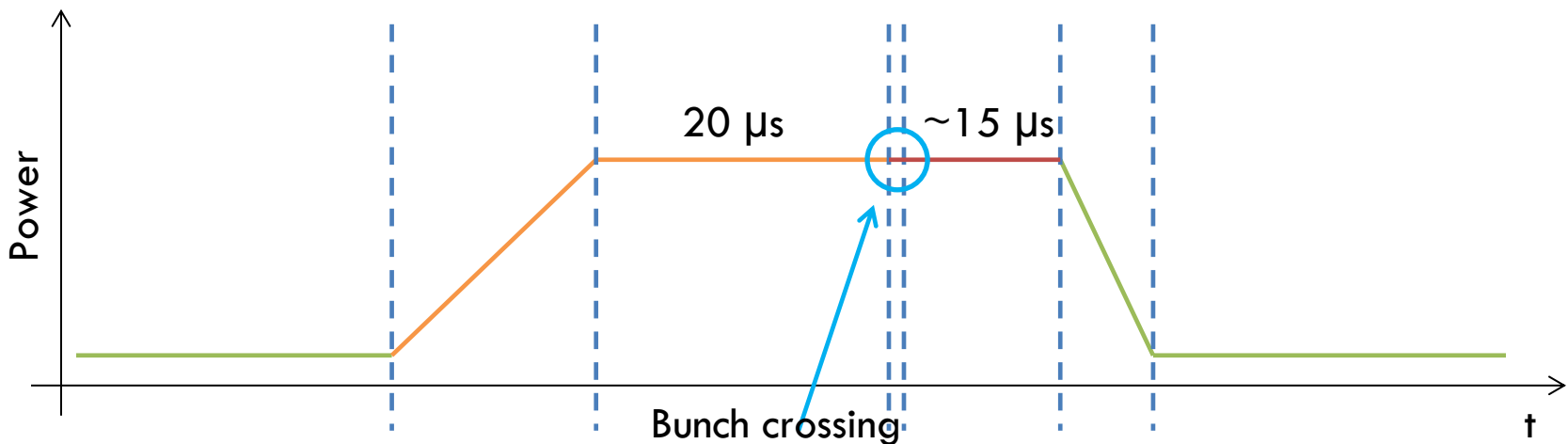
End-of-column functionality

- One end-of-column per each two columns (as they share the digital part)

- The functionalities of the block are managing the clock gating, keep track of the data during readout and provide the array with configuration data.

- The readout of the chip is done serially, one "double column" at a time. Each pixel shifts the data to the next one making the counters work as a long shift register, using a fast readout clock (320 MHz)

- The counters are connected together (and to the pixels directly above and below) to act as a single shift register during the data readout phase.

- Each end-of-column has a state machine that counts the number of pixels being read out (with multiple counters, taking into account skipped pixels and skipped clusters) to be able send a start-reading signal to the next column

Periphery and end-of-column

- A periphery logic with a command register is implemented to control all the features of the chip

- Columns are read serially and programmed in parallel

- DACs to generate reference voltages are included. An external absolute voltage reference is needed due to the lack of a band-gap block.

- A power pulsing and clock gating scheme has been implemented allowing to reduce the average power consumption to less than 50 mW/cm^2 (allowing the use of air cooling)
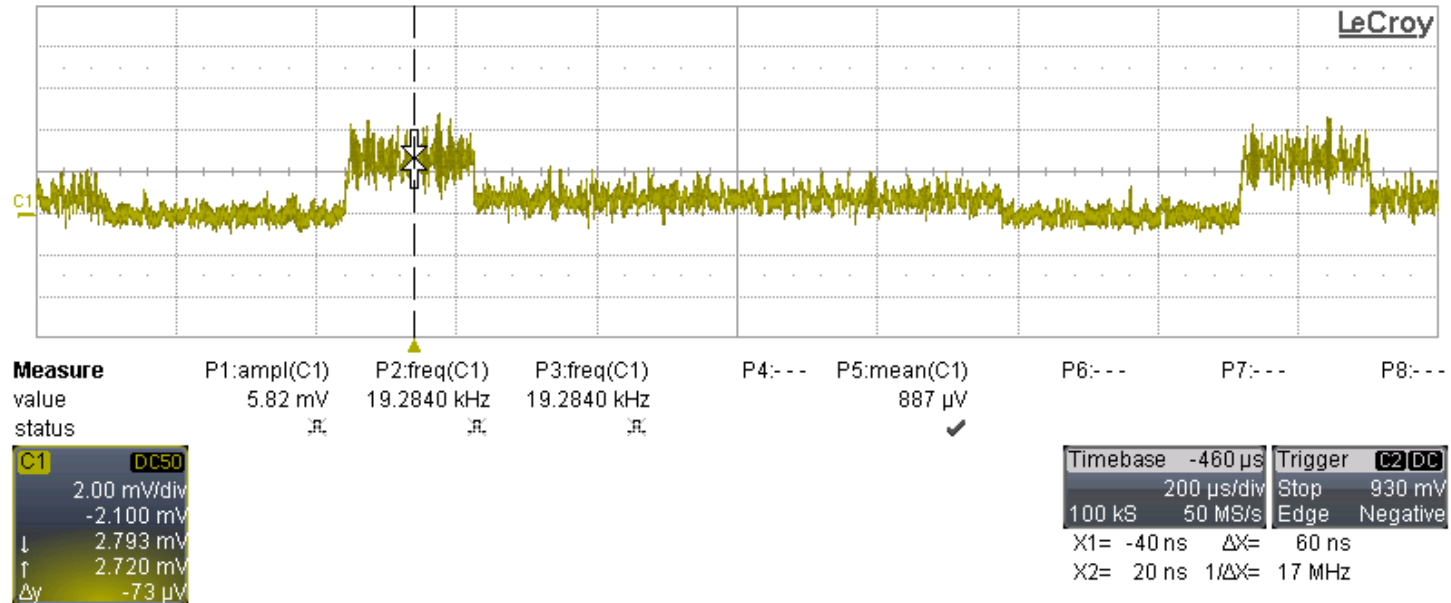
Other analog tests
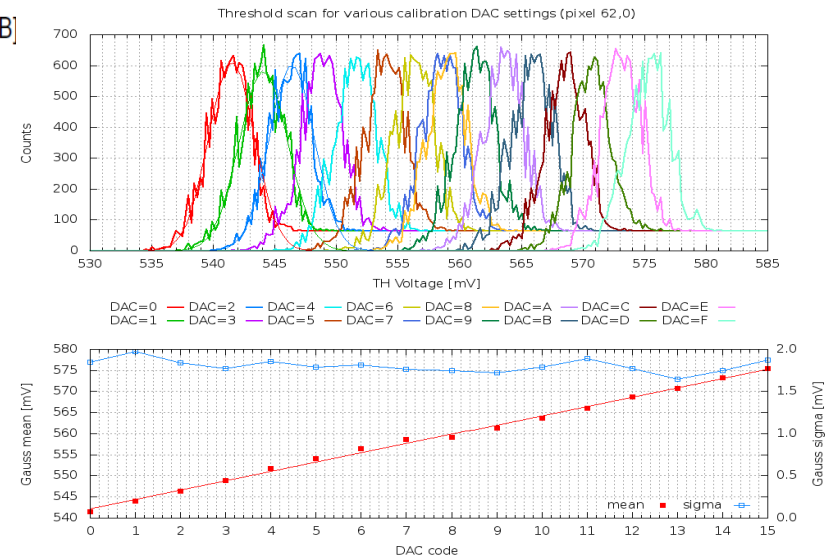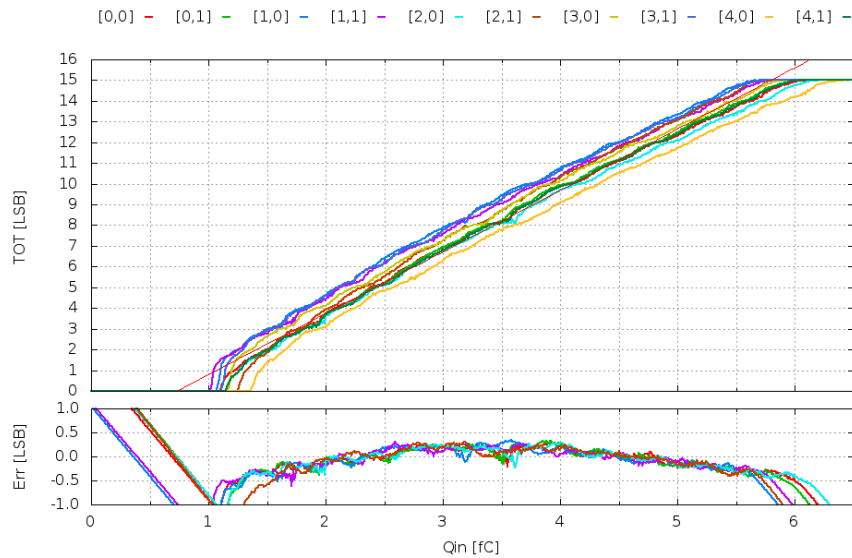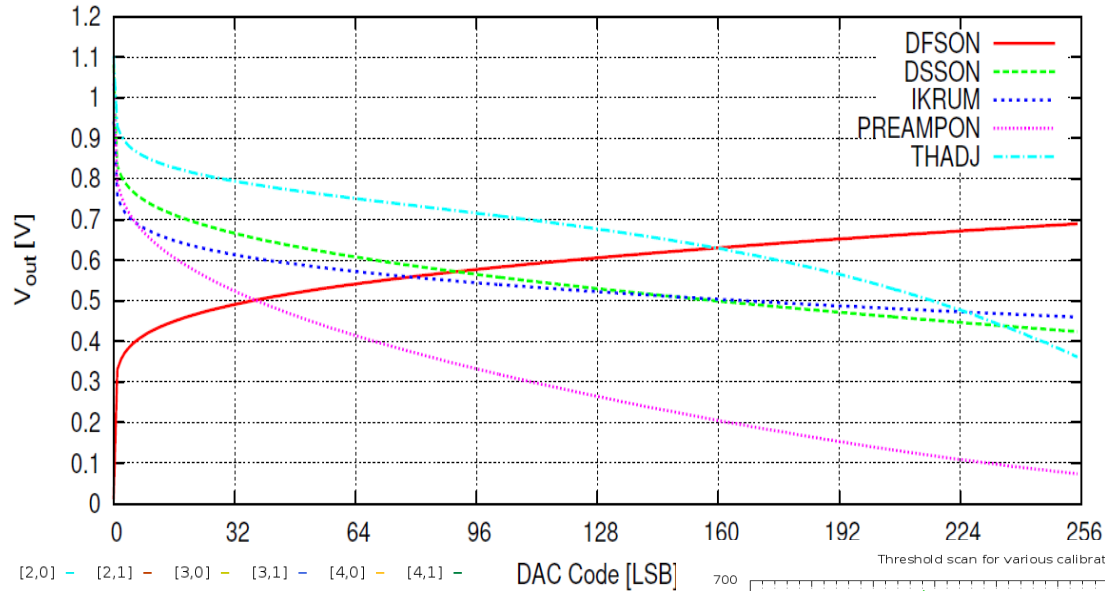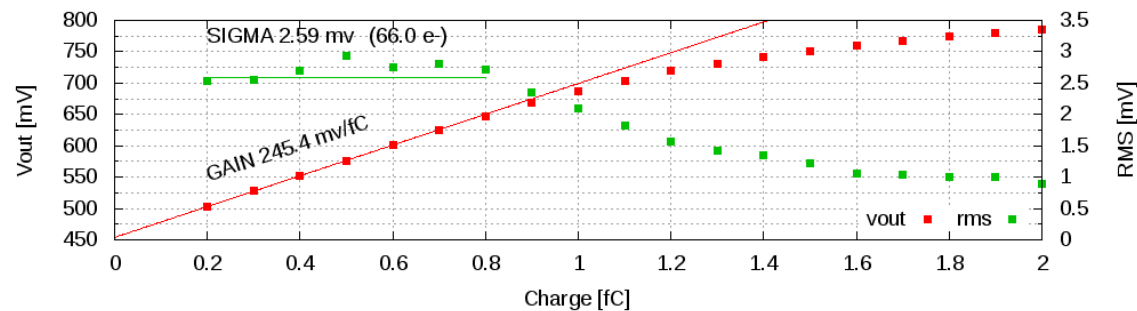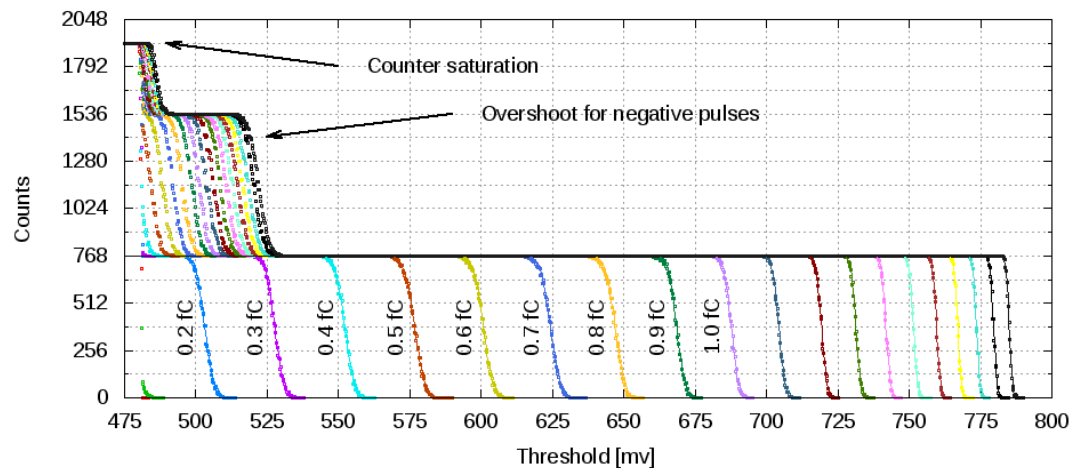
Digital power consumption

- Change in power consumption between acquisition, readout and idling can be seen
- Total power consumption of the digital part is lower than 4 mW during readout
- Average power consumption of the digital part is lower than 1 mW

Other analog tests

- Noise and gain measurements were performed on some pixels injecting test pulses, with results closely matching simulations

- Results are to be considered preliminary, noise sources are being investigated

Periphery blocks tests

- Periphery DACs were tested
- Their characteristics were found to be consistent with simulations within the uncertainties due to process variations
- The variation of power consumption changing the biasing currents of analog blocks was measured and it matched expected values
- The power pulsing control system works according to specifications reducing the power consumption by more than one order of magnitude
- The power-on and power-off times can be programmed
- The front-end wake-up time is less than 15 μs