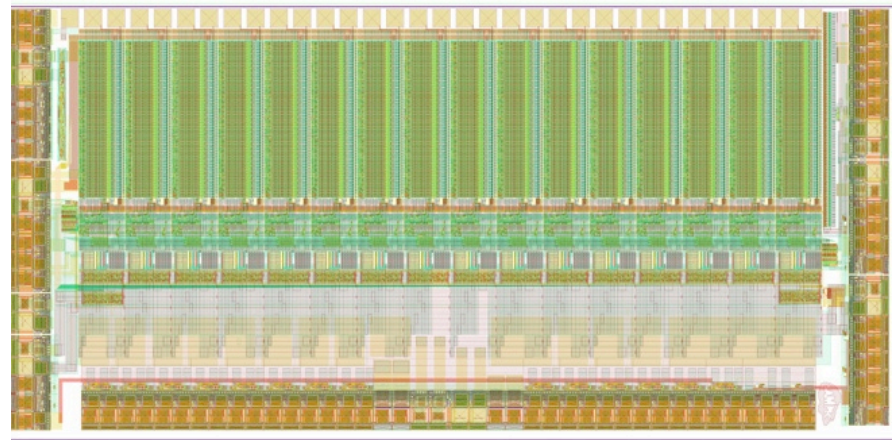


FROM RESEARCH TO INDUSTRY



The SamPic readout chip

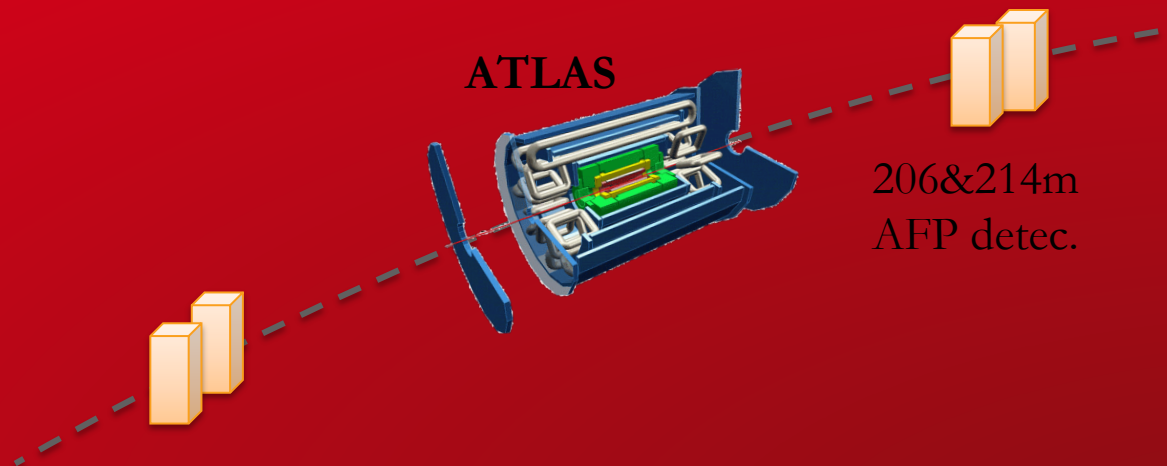
Phd Thesis work supervised by E. Delagnes and C.Royon



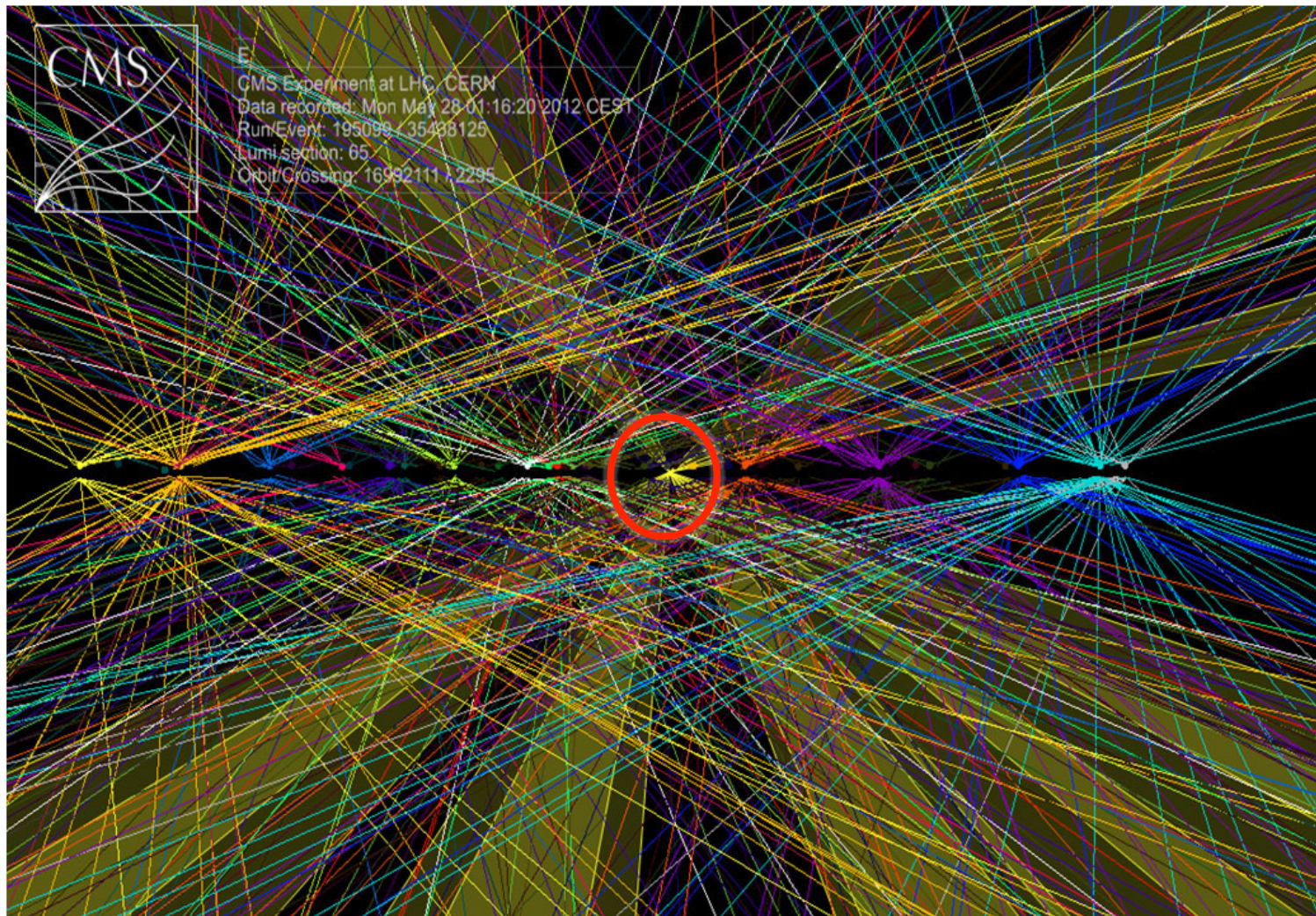
LHC Working Group on Forward Physics and Diffraction | Hervé Grabas

27 AUGUST 2013

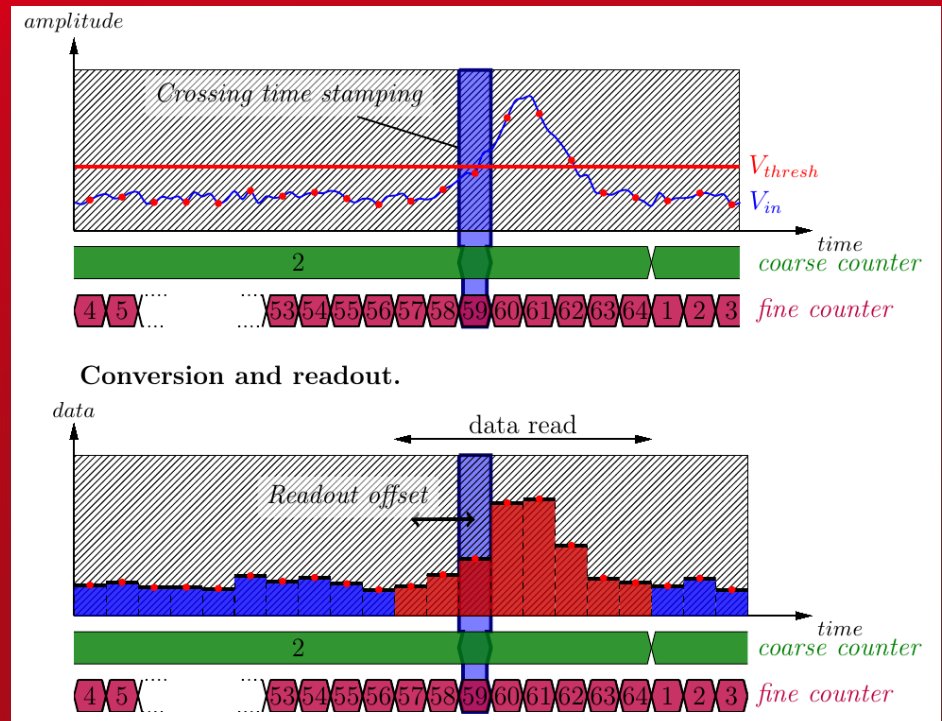
INTRO: MEASURE PICOSECOND TIME OF FLIGHT IN PARTICLE DETECTORS



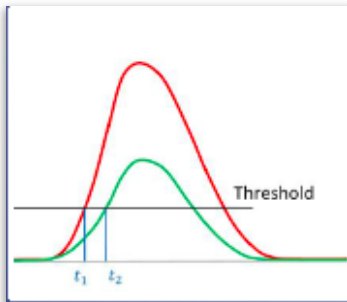
PILE-UP SUPPRESSION



TIME MEASUREMENT

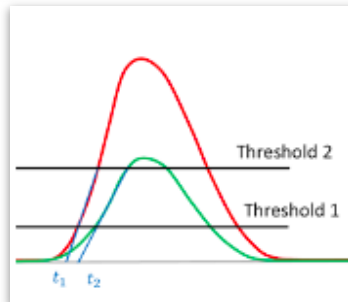


Single threshold



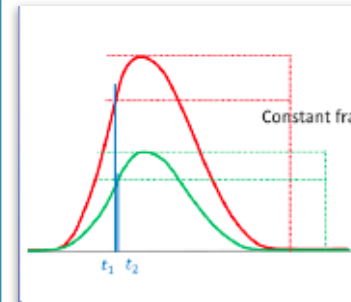
Advantage of simplicity. Poor results

Multiple threshold



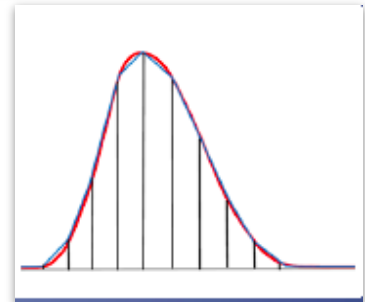
Basically interpolation on the rising edge.

Constant fraction



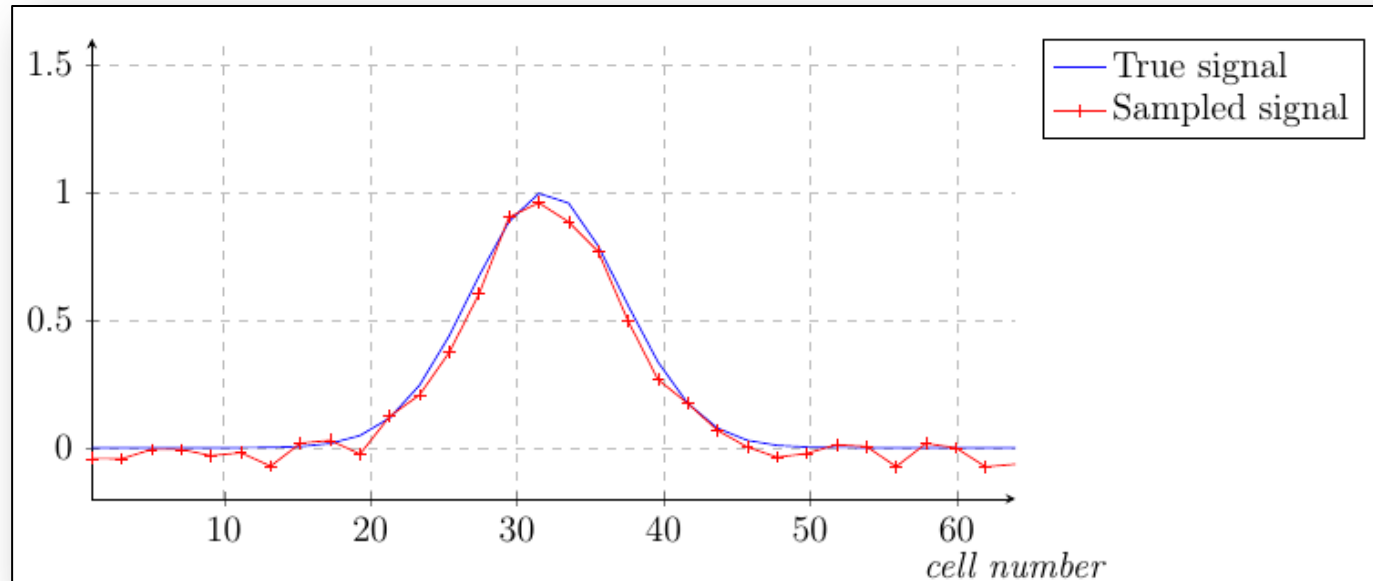
Complicated hardware. Relatively good precision.

Sampling



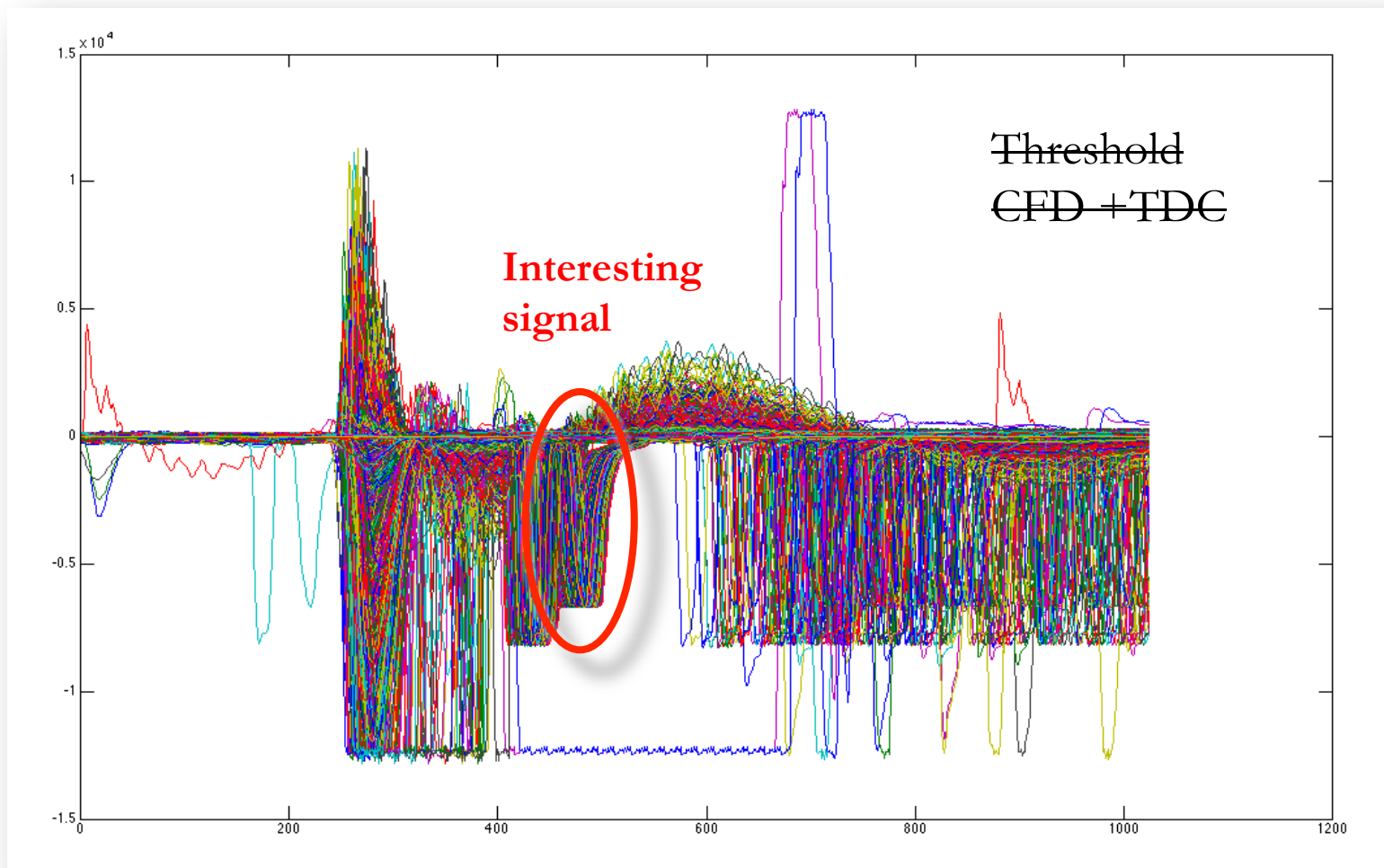
All digital algorithm possible: Mean square, Cross-correlation, ...

TIME DELAY ESTIMATORS



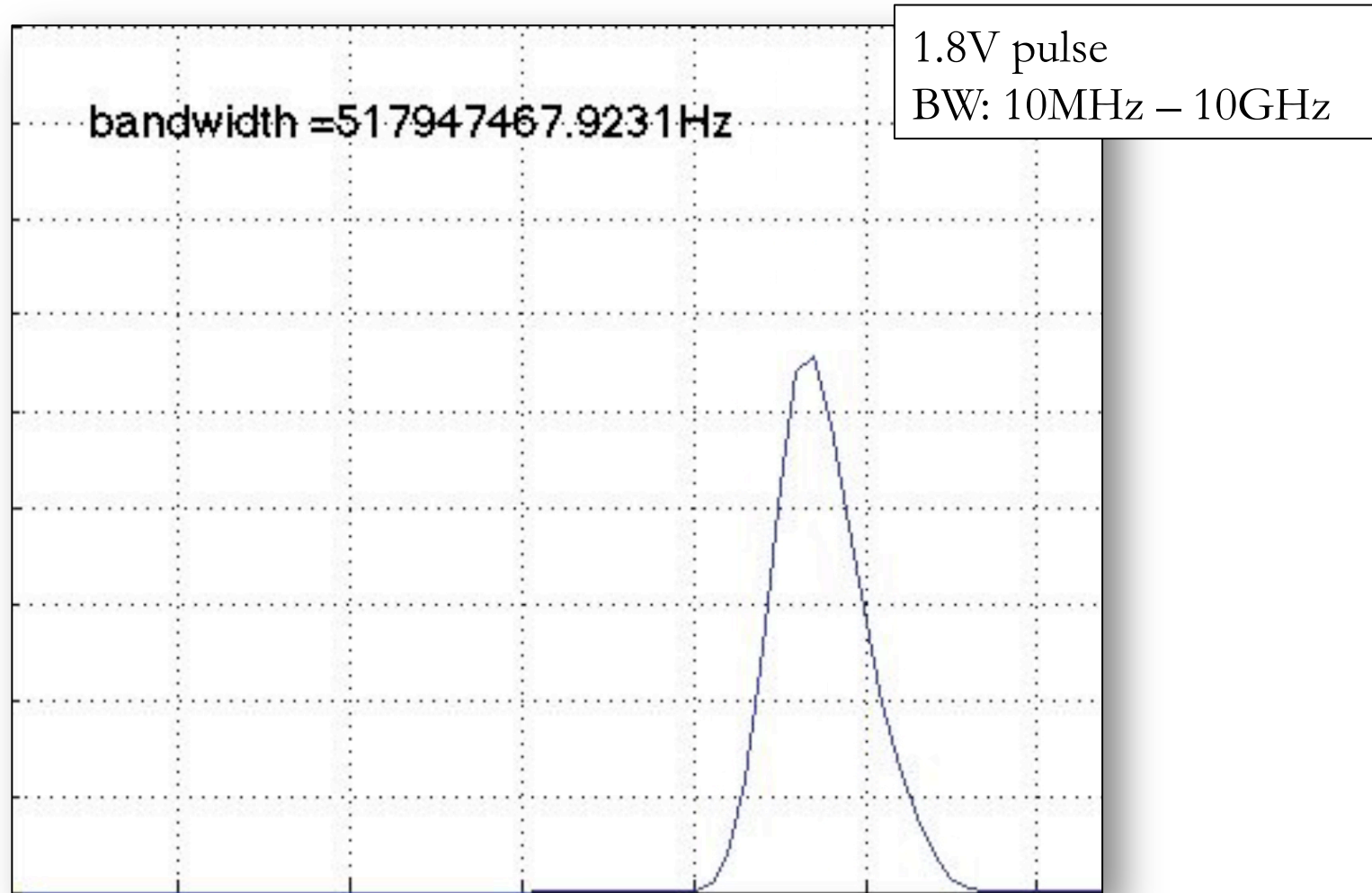
- Normalized cross-correlation
$$c[k] = \frac{\sum_0^{N-1} s[i] \times t[i - k]}{\sqrt{\sum_0^{N-1} s[i]^2 \times \sum_0^{N-1} t[i]^2}} \quad k \in [-N + 1..N - 1]$$
- Sum of absolute difference
$$a[k] = \sum_0^{N-1} |s[i] - t[i - k]| \quad k \in [-N + 1..N - 1]$$
- Least mean squares
$$l[k] = \sum_0^{N-1} (s[i] - t[i - k])^2 \quad k \in [-N + 1..N - 1]$$

WHY SAMPLING?

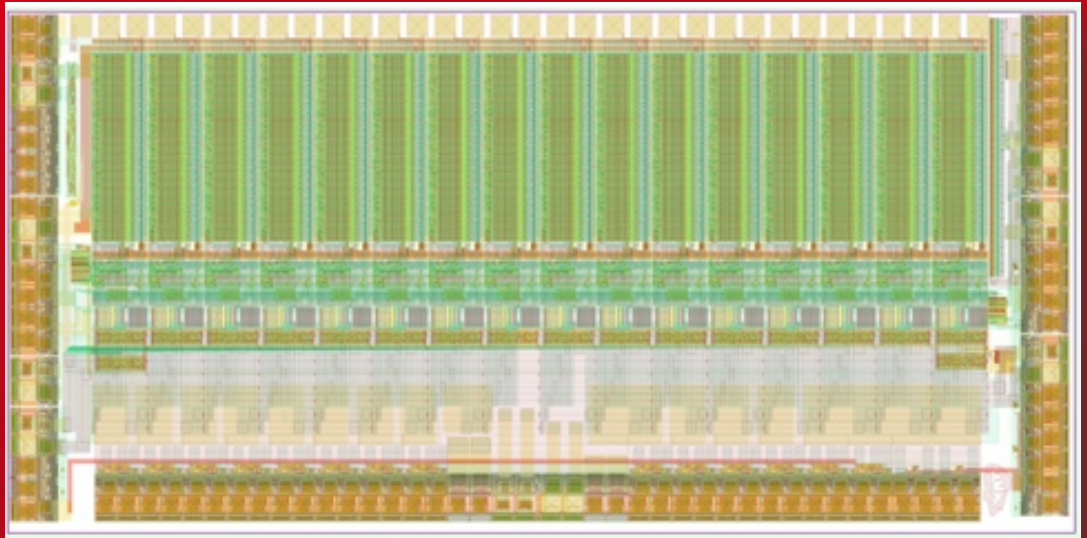


SPS CERN test beam – October 2012

WHY HIGHER BANDWIDTH?



THE SAMPIC CHIP



SamPic is a CMOS chip designed to read the forward timing detectors of ATLAS. **S**ampler for **P**icosecond time pick-off.

R&D financed by P2IO



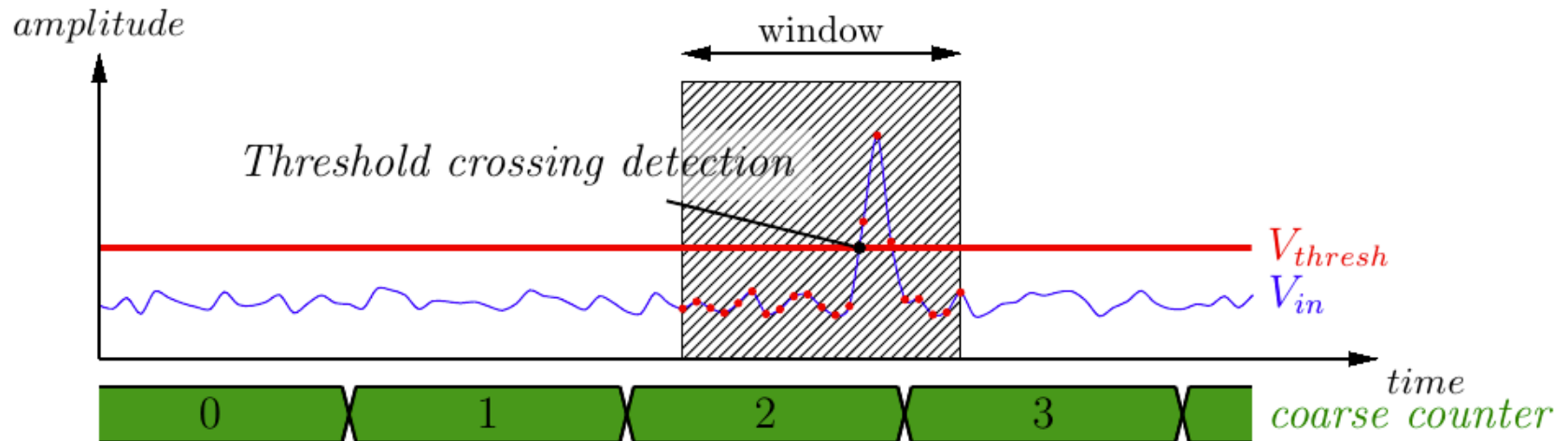
Goals:

- Technology evaluation (IBM 0.18 μ m)
- Tests of design choices (DLL & SCA architecture)
- Simultaneous Read&Write
- Creating a multi-channel chip easily integrable in large-scale experiments (ATLAS).

Detection of 'Event of interest' above threshold.

- Adjustable threshold (DAC).
- Pulse polarity (rising or falling edge).
- Additional post-trigger delay.

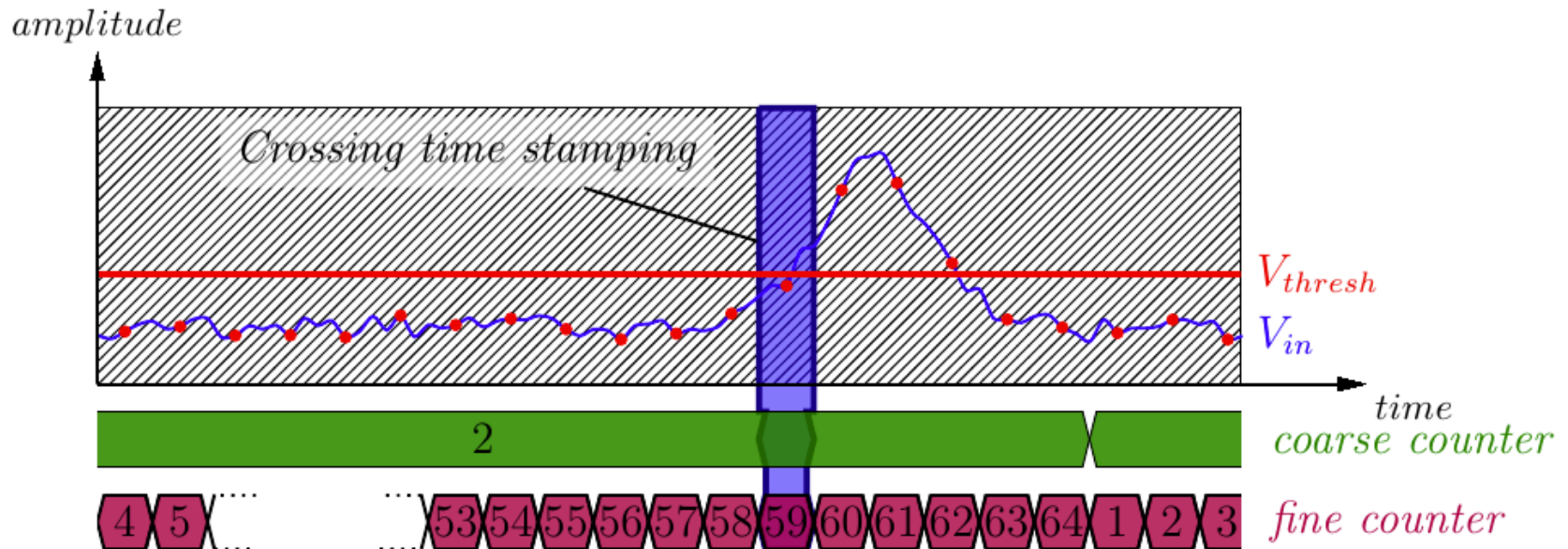
Fast pulse detection.



Sampling & time-stamping.

- 64 points from 1 to 10Gs/s.
- TDC 18 bits – 100ps precision.

Time-stamping and analog sampling.

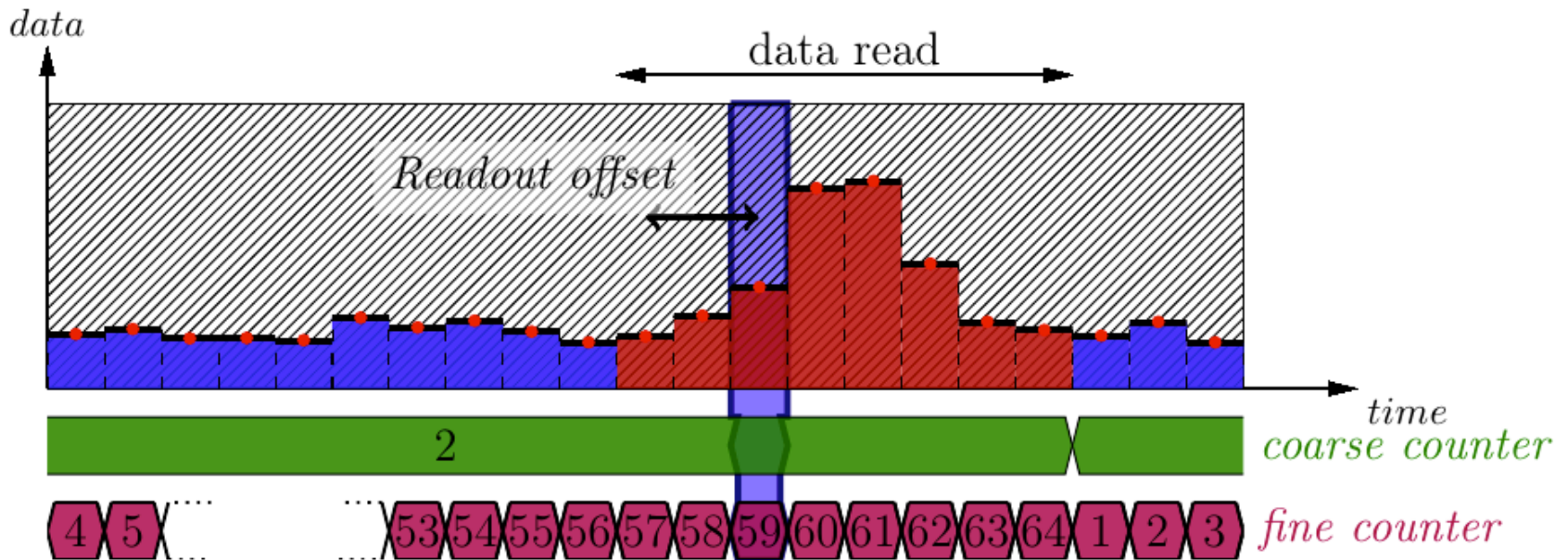


ADC CONVERSION AND REGION OF INTEREST READOUT

Conversion and readout.

- Wilkinson 11 bits - 2GHz.
- Region of interest readout LVDS 400MHz.

Conversion and readout.

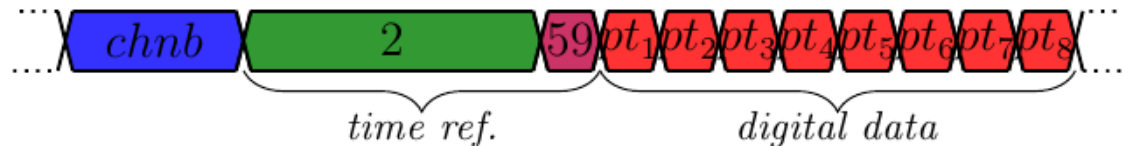


Priority token readout between the 16 channels.

- If channels 2, 5 and 15 are hit they will be sequentially read, until no more available data.
- Process transparent to the user.

Structure of readout data.

Data packet out.



SPECIFIC FEATURES OF SAMPIC

- Internal discriminators on all channels (with indiv. thresholds).
- 64 fully recorded samples (no dead zone).
- High bandwidth design.
- Reset before write (ghosts pulses removal).
- Gray code ADC conversion (limitation of metastability errors).
- Wide sampling range (Fast and Slow DLL modes).
- Fully configurable by serial link.

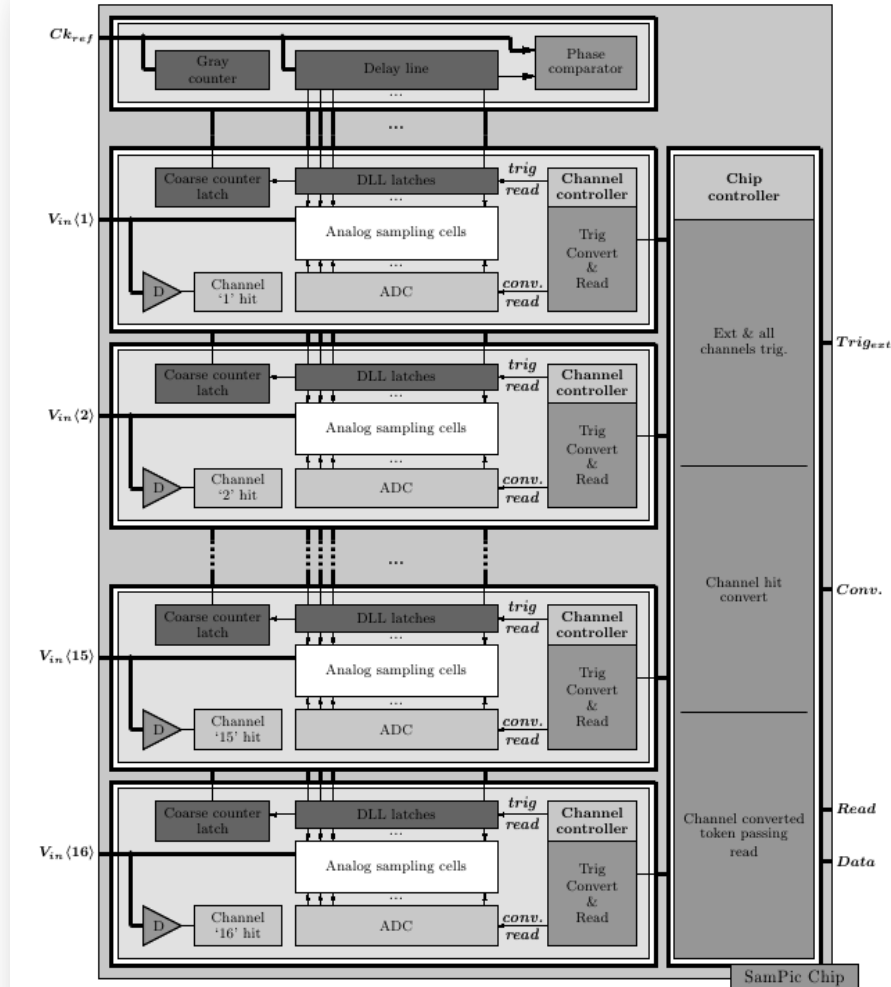


Figure 1 – Top level bloc diagram of the SamPic chip.

RESULTS & PERFORMANCES



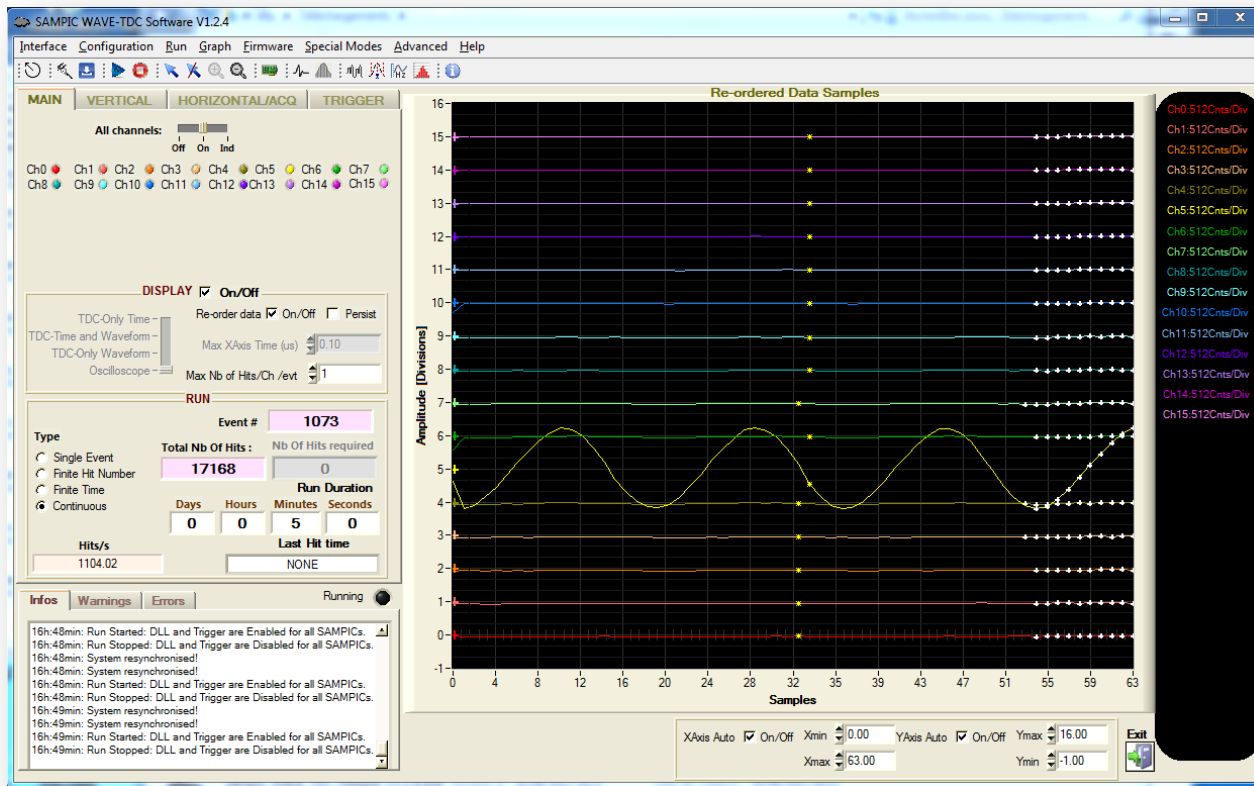
THE ACQUISITION BOARD (LAL)



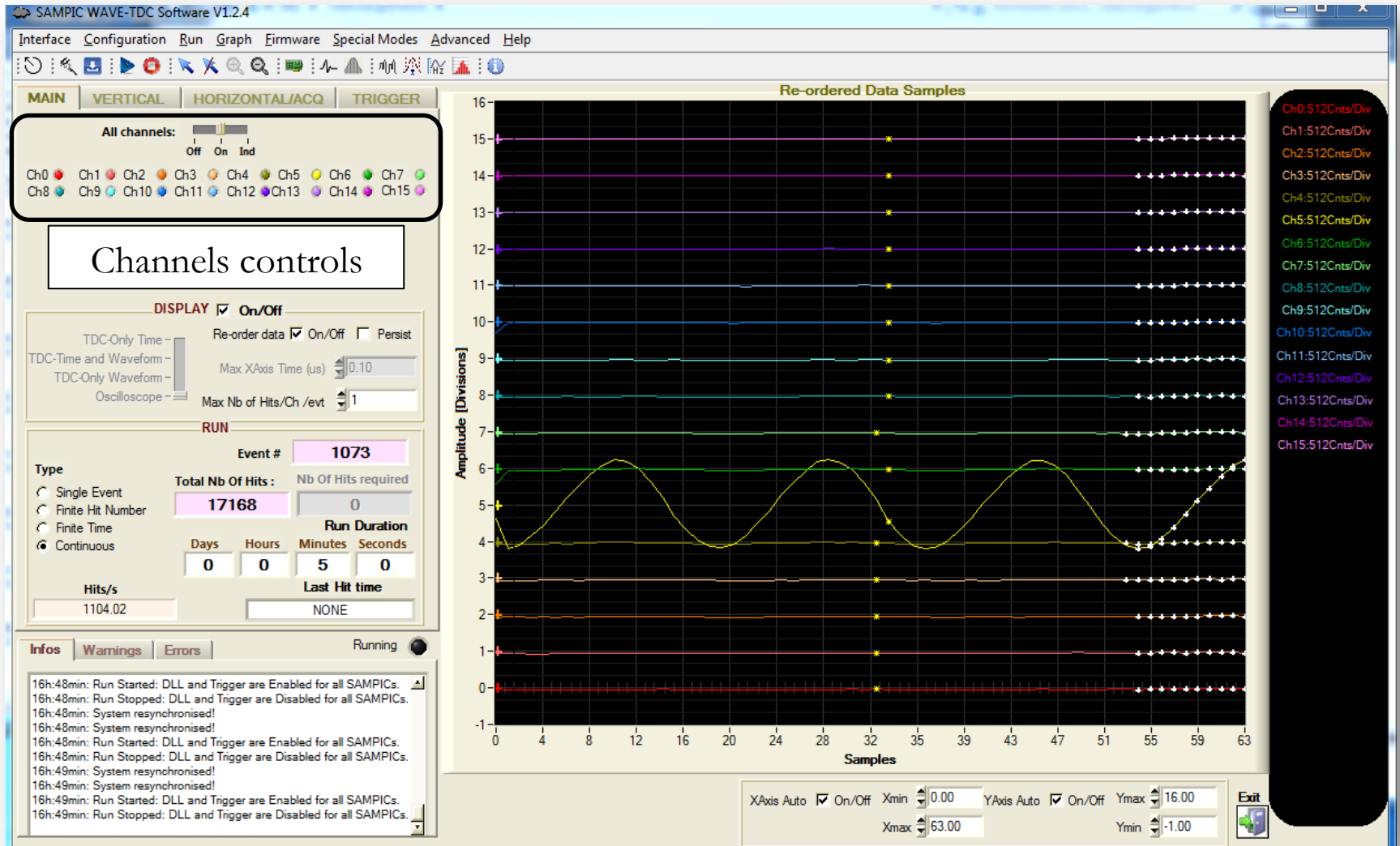
Jihane Maalmi
Dominique Breton
Pascal Rusquart

THE ACQUISITION SOFTWARE (LAL)

- 5V voltage supply – 1Amp.
- USB – Ethernet – Fiber Optic readout.
- Windows PC with LAL USB DLLs (easy: .exe 5min install).

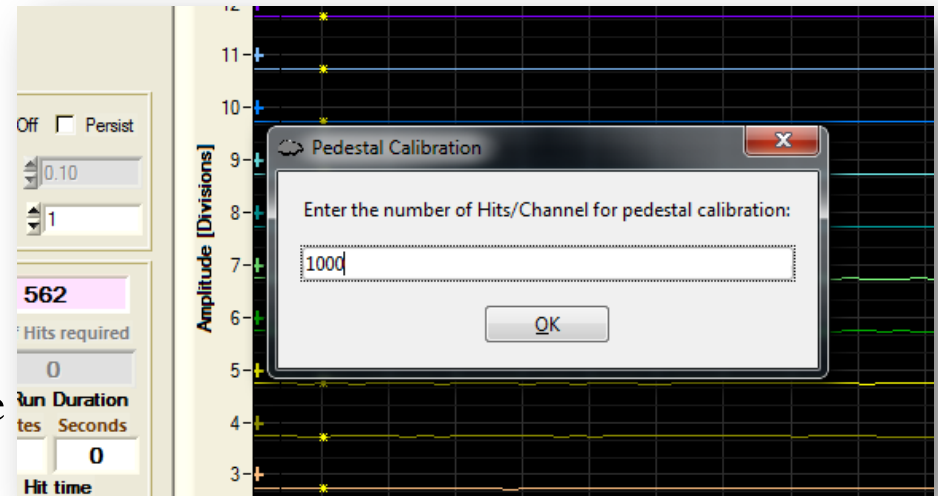


GUI – EASY CONFIGURATION AND MONITORING

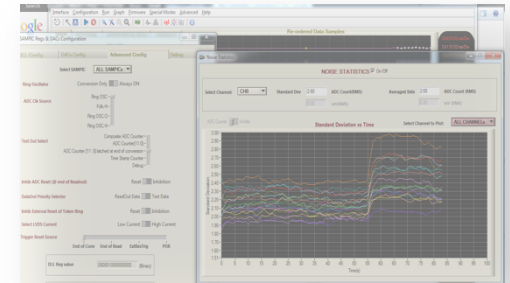


EXAMPLE OF FEATURE : PEDESTAL CALIBRATION

- Simple graphic interface for all calibrations.
- Calibration parameters loaded automatically at start-up.
- Pedestal & Fix pattern sampling time jitter correction.



- Save data to file.
- Noise measurements.
- Sampling time jitter measurements.
- Sampling frequency modification.
- Single event – Continuous – Finite Hit number – Finite time acquisition mode.
- Time measurement – Charge measurement mode.
- DLL jitter monitoring.
- Hit rate monitoring.
- On-board internal pulsers for calibrations.
- Any other requirements, ...



SAMPIC DOCUMENTATION

2. Electrical requirements.

1. Power supplies.

In its standard mode of use, SAMPIC must be supplied between **pad-PV** and **vddn-LV0**. All the **vddn** may be connected to a common power supply, but it is advised to use a true low impedance power supply plane to bring it to the chip and to use typically one 100nF bypass capacitor for each **vddn**, located as close as possible to the chip.

+ Description of the power supplies connection and typical values

Table 2-1: Min/Max values of the power supplies connection and typical values

Table 2-1 is a table describing precisely the functions and connectivity of each power supply. Please refer to the **pinout** for pad location and numbering.

Name	Description	Additional features	Pad connections	Pin #
vddn-LV0	Standard for the 16x16 Williams comparators.	This pad is locally decoupled in the comparator with a capacitance of 100pF for 2 pads (typical).	Pad to the core control supply group (pinout: vddn-LV0).	36
vddn-LV1	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV1 (typical).	37
vddn-LV2	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV2 (typical).	38
vddn-LV3	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV3 (typical).	39
vddn-LV4	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV4 (typical).	40
vddn-LV5	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV5 (typical).	41
vddn-LV6	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV6 (typical).	42

SAMPIC 1.0

vddn-LV0	Standard for the 16x16 Williams comparators.	This pad is locally decoupled in the comparator with a capacitance of 100pF for 2 pads (typical).	Pad to the core control supply group (pinout: vddn-LV0).	36
vddn-LV1	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV1 (typical).	37
vddn-LV2	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV2 (typical).	38
vddn-LV3	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV3 (typical).	39
vddn-LV4	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV4 (typical).	40
vddn-LV5	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV5 (typical).	41
vddn-LV6	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV6 (typical).	42

SAMPIC 1.0

vddn-LV0	Standard for the 16x16 Williams comparators.	This pad is locally decoupled in the comparator with a capacitance of 100pF for 2 pads (typical).	Pad to the core control supply group (pinout: vddn-LV0).	36
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vddn-LV2	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV2 (typical).	38
vddn-LV3	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV3 (typical).	39
vddn-LV4	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV4 (typical).	40
vddn-LV5	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV5 (typical).	41
vddn-LV6	Standard for the core control counter.	Not connected to the registers.	Decoupling for 32x16 vddn-LV6 (typical).	42

Table 2-1: Min/Max values of the power supplies connection and typical values

2. Digital levels.

Two types of digital inputs are used for the SAMPIC chip:

- LVCMOS differential inputs. These inputs are not internally terminated (differential input resistance is $> 10k\Omega$).
- CMOS inputs (high level = **vddn**, low level = 0).

Two types of digital outputs are available:

- CMOS outputs (high level = **vddn**, low level = 0).
- LVCMOS outputs (high level = **vddn**, low level = 0).

An external terminating resistor **Rterm** must be connected between the positive and negative outputs of the signal.

SAMPIC 1.0

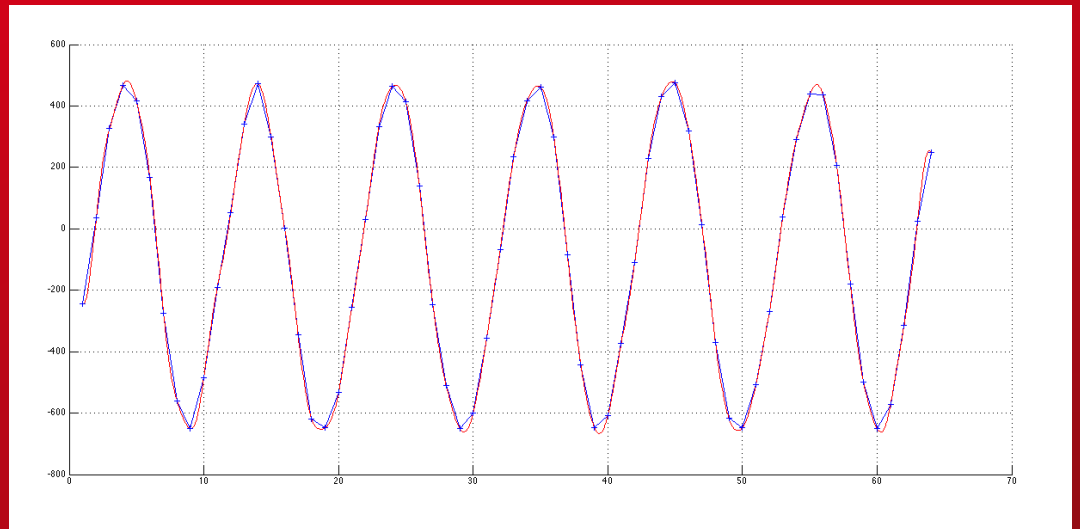
Get a high level, a programmable current **I_{out}**, defined between 100pA to 10nA by 100pA steps (bits 13 and 12 of the register **R_{out}**), is sourced by the positive input and sunk by the negative one.

For a low level, a current with the same magnitude but with opposite sign is sunk by the positive output and sourced by the negative one.

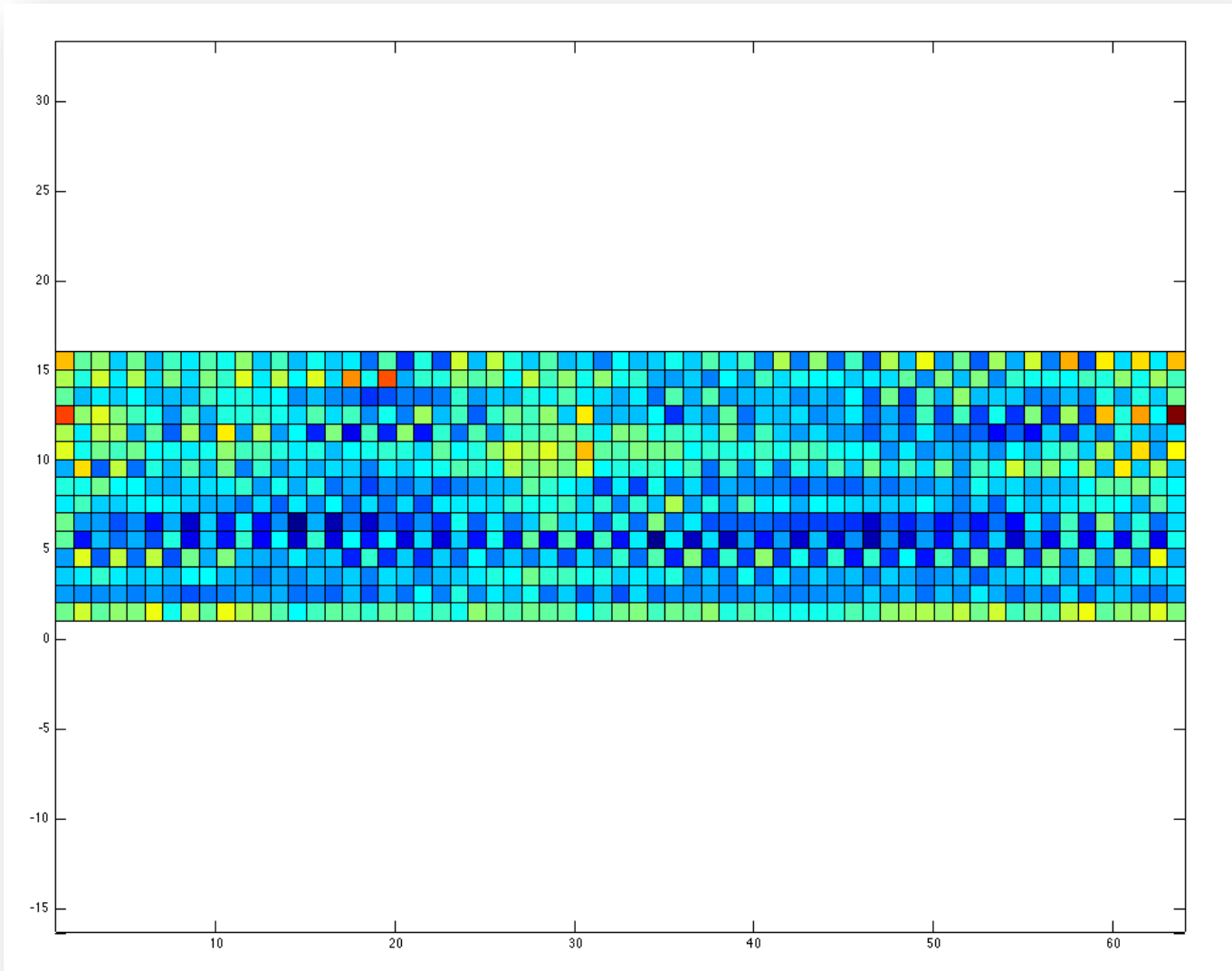
The common mode output voltage (**V_{out,CM}**) is internally set to 1.25V. In the standard mode of operation, **R_{out}** (bits 13 and 12) is set to 100pA. The common mode output voltage **V_{out,CM}** is set to 1.25V. In this case, the voltage levels on the 2 outputs are 1.5V and 0.9V, giving a differential voltage swing compatible with standard LVCMOS receivers.

Name	Description	Min	Typ	Max	Unit
vddn-LV0	Power supply voltage	1.5	1.5	1.5	V
vddn-LV1	Vddn power			min.	
vddn-LV2	Common mode output voltage	1.2			V
vddn-LV3	LVDS output swing	0.4			V
vddn-LV4	Low level for LVDS input	-0.1	0	0.6	V
vddn-LV5	High level for LVDS input	1.5	1.8	1.9	V
vddn-LV6	Input resistance for the digital inputs (CMOS or LVDS)			min.	ohm
vddn-LV7	Input capacitance for the digital inputs			1	ps
vddn-LV8	Turn-on for LVDS outputs (dependent on data control)	0.0 to 0.1		min.	ns
vddn-LV9	Load capacitance required for LVDS outputs		100		pF
vddn-LV10	Common mode output for LVDS outputs		1.25		V
vddn-LV11	LVDS differential output swing (Data setting, 10 ohm-terminated)				V
vddn-LV12	LVDS differential output level	0	0	0.2	V
vddn-LV13	LVDS differential input	1.5	1.8	1.9	V
vddn-LV14	Outputs				

SAMPIC PERFORMANCES



- Noise floor at 1mV for input dynamic of 1V.
- Noisiest cell are at 1.3mV
- Result with no shielding nor filtering applied.
- RF shielding and better insulation will improve things.



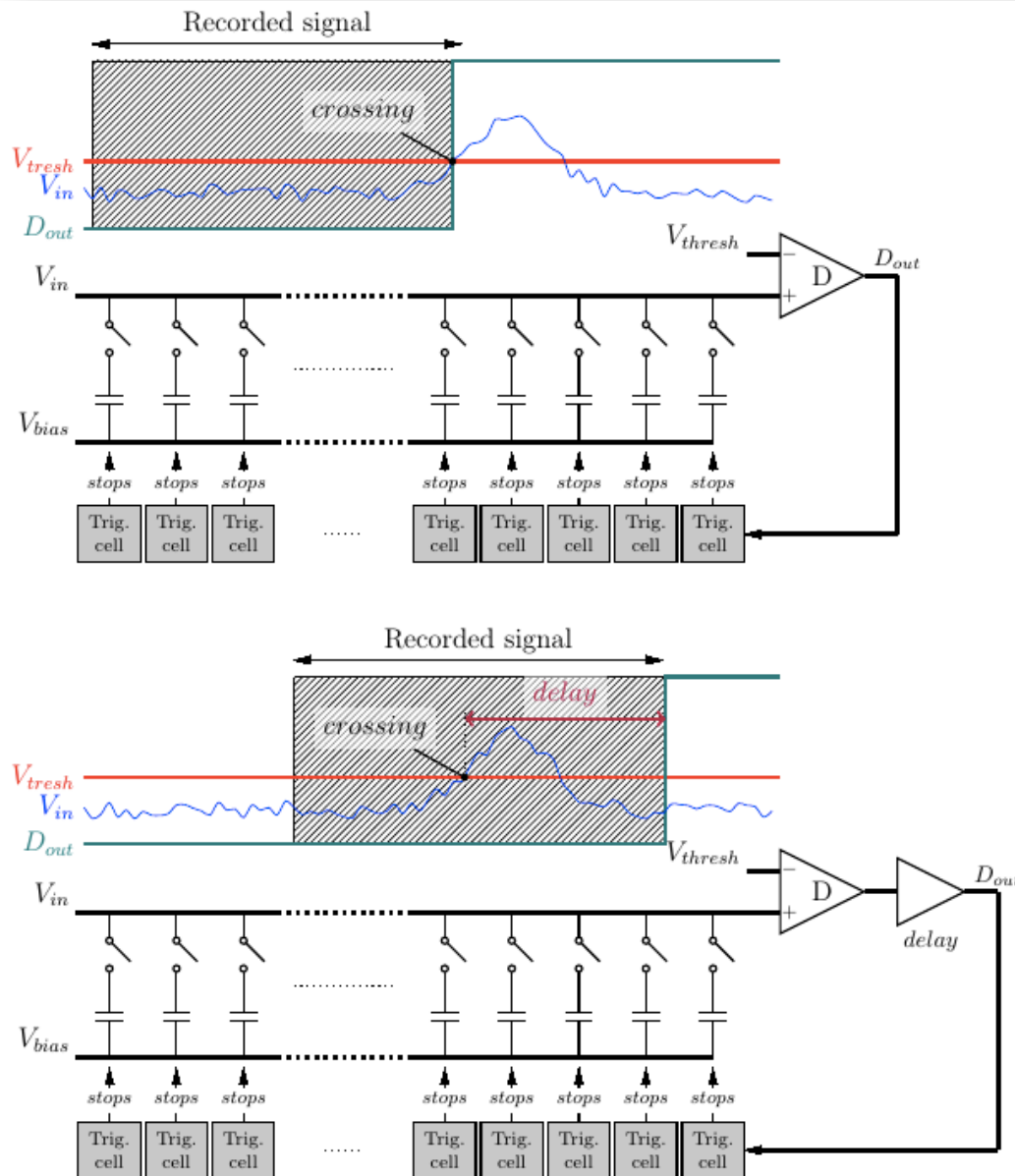
Bandwidth

- Measurements show 1.5GHz 3db-bandwidth in all channels.
- Bandwidth is uniform over all 64x16 cells.
- No resonance peak.

Trigger

- All internal triggers functional.
- Adjustable threshold per channel.
- Adjustable delay per channel.
- External trigger for selected channels possible.

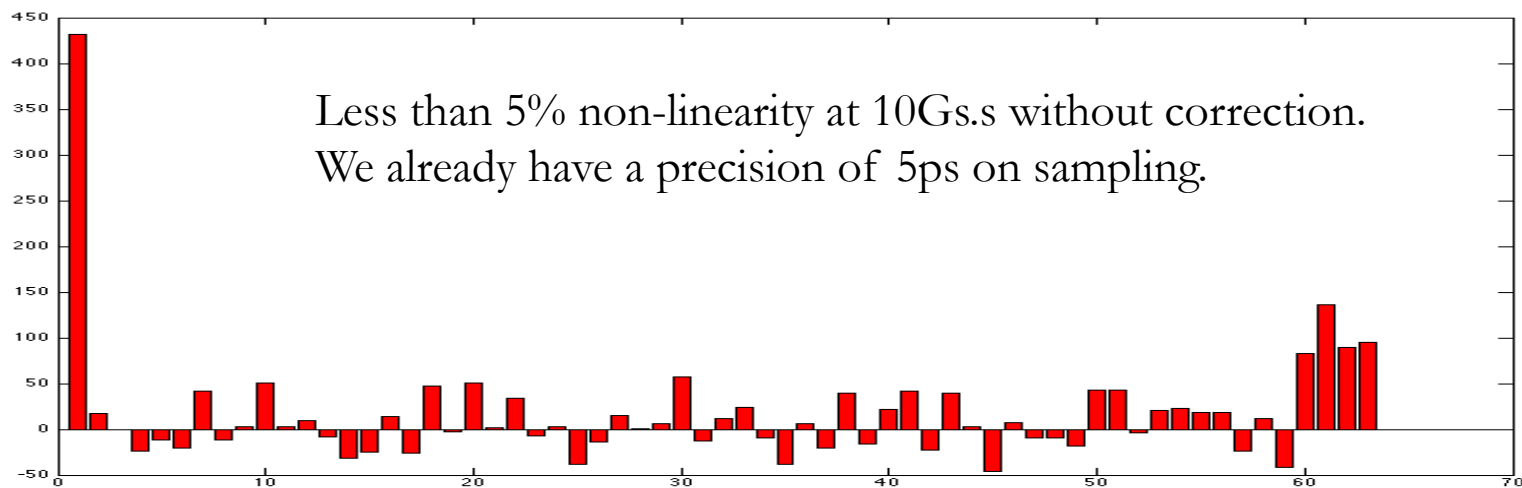
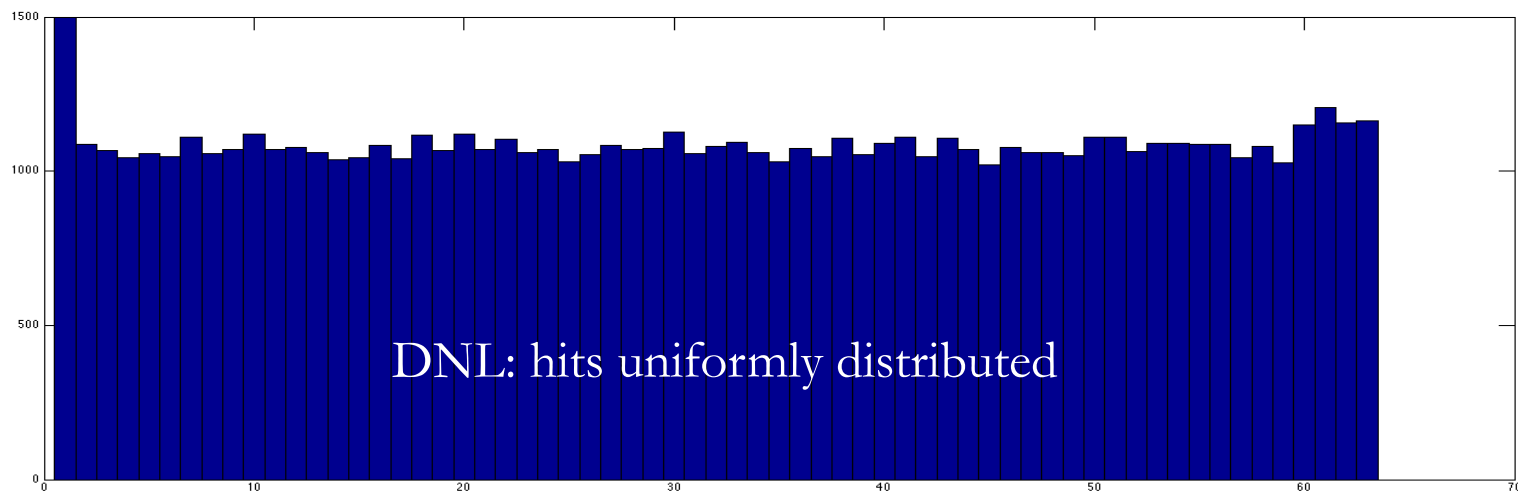
POST TRIGGER



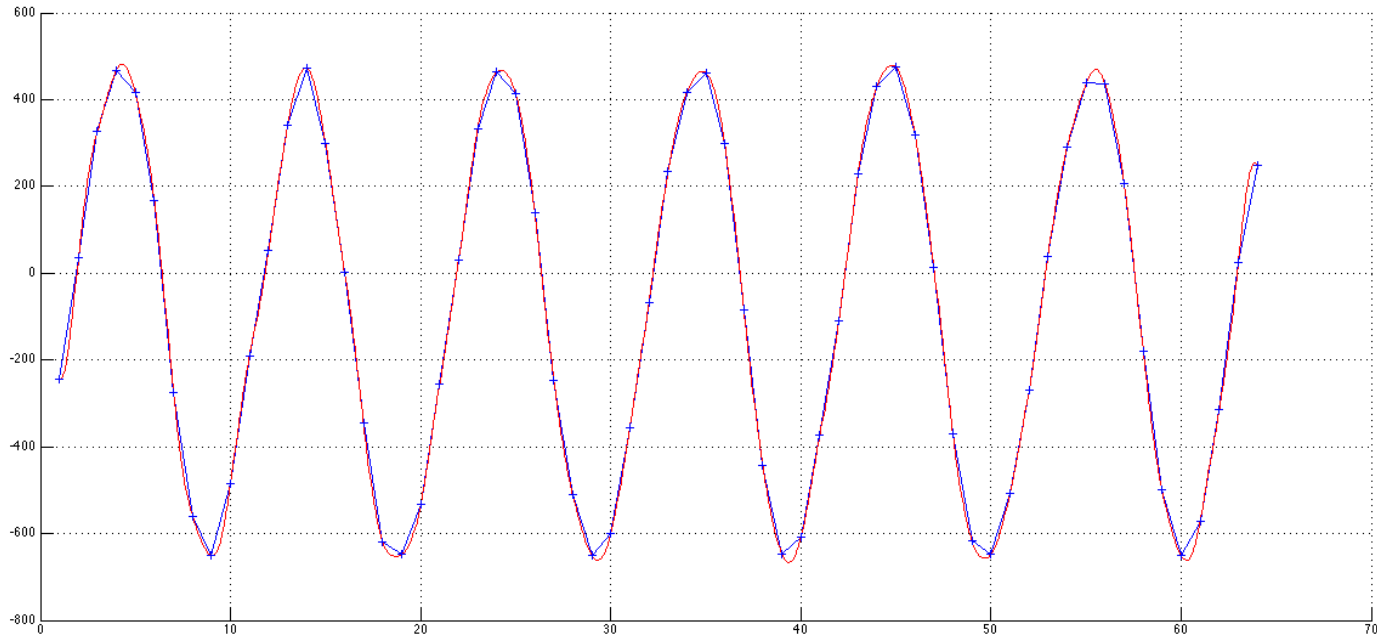
3 post-trig modes

- No delay
- 800ps delay
- 1.6ns delay

DLL STABILITY AND NON-LINEARITY CORRECTIONS



QUALITY OF SAMPLING



1GHz sine wave 64 samples 'out of the box' (pedestal cal. only) @ 10Gs/s.

64 usable data points.

Will improve with DNL calibration.

Will improve with linearity corrections.

The SamPic rules for Hits – Conversion & Readout

- Rule 1. All SamPic channels that are **not triggered** are tacking data.
- Rule 2. All triggered channels that are **not holding data to read** are converted **simultaneously**. User activated.
- Rule 3. All converted channels are readout **sequentially**. User activated.

Maximum SamPic Hit rate:

- 1 μ s for conversion
- 2.5ns/word read (min 20ns – max 170ns x 16).
- SamPic can take data during read sequence.
- Hit rate does not vary if int. or ext trigger used.
- Currently software limited!
- Acquisition board is Optic fiber ready and Ethernet ready

RUN

Event # **1073**

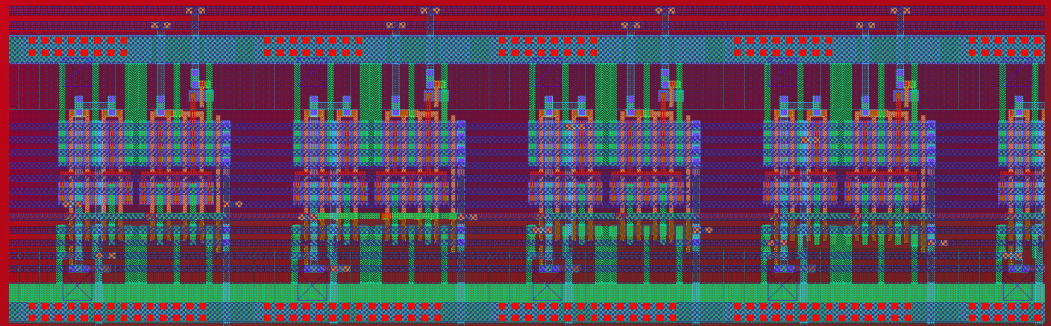
Type
☐ Single Event
☐ Finite Hit Number
☐ Finite Time
☒ Continuous

Total Nb Of Hits : **17168** Nb Of Hits required : **0**

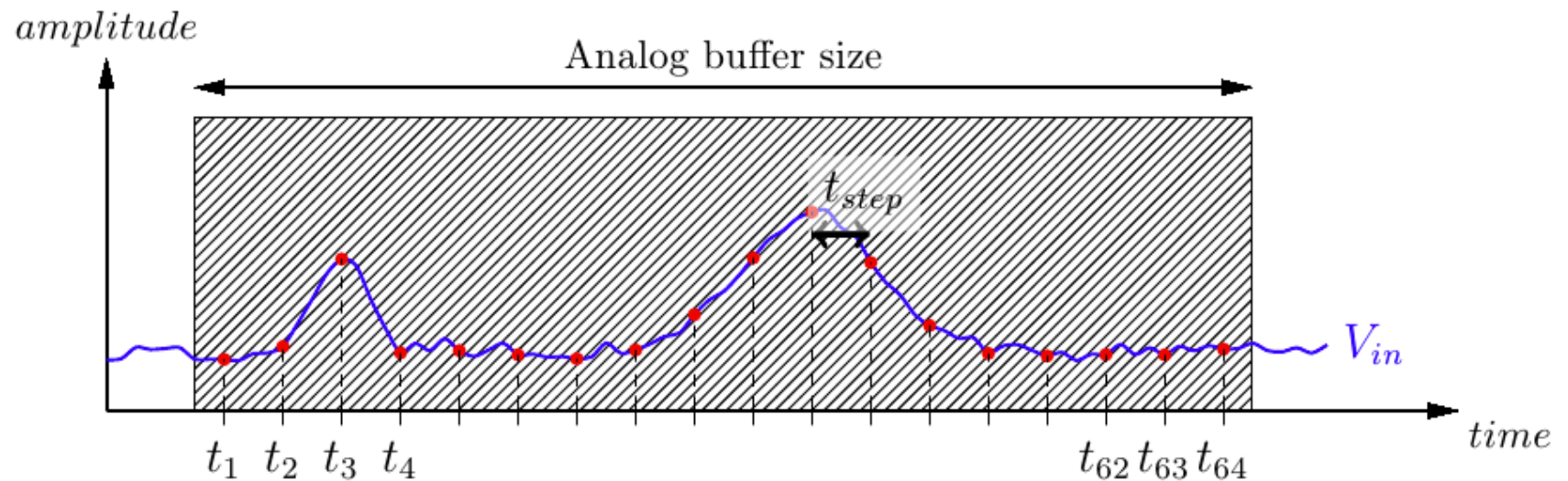
Run Duration
 Days: **0** Hours: **0** Minutes: **5** Seconds: **0**

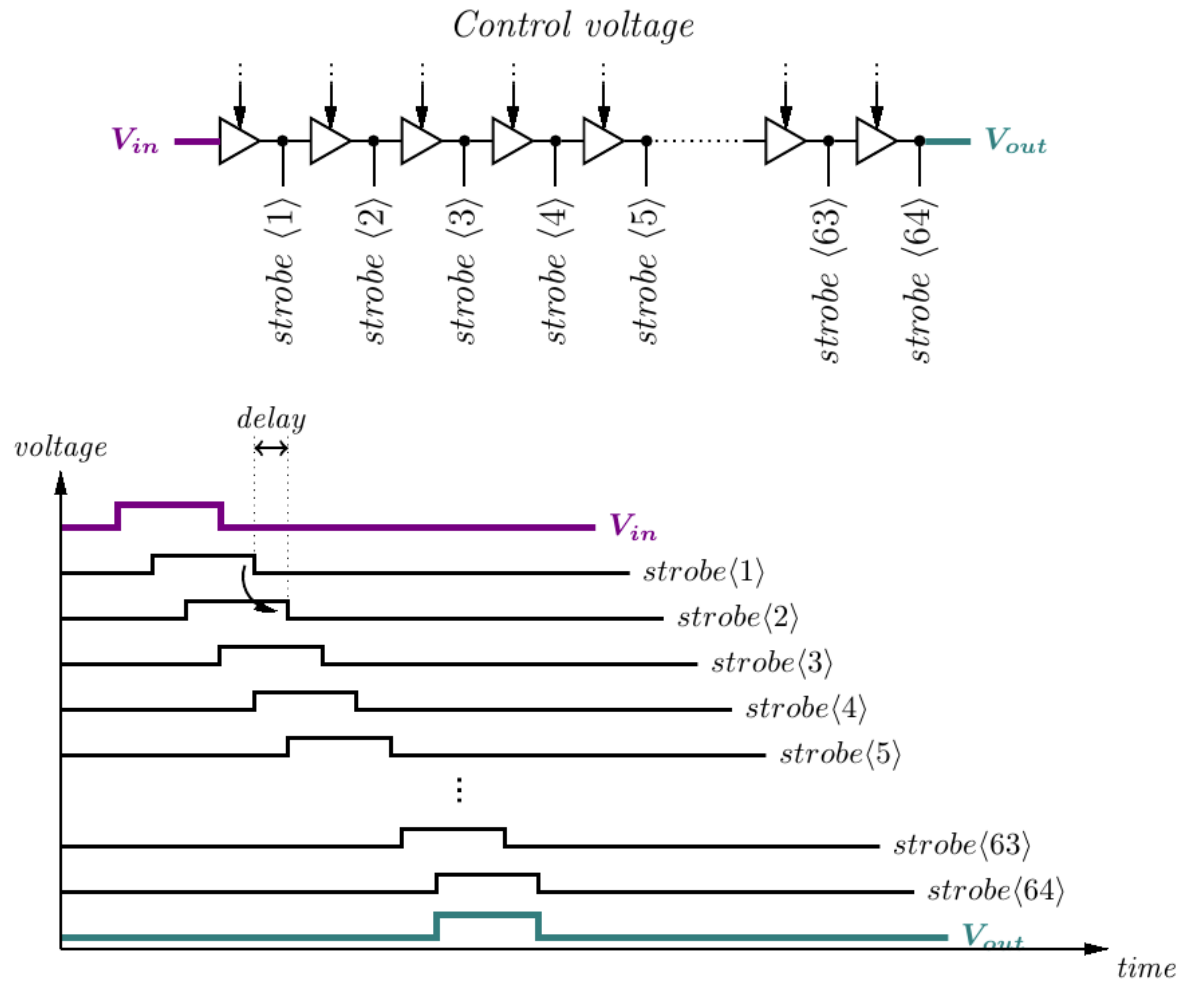
Hits/s: **1104.02** Last Hit time: **NONE**

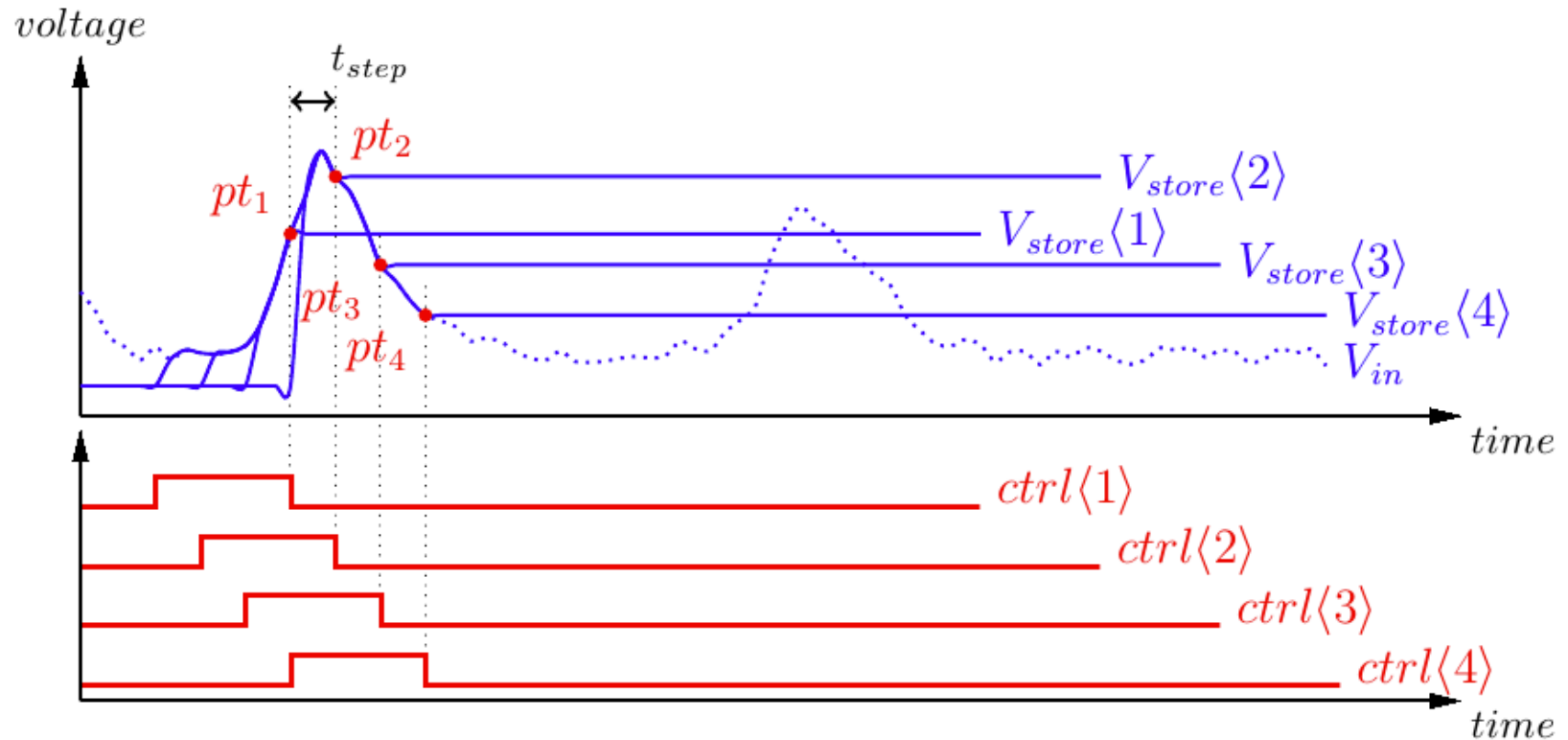
DÉTAIL D'UNE STRUCTURE: LA DLL

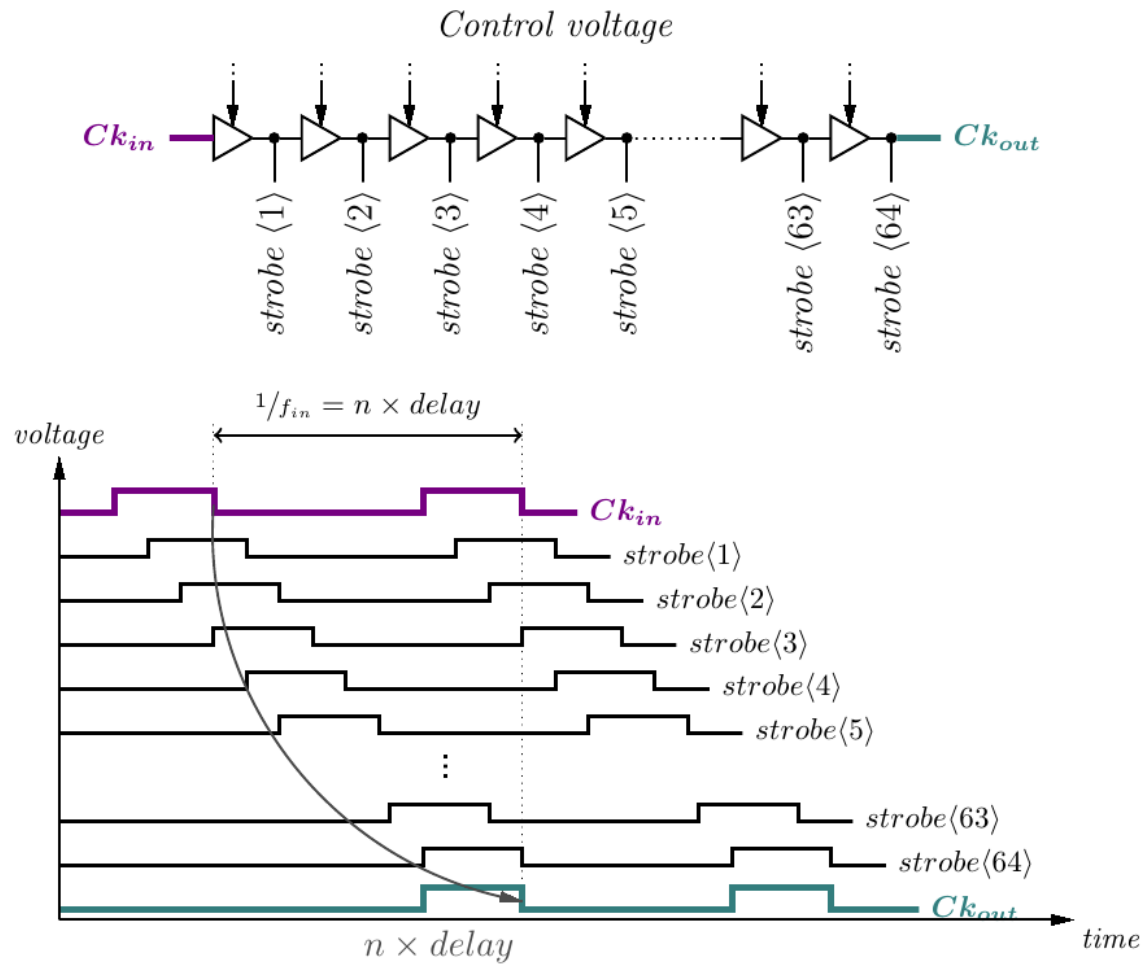


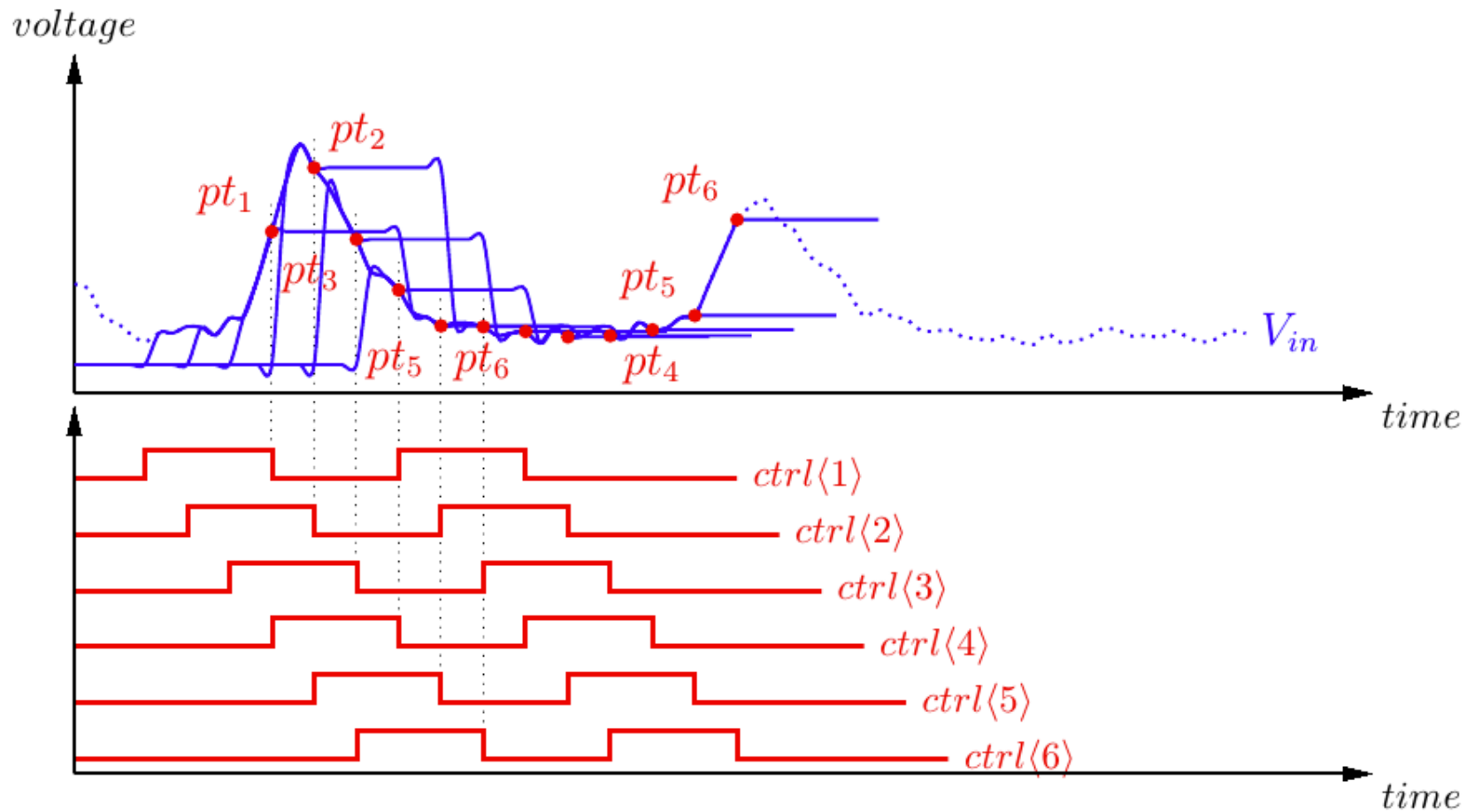
Le rôle de la DLL est de définir les instants d'échantillonnages t_1, t_2, \dots, t_{64} dans SamPic.

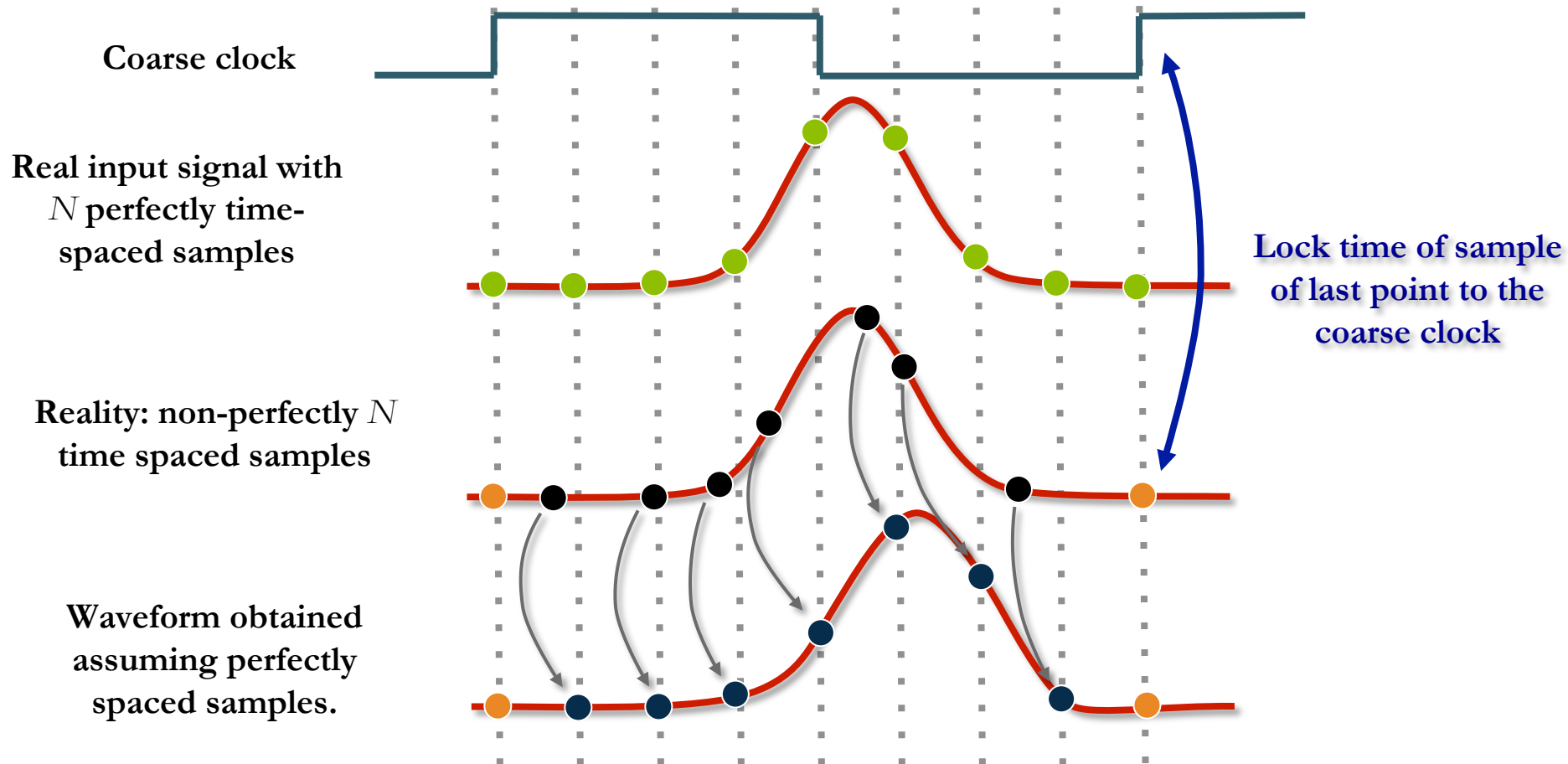








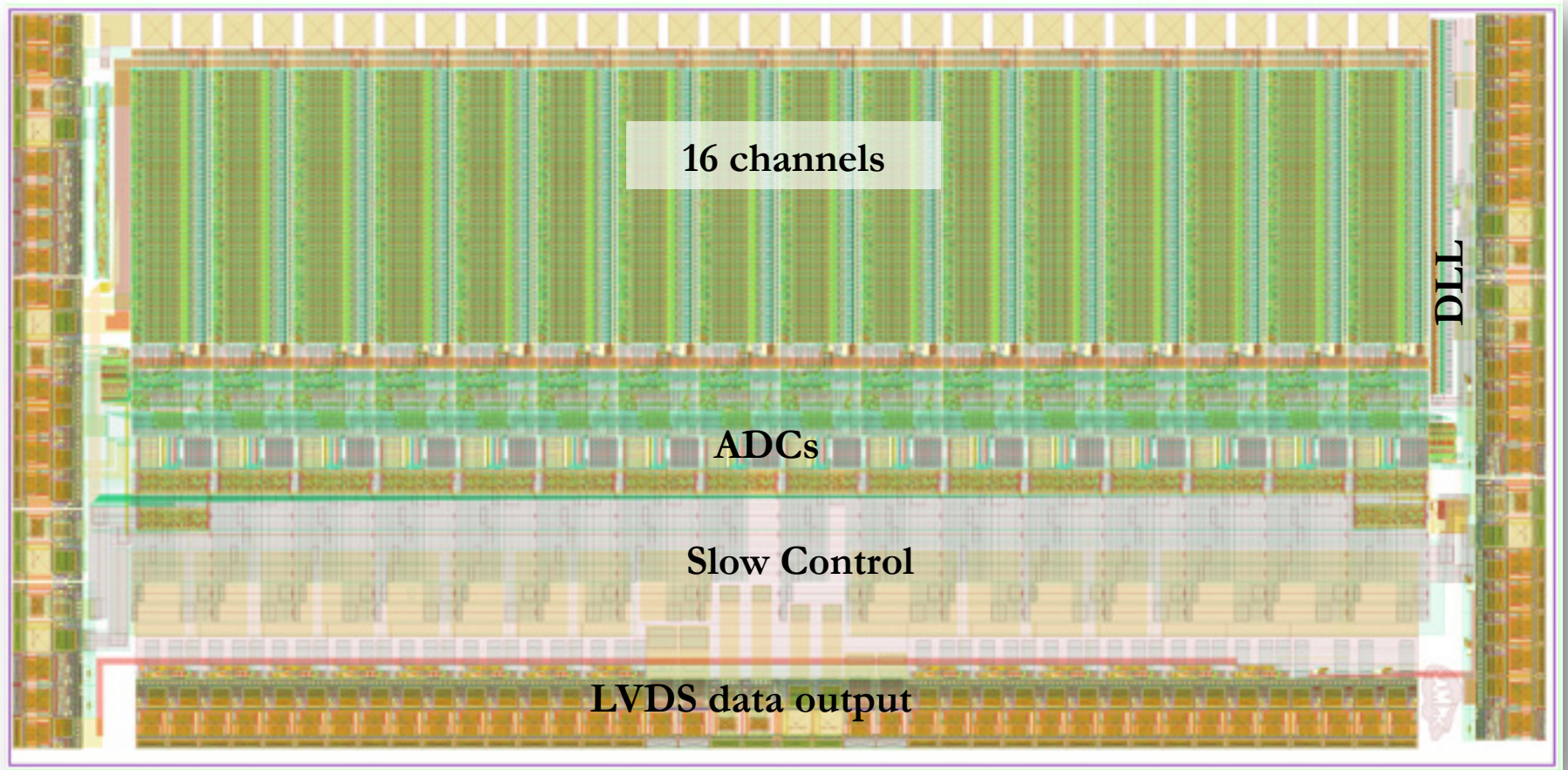




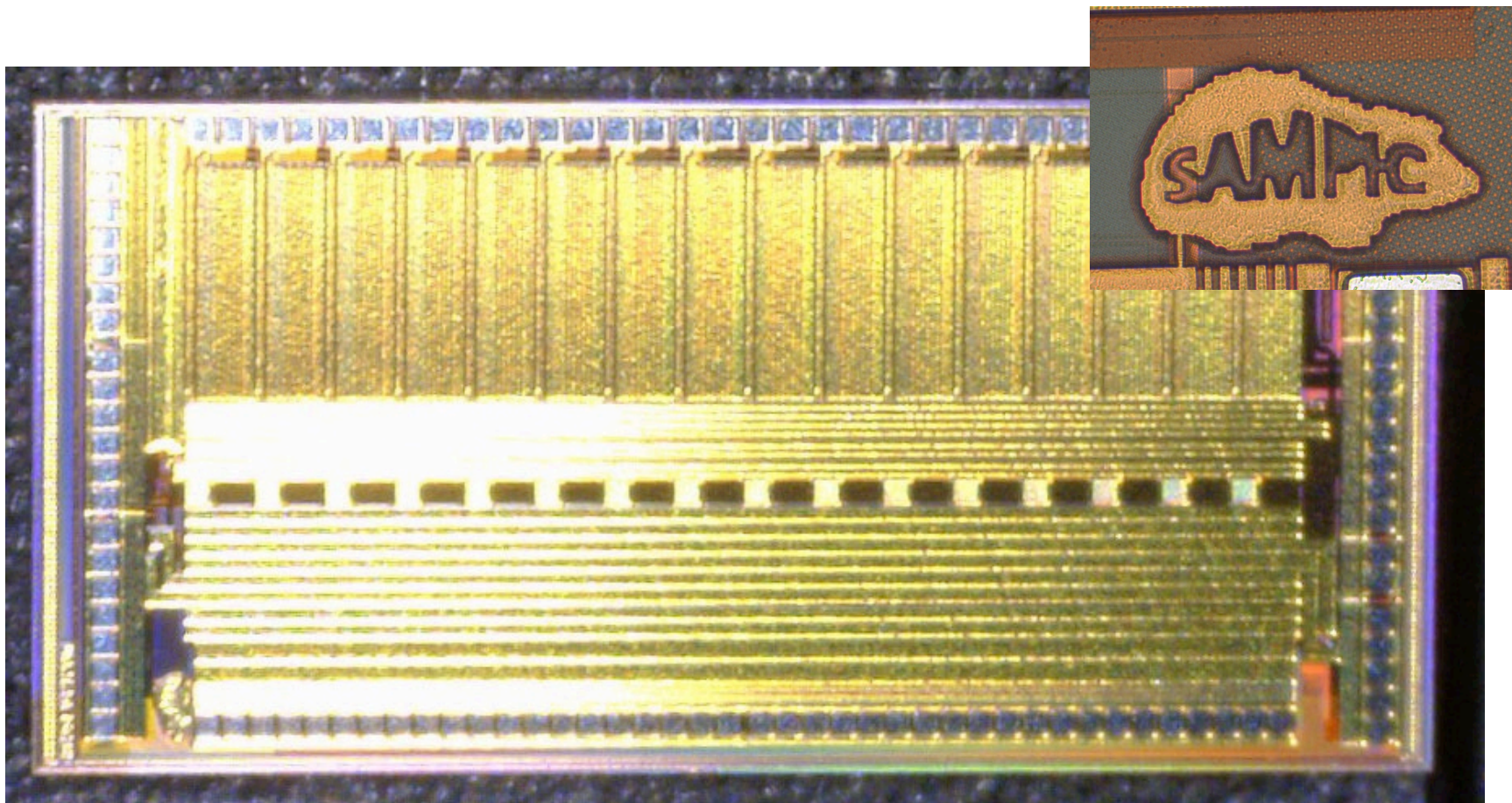
CONCLUSION

SAMPIC CHARACTERISTICS

	Measure
Channel number	16
Input bandwidth	1.5 GHz
Sampling frequency	1 - 10GHz
ADC precision	11bit
Noise	1mV
Range	1V
Conversion time	1 μ s
Readout clock	400MHz max. (* not verified)
Readout time	2.5ns/word+ header x nb of channels



THE SAMPIC CHIP



Commissariat à l'énergie atomique et aux énergies alternatives
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Direction DSM
Département IRFU
Service SEDI

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