The Radiation Hard GBTX Link Interface Chip

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CERN, Switzerland

GBTX People

- The GBTX is the product of the imagination and work of many people going from the basic ideas through the specifications, design and testing. These people are:
  - *Sophie Baron*
  - *Sandro Bonacini*
  - *Pedro Cardoso*
  - *Jorgen Christiansen*
  - *Ozgur Cobanoglu*
  - *Xavi Cudie*
  - *Federico Faccio*
  - *Sebastian Feger*
  - *Diego Figueiredo*
  - *Rui Francisco*
  - *Tullio Grassi*
  - *Ping Gui*
  - *Pedro Leitao*
  - *Alessandro Marchioro*
  - *Paulo Moreira*
  - *Christian Paillard*
  - *Karolina Poltorak*
  - *David Porret*
  - *Rafael Sune*
  - *Filip Tavernier*
  - *Guoying Wu*
  - *Ken Wyllie*
  - *(At some point the list must end but, if you feel you should be in it please let me know…)*

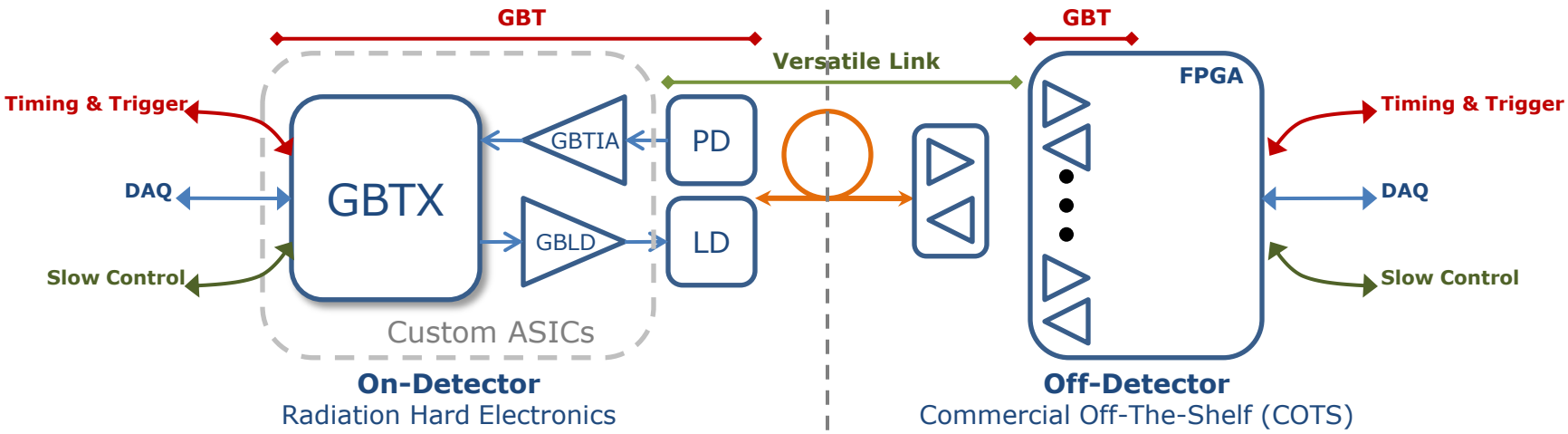
Outline

- Radiation hard optical Link
- The GBT system
- The GBTX up-link
- The GBTX down-link
- Phase-shifter
- xPLL
- ePLL
- Controlling the GBTX
- Interfacing with the GBLD
- Built-in test features
- SEU tests
- Power consumption
- Testing Status
- GBTX future

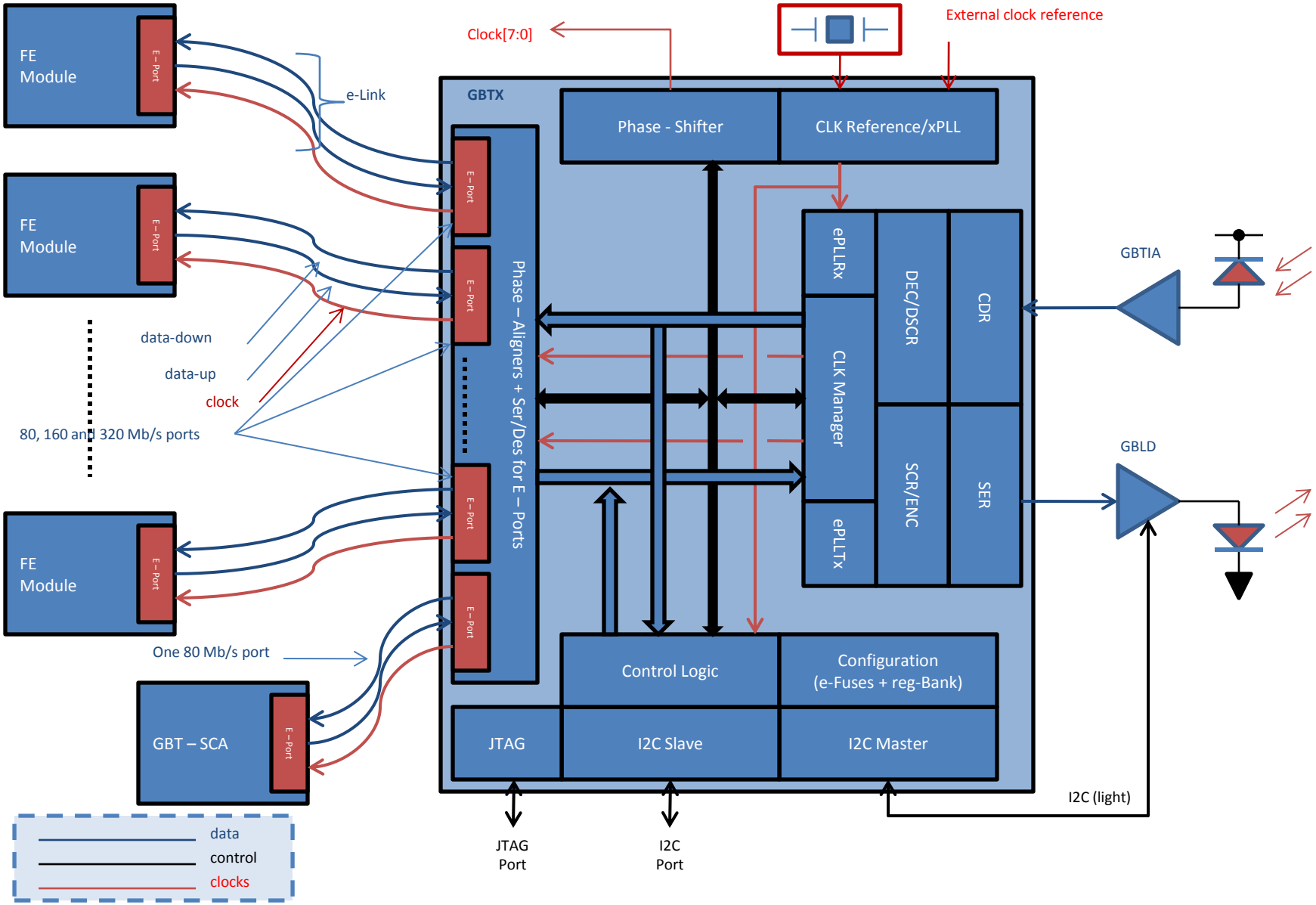
Radiation Hard Optical Link

Development of an high speed bidirectional radiation hard optical link:

- *GBT project:*
  - ASIC design
  - Verification
  - Functionality testing
  - Packaging
- *Versatile link project:*
  - Opto-electronics
  - Radiation hardness
  - Functionality testing
  - Packaging

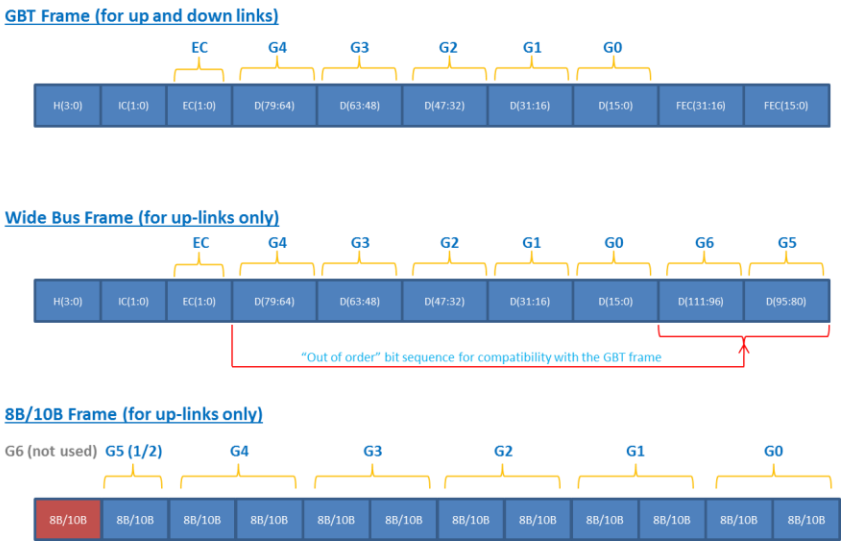


The GBT System



GBTX Data Bandwidth

- The GBTX supports three frame types:
  - ***"GBT" Frame***
  - ***"Wide Bus" Frame***
  - ***"8B/10B" Frame***
- "GBT" Mode
  - User bandwidth: 3.28 Gb/s
    - Up/down-links
- "Wide Bus" and "8B/10B"frames are only supported for the uplink
  - The downlink always uses the "GBT" frame.
- "8B/10B" Mode
  - Downlink data 8B/10B encoded
  - No FEC
  - User bandwidth: 3.52 Gb/s
- "Wide Bus" Mode:
  - Uplink data scrambled
  - No FEC
  - User bandwidth: 4.48 Gb/s



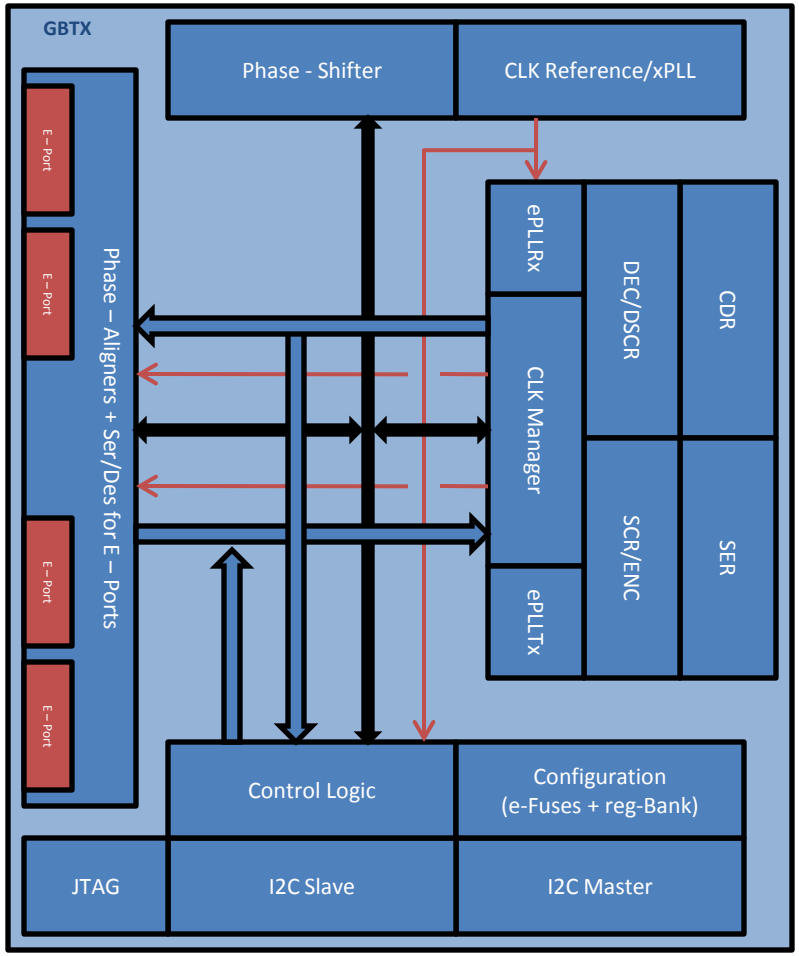
GBT Frame:

- Frame Synchronization:
  - DC balanced and "redundant" header
- Forward Error Correction:
  - Interleaved Reed-Solomon double error correction
  - 4-bit symbols (RS(15,11))
  - Interleaving: 2
  - Error correction capability:
    - 2 Interleaving × 2 RS = 4 symbols = 16-bits
  - Code efficiency: 88/120 = 73%

GBTX Functionality (1/4)

e-Links

- 40 bi-directional e-Links
  - Up to 40 @ 80 Mb/s
  - Up to 20 @ 160 Mb/s
  - Up to 10 @ 320 Mb/s
- e-Port data rate can be set independently for:
  - each group
  - Input / output ports
- 1 bi-directional e-Link:
  - 80 Mb/s
- 40 e-Link clocks (fixed phase) programable in frequency:
  - 40/80/160/320 MHz (per group)
  - *(independently of the bit rate)*
- Automatic, semi-automatic or user controlled phase alignment of the incoming serial data embedded in the e-Ports
  - Automatic alignment
    - Tracks temperature and voltage variations
    - Transparent to the user
    - Works on any type of data:
      - DC balanced / un-balanced
      - A few “occasional” transition enough to ensure correct operation



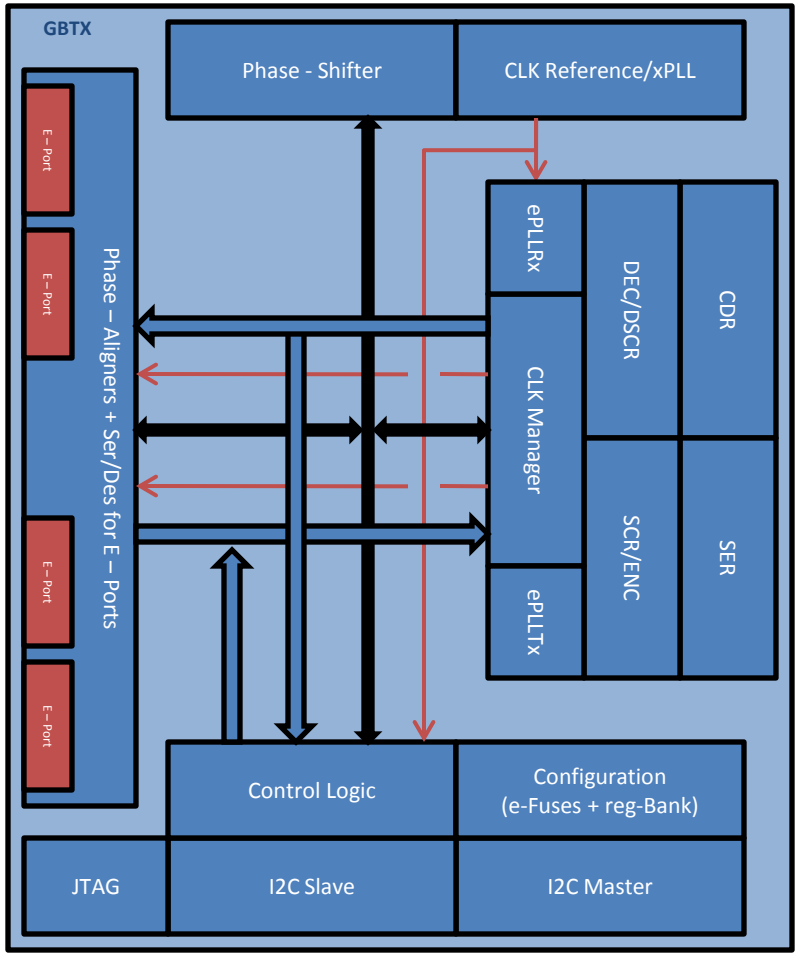
GBTX Functionality (2/4)

e-Links Special cases

- 8B/10B mode:
  - 44 input (max @ 80 Mb/s)
  - 36 output (max @ 80 Mb/s)
    - (Four outputs reused as inputs)
- Wide-Bus mode:
  - 56 input (max @ 80 Mb/s)
  - 24 output (max @ 80 Mb/s)
    - (16 “outputs” reused as inputs)

e-Links electrical characteristics

- Drivers:
  - SLVS signaling
- Receivers:
  - SLVS/LVDS signaling



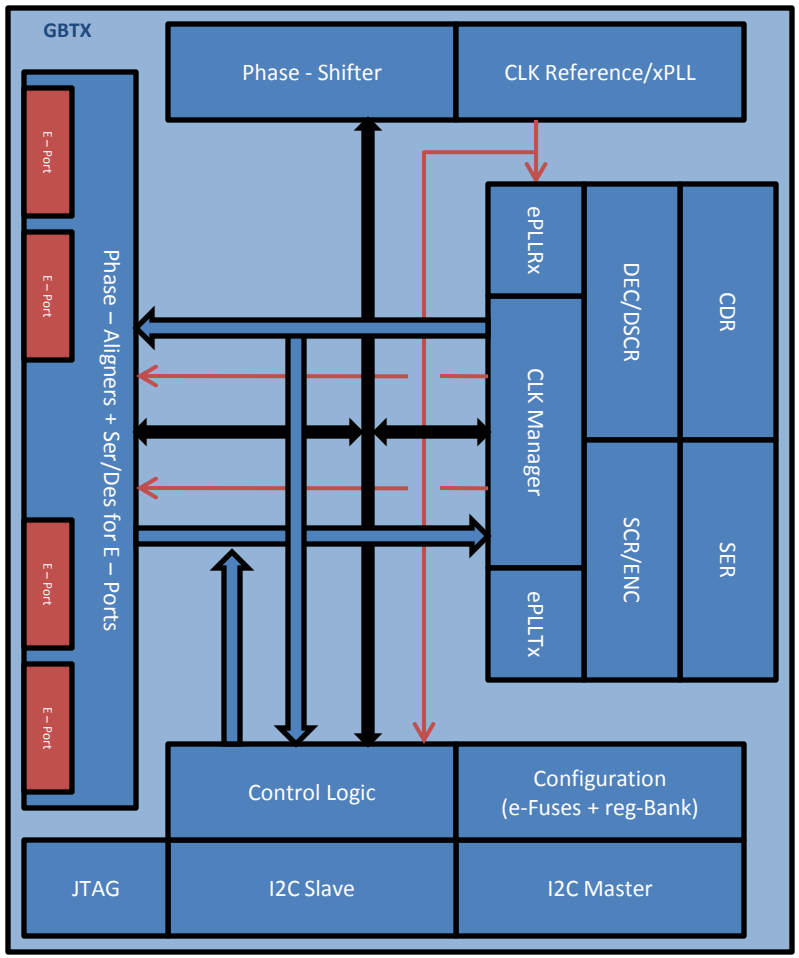
GBTX Functionality (3/4)

Phase-Shifter

- 8 independent clocks
- Programable in frequency:
  - 40 / 80 / 160 / 320 MHz
- Programable in phase:
  - 0 to 360◦
  - Phase resolution: 50 ps
    - (for all frequencies)
- Clock driver electrical levels:
  - SLVS

Reference clock:

- On package crystal
- Built-in crystal oscillator
- Built-in VCXO based PLL (xPLL)
- External reference can used as well



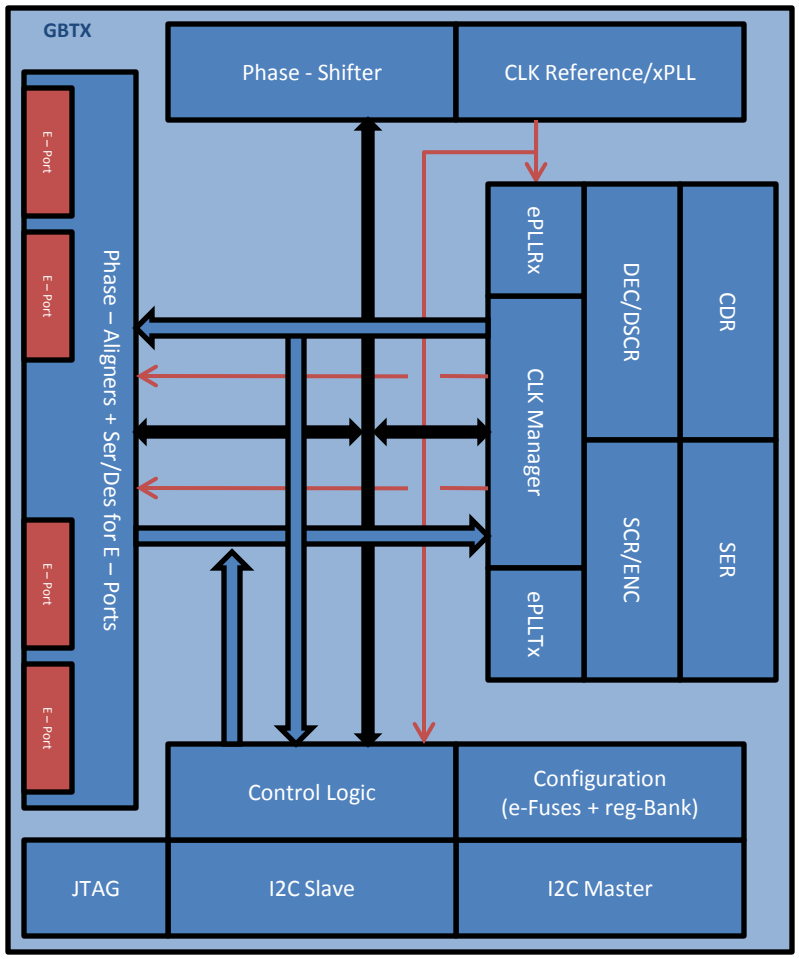
GBTX Functionality (4/4)

Chip Control

- e-Fuse register bank for burn in configuration
  - Standalone operation
  - Ready at power up
- Dynamic configuration and control
  - I2C Slave interface
  - IC control channel trough the optical link
- Watchdog circuit for chip operation supervision.

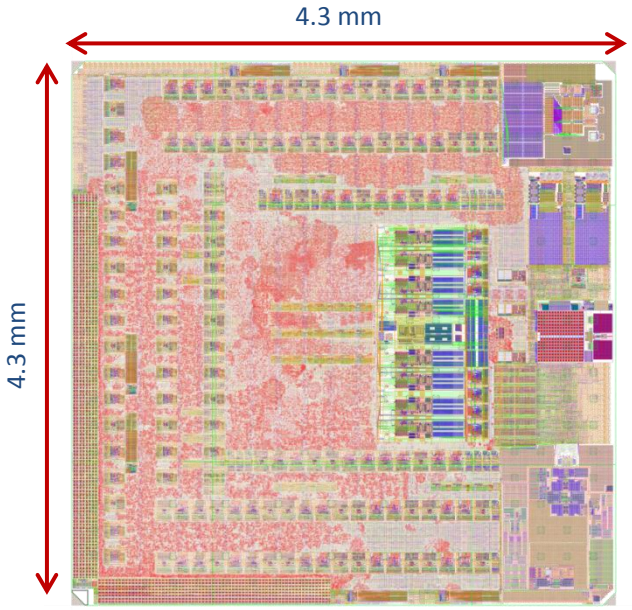
GBLD Control

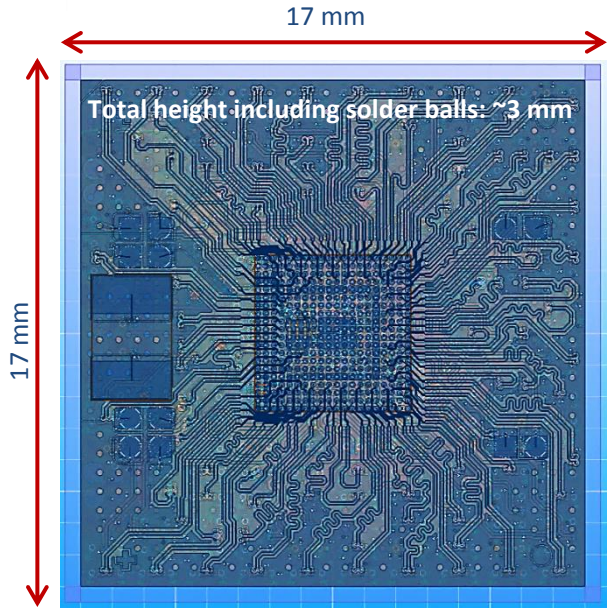
- GBLD dedicated I2C master interface
  - Copies configuration burned in the GBTX into the GBLD at start-up
  - Allows to program the GBLD either through the IC channel or through the I2C slave port



GBTX In Numbers

- ½ million gates
- Approximately:
  - 300 8-bit programable registers (all TMR)
  - 300 8-bit e-Fuse memory
- Clock tree (chip wide):
  - 9 clock trees (all TMR)
  - Frequencies: 40/80/160/320 MHz
- 7 PLLs:
  - RX: CDR PLL + Reference PLL (2.4 GHz)
  - Serializer PLL (4.8 GHz)
  - Phase-Shifter PLL (1.28 GHz)
  - xPLL (VCXO based PLL, 80 MHz)
  - (2x) ePLL (320 MHz)
- 17 master DLLs:
  - 9 for phase alignment of the e-links
  - 8 for clock de-skewing
- 56 replica delay lines:
  - For phase alignment of the e-links
- 7 power domains:
  - Serializer (1.5V)
  - DESerializer (1.5V)
  - Clock Manager (1.5V)
  - Phase shifter (1.5V)
  - Core digital (1.5V)
  - I/O (1.5V)
  - Fuses (3.3V)

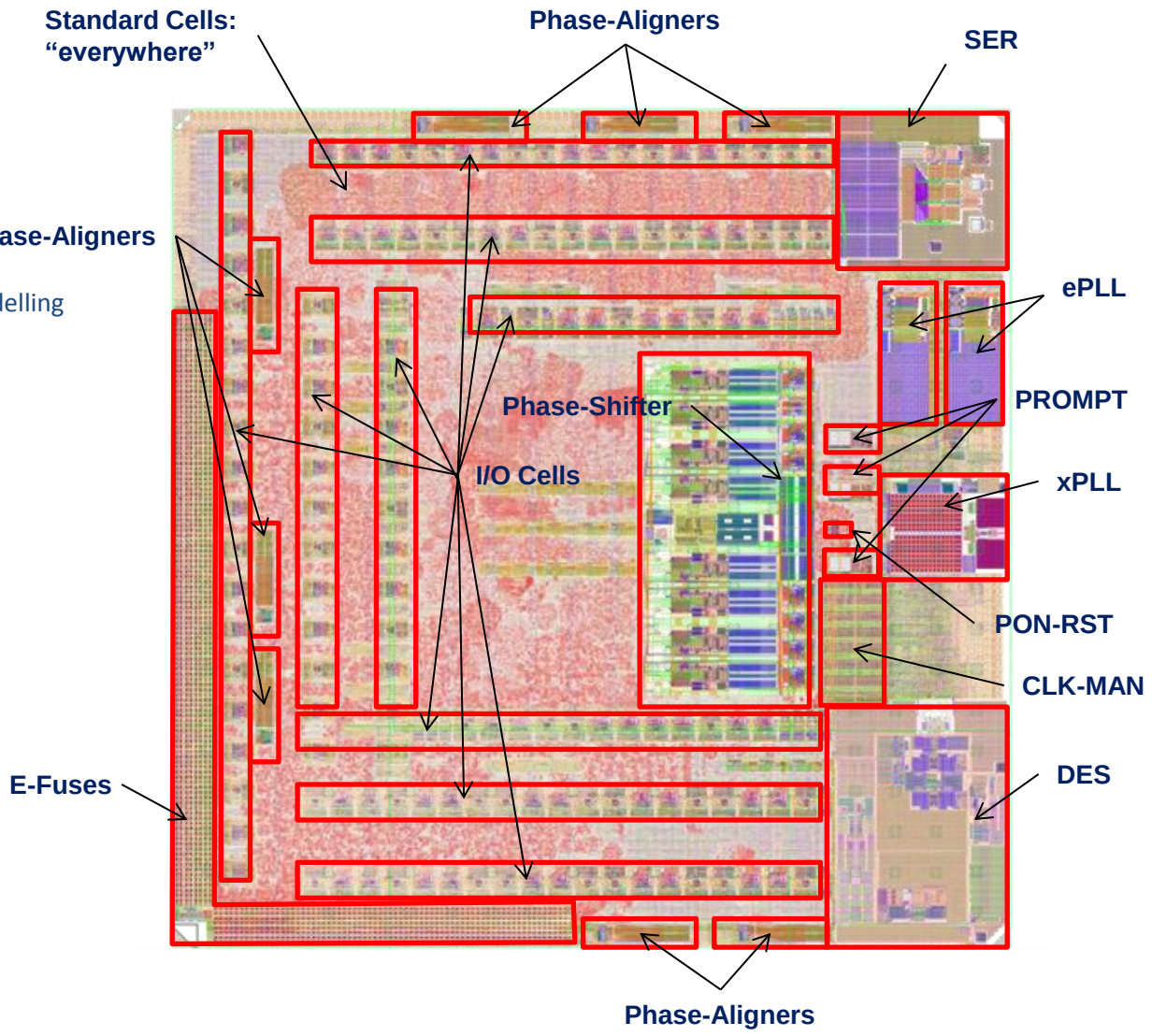




GBTX – Floor Plan and Modelling

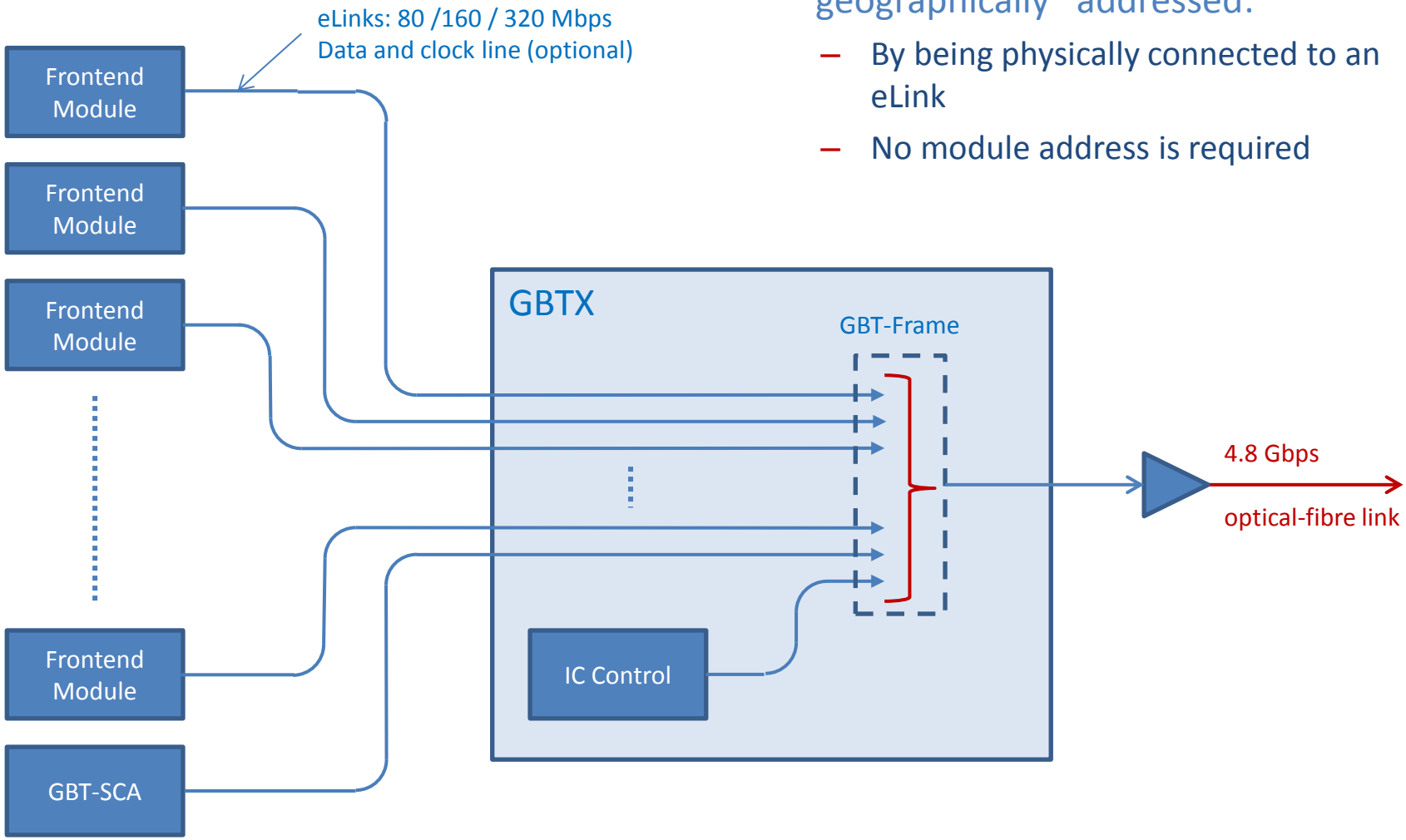
10 "Macro-cells":

- Serializer:
  - Full custom
  - "Analogue-Verilog" modelling
- Clock Manager:
  - Standard cells
  - Verilog modelling
- DESerializer
  - Full custom
  - + "custom" digital
  - + standard cells
  - "Analogue-Verilog" + Verilog modelling
- XPLL
  - Full custom
  - "Analogue-Verilog" modelling
- EPLL (x2)
  - Full custom
  - "Analogue-Verilog" modelling
- Phase-Shifter
  - Full custom
- Phase Aligners (x8)
  - Full custom
  - "Analogue-Verilog" modelling
- Prompt (x3)
  - Full custom
  - Verilog modelling
- Power on reset
  - Full custom
  - Verilog modelling
- e-Fuses (x300)
  - Foundry IP
  - Verilog modelling

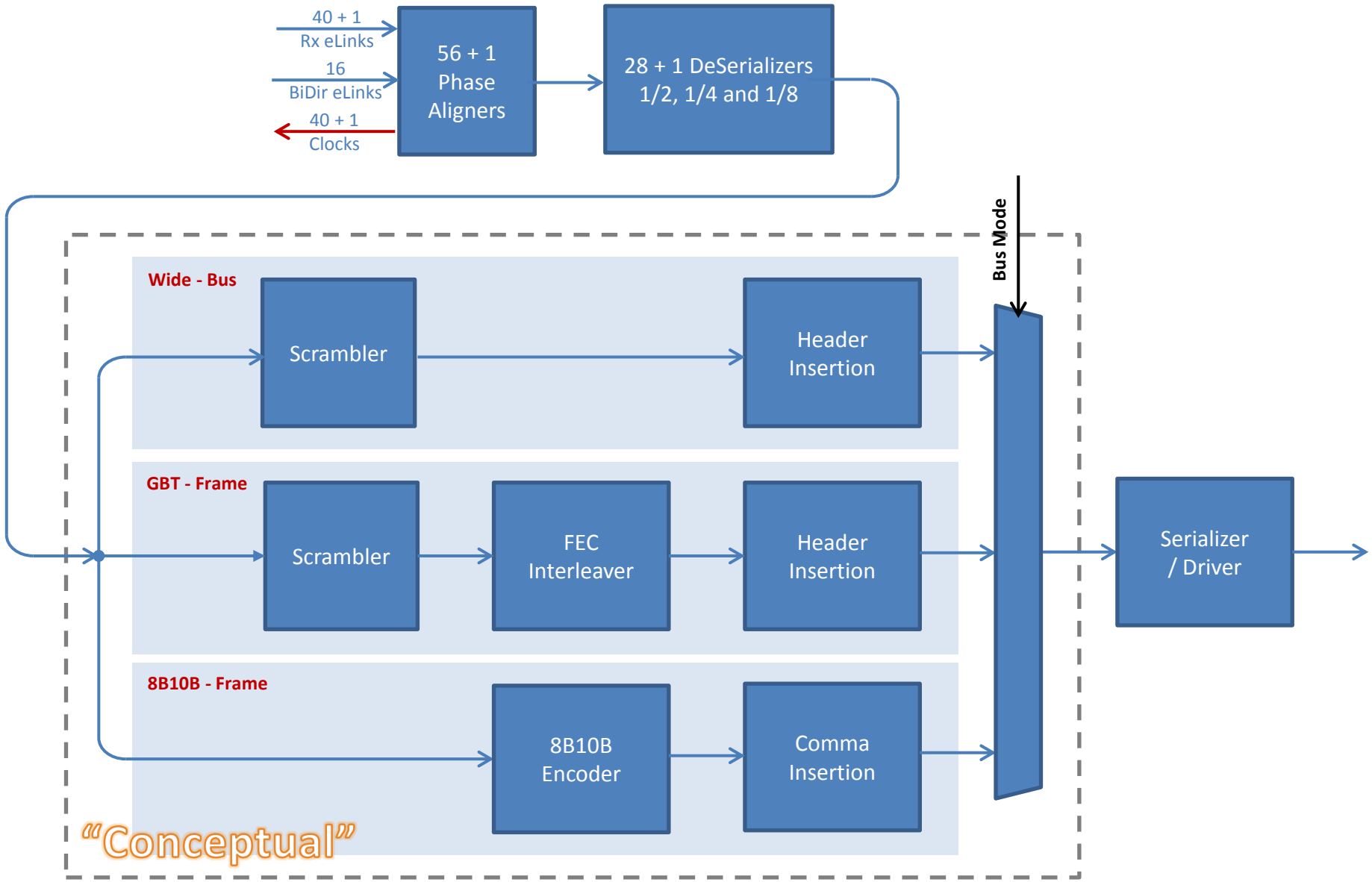


The GBTX up-link

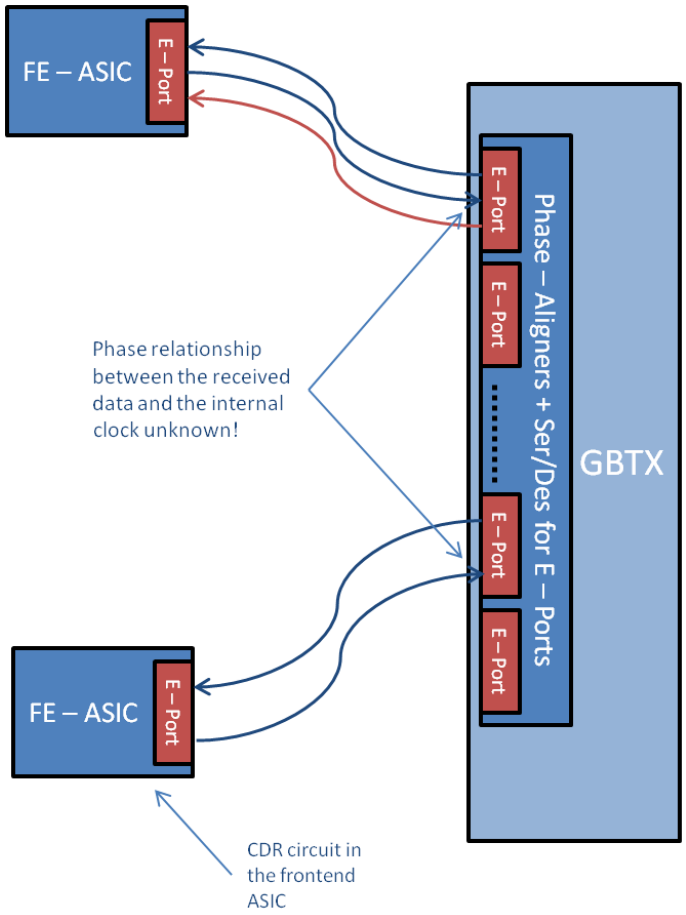
- Each eLink is associated with a specific set of bits in the frame
- Front-end modules are thus "geographically" addressed:
  - By being physically connected to an eLink
  - No module address is required

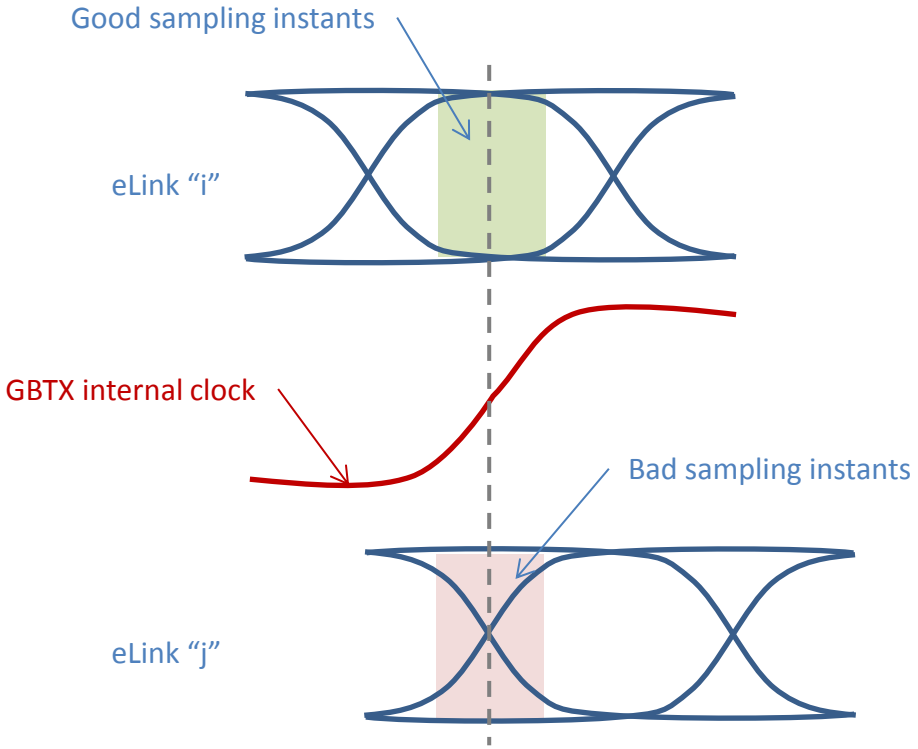


Transmitter Architecture



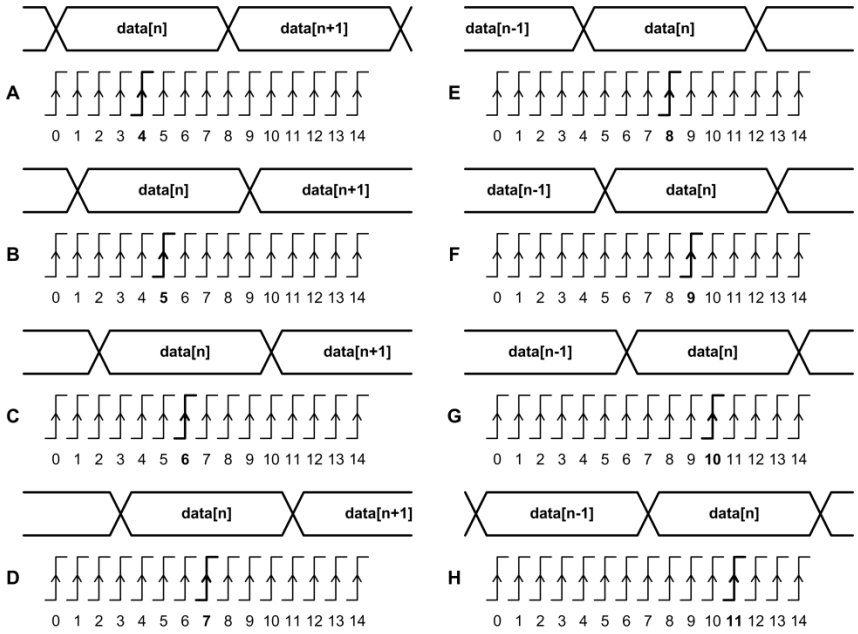
Up eLink – Phase Alignment





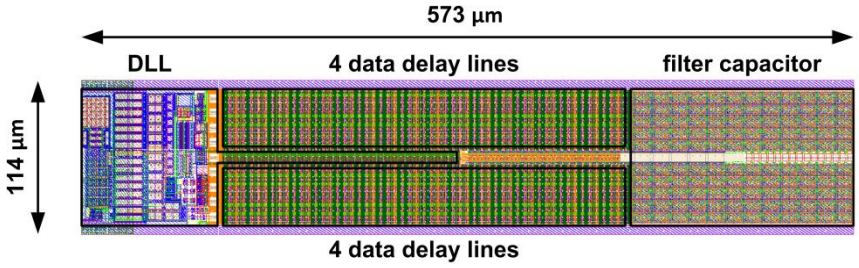
- The phase of the incoming data signals is "unknown" in relation to the internal sampling clock!
- There are up to 57 eLink inputs (potentially) all with random phase offsets
- The solution:
  - "Measure" the phase offset of each eLink input
  - Delay individually each incoming bit stream to phase align it with the internal sampling clock

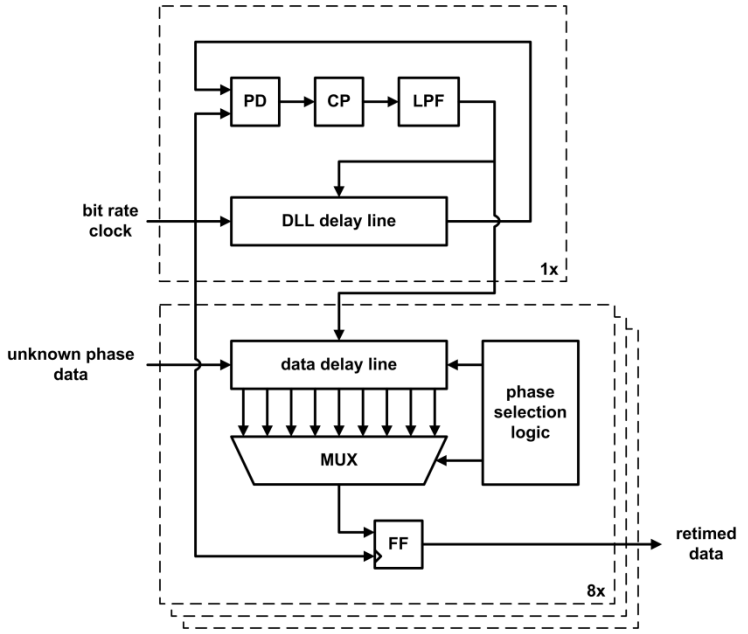
Phase Aligner



(The above picture is just for "easy representation". In reality the sampling clock phase is fixed and the data phase is adjusted.)

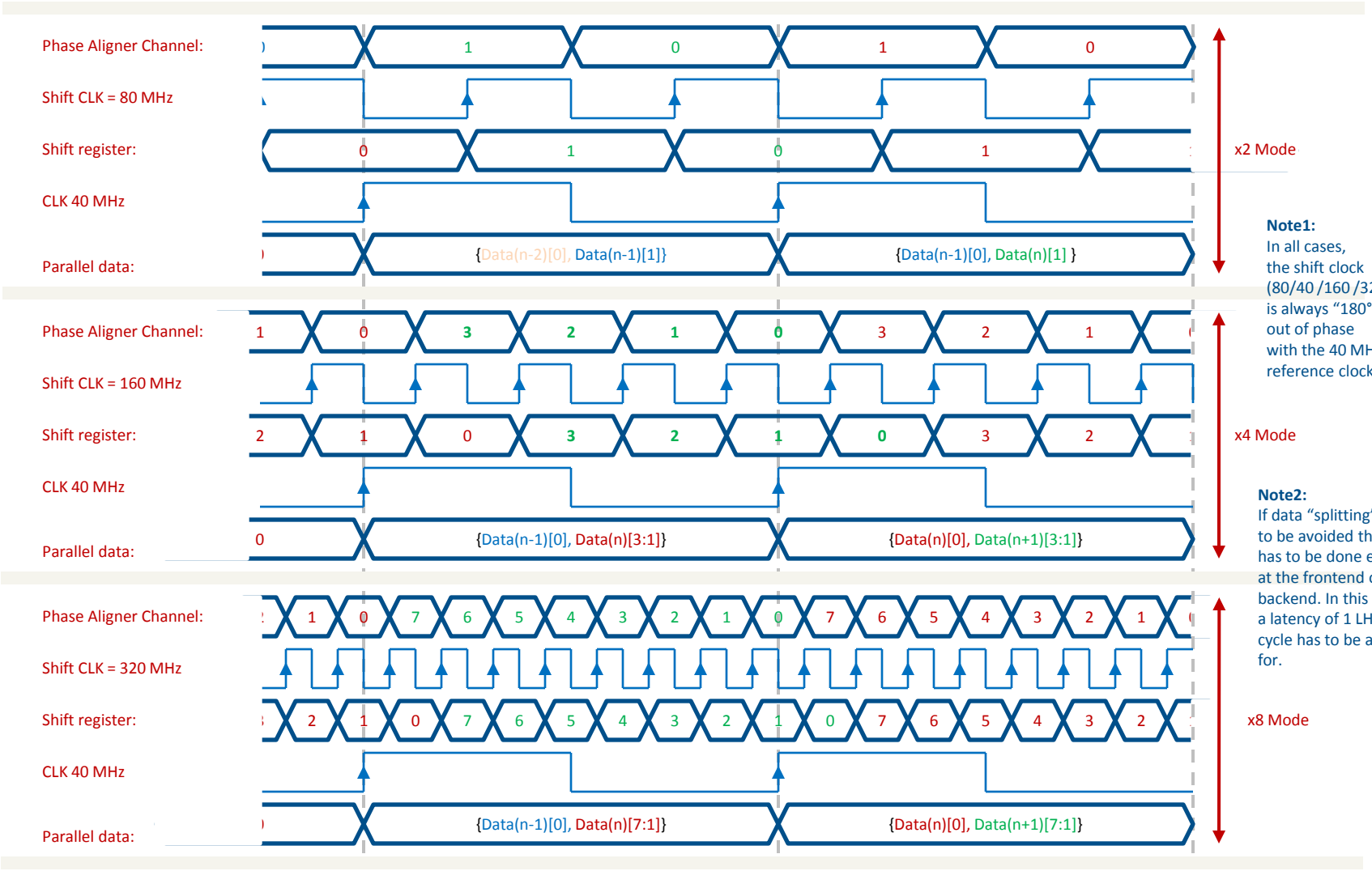
- The total delay line delay is equal to 7/4 T_{bit}
- The delay line is divided into 14 equal delay intervals $T_{bit}/8$
- In the automatic mode the circuit can tolerate jitter which is ±3/8 T_{bit}





- One master DLL and eight replica delay lines
- Three modes of operation:
  - Static phase selection:
    - A system calibration must be done
  - Training with learned static phase:
    - 1st a training pattern is sent to the GBTX over the e-Link
    - 2nd after training the phase is fixed:
  - Automatic phase tracking:
    - No system calibration required
    - No need for DC balanced data
- Unused channels can be powered Off
- Power: 4 mW (for 8 channels)

eLink Data Latency

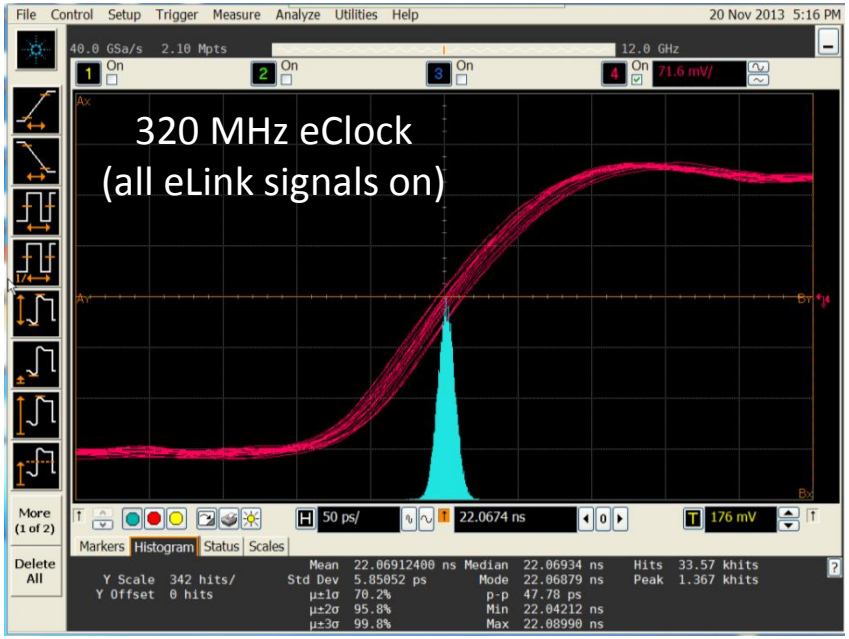


Important note:
A “word” might (it most likely will) span across a 40 MHz clock cycle boundary! (De-Serializer doesn’t know about the data structure!)
How the words will split depends on the link “return path” delay and on the phase programmed on the phase aligner.

Tx eClock Jitter

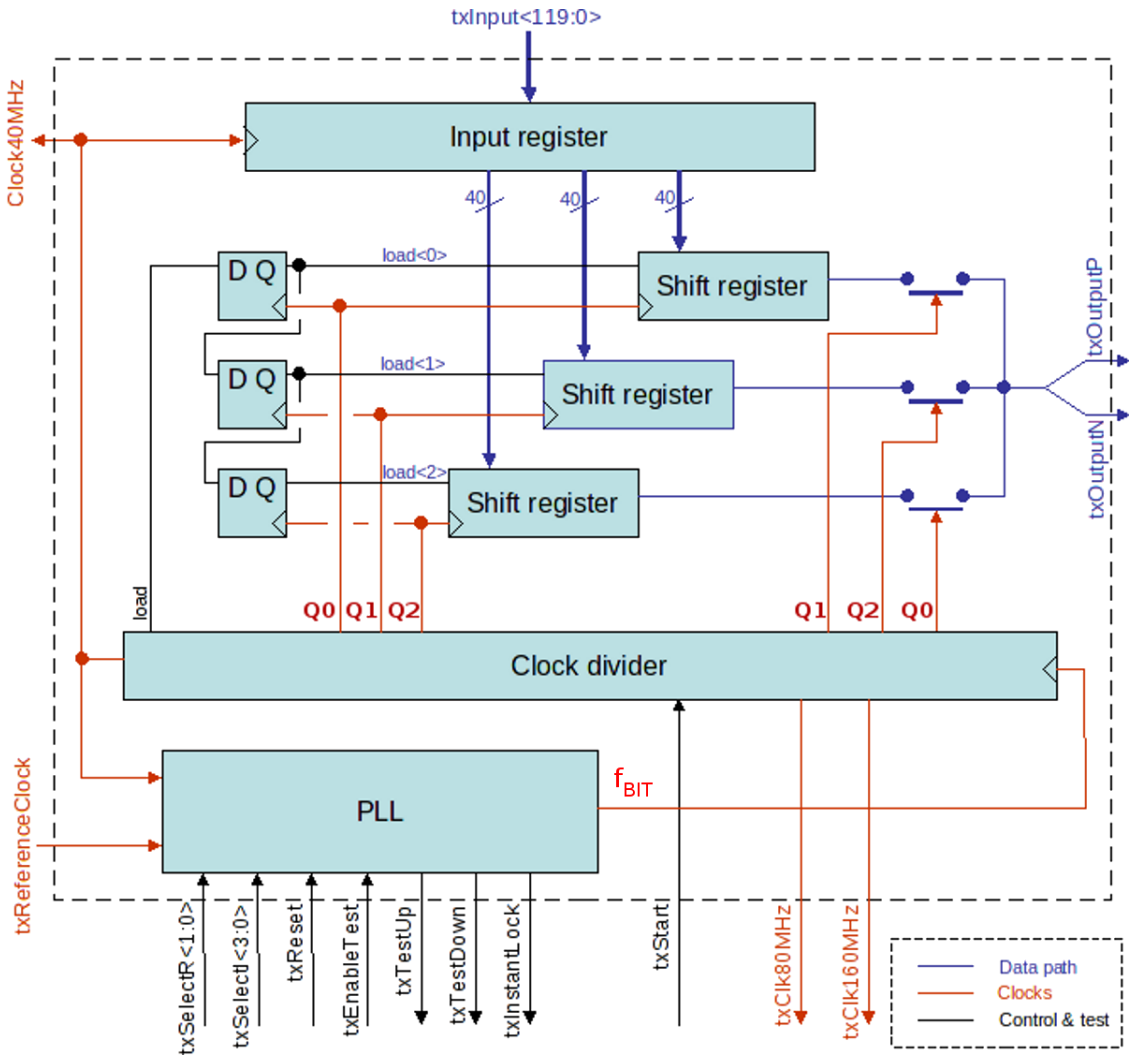
- "Absolute jitter"
  - Scope triggered by the FPGA transmitter reference clock
  - SLVDS driver with maximum current settings

eLink Clocks	Simplex Tx Operation	
Frequency	Jitter σ	Jitter P-P
[MHz]	[ps]	[ps]
40	6.0	47.8
80	5.9	45.0
160	5.6	49.4
320	5.7	44.4

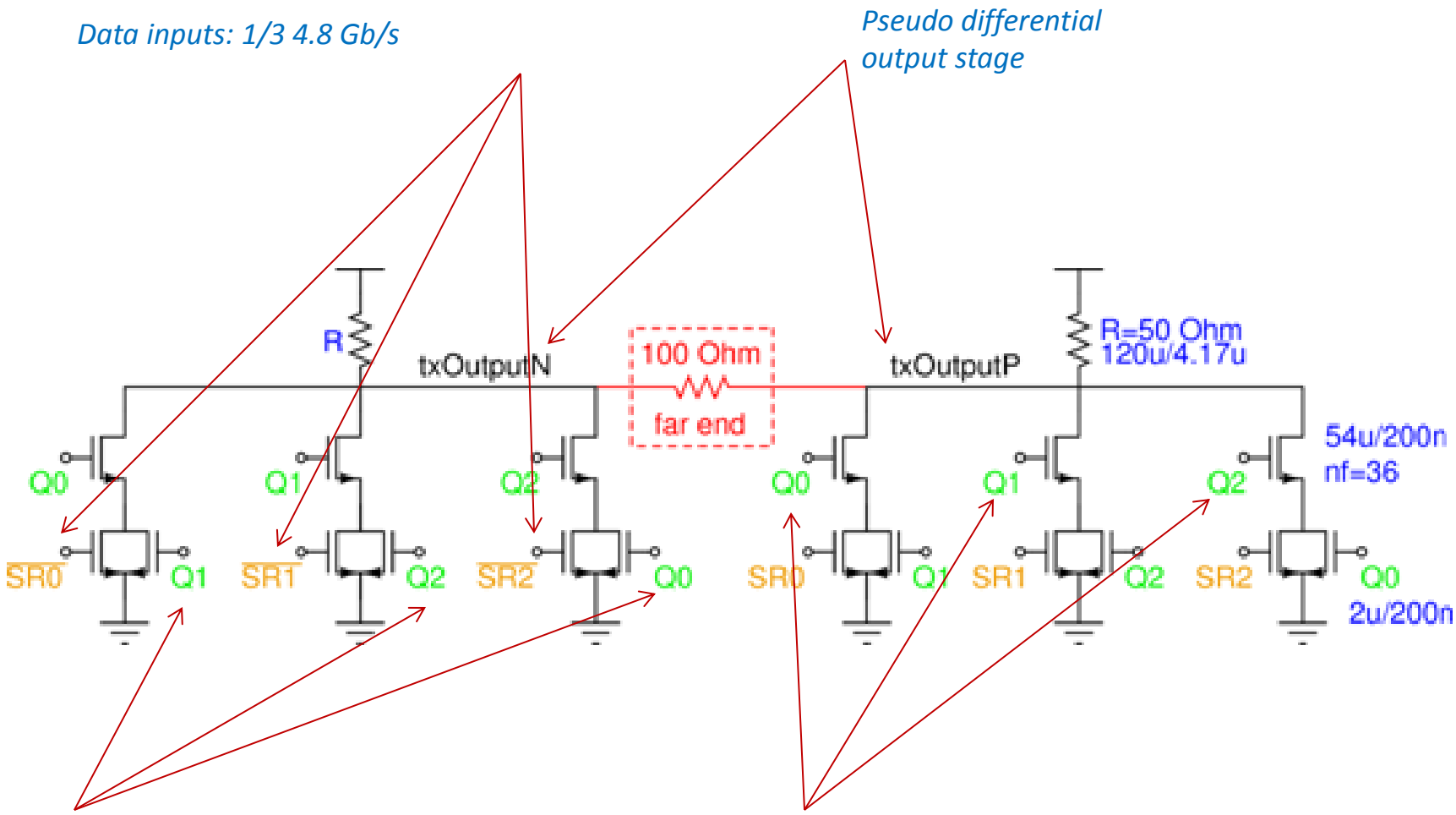


Serializer: Architecture

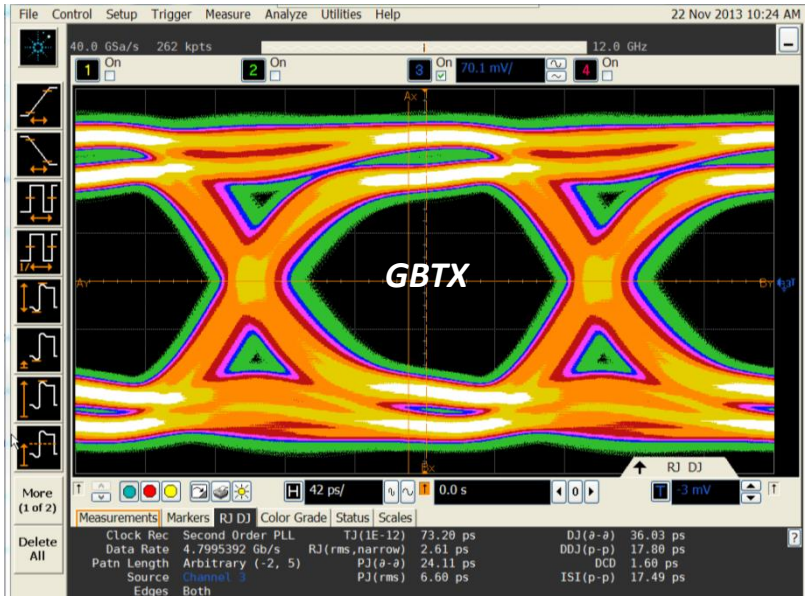
- Serializer:
  - 4.8 Gb/s
  - 120-bit shift register
    - 3 × 40-bit shift register (f=1.6 GHz)
    - 3-to-1 fast multiplexer (f=4.8 GHz)
- Data path:
  - No SEU protection
  - SEUs handled by the Reed-Solomon CODEC
- Clock divider:
  - Divide by 120
  - f = 4.8 GHz
  - Triple voted for SEU robustness
- PLL:
  - SEU hardened VCO
  - SEU hardened Clock Divider
    - Based on "custom" dynamic flip-flop
  - The PLL clock is used a the transmitter master clock (and not the reference clock)

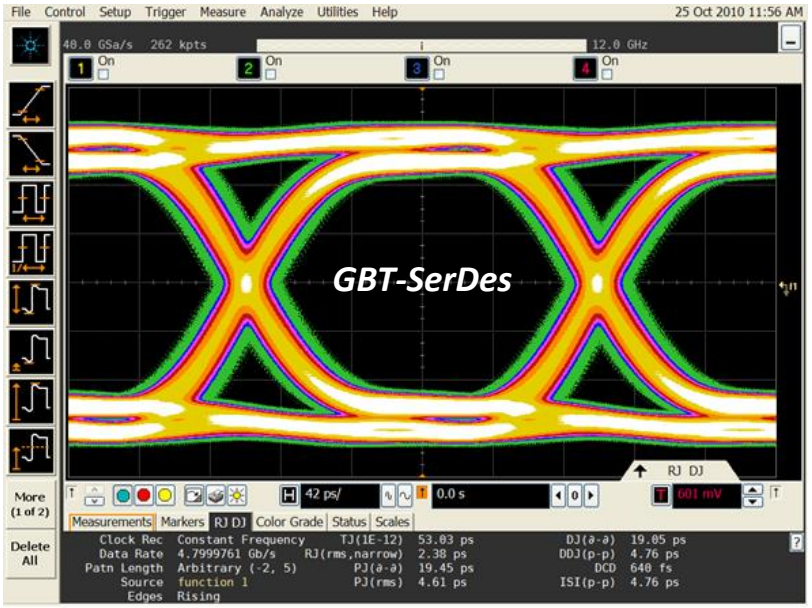


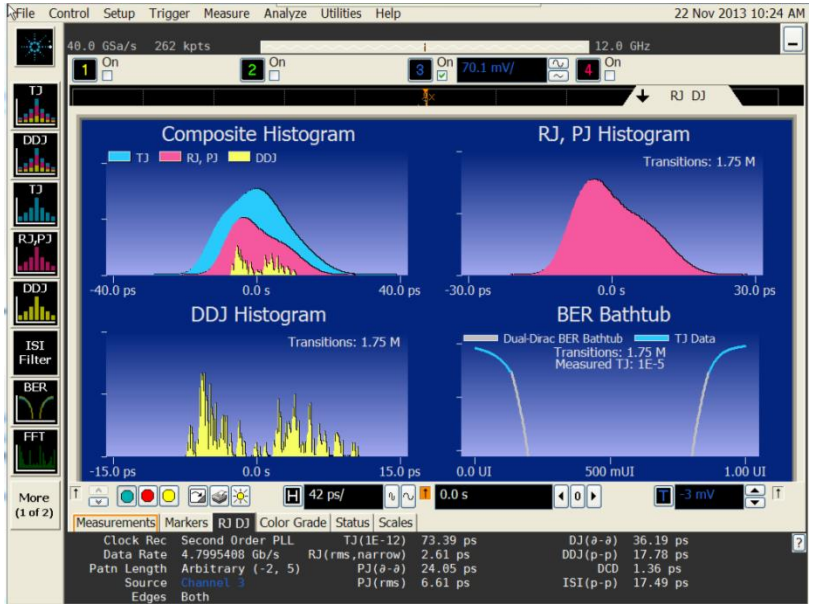
Fast-Mux / Line Driver



Tx Eye-Diagram





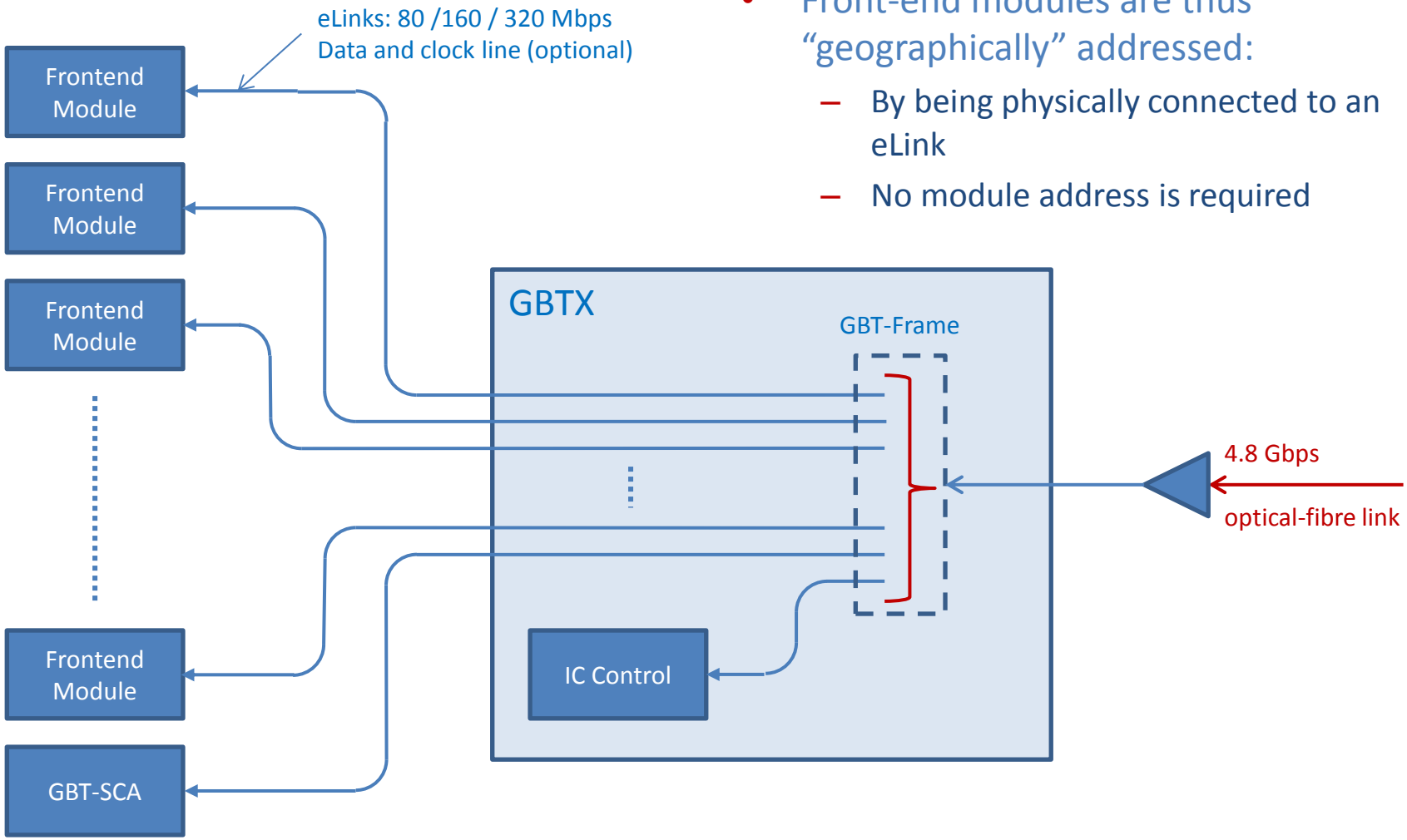


The same driver in the GBTX and GBT-SerDes!
However the clock phases were rotated to allow operation at 2.4 Gb/s
Simulations have not yet reveal the cause of the degradation!!!

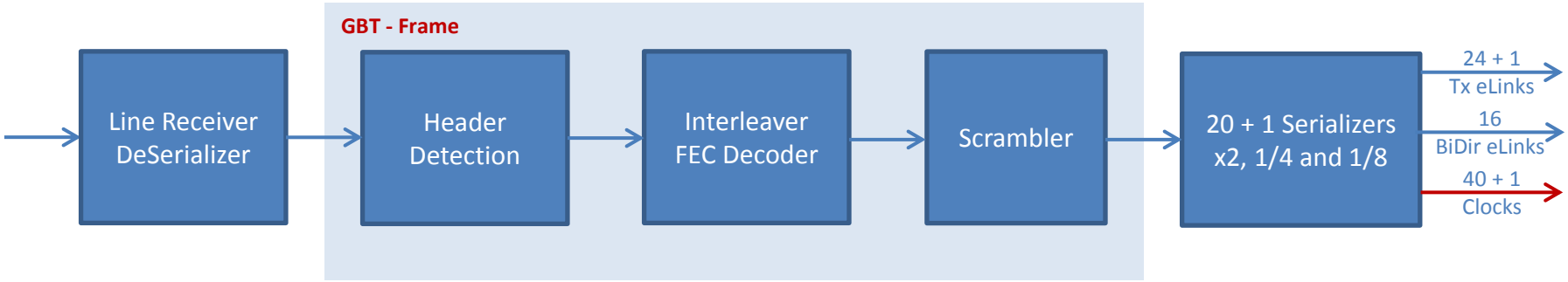
	GBTX	GBT-SerDes
TJ (1e-12)	73.2 ps	53.8 ps
RJ (rms)	2.6 ps	2.4 ps
PJ (d-d)	24.1 ps	19.4 ps
PJ (rms)	6.6 ps	4.6 ps
DJ (d-d)	36.0 ps	19.0 ps
DDJ (p-p)	17.8 ps	4.8 ps
DCD	1.6 ps	0.64 ps
ISI (p-p)	17.5 ps	4.8 ps
tr / tf	100 ps	80 ps
Max Data Rate	5.4 Gb/s	6.0 Gb/s

The GBTX down-link

- As for the up link, each eLink is associated with a specific set of bits in the frame
- Front-end modules are thus "geographically" addressed:
  - By being physically connected to an eLink
  - No module address is required

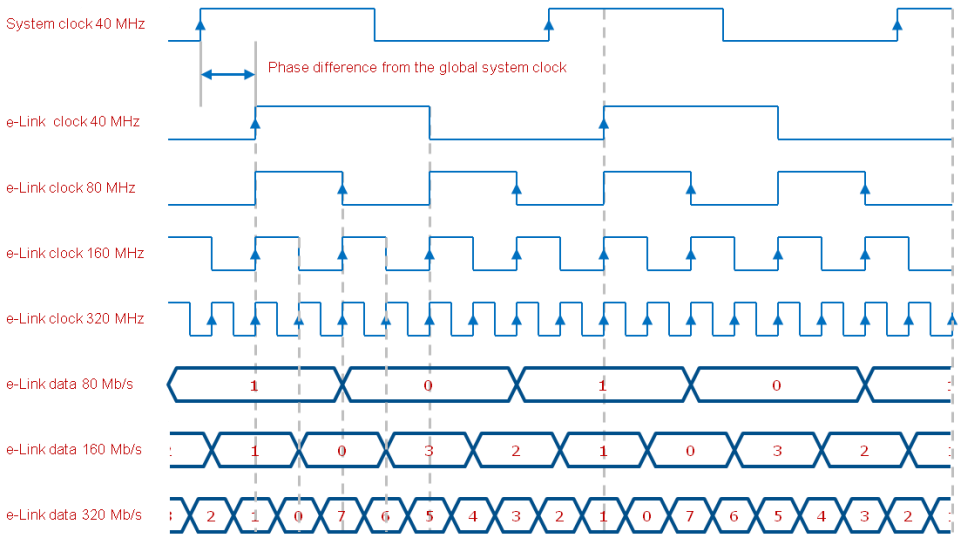


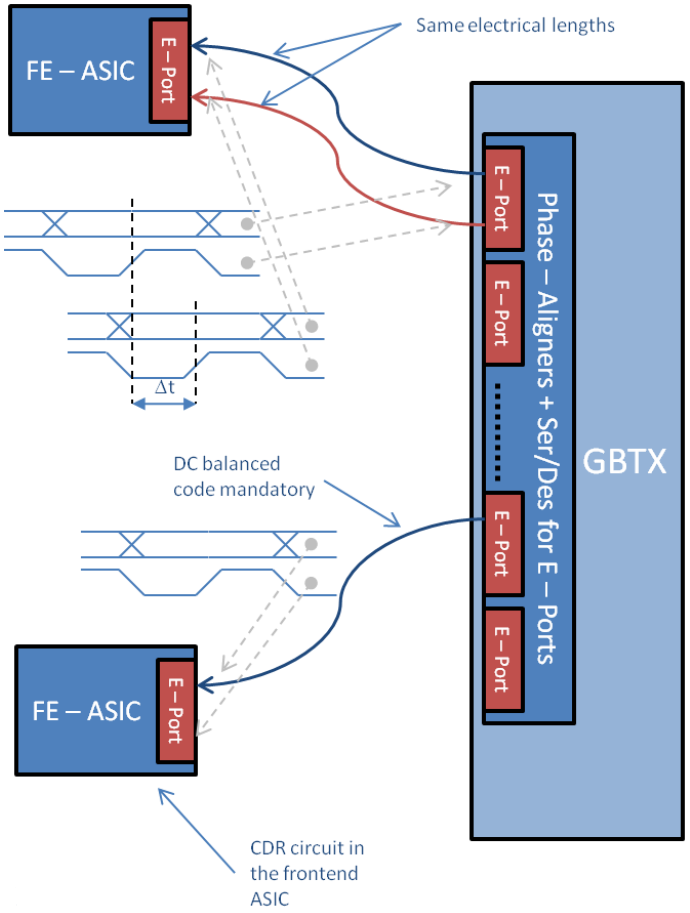
Receiver Architecture



Down eLink – Phase Alignment

- Data and clock phases are aligned at the output of the ePort drivers
- The system designer must ensure that clock and data phases “track each other” in the frontend modules
- eClocks frequency can be programed independently of the eLink data rate
- It is possible avoid the eLink clocks but clock recovery must be used in the frontend
  - In this case the data transmitted over the eLinks must be DC balanced



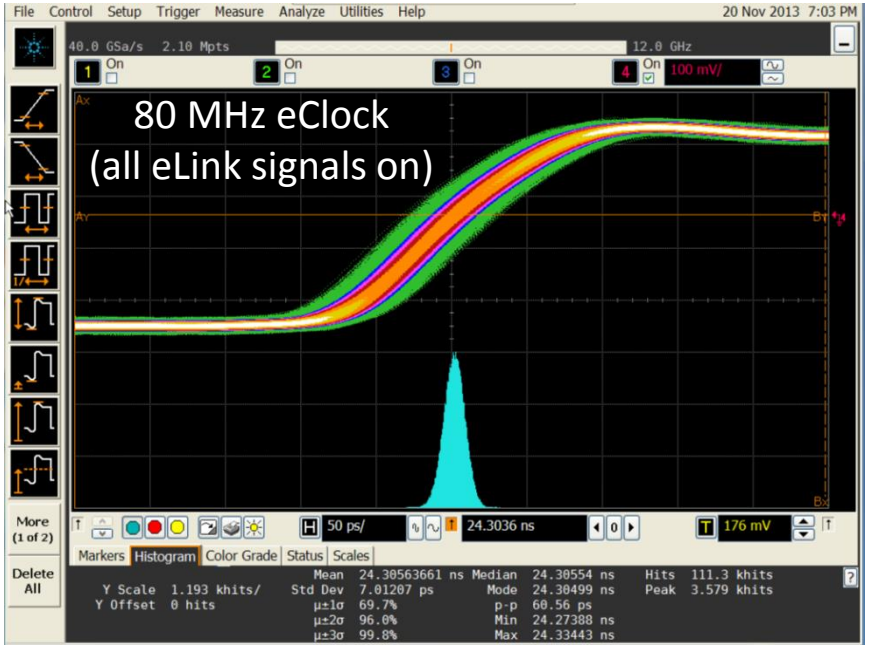


Rx eClock Jitter

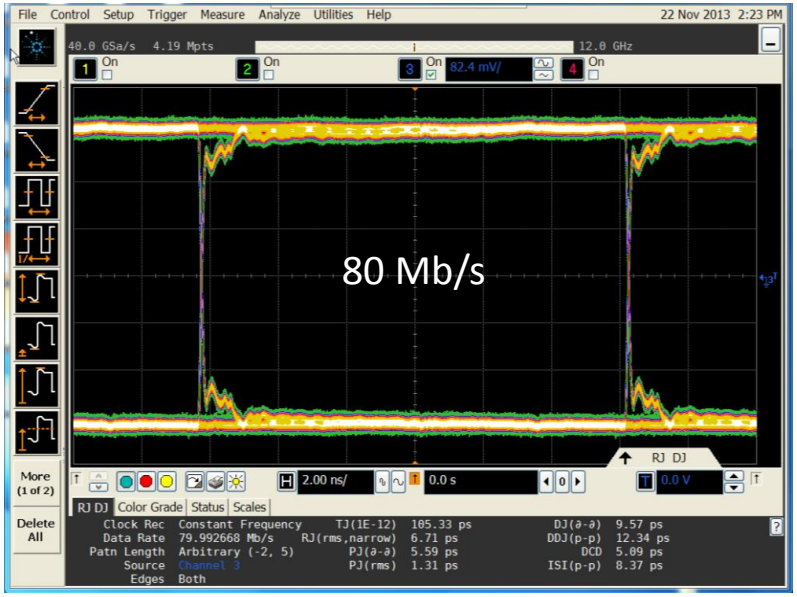
- "Absolute jitter"
  - Scope triggered by the FPGA transmitter reference clock
  - SLVDS driver with maximum current settings

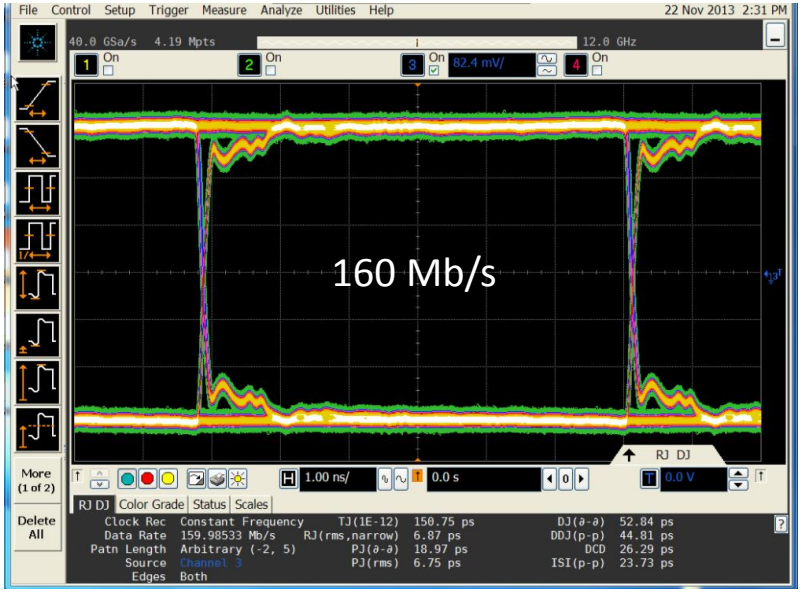
eLink Clocks	Simplex Rx Operation	
Frequency [MHz]	Jitter σ [ps]	Jitter P-P [ps]
40	7.2	60.5
80	6.8	56.7
160	5.9	45.6
320	5.8	47.8

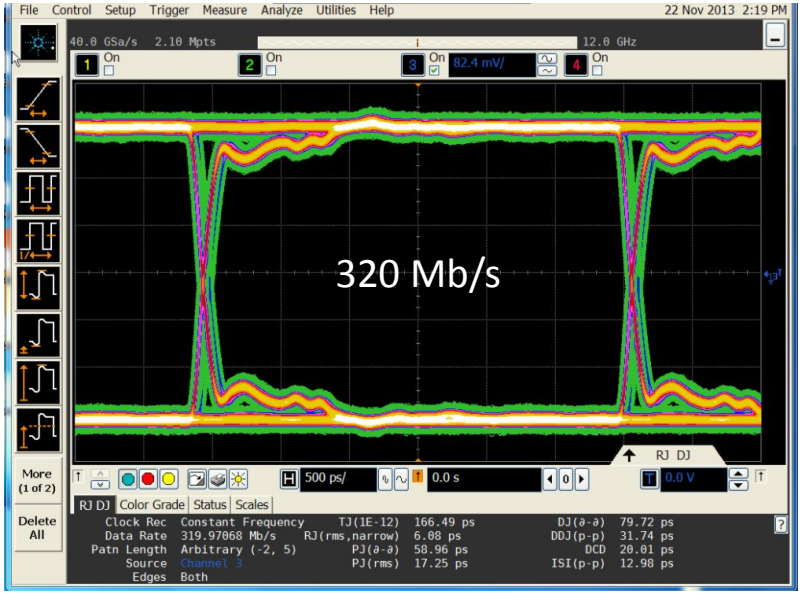
eLink Clocks	Duplex Rx Operation	
Frequency [MHz]	Jitter σ [ps]	Jitter P-P [ps]
40	7.2	58.9
80	6.7	55.0
160	5.9	47.2
320	5.7	43.9



eLink eye-diagrams

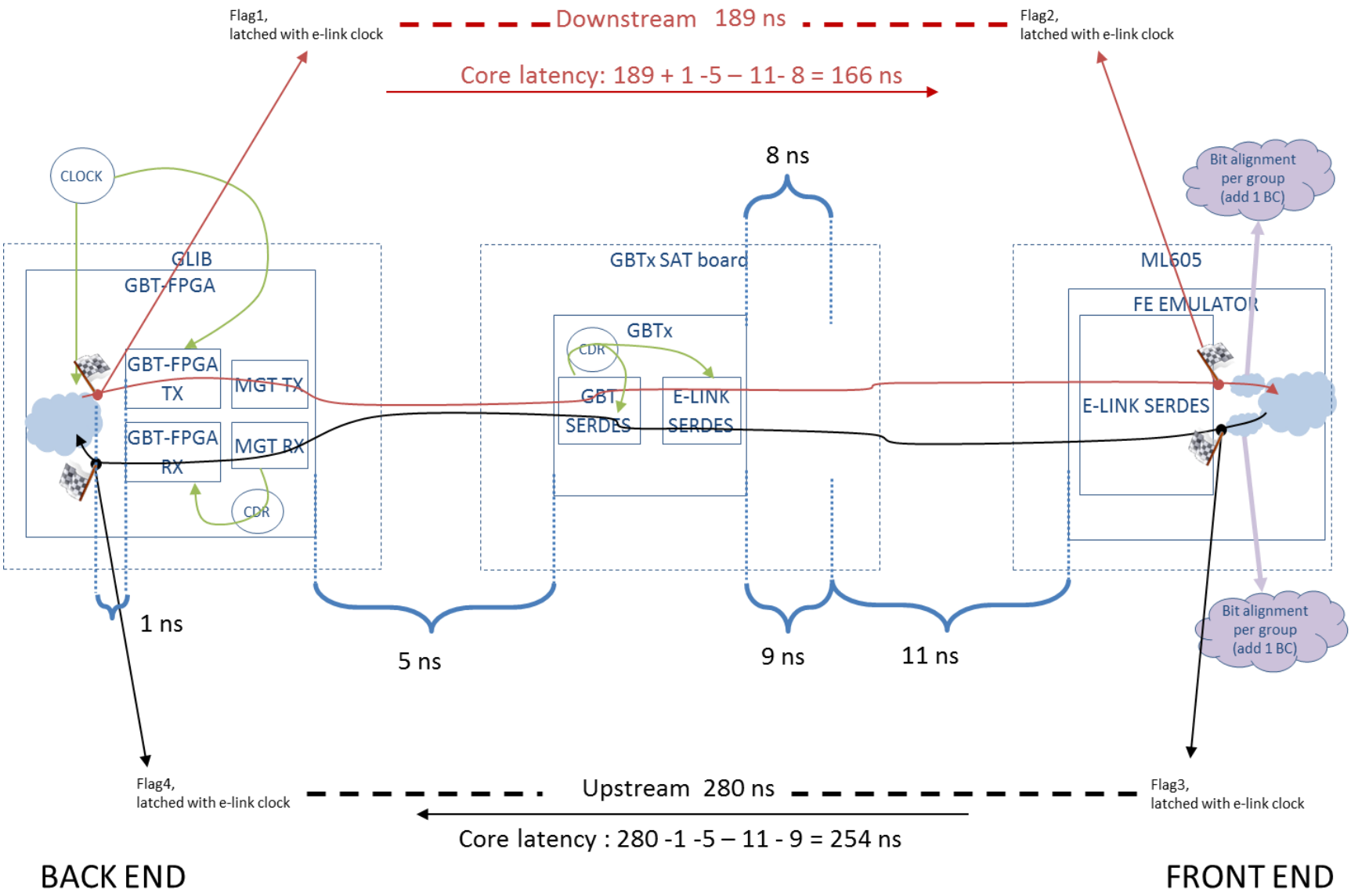




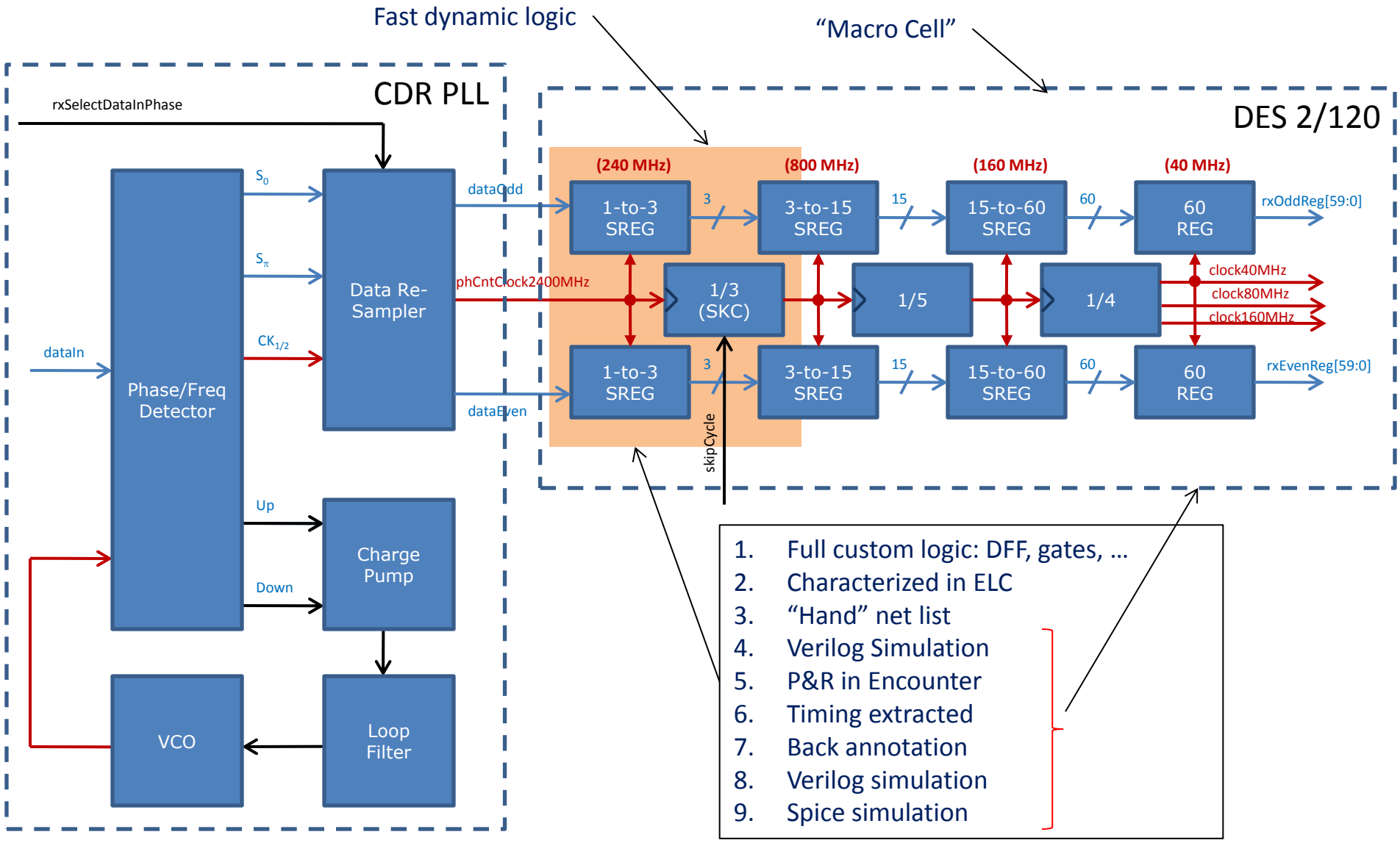


	80 Mb/s	160 Mb/s	320 Mb/s	Units
TJ (1e-12)	105.3	150.8	166.5	ps
RJ (rms)	6.7	6.9	6.9	ps
PJ (d-d	5.6	19.0	59.0	ps
PJ (rms)	1.3	6.8	17.2	ps
DJ (d-d)	9.6	52.8	79.7	ps
DDJ (p-p)	12.3	44.8	31.7	ps
DCD	5.1	26.3	20.0	ps
ISI (p-p)	8.4	23.7	13.0	ps

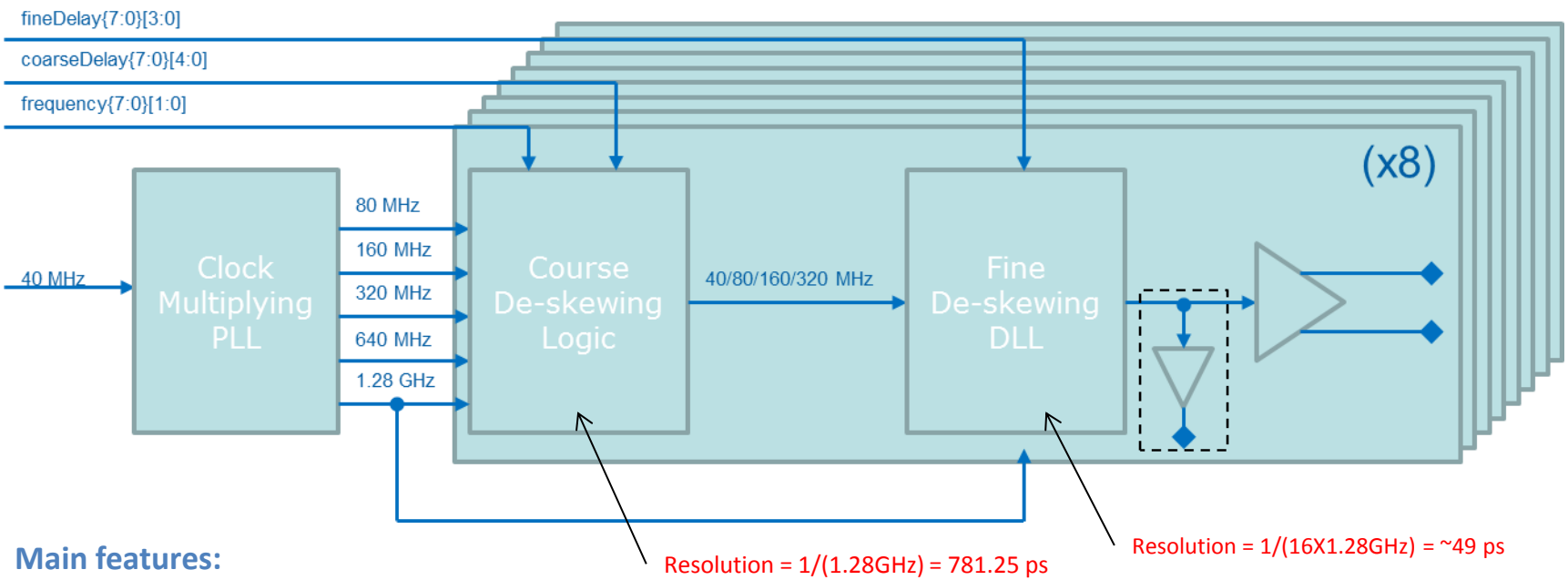
System Latency



DESerializer Architecture



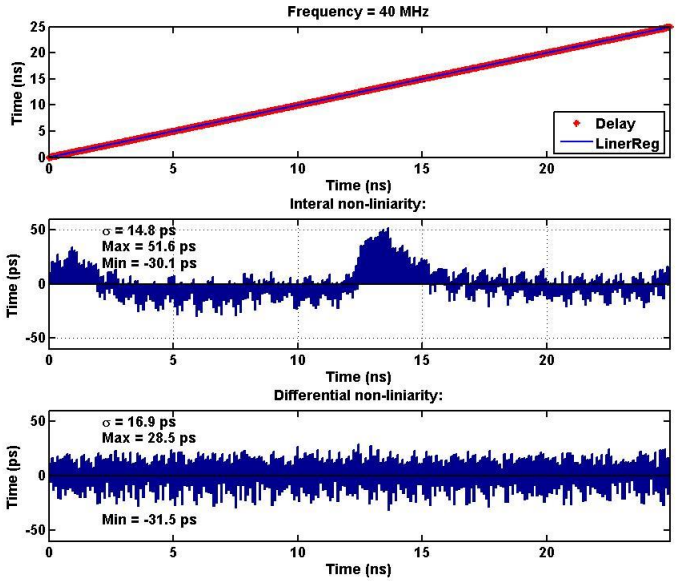
Phase Shifter

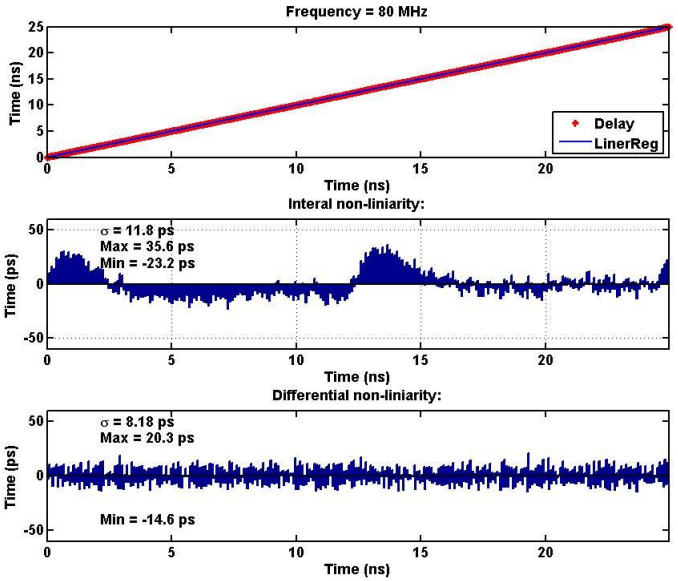


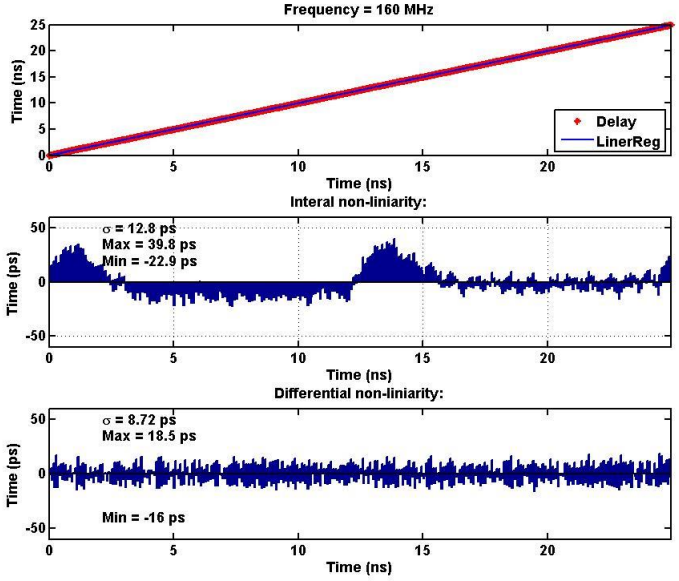
Main features:

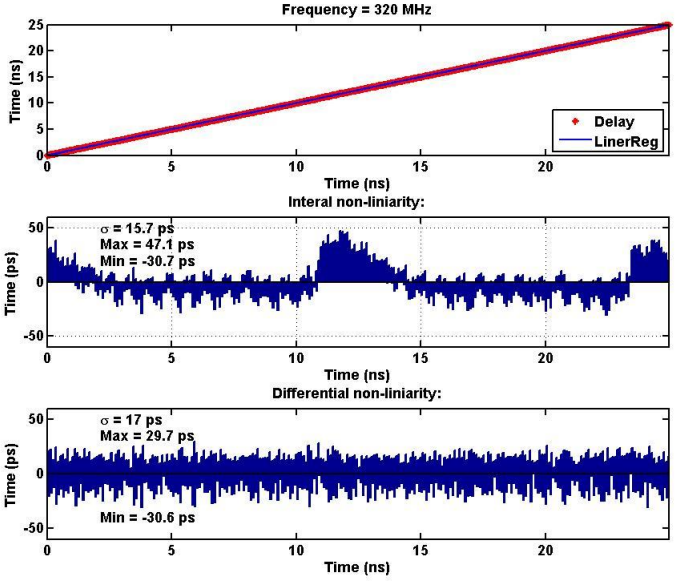
- 8 – channels
- Clock frequencies: 40, 80, 160 and 320 MHz
- Phase resolution: 48.8 ps
- Phase span: 0 to 2π
- 1 PLL + Counter generates frequencies: 40, 80, 160, 320, 640 and 1280 MHz
- 1 DLL per channel
- Mixed digital/analogue phase shifting technique:
  - Coarse deskewing – Digital
  - Fine deskewing – Analogue
- Differential non-linearity: < 6.7% LSB
- Integral non-linearity: INL < 6.5% LSB
- Power consumption: 5.6 mW/channel

Phase-Shifter Performance (1/3)









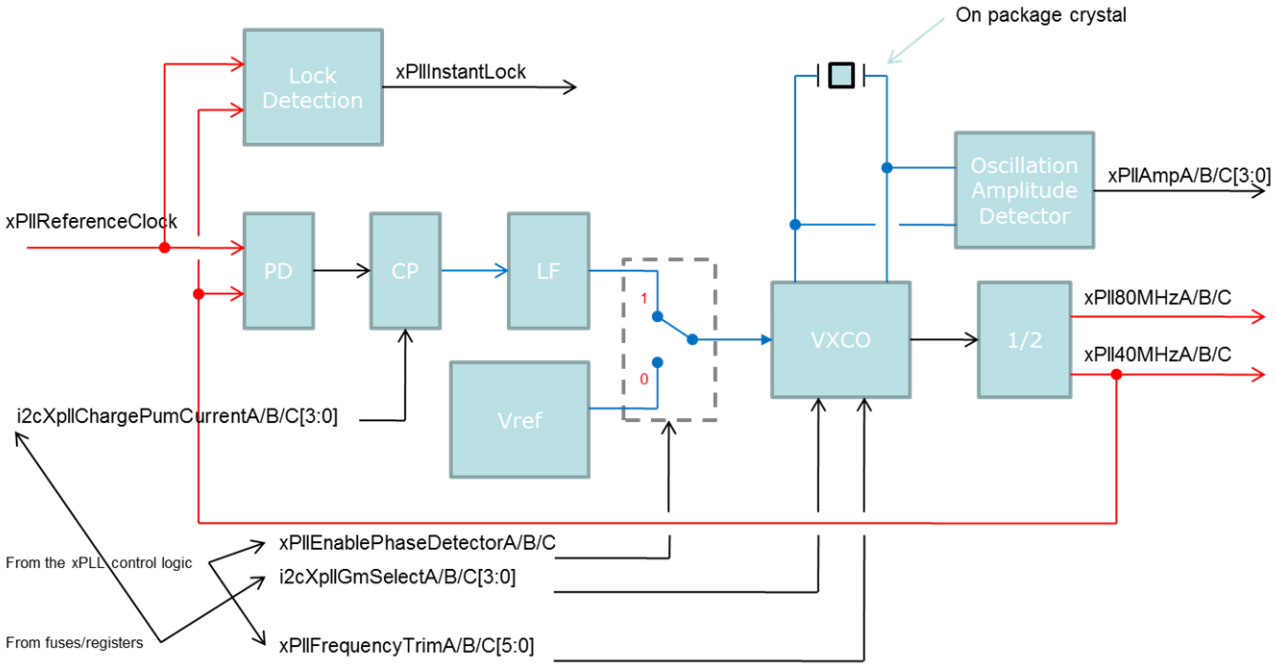
Phase-Shifter Performance (2/3)

Non-Linearity		Integral			Differential		
Frequency	Δt [ps]	σ [ps]	Max [ps]	Min [ps]	σ [ps]	Max [ps]	Min [ps]
40 MHz	50	14.8	51.6	-30.1	16.9	28.5	-31.5
80 MHz	50	11.8	35.6	-23.2	8.2	20.3	-14.6
160 MHz	50	12.8	39.8	-22.9	8.7	18.5	-16.0
320 MHz	50	15.7	47.1	-30.7	17.0	29.7	-30.6

Phase-Shifter Performance (3/3)

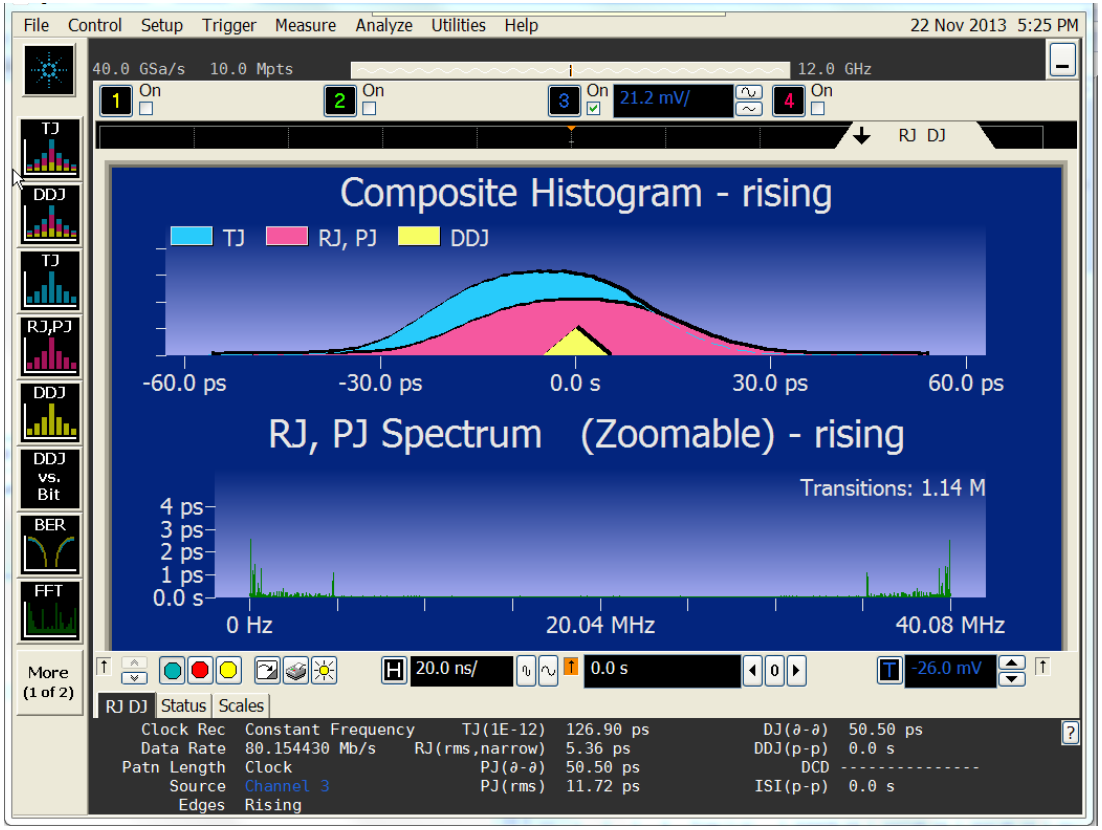
Jitter		Min Delay (0 ns)		Max Delay (25 ns)	
Frequency	Mode	σ [ps]	P-P [ps]	σ [ps]	P-P [ps]
40 MHz	Simplex Tx	3.8	37.0	4.4	40.7
80 MHz	Simplex Tx	3.4	36.7	3.8	37.5
160 MHz	Simplex Tx	4.8	36.2	8.5	48.6
320 MHz	Simplex Tx	13.5	63.0	15.2	67.3
40 MHz	Duplex	3.9	40.9	4.4	45.0
80 MHz	Duplex	3.6	35.0	3.8	37.5
160 MHz	Duplex	5.4	42.3	8.9	49.5
320 MHz	Duplex	13.4	65.7	15.3	70.6

xPLL



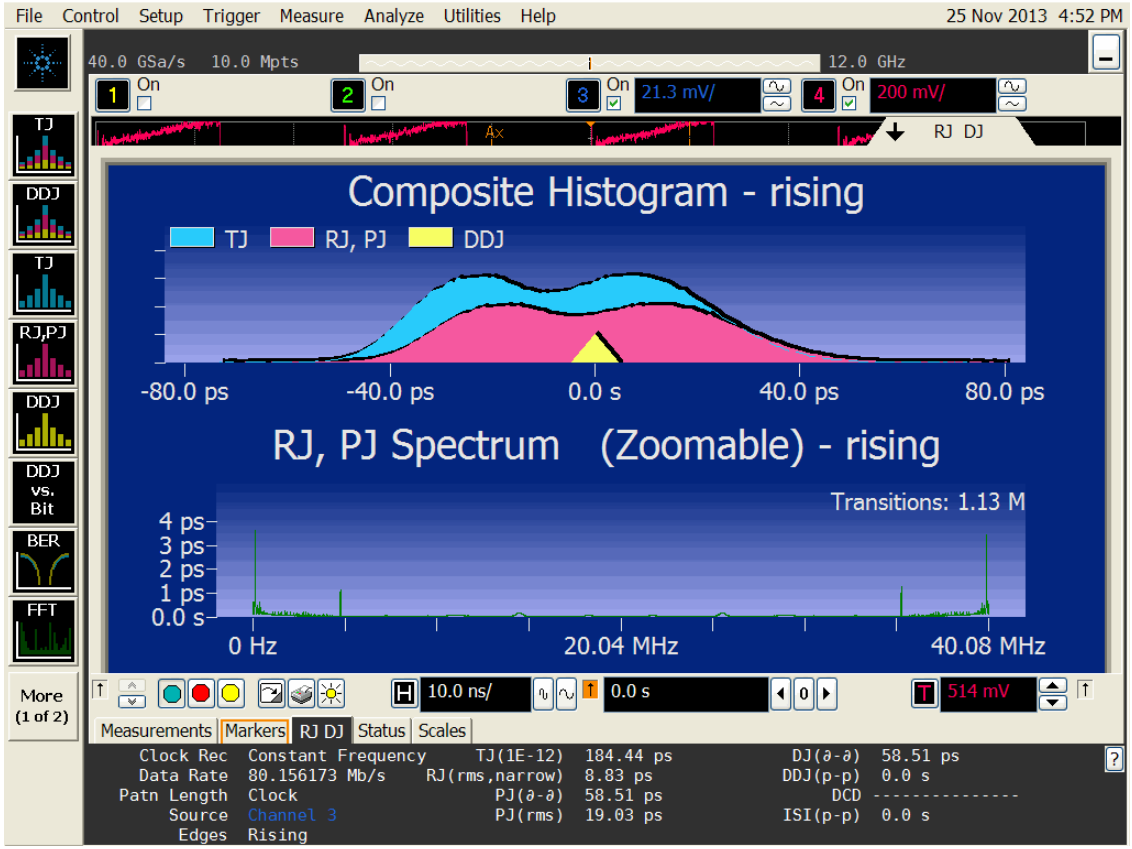
- Phase-Locked Loop based on a Quartz Crystal Oscillator (VCXO)
- On package Quartz Crystal tailored to the LHC frequency
- Three main functions:
  - Clock reference (for systems without clock reference)
  - Jitter cleaning PLL for systems with a “noisy” system clock
  - Watchdog clock source

xPLL Performance – VCXO Mode



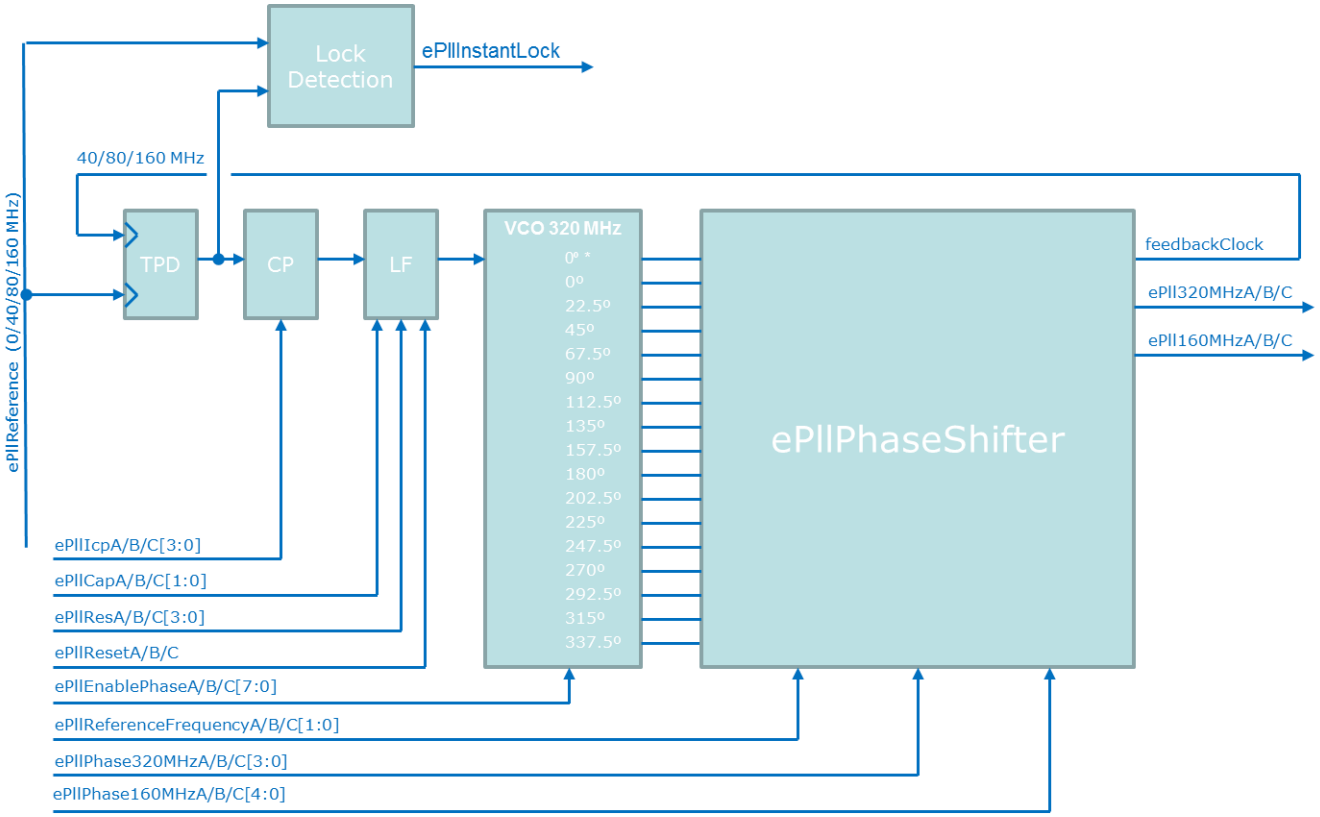
VCXO Mode	40 MHz	Units
TJ (1e-12)	126.9	ps
RJ (rms)	5.4	ps
PJ (d-d	50.5	ps
PJ (rms)	11.7	ps
DJ (d-d)	50.5	ps

xPLL Performance – PLL Mode



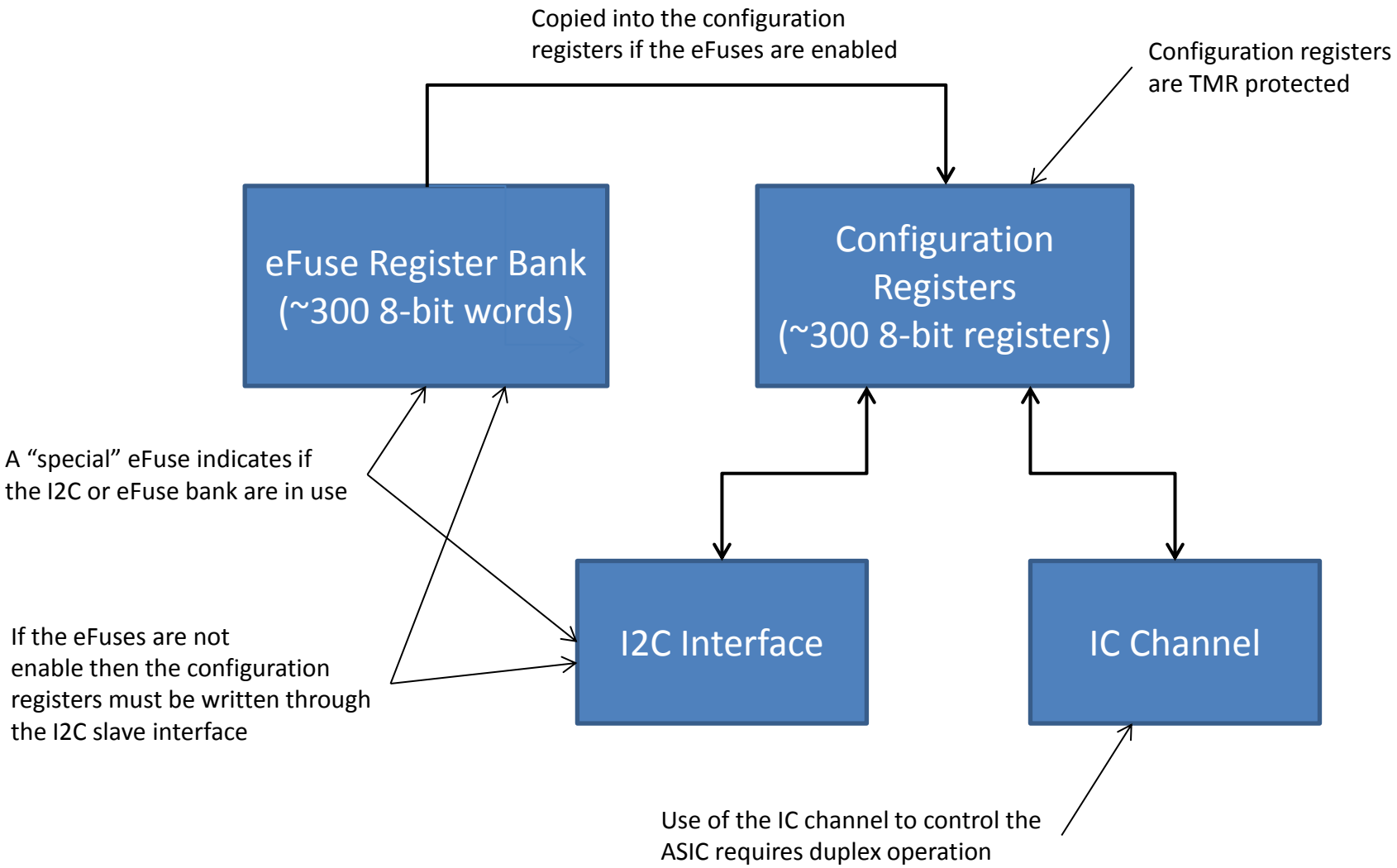
VCXO Mode	40 MHz	Units
TJ (1e-12)	184.4	ps
RJ (rms)	8.8	ps
PJ (d-d	58.5	ps
PJ (rms)	19.0	ps
DJ (d-d)	58.5	ps

ePLL

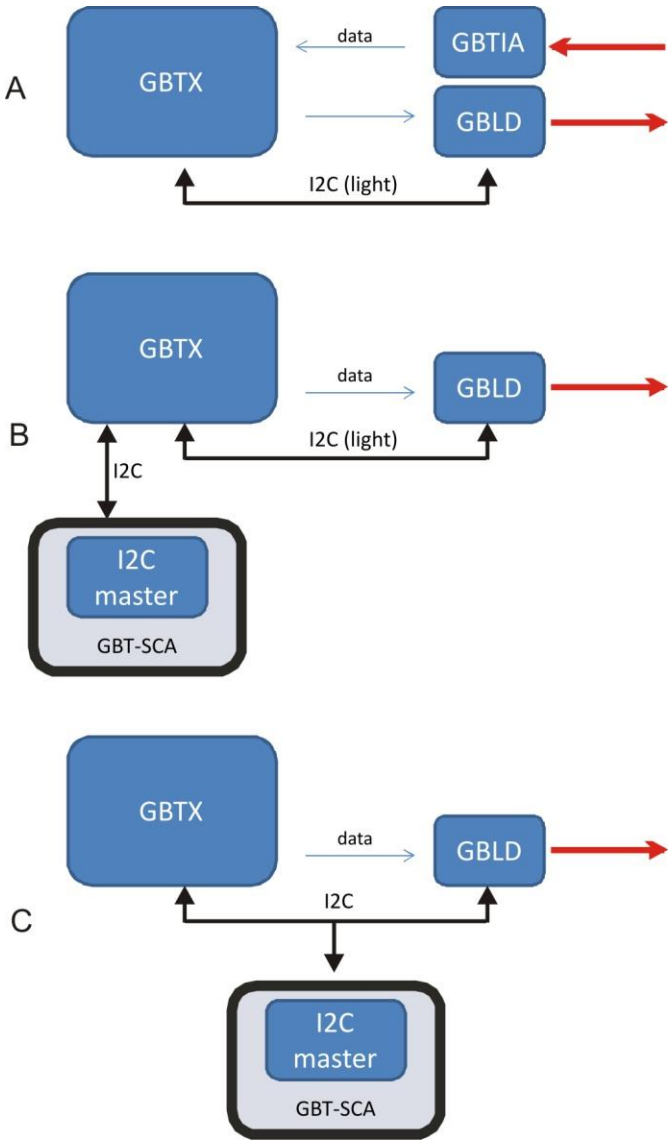


- Two ePLLs are used to generate the 160 and 320 MHz clocks needed to run the ePorts at 160 and 320 Mb/s respectively
- It allows phase shifting the internal clocks with 200 ps resolution
  - This is only for internal timing, can't be used for phase adjust of the eLink clocks
- The operation of the ePLLs is transparent to the users.
- The performance of the device is reflected on the ePort clocks at 160 and 320 MHz

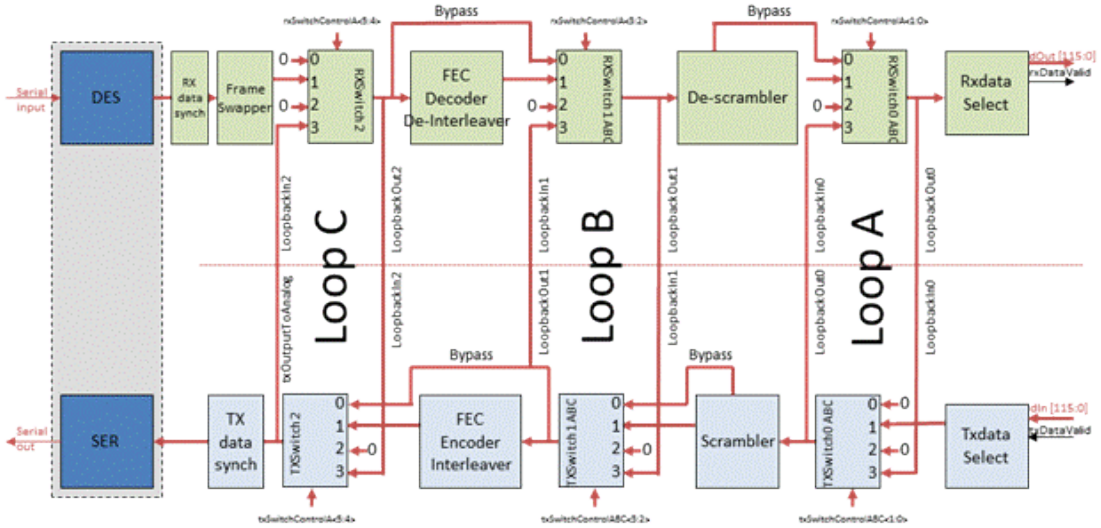
Controlling the GBTX



Interfacing with the GBLD



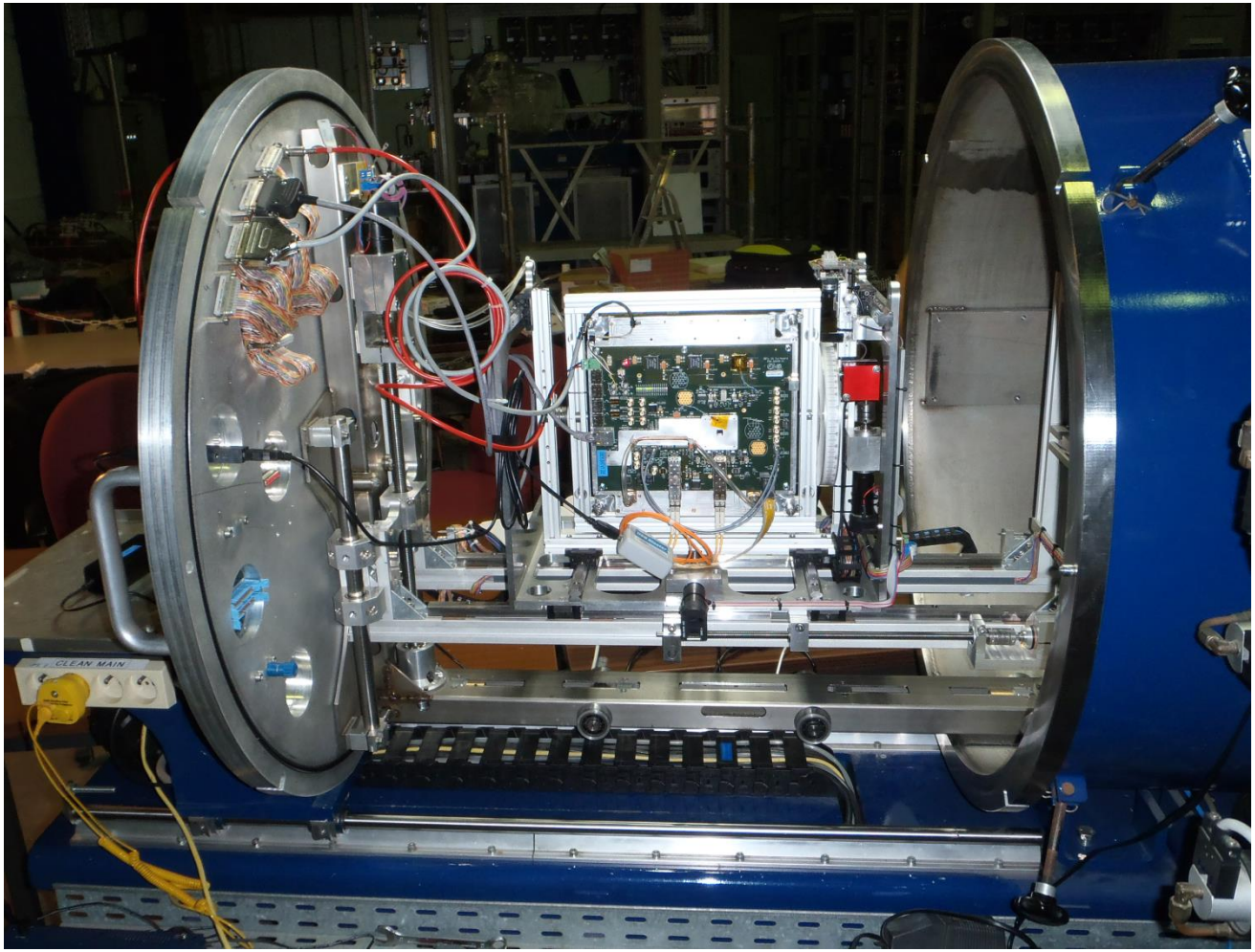
Built-in Test Features



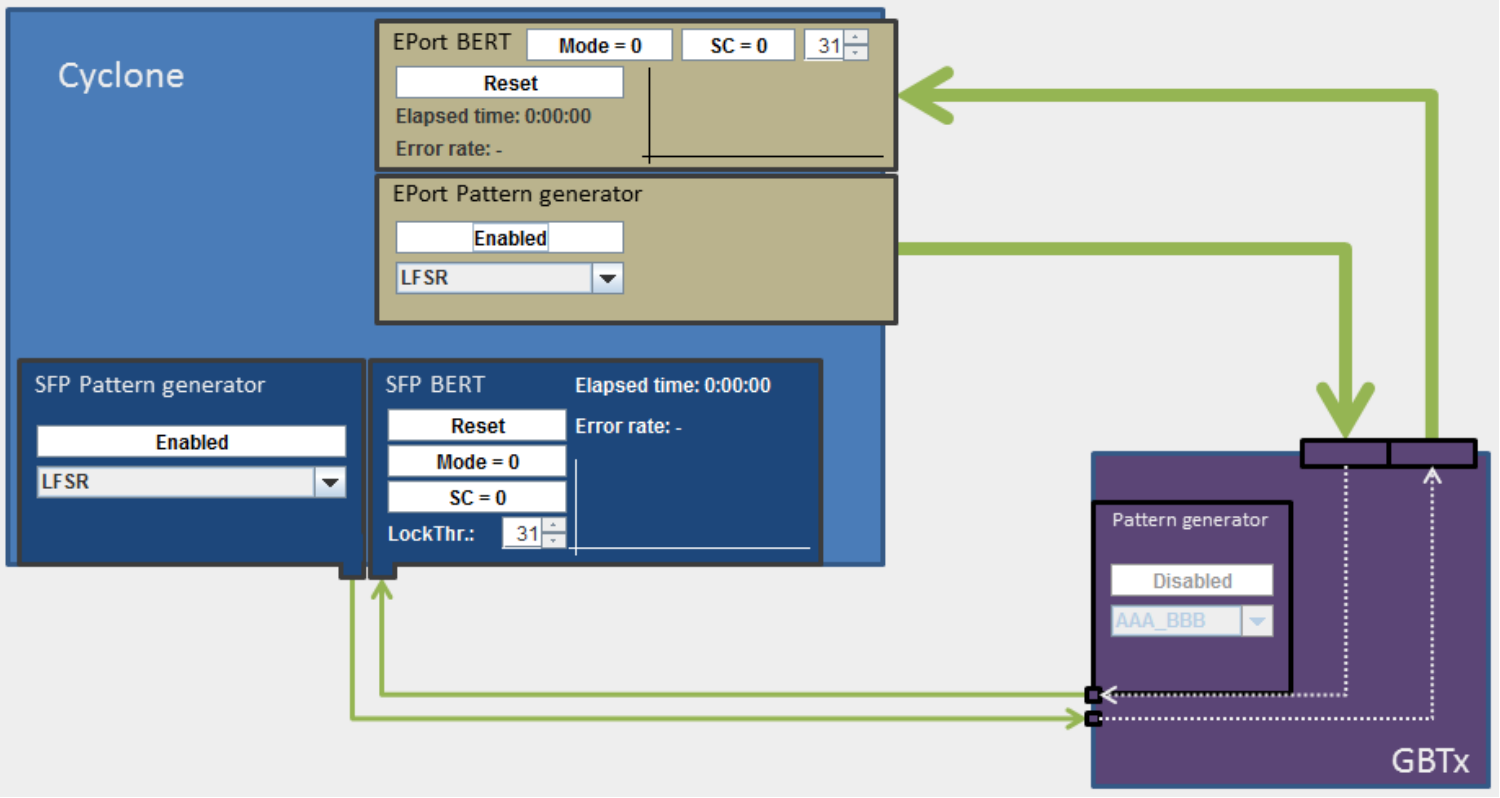
- A series of “loopbacks” allow to test the chip with different levels of depths:
  - Fast-serial to fast-serial
  - ePort to ePort
  - ePort – driver to ePort – receiver
- Tx high speed test patterns:
  - Header + AAA_BBBB_AAAA_BBBB_AAAA_BBBB_AAAA_BB
  - Header + counter[25:0] + counter[29:0] + counter[29:0] + counter[29:0]
  - Header + 4’h0 + prbs[6:0] x 16
- Rx bit error counter:
  - Works with the fixed pattern
- ePort patterns to validate the GBTX to Frontend timing

SEU TEST – Louvain-la-Neuve

Heavy Ion Irradiation Facility (HIF)

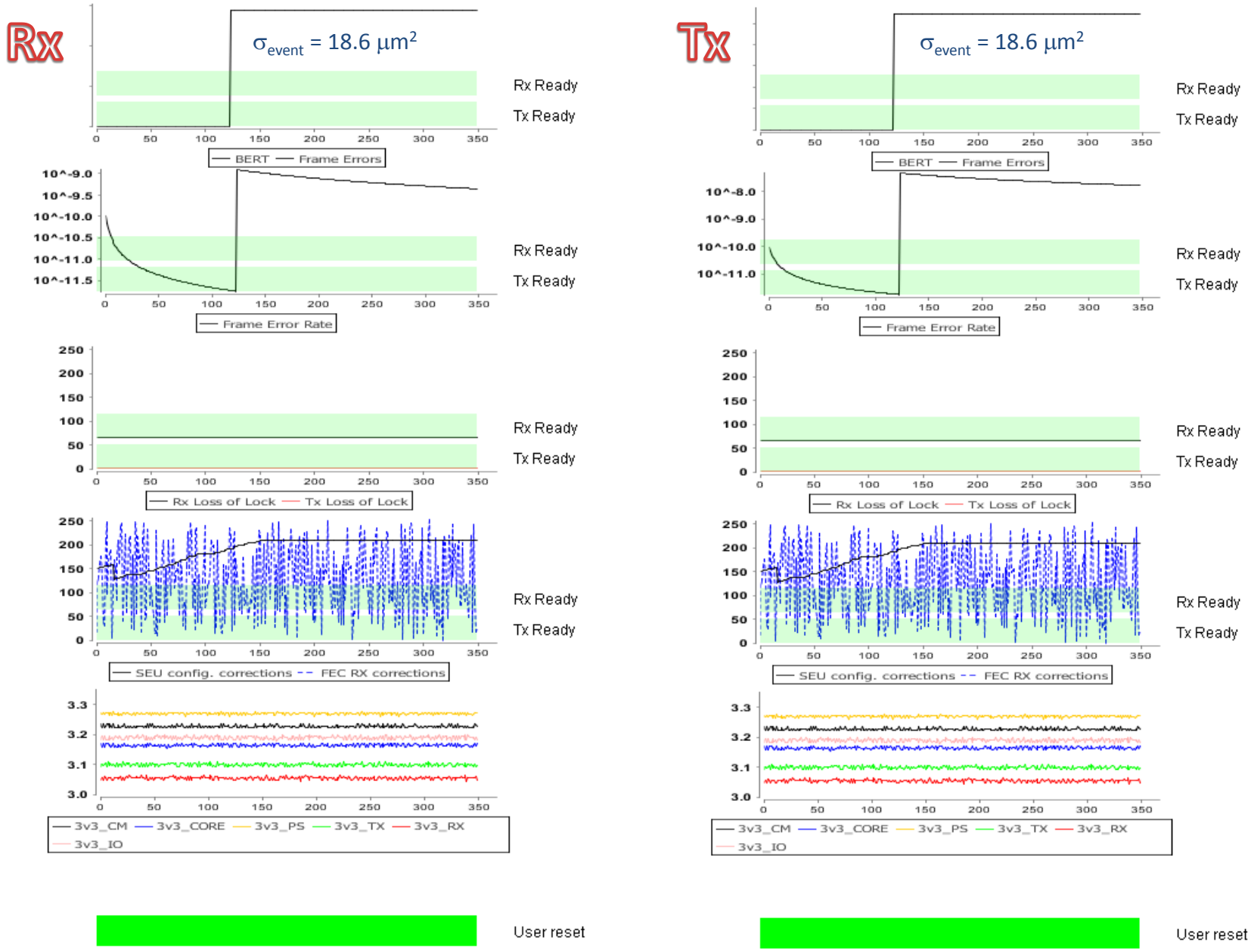


SEU Test Setup

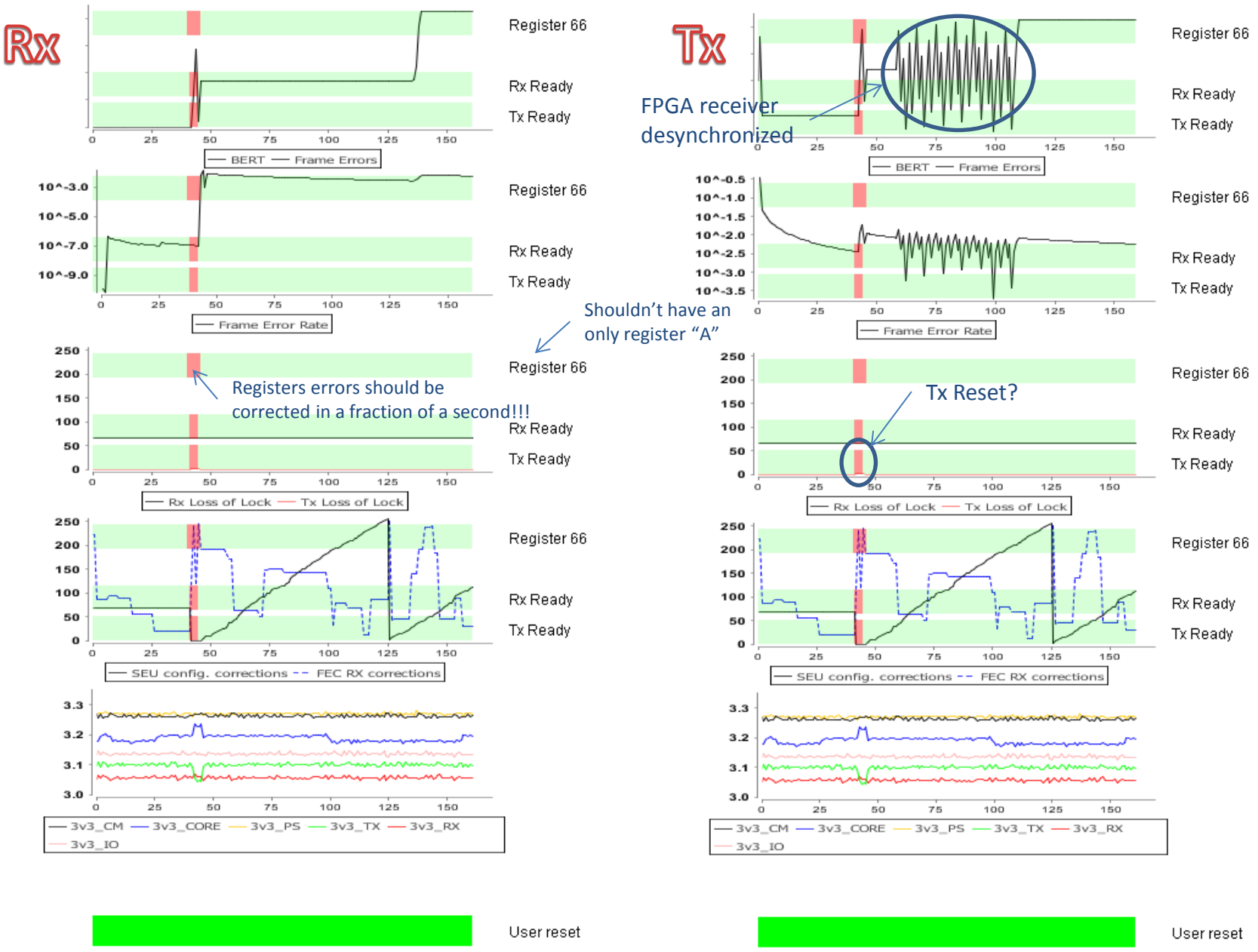


- Tested Cases:
  - High Speed loopback
  - Simplex Tx:
    - 80 and 160 Mb/s ePorts
    - Max and min phase-aligner delay
  - Simplex Rx:
    - 80 Mb/s ePorts
  - Duplex:
    - 80 Mb/s ePorts
  - "Special" duplex
    - Both Tx and Rx clocked by the reference clock
- Ion type:
  - Ar – 372
    - LETeff = 10.2 MeV/ mg cm2
  - Ne – 235
    - LETeff = 3 MeV/ mg cm2
- 8 hour time slot:
  - 22 "test" runs
- Faced some problems with the test setup:
  - "Fixed" latency FPGA Rx needs to be used
  - Robust lock tracking FPGA Rx must be used

Duplex, ePorts 160 Mb/s , Ne: LETeff = 3 MeV/ mg cm^2, flux 15.4k i/cm^2 s



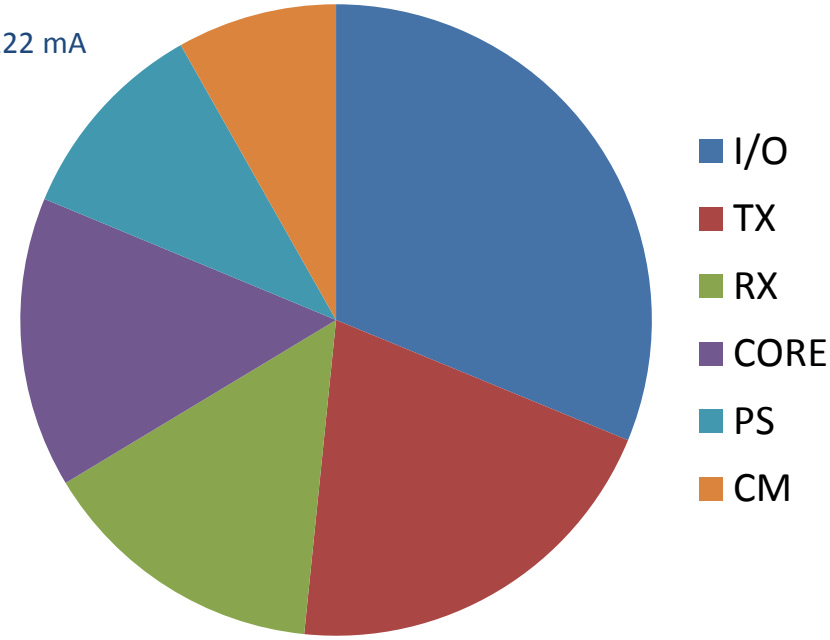
Duplex, ePorts 160 Mb/s , Ar: LETeff = 10.2 MeV/ mg cm^2, flux 8k i/cm^2 s



GBTX Power Consumption (1/2)

All power supplies voltages = 1.5V except EfusePower = 3.3V

- I/O (gndIO/vddIO):
  - P = 41 × 8.2 mW (Data SLVS-Tx) + 41 × 8.2 mW (CLK SLVS-Tx) + 41 × 0.65 mW (SLVS-Rx) = **698 mW**, I = 466 mA
- TX (gndTx/vddTx):
  - P = **456 mW**, I = 304 mA
- RX (gndRx/vddRx):
  - P = **330 mW**, I = 220 mA
- CORE (GND/VDD):
  - P = 305 mW (Standard cells) + 8 × 3.5 mW (Phase-Aligners) = **333 mW**, I = 222 mA
- PS (gndPS/vddPS):
  - P = 42 mW (PLL) + 8 × 16 mW (channel) + 8 × 8.2 mW (SLVS-Tx) = **236 mW**, I = 157 mA
- CM (gndCm/vddCm):
  - P = 2 × 41.5 mW (E-PLL) + 100 mW (XPLL) = **183 mW**, I = 122 mA
- E-Fuses (EfusePower):
  - P = **465 mW** , I = 141 mA
  - (Only during e-fuse programming. Not added to the total power figure below.)
- **Total:**
  - **P = 2.2 W**
  - (This is worst case power consumption: all functions ON, worst case simulations)



GBTX Power Consumption (2/2)

Case study:

- *Hypothetical* CMS Tracker upgrade configuration:
  - E-Links:
    - 20 × Data-In @ 160 Mb/s
    - 1 × Clock @ 160 MHz
    - 2 × Data-Out @ 160 Mb/s
  - Phase-Adjustable clocks:
    - 2 × Clock @ 40 MHz
    - 2 × Clock @ 160 MHz

Mode:	TRANSCEIVER
E-Links:	
Data rate [Mb/s]:	160
# Data outputs:	2
# Clock outputs:	1
# Data inputs:	20
EC-Channel:	
State:	Disabled
Phase-Shifter:	
State:	Enabled
# Channels	4
Circuit:	Power [mW]
Transmitter:	
	456
Receiver:	
	330
Clock Manager	
E-PLL:	83
XPLL:	100
Total:	183
Phase-Shifter:	
PLL:	42
Channel:	64
SLVS-TX:	33
Total:	139
I/O:	
Data SLVS-Tx:	16
CLK SLVS-Tx:	8
Data SLVS-Rx:	13
Total:	38
CORE:	
Standard Cells:	305
Phase-Aligners:	14
Total:	319
Total Power [mW]:	1464

GBTX Future

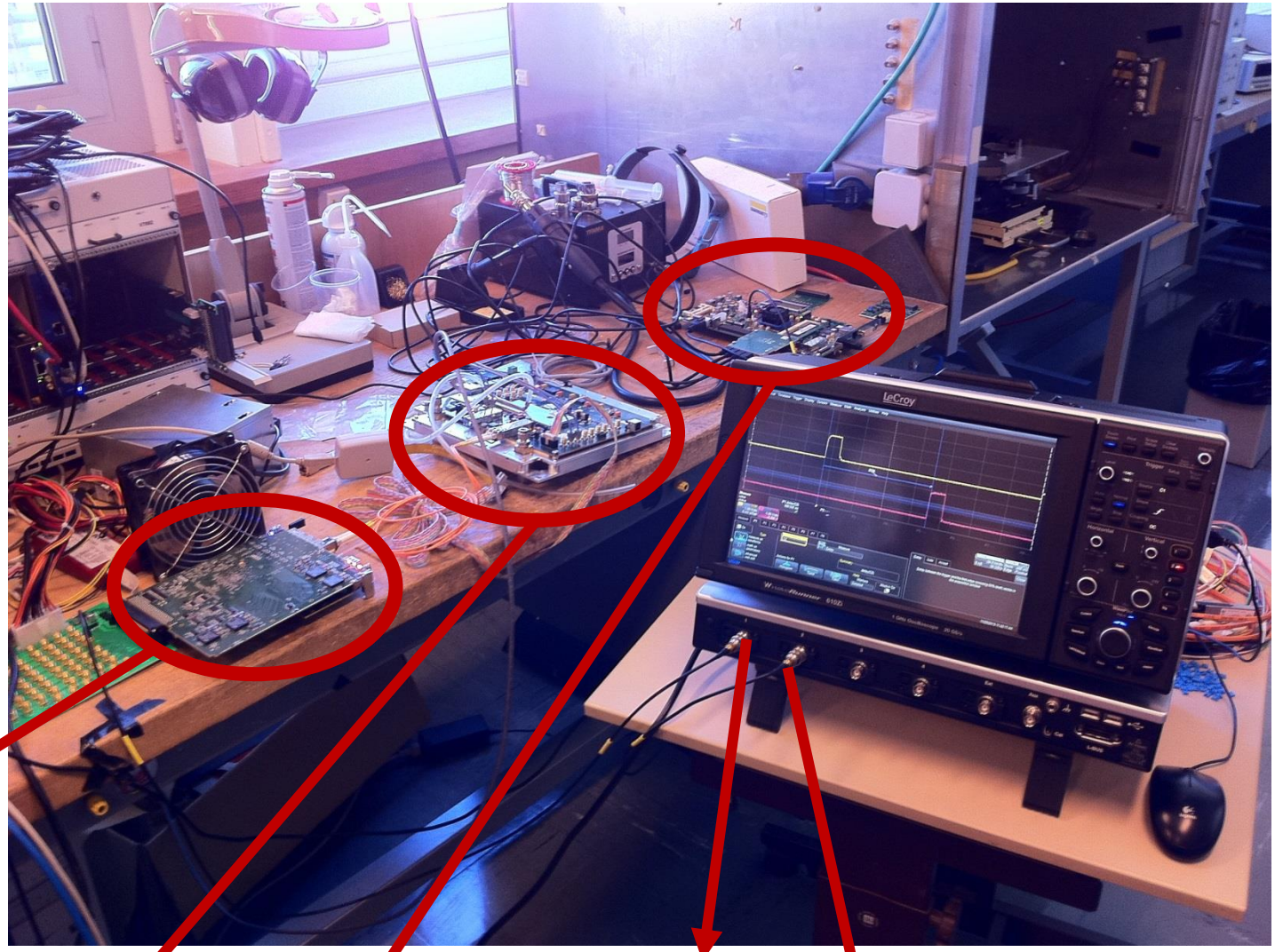
- Q4 – 2013
  - Finalize chip characterization: November– December
  - Total dose irradiation tests: December
  - Samples available for prototyping: December
    - Only small quantities available (< 30)
- Q1 – 2014
  - Second run of SEU tests: February
  - Depending on the SEU test results small changes might be required to improve the robustness of the circuit
  - Although the circuit is fully functional a “a few small corners need to be rounded” to make it “plug-and-play” for the users
- Q2 – 2014
  - Additional 100 GBTX samples available
  - Split Engineering Run to produce in quantities:
    - GBTX
    - GBTIA
    - GBLD V4/V5
    - GBT-SCA
- Q3 – 2014
  - Chips available from the foundry
  - ASIC Packaging
- Q4 – 2014
  - ASIC production testing
  - First production ASICs distributed to the users

Additional Slides

GBTx latency measurement

- Has to include
  - Back end: GBT-FPGA IP core (Rx or Tx)
  - Front End: E-links IP core (Serializer or Deserializer)

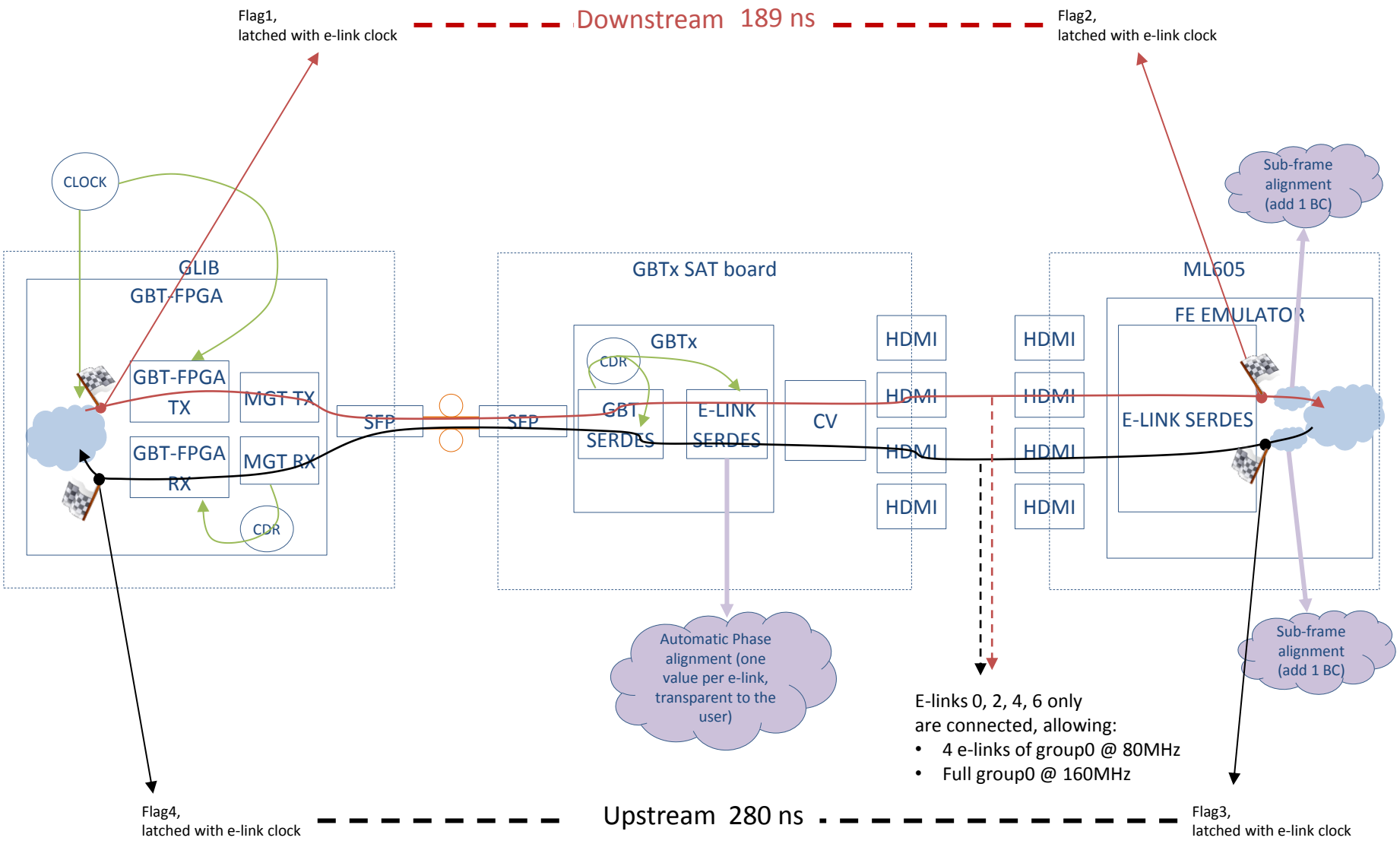
  To allow pattern detection for flag rising
- We used a test system presented at TWEPP, including:
  - BE: GLIB
  - GBTX: SAT board
  - FE: ML605 (virtex6) equipped with an HDMI-FMC
- We removed all the system specific delays (cables, PCB, etc)



BACK END
(GLIB)

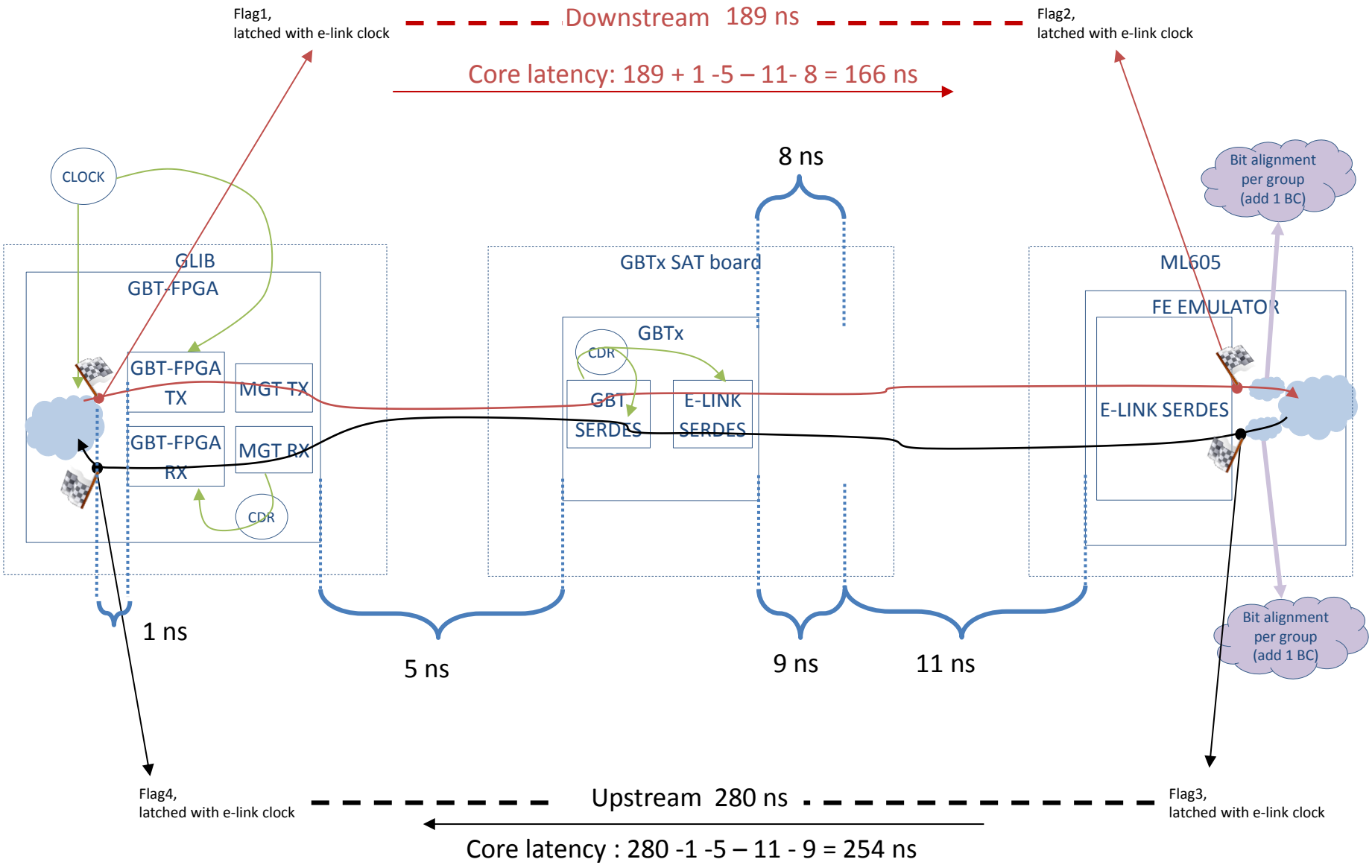
GBTx SAT
board

FRONT END
(ML605 + HDMI FMC)



BACK END

FRONT END


Flag1,
latched with e-link clock
Downstream 189 ns
Flag2,
latched with e-link clock
Core latency: 189 + 1 -5 – 11- 8 = 166 ns
8 ns
Bit alignment
per group
(add 1 BC)
CLOCK
GLIB
GBT-FPGA
GBT-FPGA
TX
MGT TX
GBT-FPGA
RX
MGT RX
CDR
GBTx SAT board
GBTx
CDR
GBT
SERDES
E-LINK
SERDES
ML605
FE EMULATOR
E-LINK SERDES
1 ns
5 ns
9 ns
11 ns
Bit alignment
per group
(add 1 BC)
Flag4,
latched with e-link clock
Upstream 280 ns
Flag3,
latched with e-link clock
Core latency : 280 -1 -5 – 11 - 9 = 254 ns
BACK END
FRONT END

Total

Architecture: GBT encoding scheme and e-links @ 160 MHz,

Downstream Core Latency:

GBT-FPGA Tx + GBTx + FE GBT deserializer =

166ns = 6.65 BC

Upstream Core Latency:

FE GBT serializer + GBTx + GBT-FPGA Rx (latency optimized) =

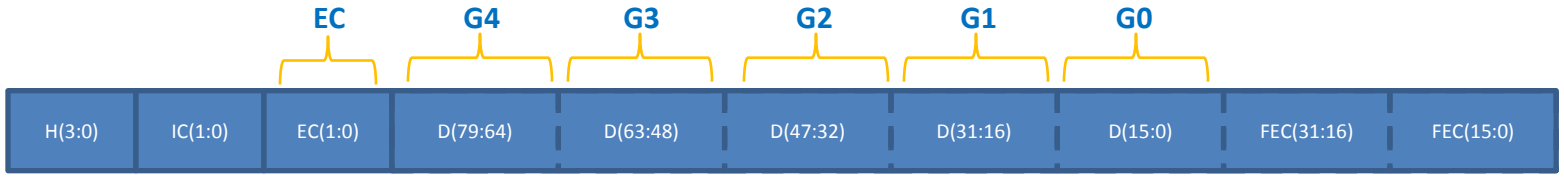
254 ns = 10.1 BC

Without the bit alignment (per group), to be done either in the Front End or in the Back End:

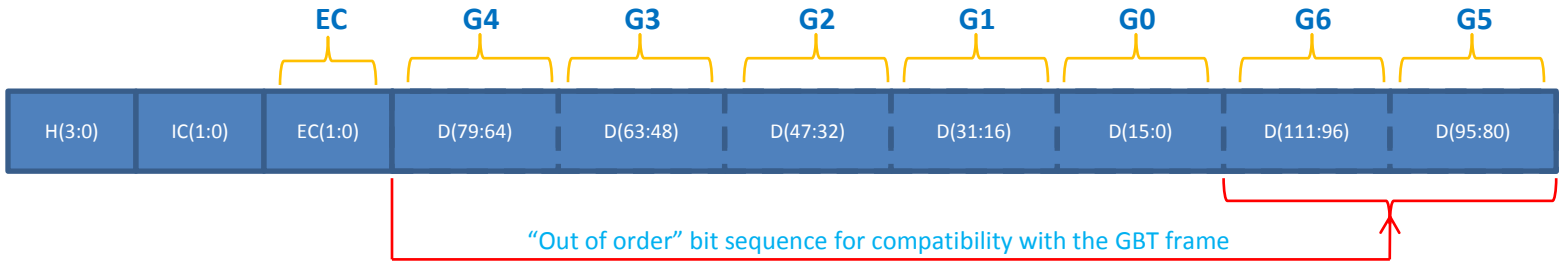
=> **you should add 1 BC (for bit alignment) to have a realistic value, plus the length of your cables and PCB traces**

GBTX Frames

GBT Frame (for up and down links)



Wide Bus Frame (for up-links only)



8B/10B Frame (for up-links only)