The Timepix3 chip

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On behalf of the Medipix3 collaboration

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\textsuperscript{b} CERN
\textsuperscript{c} NIKHEF
• **Introduction**
  – Timepix3 Motivation
  – Pixel operation

• **Measurements**
  – Timepix3 Readout System
  – PC and iTOT mode:
    • Single Pixel gain and ENC
    • Full chip ENC
    • Equalization
  – TOA and TOT:
    • TOT linearity
    • Timewalk
    • TOT linearity
  – Results summary
  – Wafer Probing
  – Timepix3 TPC [Preliminary]

• **Conclusions**
Hybrid Pixel Detectors Operation Modes

• In a hybrid pixel detector the energy threshold is used to eliminate noise or low energy events → Noise-free system

• Nature of measurements after discriminator:
  – Particle Counting (PC)
    • Count of number of events in a fix time (Shutter)
  – Time-Over-Threshold (TOT)
    • TOT charge per event
    • iTOT integral of the charge over a fix time (Shutter)
  – Time of Arrival (TOA)
    • Measure of the arrival time (Time stamping)
  – Binary (Bi)
    • 1 bit per event tagged with Bx
## Hybrid pixel ASICs classification
(from 2012 seminar)

<table>
<thead>
<tr>
<th>Chip Name</th>
<th>Technology</th>
<th>Year</th>
<th>Pixel Size [um]</th>
<th>Pixel Array</th>
<th>Pixel Operation</th>
<th>Bits/Pixel</th>
<th>Data Type</th>
<th>Start readout</th>
<th>Acquisition Type</th>
<th>Trigger Readout</th>
<th>Output data port</th>
</tr>
</thead>
<tbody>
<tr>
<td>Medipix2</td>
<td>IBM 250n</td>
<td>2005</td>
<td>55</td>
<td>256*256</td>
<td>PC</td>
<td>14</td>
<td>Full frame</td>
<td>External</td>
<td>Non-continuous</td>
<td>No</td>
<td>32-bit CMOS DDR</td>
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<tr>
<td>EIGER</td>
<td>UMC 250nm</td>
<td>2010</td>
<td>75</td>
<td>256*256</td>
<td>PC</td>
<td>4, 8 or 12</td>
<td>Full frame</td>
<td>External</td>
<td>Continuous</td>
<td>No</td>
<td>1,2,4 or 8-LVDS</td>
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<tr>
<td>Medipix3RX</td>
<td>IBM 130n</td>
<td>2012</td>
<td>55</td>
<td>256*256</td>
<td>PC</td>
<td>1,6,12 or 24</td>
<td>Full frame</td>
<td>External</td>
<td>Continuous</td>
<td>No</td>
<td>1,2,4 or 8-LVDS</td>
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<tr>
<td>Timepix</td>
<td>IBM 250n</td>
<td>2006</td>
<td>55</td>
<td>256*256</td>
<td>PC, TOT or TOA</td>
<td>14</td>
<td>Full frame</td>
<td>External</td>
<td>Non-continuous</td>
<td>No</td>
<td>32-bit CMOS DDR</td>
</tr>
<tr>
<td>SmallPix</td>
<td>IBM 130n</td>
<td>2014</td>
<td>35-40</td>
<td>384<em>384 512</em>512</td>
<td>TOA and TOT</td>
<td>24-32</td>
<td>0-compressed</td>
<td>External</td>
<td>Continuous</td>
<td>No</td>
<td>1,2,4 or 8-LVDS</td>
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<tr>
<td>ClicPix_demo</td>
<td>TSMC 65nm</td>
<td>2012</td>
<td>25</td>
<td>64*64</td>
<td>TOT and TOA</td>
<td>9</td>
<td>0-compressed</td>
<td>External</td>
<td>Continuous</td>
<td>No</td>
<td>1,2,4 or 8-LVDS</td>
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<tr>
<td>Alice1LHCb</td>
<td>IBM 250n</td>
<td>2001</td>
<td>50*425</td>
<td>256*32</td>
<td>TOA and Binary</td>
<td>2 FIFO of 8 bit BCO</td>
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<td>Continuous</td>
<td>Yes</td>
<td>32-GTL @ 40 Mbps</td>
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<tr>
<td>PSI46 (CMS)</td>
<td>IBM 250n</td>
<td>2005</td>
<td>100*150</td>
<td>52*80</td>
<td>Analog</td>
<td>?</td>
<td>0-suppressed</td>
<td>External</td>
<td>Continuous</td>
<td>Yes</td>
<td>6-8 bit analog @ 40 MHz</td>
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<tr>
<td>FEI3 (ATLAS)</td>
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<td>2006</td>
<td>50 *400</td>
<td>160*18</td>
<td>TOA and TOT</td>
<td>?</td>
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<td>External</td>
<td>Continuous</td>
<td>Yes</td>
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<td>2011</td>
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<td>TDCpix (NA62)</td>
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<td>300</td>
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<td>48</td>
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<td>Data driven</td>
<td>Continuous</td>
<td>No</td>
<td>4 CML @ 3.2 Gbps</td>
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<td>ToPIX (PANDA)</td>
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<td>TOA and TOT</td>
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<td>0-suppressed</td>
<td>Data driven</td>
<td>Continuous</td>
<td>No</td>
<td>1-LVDS @ 312.4 M</td>
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<td>Data driven</td>
<td>Continuous</td>
<td>No</td>
<td>1 to 8-SLVDS DDR @ 640 Mbps</td>
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<td>IBM 130n</td>
<td>2014</td>
<td>55</td>
<td>256*256</td>
<td>PC</td>
<td>30</td>
<td>0-suppressed</td>
<td>Data driven</td>
<td>Continuous</td>
<td>Semi-Continuous</td>
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<tr>
<td>Dosepix</td>
<td>IBM 130n</td>
<td>2010</td>
<td>220</td>
<td>16*16</td>
<td>TOT</td>
<td>256</td>
<td>Full frame</td>
<td>External</td>
<td>Continuous</td>
<td>Semi-Continuous</td>
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</tr>
</tbody>
</table>

**Categories:**
- **Imaging**
- **HEP Low Rate**
- **HEP Triggered**
- **HEP Trigger-less**
- **Dosimetry**
Timepix (2006)

- IBM 250nm 6-metals
- Operation modes:
  - Particle arrival time (TOA)
  - Charge information \((i_{TOT})\)
  - Event counting (PC)
- Frame based readout

Timepix Pixel Schematic

Timepix picture

14.111 mm

55 µm

16.12 mm
Timepix chip architecture

Main Specs:
- 256x256 55µm square pixels
- Analog Power → 440mW
- Bits stored in pixel → 14
- Serial readout (@100Mbps) → 9.17 ms
- Parallel readout (@100Mbps) → 287 µs
- Full custom design
- > 36M Transistors
The Timepix (2006) has proven to be a versatile chip with a large range of applications:

- X-ray radiography, X-ray polarimetry, low energy electron microscopy
- Radiation and beam monitors, dosimetry
- 3D gas detectors, neutrons, fission products
- Gas detector, Compton camera, gamma polarization camera, fast neutron camera, ion/MIP telescope, nuclear fission, astrophysics
- Imaging in neutron activation analysis, gamma polarization imaging based on Compton effect
- Neutrino physics
- Main Linear Collider application: pixelated TPC readout

> 350 original paper citations
Timepix3 motivation

• Main driving requirements:
  1. Simultaneous TIME (TOA) and CHARGE (TOT) information per pixel
  2. Minimize dead time → Event-by-event readout and 0-suppressed
  3. Monotonic TOT in both detection polarities
  4. Improve time measurements resolution

• Experience gained in the design of the Medipix3 chip (2009):
  – Technology (130nm CMOS)
  – Building blocks recycled (CERN’s HD Standard Cell library, DACs, ...)

• Designed by CERN, Nikhef and Bonn University with the support of the Medipix3 Collaboration
CERN 130nm HD Library

- **Physical specs:**
  - “Mainly” Low power transistors
  - Row Height is fixed to 2.4 µm
  - Well Tap library
- **Maximum frequency < ~700 MHz (@1.5V)**
- **Encounter Library Characterizer (ELC) used:**
  - Full Synopsis library:
    - lib, ecsm, ecsm_si and ccs
    - delays, static and dynamic power
    - Corners:
      - 1.2V: -55C FF, 25C TT and 125C SS
      - 1.5V: -55C FF, 25C TT and 125C SS
  - Verilog library
  - LEF files
  - HTML documentation
- ~50 cells are available in the library
- Used in Medipix3RX
CERN 130nm HD Special cells (I)

- Cells with “non-standard” functional behaviour can be integrated

VOTERI_B_XL
(VeloPix)

NOR5_A_XL
(Medipix3RX)
CERN 130nm HD Special cells (II)

• Cells with non-standard row height are also possible to integrate:
  – Row height multiple (2.4 µm)
  – Pitch length multiple (0.4 µm)
# Timepix vs Timepix3

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pixel arrangement</strong></td>
<td>256 x 256</td>
<td></td>
</tr>
<tr>
<td><strong>Pixel size</strong></td>
<td>55 x 55 µm²</td>
<td></td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>250nm CMOS - 6Metals</td>
<td>130nm CMOS - 8Metals</td>
</tr>
<tr>
<td><strong>Acquisition modes</strong></td>
<td>1) Charge (iTOT) 2) Time (TOA) 3) Event counting (PC)</td>
<td>1) Time (TOA) AND Charge (TOT) 2) Time (TOA) 3) Event counting (PC) AND integral charge (iTOT)</td>
</tr>
<tr>
<td><strong>Readout Type</strong></td>
<td>1) Full-Frame</td>
<td>1) Data driven (DD) 2) Frame (FB)</td>
</tr>
<tr>
<td><strong>Zero suppressed readout</strong></td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td><strong>Dead time per pixel</strong></td>
<td>&gt; 300µs</td>
<td>&gt; 475ns</td>
</tr>
<tr>
<td></td>
<td>readout time of one frame</td>
<td>Pulse measurement time + packet transfer time</td>
</tr>
<tr>
<td><strong>Minimum timing resolution</strong></td>
<td>10ns</td>
<td>1.562ns</td>
</tr>
<tr>
<td><strong>On-chip Power pulsing (PP)</strong></td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td><strong>Minimum detectable charge</strong></td>
<td>~750e-</td>
<td>&gt;500e-</td>
</tr>
<tr>
<td><strong>Output bandwidth</strong></td>
<td>1 LVDS ≤200Mbps 32 CMOS ≤3.2Gbps</td>
<td>1 to 8 SLVS @640Mbps DDR ≤5.2Gbps</td>
</tr>
</tbody>
</table>

25th February 2014

ESE Seminar – X.Llopart
Swiss technology comparison

Timepix (2006)  
Timepix3 (2013)
Trigger-less **frame based** and zero-suppressed readout

- Maximum frame rate (all pixels hit): 1300 fps @5.12Gbps
Maximum frame rate [fps]
Frame Based Readout

Worst case: all pixels readout
48bit/pixel and 8b10b → 3.932 Mbits/frame (x2.5 Mpix3)

~1300 fps
Trigger-less \textbf{event-by-event} data driven and zero-suppressed readout

- Achievable count rate:
  - uniformly distributed events $\rightarrow$ $\sim 40$ Mhits/s/cm$^2$ @5.12Gbps
- Full matrix readout: $\sim 800$ $\mu$s @5.12Gbps
Maximum Event Readout
Data Driven Readout

Limited by output block bandwidth

Limited by Periphery bandwidth

85.3 Mhits/s

number of active links @640Mbps and 8b10b ON
Pixel Operation in **TOA & TOT [DD]**

- **Tpeak < 25ns**
- **Preamp Out**
- **Disc Out**
- **Clk (40MHz)**
- **Global TOA (14-bit)**: 16382, 16383, 16384, 0, 1, 2, 3, 4
- **VCO Clk (640MHz)**
- **TOA (14-bit)**: X, 16383
- **TOT Clk (40MHz)**: TOT (10 bits) = 4

Pixel Readout Starts (475ns → 19 clock cycles)
Pixel Operation in **TOA only [DD]**

- **Preamp Out**
- **Disc Out**
- **Clk (40MHz)**
- **Global TOA (14-bit)**: 16382, 16383, 16384, 0, 1, 2, 3, 4
- **VCO Clk (640MHz)**
- **TOA (14-bit)**: X, 16383

- **Tpeak < 25ns**
- **Pixel Readout Starts (475ns → 19 clock cycles)**
- **FTOA (4 bits) = 7**
- **TOA (14 bits) = 16383**
Pixel Operation in PC and iTOT [FB]

Pixel readout can start in Data Driven or Frame based

PC (14 bits) = 3

iTOT (14 bits) = 5
Timepix3 Pixel Schematic

Front-end (Analog)
- Input pad
- TestBit
- Global threshold (LSB= ~10e⁻)
- Leakeage Current compensation
- Preamp
- 3fF
- TpA, TpB

Front-end (Digital)
- TOA & TOT
- TOA (14-bit)
- TOT (10-bit)
- FTOA (4-bit)
- Control voltage
- Clock gating
- Synchronizer
- Counters & Latches
- OP Mode
- Time stamp
- 640MHz
- 14-bit

Super pixel (Digital)
- Common for 8 pixels
- Control
- VCO @640MHz
- Deserializer [1x31]
- Super pixel FIFO [2x31]
- Data out to EOC
- Token arbitration
- 31-bits
- 37-bits
- 31-bits
- 640MHz
- 40MHz

25th February 2014
ESE Seminar – X.Llopard
T. Poikela
## Timepix3 Pixel Operation

### Acquisition Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>Superpixel VCO</th>
<th>Measurement type</th>
<th>On-pixel counter depth</th>
<th>Valid Data bits</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Time (TOA) AND Charge (TOT)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>TOA, TOT, Fast ToA</td>
<td>14-bit (gray counter), 10-bit (LFSR with overflow), 4-bit (binary counter with overflow)</td>
<td></td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>TOA, TOT, Event Counter</td>
<td>14-bit (gray counter), 10-bit (LFSR with overflow), 4-bit (LFSR with overflow)</td>
<td>28</td>
</tr>
<tr>
<td><strong>Time (TOA)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>TOA, Fast ToA</td>
<td>14-bit (gray counter), 4-bit (binary counter with overflow)</td>
<td>18</td>
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<td>OFF</td>
<td>OFF</td>
<td>TOA, Event Counter</td>
<td>14-bit (gray counter), 4-bit (LFSR with overflow)</td>
<td></td>
</tr>
<tr>
<td><strong>Event counting (PC) AND integral charge (iTOT)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>iTOT, Event counter</td>
<td>14-bit (LFSR), 10-bit (LFSR with overflow)</td>
<td>28</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>iTOT, Event counter</td>
<td>14-bit (LFSR), 10-bit (LFSR with overflow), 4-bit (LFSR with overflow)</td>
<td></td>
</tr>
</tbody>
</table>

- 4 Look-up-tables (LUT) needed to decode pixel data:
  - 14-bit gray counter
  - 14-bit LFSR
  - 10-bit LFSR
  - 4-bit LFSR
Asynchronous column data transfer

- 2-phase handshake protocol using single rail coding
- Globally-asynchronous locally-synchronous column readout protocol (GALS)

<table>
<thead>
<tr>
<th>CORNER</th>
<th>SS 1.4V 125C [MHits]</th>
<th>TT 1.5V 25C [MHits]</th>
<th>FF 1.6V -55C [MHits]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SP 0 only</td>
<td>0.45</td>
<td>0.45</td>
<td>0.45</td>
</tr>
<tr>
<td>SP 63 only</td>
<td>0.41</td>
<td>0.45</td>
<td>0.465</td>
</tr>
<tr>
<td>All SPs</td>
<td>1.36</td>
<td>1.5</td>
<td>1.6</td>
</tr>
<tr>
<td>Full Matrix</td>
<td>174</td>
<td>192</td>
<td>205</td>
</tr>
</tbody>
</table>
Pixel Matrix Clock distribution

- Nominal clock frequency is 40MHz (up to 80MHz)
- Synchronous clock distribution in the pixel matrix required for TOA time stamping:
  - Simulated bottom to top skew is (1.05ns, 1.45ns and 2ns) in (FF, TT and SS) corners
- Minimize peak digital current consumption:
  - Configurable double-column pixel matrix clock phase shift:
  - In pixel clock is gated if pixel is not hit

<table>
<thead>
<tr>
<th>Number of phases</th>
<th># Columns with same clk phase</th>
<th>phase delay</th>
<th>Peak current clk distribution only</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>128</td>
<td>25ns</td>
<td>1.075 A</td>
</tr>
<tr>
<td>2</td>
<td>64</td>
<td>12.5ns</td>
<td>537.6 mA</td>
</tr>
<tr>
<td>4</td>
<td>32</td>
<td>6.25ns</td>
<td>268.8 mA</td>
</tr>
<tr>
<td>8</td>
<td>16</td>
<td>3.125ns</td>
<td>134.4 mA</td>
</tr>
<tr>
<td>16</td>
<td>8</td>
<td>1.5625ns</td>
<td>67.2 mA</td>
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</tbody>
</table>
Timepix3 Active Periphery

- **Slow Control & Command Decoder**
- **PLL**
- **Bus Controller**
- **Analog Periphery Control Logic**
  - 1 BandGap 18 Global DACs
  - E-Fuses 32 bits
- **Data output DDR 8b10b encoding (1 to 8 links) Up to 8x640 Mbps (5.12 Gbps)**

**Key Components:**
- **VCO Buffers**
- **EoC**
- **8x Serializer 8b10b DDR**
- **Clk40**
- **Buffered bias voltages**
- **64 VCO control voltage buffers**

**Dimensions:**
- 1260 μm
- 14080 µm

**Date:** 25th February 2014
# Timepix3 IO

## Timepix3 Differential I/O

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>$V_{\text{ID}}$ (mV)</th>
<th>$V_{\text{ICM}}$ (V)</th>
<th>$V_{\text{OD}}$ (mV)</th>
<th>$V_{\text{OCM}}$ (V)</th>
</tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>DataIn</td>
<td>I</td>
<td>SLVS/LVDS</td>
<td>80</td>
<td>1500</td>
<td>0.1</td>
</tr>
<tr>
<td>EnableIn</td>
<td>I</td>
<td>SLVS/LVDS</td>
<td>80</td>
<td>1500</td>
<td>0.1</td>
</tr>
<tr>
<td>Reset</td>
<td>I</td>
<td>SLVS/LVDS</td>
<td>80</td>
<td>1500</td>
<td>0.1</td>
</tr>
<tr>
<td>T0_Sync</td>
<td>I</td>
<td>SLVS/LVDS</td>
<td>80</td>
<td>1500</td>
<td>0.1</td>
</tr>
<tr>
<td>Shutter</td>
<td>I</td>
<td>SLVS/LVDS</td>
<td>80</td>
<td>1500</td>
<td>0.1</td>
</tr>
<tr>
<td>EnablePowerPulsing</td>
<td>I</td>
<td>SLVS/LVDS</td>
<td>80</td>
<td>1500</td>
<td>0.1</td>
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<tr>
<td>ExtTPulse</td>
<td>I</td>
<td>SLVS/LVDS</td>
<td>80</td>
<td>1500</td>
<td>0.1</td>
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<td>ClkIn40</td>
<td>I</td>
<td>SLVS/LVDS</td>
<td>80</td>
<td>1500</td>
<td>0.1</td>
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<tr>
<td>ClkInRefPLL</td>
<td>I</td>
<td>SLVS/LVDS</td>
<td>80</td>
<td>1500</td>
<td>0.1</td>
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</table>

## Timepix3 CMOS I/O

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>$V_{\text{IL}}$ (V)</th>
<th>$V_{\text{IH}}$ (V)</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>SLVS_TERM</td>
<td>I</td>
<td>CMOS</td>
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</tr>
</tbody>
</table>

## Timepix3 Analog I/O

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>$V_i$ (V)</th>
<th>$V_o$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>DACOut</td>
<td>O</td>
<td>Analog</td>
<td></td>
</tr>
<tr>
<td>ExtDAC</td>
<td>I</td>
<td>Analog</td>
<td>-0.2</td>
</tr>
</tbody>
</table>
## Periphery Command List

<table>
<thead>
<tr>
<th>Periphery Operation Header [8 bits]</th>
<th>Header</th>
<th>DataIN [16 bits]</th>
<th>DataOut [40 bits]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SenseDACsel</td>
<td>I</td>
<td>0x00</td>
<td>[DAC Code][4:0]</td>
</tr>
<tr>
<td>ExtDACsel</td>
<td>I</td>
<td>0x01</td>
<td>[DAC Code][4:0]</td>
</tr>
<tr>
<td>SetDAC_Code</td>
<td>I</td>
<td>0x02</td>
<td>[DAC Value][13:5]</td>
</tr>
<tr>
<td>ReadDAC_code</td>
<td>I</td>
<td>0x03</td>
<td>[DAC Code][4:0]</td>
</tr>
<tr>
<td>EFuse_Burn</td>
<td>I</td>
<td>0x08</td>
<td>{FuseProgramConfig}[10:0]</td>
</tr>
<tr>
<td>EFuse_Read</td>
<td>I</td>
<td>0x09</td>
<td>{8'b0}[39:32][ChipID][31:0]</td>
</tr>
<tr>
<td>EfuseRead_BurnConfig</td>
<td>O</td>
<td>0x0A</td>
<td>{FuseProgramConfig}[20:0]</td>
</tr>
<tr>
<td>TP_Period</td>
<td>I</td>
<td>0x0C</td>
<td>{TPphase}[11:8]</td>
</tr>
<tr>
<td>TP_PulseNumber</td>
<td>I</td>
<td>0x0D</td>
<td>{TPperiod}[7:0]</td>
</tr>
<tr>
<td>TPConfig_Read</td>
<td>O</td>
<td>0x0E</td>
<td>{TPnumber}[15:0]</td>
</tr>
<tr>
<td>TP_internalfinished</td>
<td>O</td>
<td>0x0F</td>
<td>8'b[0000_1111][ChipID][31:0]</td>
</tr>
<tr>
<td>OutBlockConfig</td>
<td>I</td>
<td>0x10</td>
<td>[OutputBlockConfig][12:0]</td>
</tr>
<tr>
<td>OutBlockConfig_Read_en</td>
<td>O</td>
<td>0x11</td>
<td>[27'b0][39:13][OutputBlockConfig][12:0]</td>
</tr>
<tr>
<td>PLLConfig</td>
<td>I</td>
<td>0x20</td>
<td>{PLLConfig}[7:0]</td>
</tr>
<tr>
<td>PLLConfig_Read_en</td>
<td>O</td>
<td>0x21</td>
<td>{32'b0}[39:8][PLLConfig][7:0]</td>
</tr>
<tr>
<td>GeneralConfig</td>
<td>I</td>
<td>0x30</td>
<td>{GeneralConfig}[11:0]</td>
</tr>
<tr>
<td>GeneralConfig_Read_en</td>
<td>O</td>
<td>0x31</td>
<td>{SLVSConfig}[4:0]</td>
</tr>
<tr>
<td>SLVSConfig</td>
<td>I</td>
<td>0x34</td>
<td>{35'b0}[39:6][SLVSConfig][4:0]</td>
</tr>
<tr>
<td>SLVSConfig_Read_en</td>
<td>O</td>
<td>0x35</td>
<td>{PowerPulsingPattern}[7:0]</td>
</tr>
<tr>
<td>PowerPulsingPattern</td>
<td>I</td>
<td>0x3C</td>
<td>{32'b0}[39:8][PowerPulsingPattern][7:0]</td>
</tr>
<tr>
<td>PowerPulsingON_finished</td>
<td>O</td>
<td>0x3D</td>
<td>8'b[0011_1111][ChipID][31:0]</td>
</tr>
<tr>
<td>Timer</td>
<td>I</td>
<td>0x40</td>
<td>[SetTimer[15:0]][15:0]</td>
</tr>
<tr>
<td>SetTimer_15_0</td>
<td>I</td>
<td>0x41</td>
<td>[SetTimer[31:16]][15:0]</td>
</tr>
<tr>
<td>SetTimer_31_16</td>
<td>I</td>
<td>0x42</td>
<td>[SetTimer[47:32]][15:0]</td>
</tr>
<tr>
<td>SetTimer_47_32</td>
<td>I</td>
<td>0x43</td>
<td>8'b[39:32][Timer[31:0]][31:0]</td>
</tr>
<tr>
<td>RequestTimeLow</td>
<td>O</td>
<td>0x44</td>
<td>24'b[39:16][Timer[47:32]][15:0]</td>
</tr>
<tr>
<td>RequestTimeHigh</td>
<td>O</td>
<td>0x45</td>
<td>8'b[39:32][Timer[Shutter][31:0]][31:0]</td>
</tr>
<tr>
<td>TimeRisingShutterLow</td>
<td>O</td>
<td>0x46</td>
<td>24'b[39:16][TimerShutter[47:32]][15:0]</td>
</tr>
<tr>
<td>TimeRisingShutterHigh</td>
<td>O</td>
<td>0x47</td>
<td>8'b[39:32][TimerShutterL][31:0][31:0]</td>
</tr>
<tr>
<td>TimeFallingShutterLow</td>
<td>O</td>
<td>0x48</td>
<td>24'b[39:16][TimerShutterL[47:32]][15:0]</td>
</tr>
<tr>
<td>TimeFallingShutterHigh</td>
<td>O</td>
<td>0x49</td>
<td>8'b[0000_1111][ChipID][31:0]</td>
</tr>
<tr>
<td>TO_Sync_Command</td>
<td>O</td>
<td>0x4A</td>
<td>{H1,H2,H3}[39:32]</td>
</tr>
<tr>
<td>ControlOperation</td>
<td>O</td>
<td>0x70</td>
<td>{ChipID}[31:0]</td>
</tr>
<tr>
<td>Acknowledge</td>
<td>O</td>
<td>0x71</td>
<td>{H1,H2,H3}[39:32]</td>
</tr>
<tr>
<td>EndOfCommand</td>
<td>O</td>
<td>0x72</td>
<td>{8'b0}[39:32]</td>
</tr>
<tr>
<td>OtherChipCommand</td>
<td>O</td>
<td>0x73</td>
<td>{ChipID}[31:0]</td>
</tr>
</tbody>
</table>

25th February 2014
Power pulsing strategy in Timepix3

• **Analog power-pulsing:**
  
  – Preamp (3µA), DiscS1 (2µA) and DiscS2 (2µA) are the ~98% of the analog power consumption in the pixel matrix (460mA)
  
  – One Periphery multiplexer for the 3 biasing lines in each double column selects between the Power-ON or Power-OFF states
  
  – Power-ON (8-bits) and Power-OFF (4-bits) values are programmed in 2 periphery DACs for each power pulsed bias line
  
  – Power pulsing multiplexer is selected by a sequential column to column signal with independent adjustable turn-on and turn off times

• **System clock gating:**
  
  – Clock gating is applied at the end of the analog power-off sequence
  
  – This feature can be disabled
Power pulsing time diagram

DataIn
- 64 bits
- PowerPulsingSettings
  - ClockDividerPP_ON[2:0] = 000
  - NumberOfSimultaneousColumnsPP_ON[5:3] = 100
  - ClockDividerPP_OFF[8:6] = 010
  - EnablePowerPulsingInDigitalDomain = 1

EnablePowerPulsing

AnalogPower
- ON (~750mW)
- OFF (<25mW)
- 0.8 µs @ 40 MHz
- 6.4 µs @ 40 MHz

Clock (internal)
- ON
- OFF
- ON

DataOut
- 0h3F3F
- ChipID
- Power Pulsing ON Finished
### Data output packet types

#### Acquisition (VCO ON)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ToA and ToT mode</td>
<td>{1010 or 1011}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Only ToA</td>
<td>{1010 or 1011}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Event Count and iToT</td>
<td>{1010 or 1011}</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Acquisition (VCO OFF)

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>ToA and ToT mode</td>
<td>{1010 or 1011}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Only ToA</td>
<td>{1010 or 1011}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Event Count and iToT</td>
<td>{1010 or 1011}</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Stop Matrix Readout or Reset Sequential

<table>
<thead>
<tr>
<th>Packet Type</th>
<th>Address [43:28]</th>
<th>dummy [27:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>{1111 or 1110}</td>
<td></td>
<td>dummy [43:0]</td>
</tr>
</tbody>
</table>

#### Pixel Matrix Configuration

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel Configuration</td>
<td>{1001}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTPR Configuration</td>
<td>{1101}</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Periphery Command

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Periphery Command</td>
<td>{0}</td>
<td></td>
<td></td>
<td></td>
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</table>

#### Periphery Configuration

<table>
<thead>
<tr>
<th>Packet Type</th>
<th>Address [43:40]</th>
<th>DataOutPeriphery [39:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acknowledge cmd</td>
<td>{0111_0000}</td>
<td></td>
</tr>
<tr>
<td>End of cmd</td>
<td>{0111_0001}</td>
<td></td>
</tr>
<tr>
<td>Other Chip cmd</td>
<td>{0111_0010}</td>
<td></td>
</tr>
<tr>
<td>Wrong cmd</td>
<td>{0111_0011}</td>
<td></td>
</tr>
</tbody>
</table>

#### Control Commands

<table>
<thead>
<tr>
<th>Packet Type</th>
<th>Address [43:40]</th>
<th>ChipID [31:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acknowledge cmd</td>
<td>{H1,H2,H3}</td>
<td>ChipID [31:0]</td>
</tr>
<tr>
<td>End of cmd</td>
<td>{H1,H2,H3}</td>
<td>ChipID [31:0]</td>
</tr>
<tr>
<td>Other Chip cmd</td>
<td>{0000_0000}</td>
<td>ChipID [31:0]</td>
</tr>
<tr>
<td>Wrong cmd</td>
<td>{H1,H2,H3}</td>
<td>ChipID [31:0]</td>
</tr>
</tbody>
</table>
Power Consumption Data Driven
[VDD=1.5V and VDDA=1.5V]

<1.5 W @80MHit/s
Power Consumption PC Frame-based

[VDD=1.5V and VDDA=1.5V]

- Data Driven limit ~100 KHz/pixel
Timepix3 Layout

Double column:
- 2x256 pixels
- 64 super pixels

Full Pixel Matrix:
- 256x256 pixels
- 128 double columns
- 8192 VCOs (640MHz)
- 177 Mtransistors

Active Periphery

Pad Extenders:
- Removed if TSV

Analog Front-End:
- 13x55 μm²
- <25% pixel area

IO Pad on digital area:
- Careful shielding
- Pad is ½ of Timepix

VCO (FTOA):
- 9.6x20 μm²
- <0.8% SP area

Super Pixel (SP):
- 2x4 pixels
- 110x220 μm²

25th February 2014
Medipix chip family

![Graph showing the relationship between transistor density per pixel and CMOS process.]
MEASUREMENTS
Timepix3 readout → SPIDR (Nikhef)

• Speedy Pixel Detector Readout (SPIDR):
  – Readout system for Medipix3 and Timepix3 (single up to quads)
  – 1 x 10Gbps Ethernet link IO

• First chips available since beginning of September 2013

• All measurements reported use data readout @640Mbps/link

---

Virtex 7 FPGA

VC707 Evaluation Board

10 Gbit Ethernet

Timepix3 Chip
Timepix3 CERN PCBs

Timepix3 CERN chip board

Timepix3 Probe card

Timepix3 translator FMC/VHDCI
Timepix3 DACs

TestPulse (~50e⁻ LSB)
Range: > 18ke⁻

VTHR (~10e⁻ LSB)
Range: 5.11 ke⁻
Pixel Data readout

- Data readout in Data Driven and Frame Based readout works as predicted in post-layout digital simulations

![Frame based Full column readout](image)

- Event rate (MHits)

- Event number

- TT1.5V25C
- SS1.4V125C
- FF1.6V-55C
- Measured
250 Test Pulses in 1 pixel

[Threshold scan in PC & iTOT mode, 1 pixel]

ENC \~ 5.7 \text{LSBrms} = \sim 60 \text{e}^-

\begin{align*}
y &= 10.4 \text{e}^-/\text{LSB} \\
R^2 &= 0.999
\end{align*}

Assuming:
\( C_{\text{test}} = 3 \text{fF} \rightarrow T_{\text{pulse}} = 20 \text{e}^-/\text{mV} \)
250 Test Pulses in 256 pixels
[Threshold scan in PC & iTOT mode, pixel matrix equalized]

Counts

Counts

\[ y = 1.0014x \]
\[ R^2 = 0.9999 \]

\[ \sim 3.9\% \text{ rms pixel-to-pixel gain variation} \]

25th February 2014
Pixel ENC

[Threshold scan over noise floor in PC & iTOT mode, 3 random pixels]

ENC = 56.7e⁻^{\text{rms}}

ENC = 56.2e⁻^{\text{rms}}

ENC = 59.8e⁻^{\text{rms}}
Full Matrix ENC

[Threshold scan over noise floor in PC & iTOT mode]

- ENC matches predictions from simulations

\( \mu = 59.9 \times 10^{-6} \)
\( \sigma = 2.85 \times 10^{-6} \)

- 9 pixels not responding
- 15 pixels ENC > 80\( \times 10^{-6} \)
Pixel-to-pixel Threshold Equalization

[Threshold scan over noise floor in PC & iTOT mode]

\[ \mu_0 = -762e^- \]
\[ \sigma_0 = 195e^- \]

\[ \mu_{eq} = 0e^- \]
\[ \sigma_{eq} = 35e^- \]

\[ \mu_F = 762e^- \]
\[ \sigma_F = 197e^- \]
Full chip minimum threshold

[Equalized pixel matrix, 16 pixels masked]

Number of active pixels vs. Threshold [e-]

- TOA and TOT in Data Driven Readout mode
- PC and iTOT in Sequential Readout mode

PC and iTOT ~400e⁻
ENC of ~60e⁻ rms

TOA and TOT (VCO ON) ~500e⁻
ENC of ~77e⁻ rms

~100e⁻
FTOA Uniformity (1.562 ns/bin)

[ Full matrix TOA & TOT mode, 1 single Test Pulse]

Vertical spread: ~3ns Test pulse propagation delay (3 bins)

Horizontal spread: 16-clock phase distribution (16 bins)

RAW TOA measurement → data 18 bins

Corrected TOA measurement

σ~0.55 LSB rms
**Timewalk and TOT linearity**

[Qin scan in TOA & TOT mode, pixel (0,0), threshold at 500e⁻, 64 events averaged]

- **Threshold at ~500e⁻**
- **TOT slope ~75ns/ke⁻**

**Electrical Test Pulse:**
- ~18 ke⁻ maximum Test Pulse
- Resolution ~50e⁻/step
Timewalk and TOT linearity

[Qin scan in TOA & TOT mode, pixel (0,0), threshold at 500e⁻, 64 events averaged]

Threshold at ~500e⁻

Timewalk < 10ns @Threshold + 1ke⁻
TOT spread

[Qin scan in TOA & TOT mode, diagonal pixels, threshold at 500e⁻]

Threshold at ~500e⁻

TOT spread ~6.5%_{rms}
## Summary of measurements

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ENC (without sensor)</td>
<td>100e⁻rms</td>
<td>59.9e⁻rms ± 2.85e⁻rms</td>
</tr>
<tr>
<td>Threshold distribution</td>
<td>250e⁻rms</td>
<td>~195e⁻rms</td>
</tr>
<tr>
<td>Threshold distribution equalized</td>
<td>35e⁻rms</td>
<td>&lt; 35e⁻rms</td>
</tr>
<tr>
<td>Minimum Threshold (without sensor)</td>
<td>&gt;650e⁻</td>
<td>&gt;400e⁻ (PC &amp; iTOT)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&gt;500e⁻ (TOA &amp; TOT)</td>
</tr>
<tr>
<td>Pixel analog power consumption</td>
<td>6.5µW @ 2.2V</td>
<td>&lt; 12µW @ 1.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&lt; 0.5µW if power pulsing ON</td>
</tr>
<tr>
<td>Measured Timewalk</td>
<td>&lt;50ns @ 1ke⁻ over threshold</td>
<td>&lt;10ns @ 1ke⁻ over threshold</td>
</tr>
<tr>
<td>TOT spread</td>
<td>~5%rms</td>
<td>~6.5%rms</td>
</tr>
</tbody>
</table>

An absolute calibration using a radiation source is needed in order to confirm the values presented.
Timepix3 Wafer Probing

1. Burning e-fuses → Produces a unique ChipID
2. Power consumption (analog, digital)
3. Control voltages (Bandgap, PTAT, PLL control, ...)
4. Register values after reset
5. DACs scan
6. Matrix configuration write & read
7. S-curves with analog test pulses (Event counting mode) → gain spread
8. Noise scan (Event counting mode) → baseline & noise spread
9. TOA & TOT measurement with digital test pulses → TOT counter, TOA gray counter, fine TOA counter & VCO
Wafer Probing Yield [W1]

- **Category A (52%)**:
  - less than 30 bad pixels (randomly distributed across the whole matrix)

- **Category B (8%)**:
  - one dead column (more than 8 bad pixels in one column),
  - or one dead super pixel (more than 4 bad pixels in one super pixel),
  - or more than 30 bad pixels

- **Category C (20%)**:
  - two dead double columns or dead super pixels,
  - or more than 256 bad pixels

- **Category K (15%)**: Kidnapper pixel

- **Category Y (5%)**: Yelling pixel
First Timepix3 based TPC

Micromegas:
- 50 μm pillars;
- square pitch of holes: 60 μm

Timepix-3:
- no protection layer:
- Few minutes data at the 2 GeV electron beam at DESY
- Moire pattern due to mismatch of TPX3 and micromegas grid (55 and 60 um, resp.)
Track projections

Hitmap, He/C4H10  
Drift time versus row number, He/C4H10  
Hitmap, Ar/C4H10  
Drift time versus row number, Ar/C4H10

Drift time versus column number, He/C4H10  
Drift time, He/C4H10  
Drift time versus column number, Ar/C4H10  
Drift time, Ar/C4H10

Gas: He-Isobutane  
Gas: Ar-Isobutane
Conclusions

• Timepix3 is a new version of the Timepix chip. Main characteristics:
  – Simultaneous TOA and TOT measurement
  – Data driven and zero-suppressed readout (80Mhits/s/chip)
  – Minimum detectable charge > 500e\(^-\) (all modes)
  – Time resolution up to 1.562 ns

• All measurements (without sensor) indicate that the Timepix3 chip is fully functional as designed

• First wafer probed shows reasonable yield comparable to Medipix3RX

• First assemblies with a semiconductor sensor should be available in < 2 months
Acknowledgements

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VTT, Information Technology, Espoo, Finland
KIT/ANKA, Forschungszentrum Karlsruhe, Germany
University of Houston, USA
Diamond Light Source, Oxfordshire, England, UK
Universidad de los Andes, Bogota, Colombia
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AMOLF, Amsterdam, The Netherlands
Technical University of Munich, Germany
Brazilian Light Source, Campinas, Brazil
Timepix4?
Wafer Probing - Digital Issues

- **Dead pixels**: Change of pixel configuration (trim DAC, mask, test pulse) is not possible

- **Kidnapper pixels**: Pixel grabs readout token and does not release it, preventing other pixels from sending data (matrix reset is required)

- **Yelling pixels**: Once pixel starts sending data, it does not stop (it produces continuous stream of ~400 khits/s)
Pixel Operation Modes

ToA/ToT Mode:
- Header: 4 bits
- Address: 16 bits
- ToA: 14 bits
- ToT: 10 bits
- Fine time: 4 bits

Only ToA mode:
- Header: 4 bits
- Address: 16 bits
- ToA: 14 bits
- Not used: 10 bits
- Fine time: 4 bits

Event count mode:
- Header: 4 bits
- Address: 16 bits
- iToT: 14 bits
- Event count: 10 bits
- Not used: 4 bits
Some photos

Diced chips in gelpack
Motivation: Data driven Readout instead of frame-based

![](image)

% of pixels hit

Readout time of pixel matrix (s)

Frame-based (Timepix)

Data driven (Timepix3)

Non-sparse

Sparse-readout

Assumptions:
32 bits/pixel
65536 pixels / chip

Break-even point

25th February 2014
ESE Seminar – X.Llopart
Voltage DAC INL and DNL

![Graph showing voltage DAC INL and DNL]

- **DNL**
- **INL**
- +1 LSB
- -1 LSB

25th February 2014
Timepix to Timepix3

Timepix (2006)

Timepix3 (2013)
Timepix chip architecture

Main Specs:
- 256x256 55µm square pixels
- Analog Power → 440mW
- Bits stored in pixel → 14
- Serial readout (@100Mbps) → 9.17 ms
- Parallel readout (@100Mbps) → 287 µs
- Full custom design
- > 36M Transistors

Dynamic power is mitigated because:
- EoC is a serializer (FSR)
  - 256-to-1 in serial readout
    - Pixel Matrix frequency clock / 256
  - 256-to-32 in parallel readout
    - Pixel Matrix frequency clock / 8
- Pixel column sequential readout clock:
  - Max readout clock frequency (parallel readout) at pixel matrix is 12.5 MHz for a 3.2 Gbps chip readout
  - Column clock tree made by one “large” buffer in the EoC