Pulsed power for a CLIC vertex detector

Cristian Alejandro Fuentes Rojas, ***PH-ESE-FE, CERN***

Outline

CLIC, CLIC detector and Vertex barrel

Restrictions for powering

Power consumption @ Vertex Barrel

Power pulsing and proposed power scheme

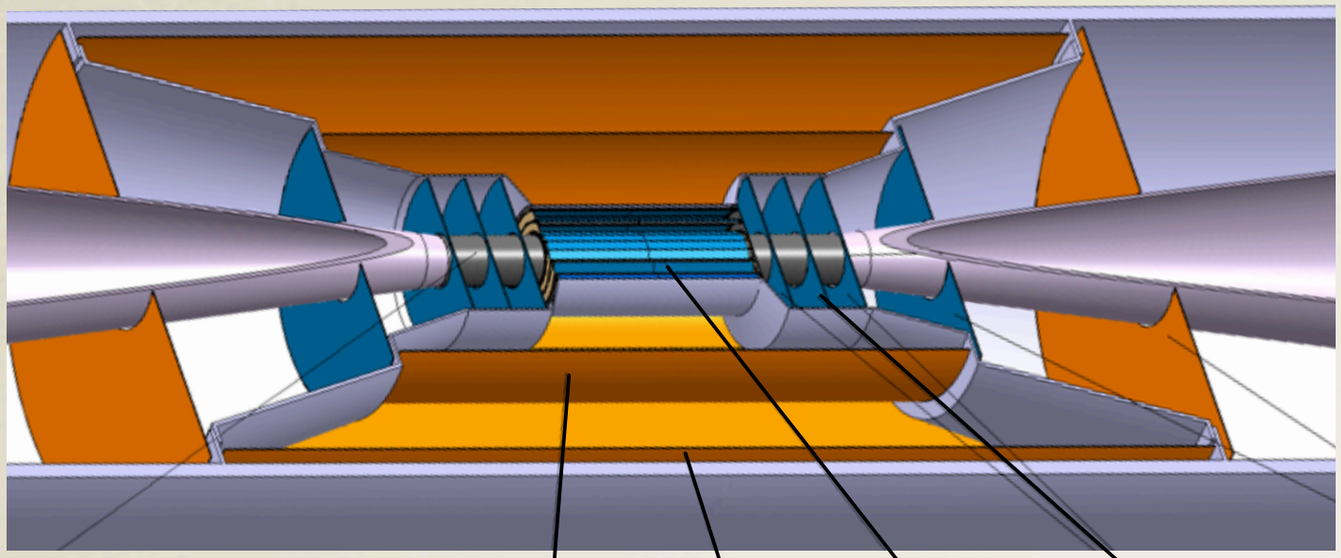
Lab prototype

Measurements and results

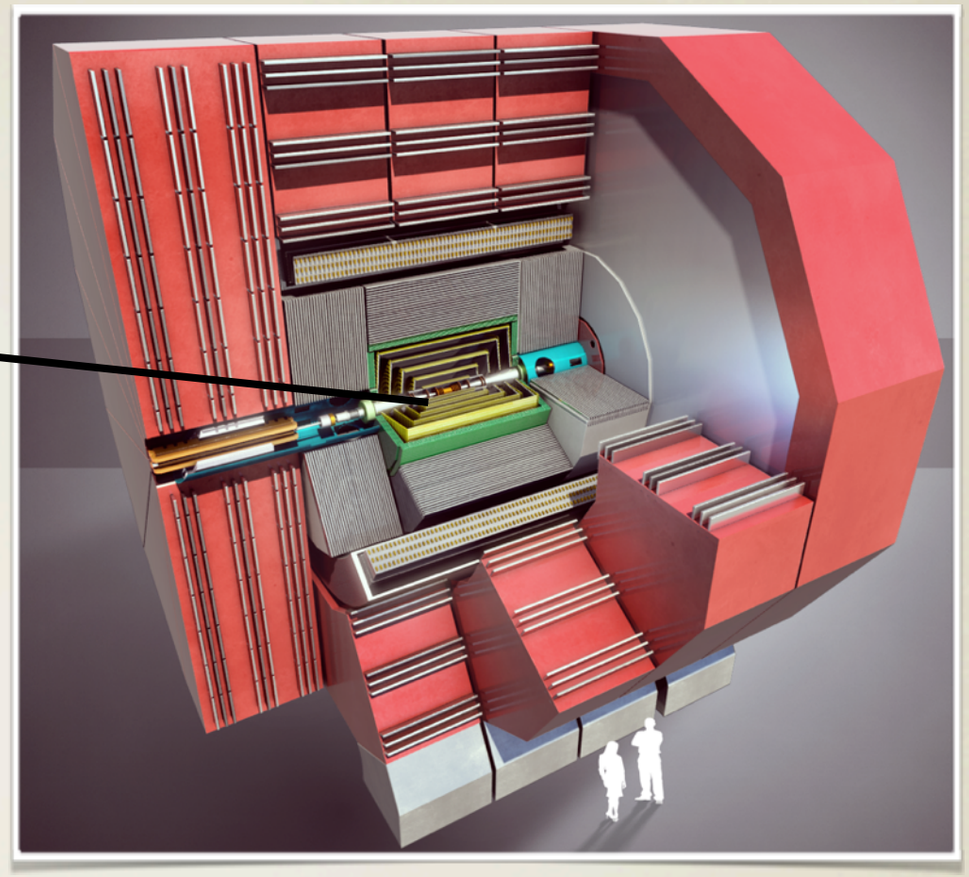
Conclusions

CLIC detector, Vertex barrel, ladder & CLICpix

CLIC_ILD inner tracking region

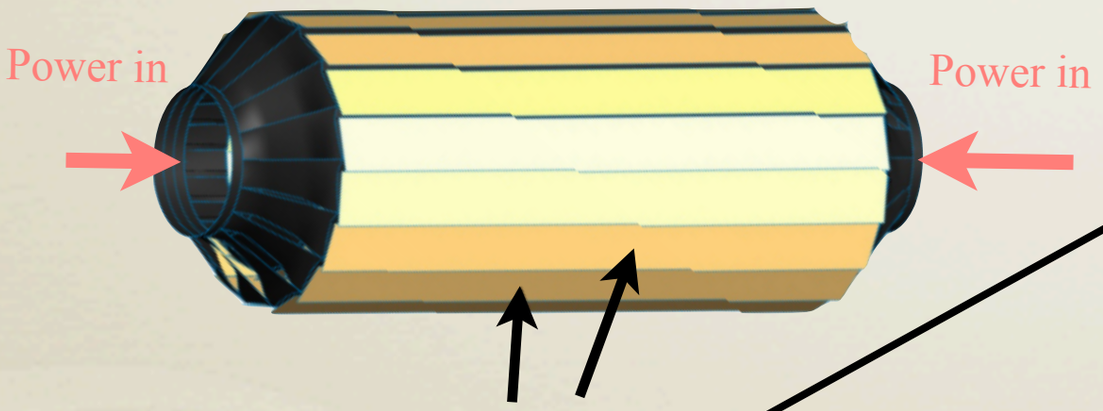


CLIC: Compact Linear Collider

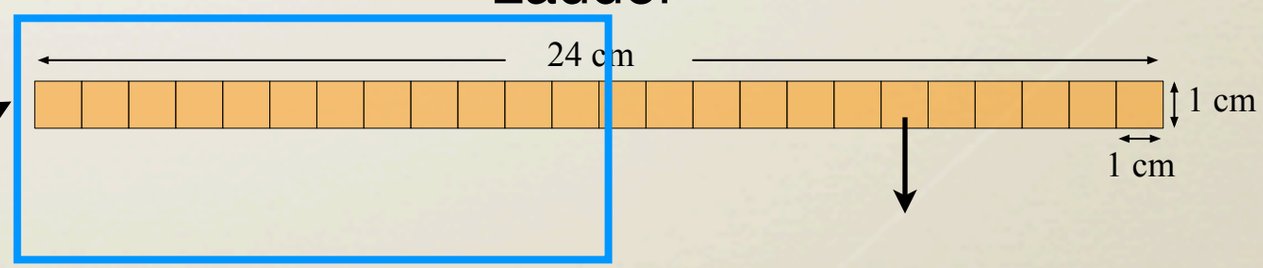


Detector

Vertex barrel



Ladder



CLICpix

Half a ladder, as we power from both sides

The ladder is formed by 24 readout ASICs (CLICpix)

Restrictions for powering

1) Material Budget: $< 0.2\%X_0$ for a detection layer, from which 0.1 $\%X_0$ is already taken by the silicon sensor + readout chip. (100 μm of silicon). This leaves, therefore, less than $0.1\%X_0$ for cooling, powering and mechanical structures.

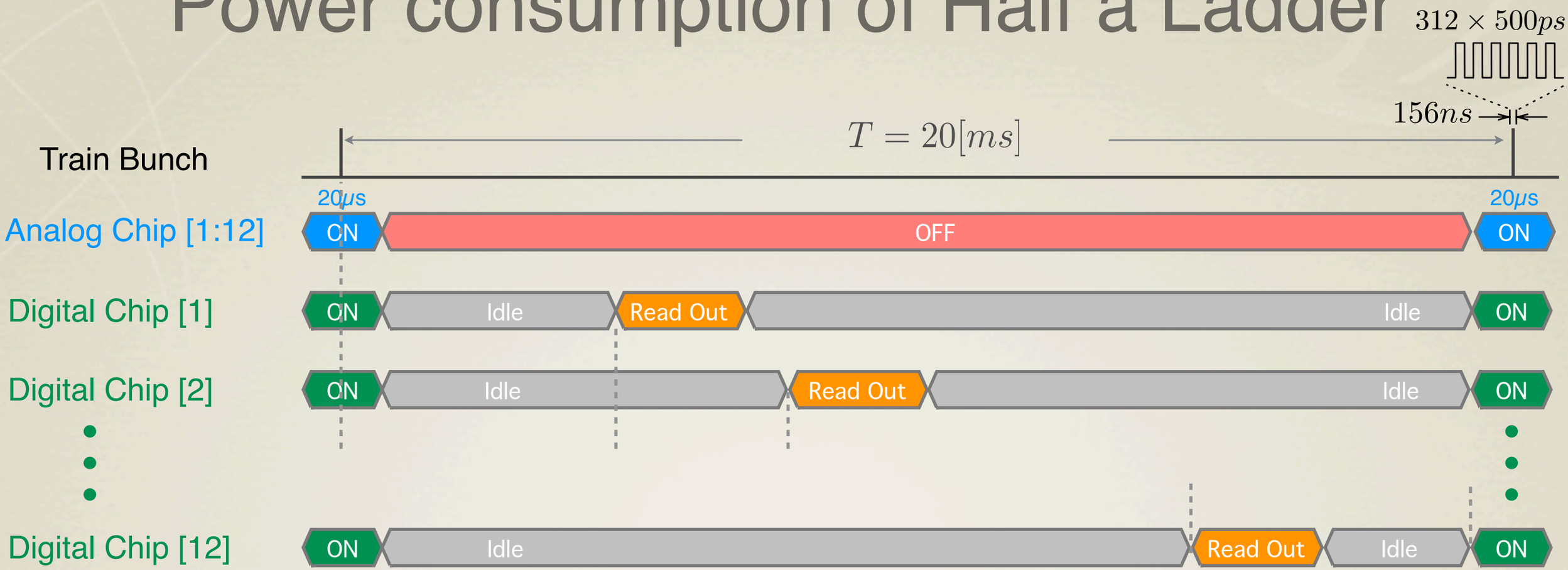
2) Low power consumption: < 50 mW/cm^2 in the sensor area, as the heat-removal solution is based on air-cooling to reduce mass.

3) High magnetic Field: 4 to 5 [Tesla] restricting the use of ferromagnetic material.

extra challenge for analog electronics

4) Regulation: within 5% (60 mV) on the ASIC during the acquisition time in order to have a correct ToT measurement. (CLICPIX specifications).

Power consumption of Half a Ladder



ON 2 W/cm² OFF Turned OFF ON 100 mW/cm² Idle 8 mW/cm² Read Out 360 mW/cm²

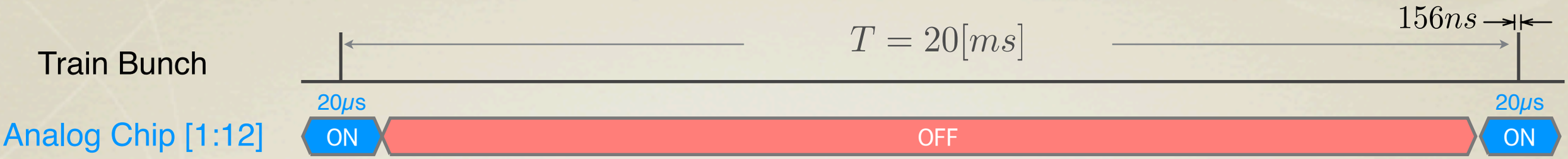
➡ Analog electronics can be turned OFF (power pulsing) to reduce the average power consumption (2m W/cm² instead of 2 W/cm² if it was ON all the time)

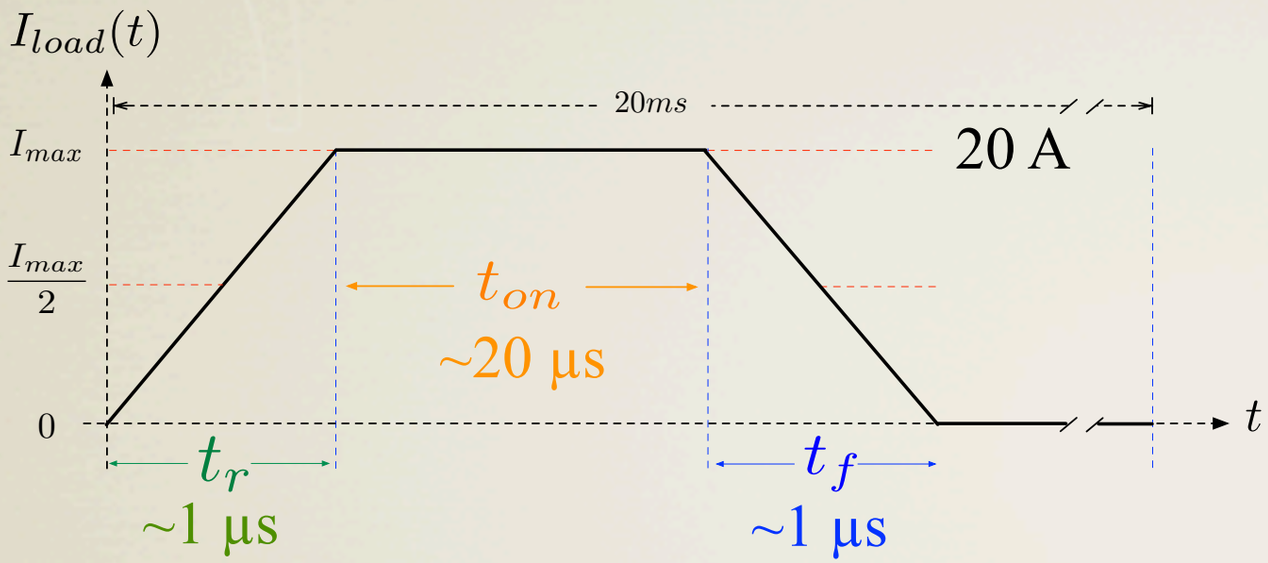
➡ One chip is readout at a time. The time the chip needs to be read out depends on the occupancy, which maximum is 3% (300 μs). Avg power consumption= 13m W/cm²

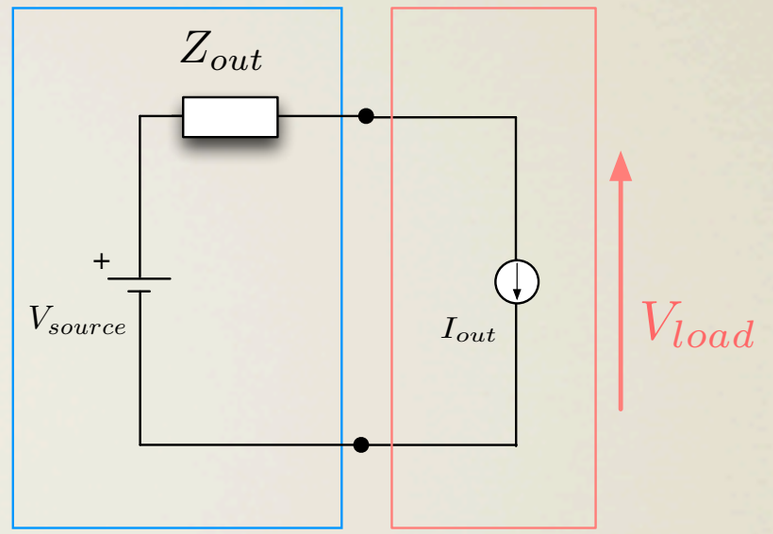
➡ Analog voltage is 1.2V while the digital is expected to be 1V.

Analog and Digital will be powered separately. In that way, their powering schemes could be optimized independently to achieve the requirements from previous slide.

Powering half a ladder (analog) (1)







Thevenin Equivalent Model

If Zout has inductance (which it will)

$$V_{load} = \ldots + L\frac{di(t)}{dt}$$

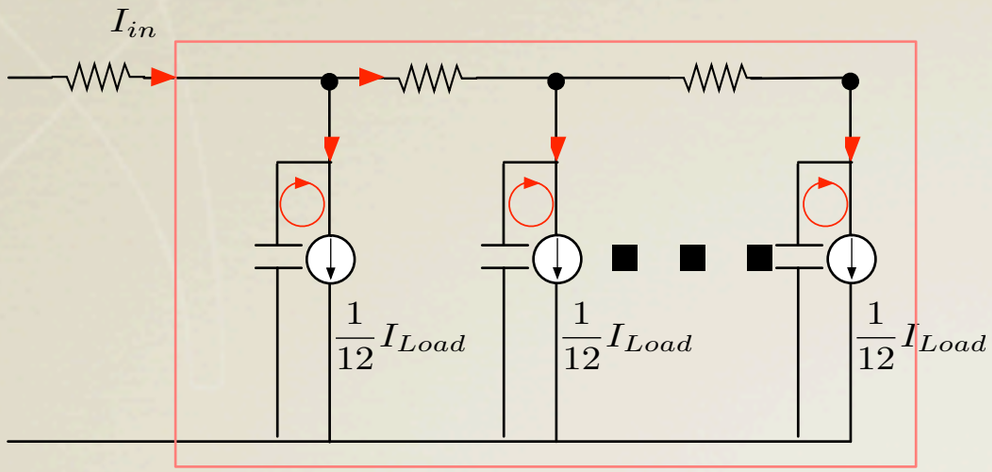
So we would like to have a gentle rise and fall times to have a good regulation.

We have defined that as 1 μs

This will be achieved by turning on the ASIC by parts.

Powering half a ladder (analog) (2)

Capacitors close to each ASIC at the FE:



$$\Delta V = I \frac{\Delta t}{C}$$

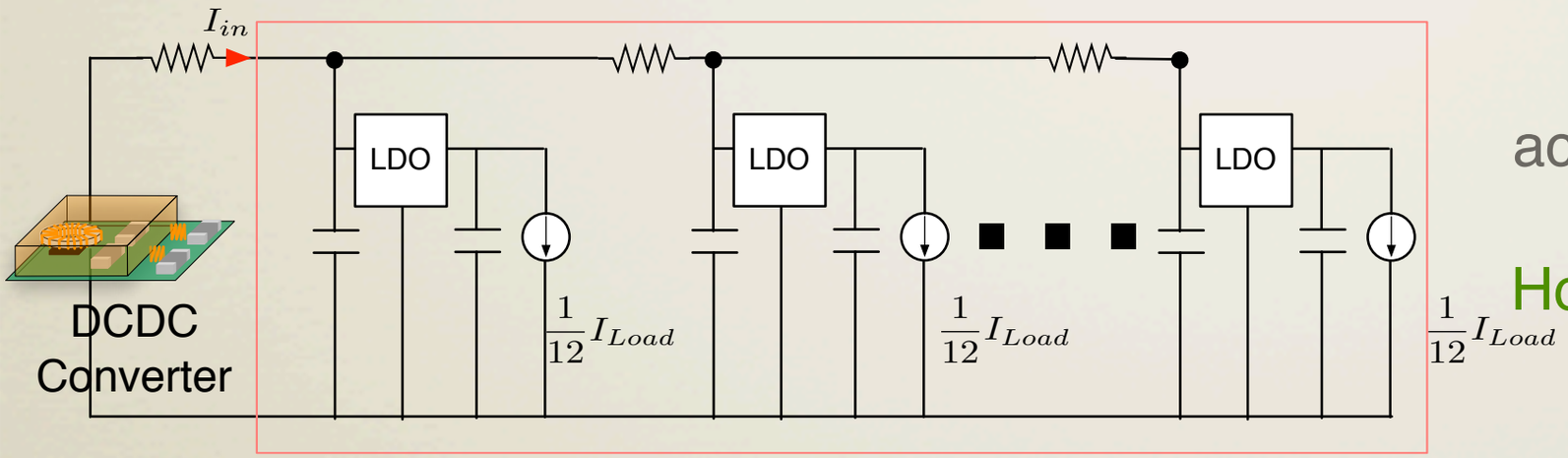
A 0805 SMD ceramic capacitor per ASIC has a $\%X_0$ =0,17!!

✔ The current loop is very small.

✖ Capacitors must be small: material restriction. (but they should reach at least 10μF).

✖ Additional regulation is still needed, as the capacitors discharge when the load is active.

Low dropout (LDO) voltage regulators added per ASIC:



The regulation in the ASIC is achieved, but the input capacitor still discharges..

How do we charge it back to its level to be ready for the next cycle?

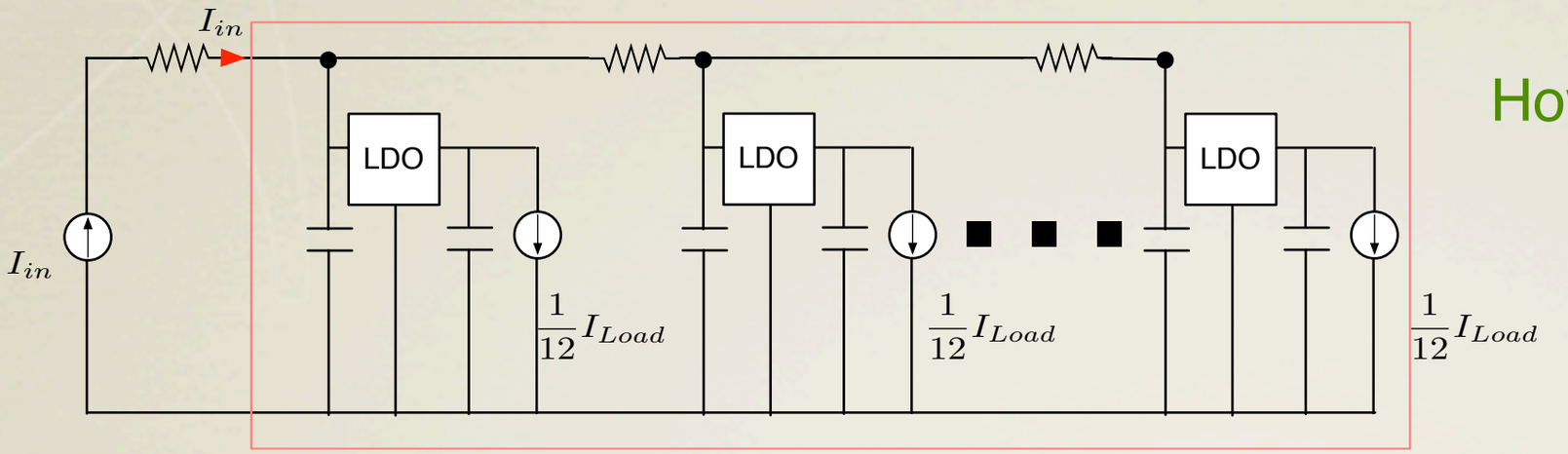
DCDC converter option: (Reported last TWEPP 2012)

✔ Its feedback loop charges up the capacitors to the required level.(easy implementation)

✖ Introduces not negligible amount of mass, too high for this particular application.

✖ Current peaks while charging the capacitor. (and it doesn't use the whole idle time)

Powering half a ladder (analog) (3)



How do we charge it back to its level to be ready for the next cycle?

...second approach.

Controlled current source at the back-end: (Presented last TWEPP 2013)

Simpler idea behind, but more difficult to implement.

An estimation of the current at the BE, using the whole period to charge the capacitor, is:

$$I_{in} = I_{load}\frac{t_{on}}{T} \approx I_{load}\frac{20\mu s}{20ms} \approx \frac{I_{load}}{1000} \approx 20mA$$

✔ Cables from the back-end to the capacitors @ FE can be really light in terms of mass.

From now on, this presentation will refer to this approach.

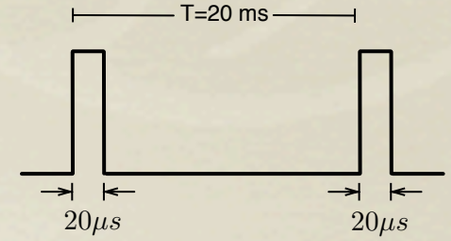
Principle and waveforms of the scheme

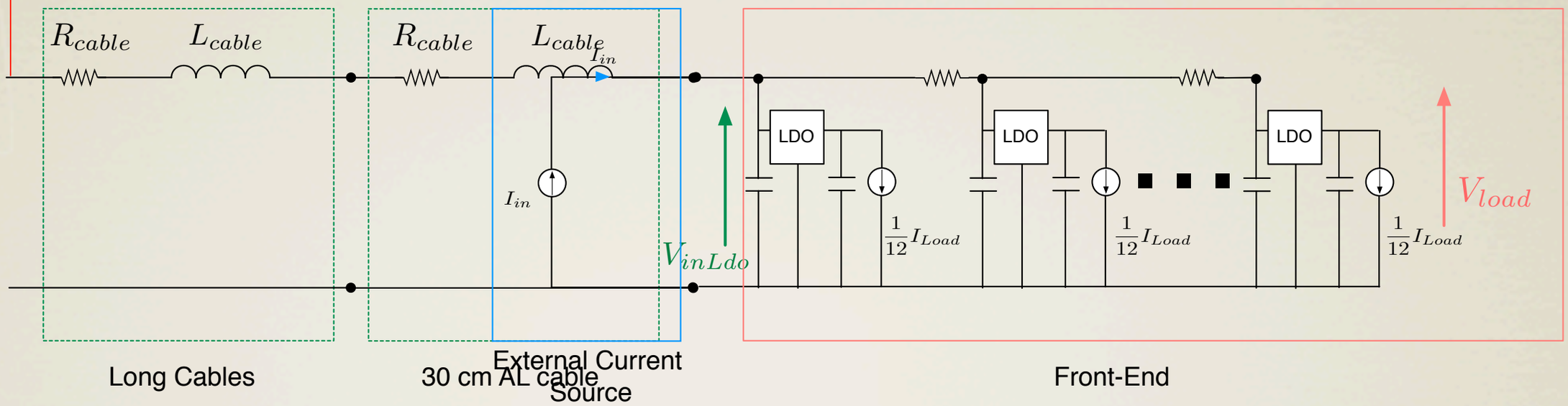
$I_{in} = f(V_{in}, t, V_{nominal})$

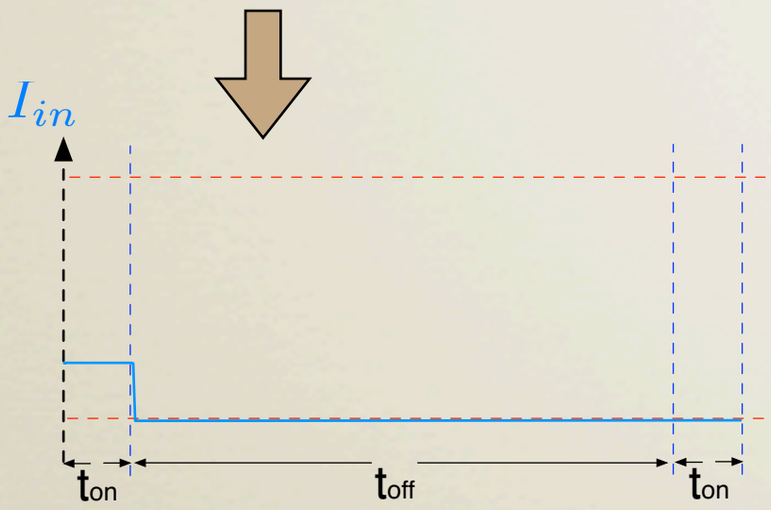
out: Control Current Source

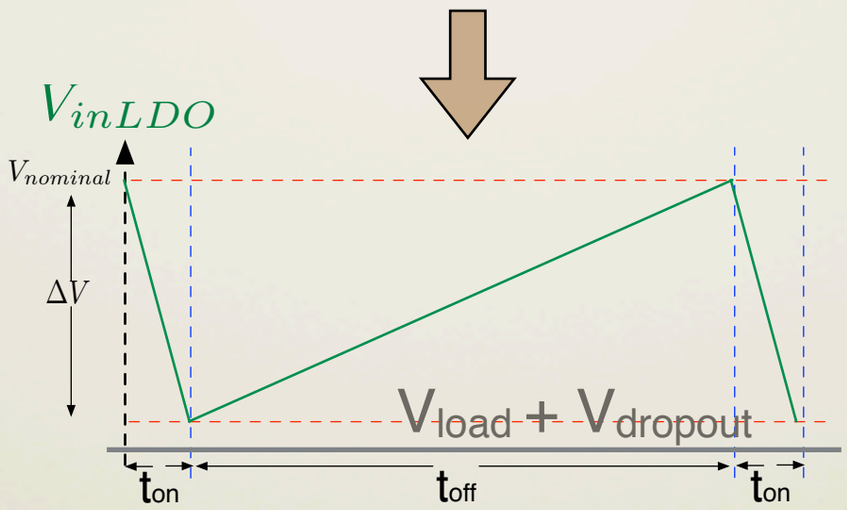
FPGA

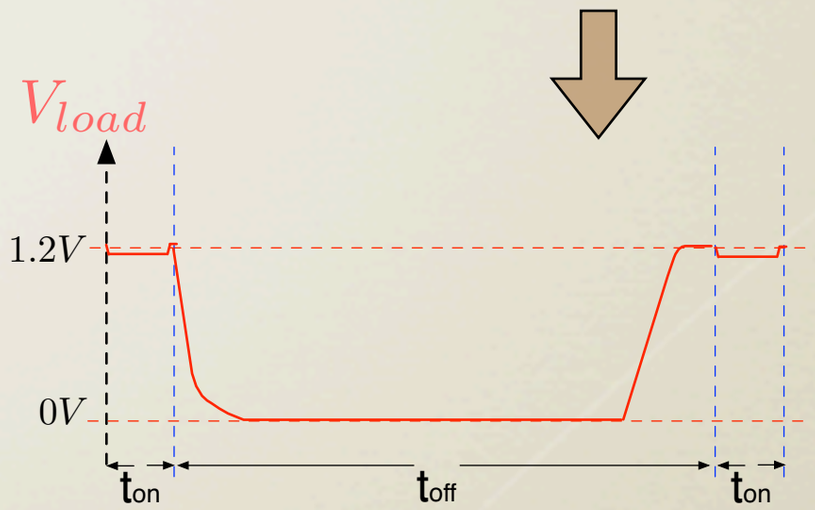
in: Voltage storage capacitors











In order to work, the following condition has to be fulfilled:

$$V_{inLDO}(t) > V_{load} + V dropout$$

$$V_{nominal} - \Delta V > V_{load} + V dropout$$

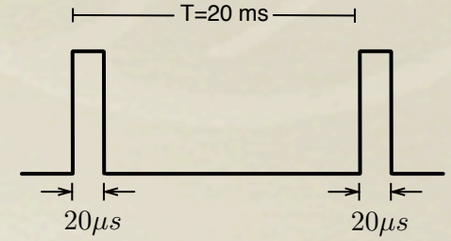
Principle and waveforms of the scheme

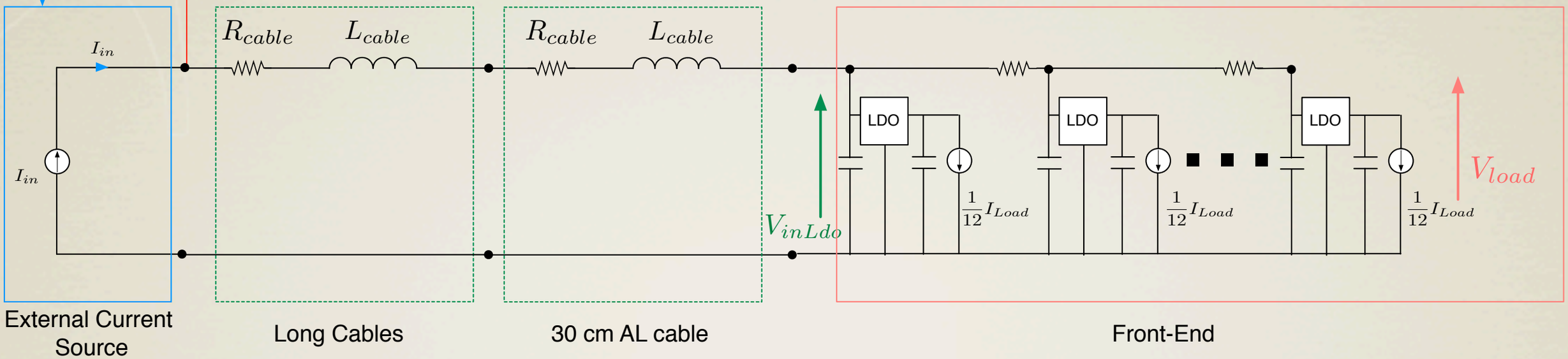
I_{in}= f (V_{in} , t , $V_{nominal}$)

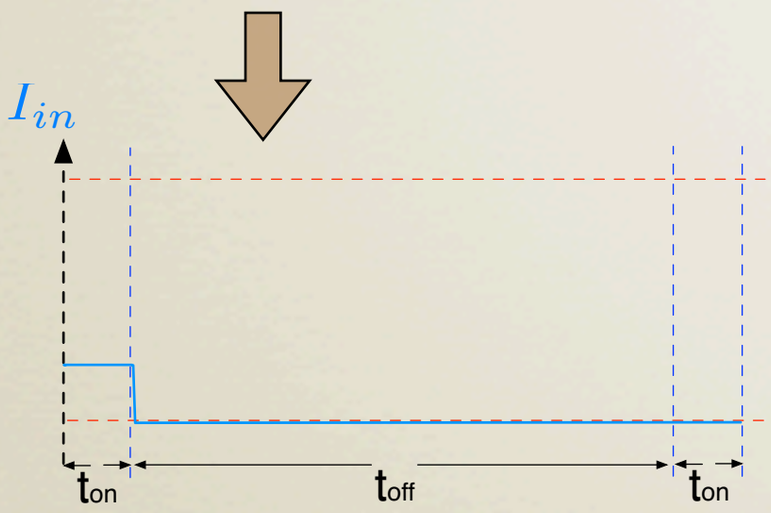
out: Control Current Source

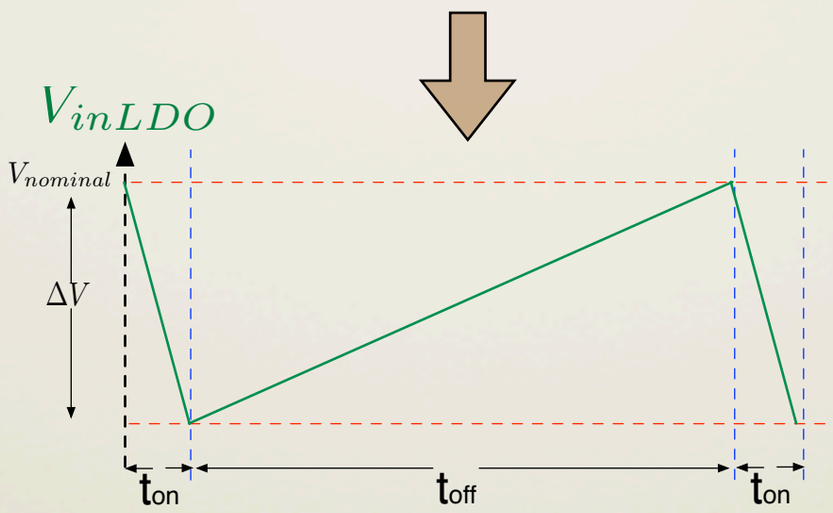
FPGA

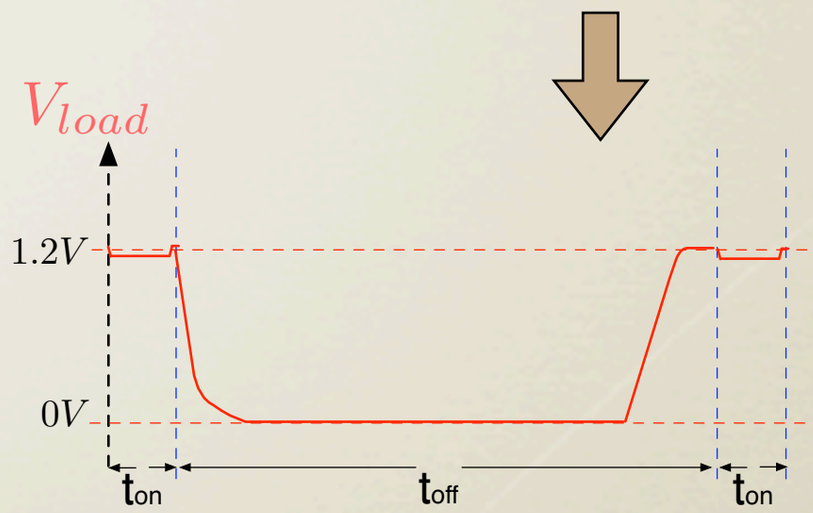
in: Voltage storage capacitors









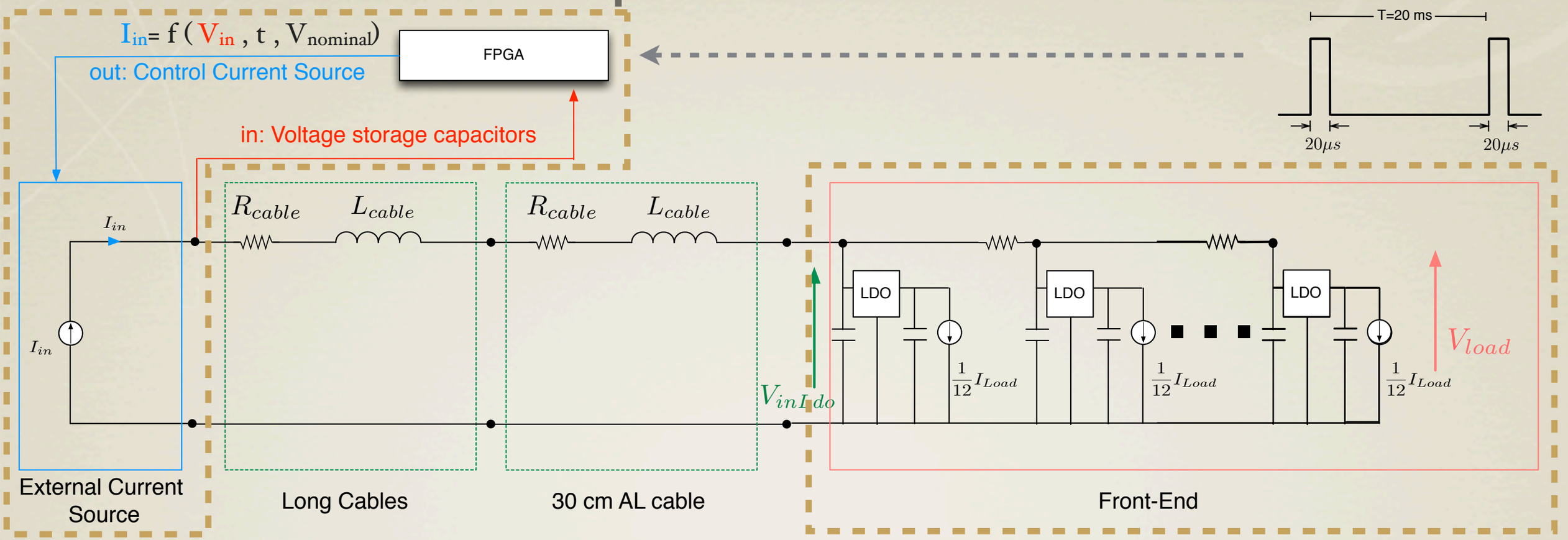


In order to work, the following condition has to be fulfilled:

$$V_{inLDO}(t) > V_{load} + V dropout$$

$$V_{nominal} - \Delta V > V_{load} + V dropout$$

Implementation



Power components back-end

+

FPGA

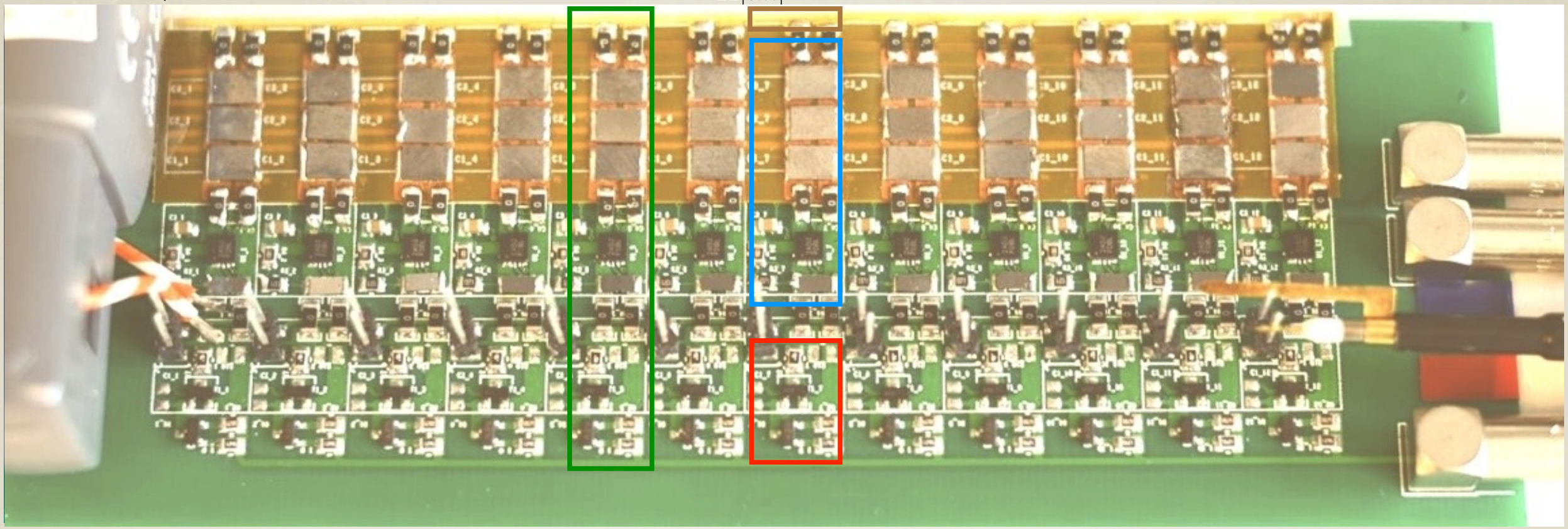
Power components in the ladder

FE ASICs or Dummy Loads

We will address this first in next slide.

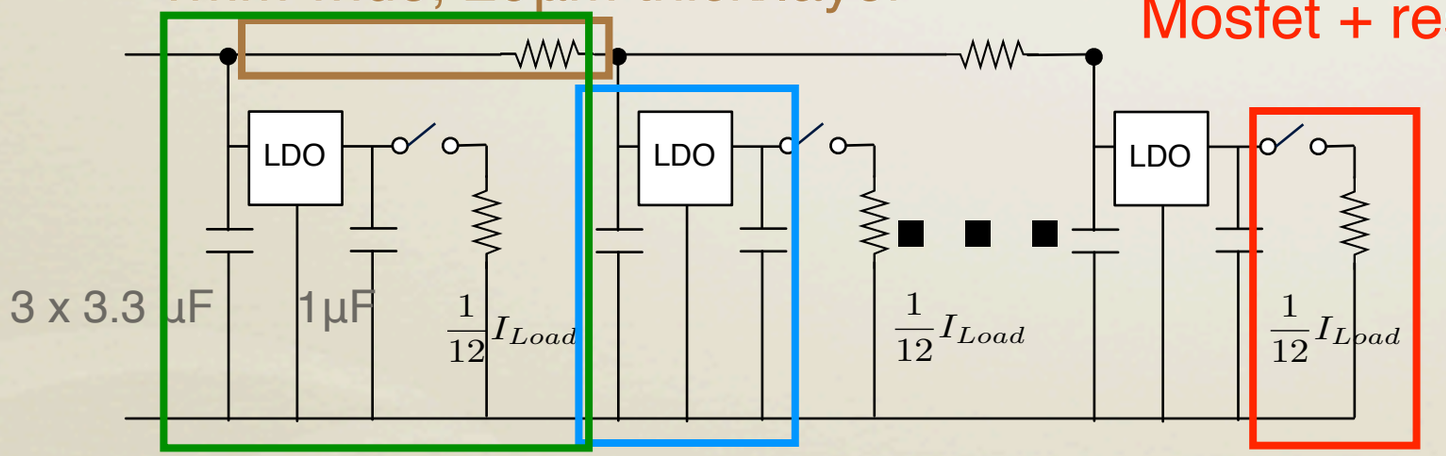
Evaluation using Analog Dummy Load

The CLICpix is being developed, so in order to test the scheme we need a dummy load.



Two layers Aluminium Flex Cable
1mm wide, 20µm thick/layer

Dummy load:
Mosfet + resistor



This duplicates 12 times, representing the 12 ASICs, the power storage, regulation and cabling.

Power storage and regulation:
input Si cap (3 x 3.3 µF) + LDO (out: 1.2V) + output Si cap (1µF)

Why aluminium cables?

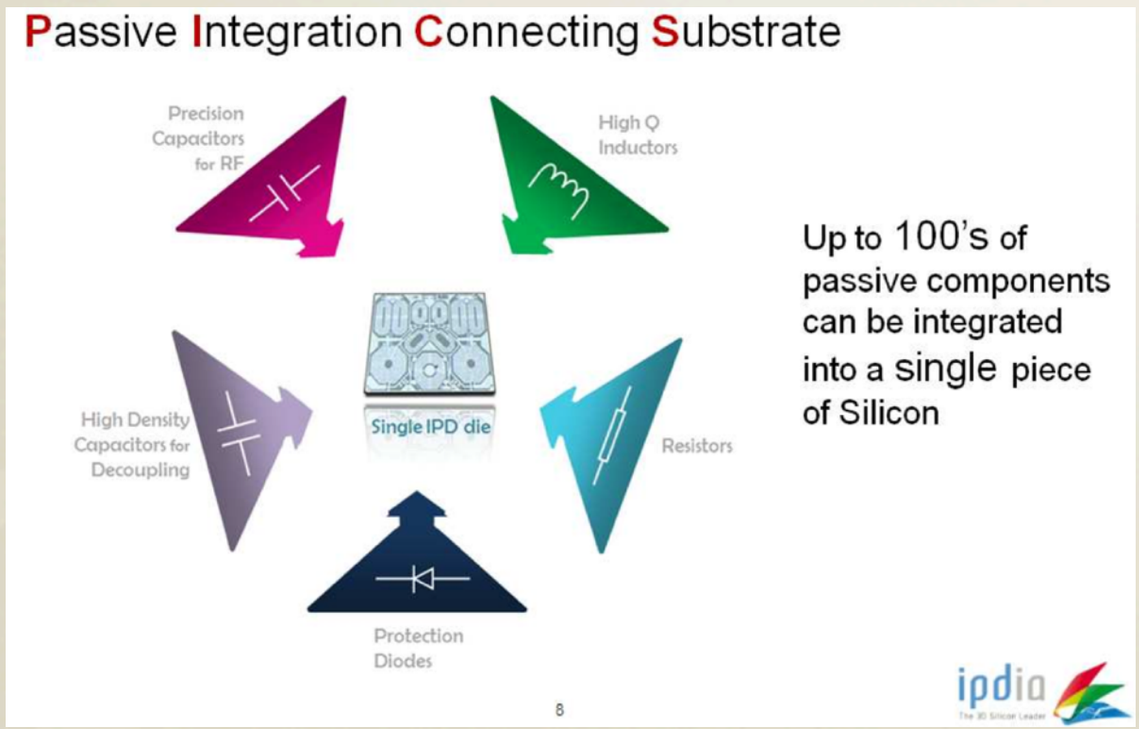
For the same resistance than a copper cable, aluminium cables have around 4 times lower material contribution. The aluminium flex cables were made at the CERN PCB shop.

Why silicon capacitors?

Low mass and flat. They can have a thickness down to 80 µm.

Ceramic capacitor of small smd package (0402 or 0201) can have comparable material. Nevertheless, their capacitance change dramatically (more than 80% of their value for some conditions) with the voltage applied (V_{bias}), making them impractical for our application.

IPDiA company can integrate all the necessary passive components into a single die

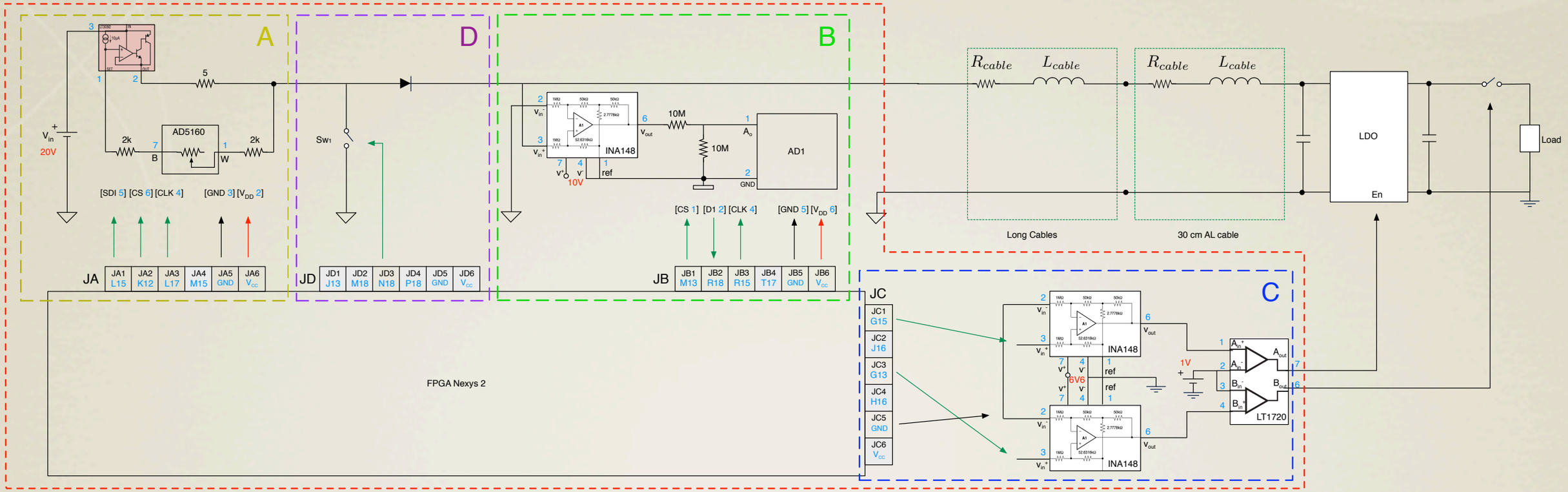


Which can be afterwards connected to the CLICpix chip using TSVs (Through Silicon Vias).

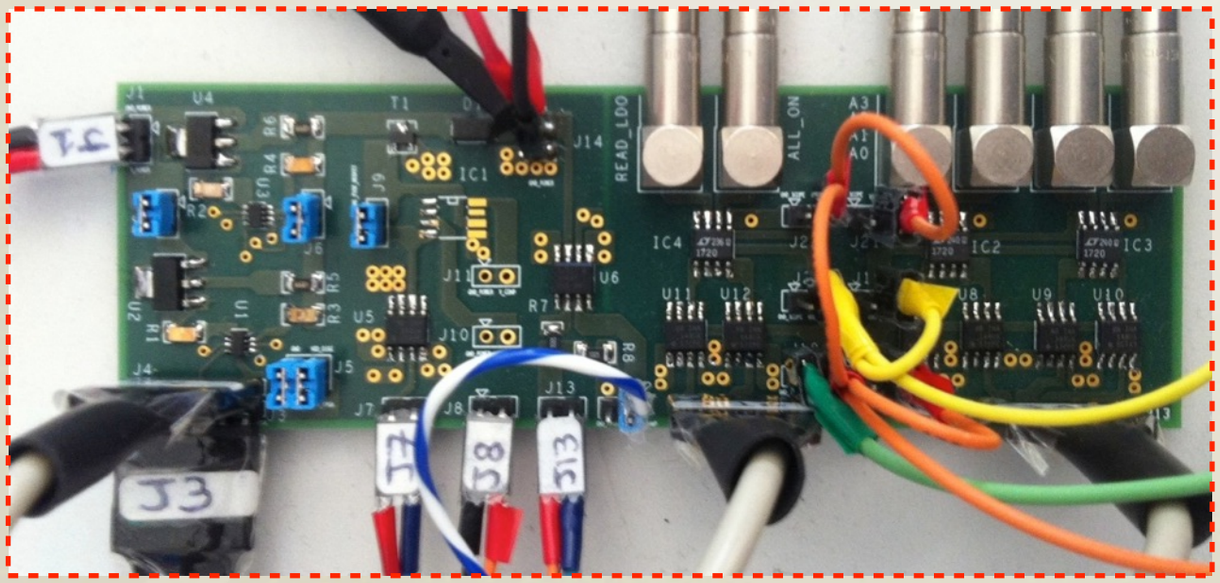
This is just a preliminary idea.

Power components BE and FPGA (Analog)

Schematic

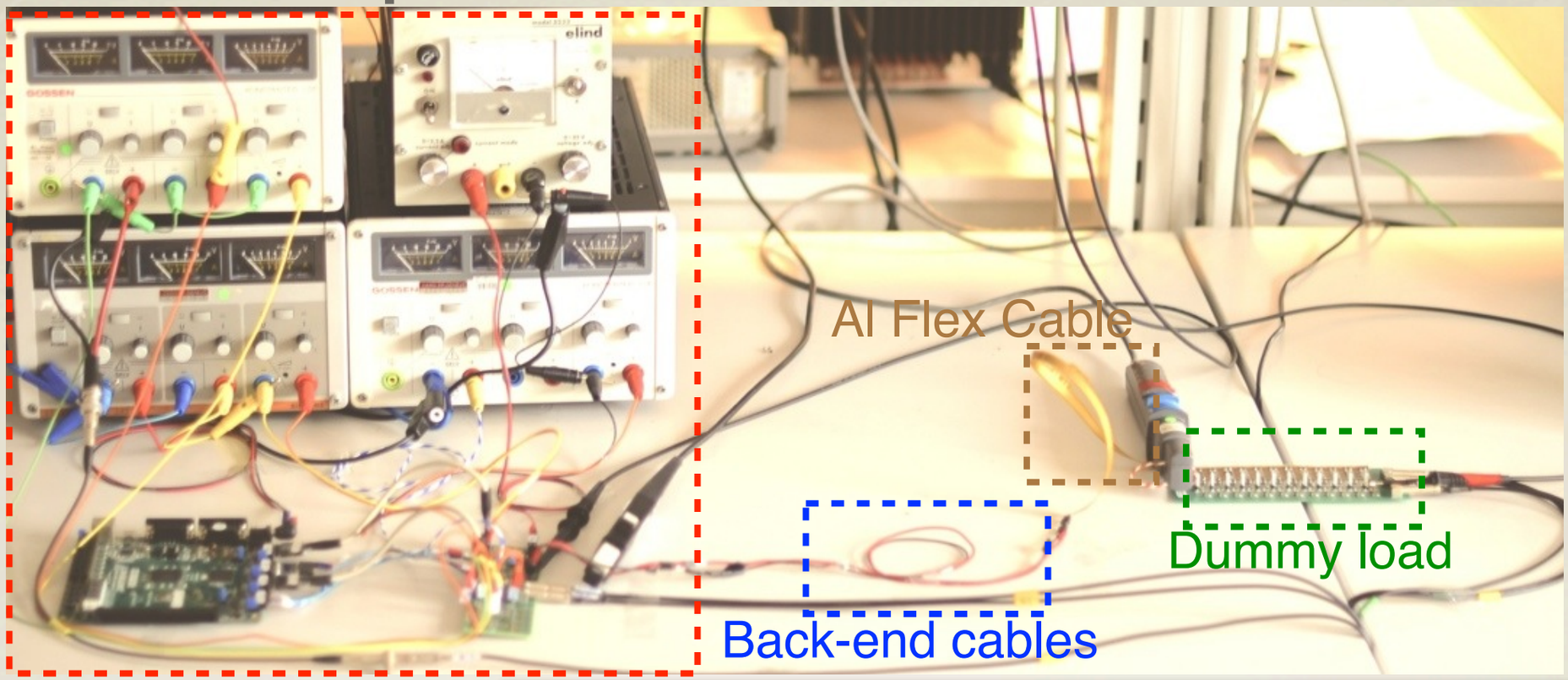


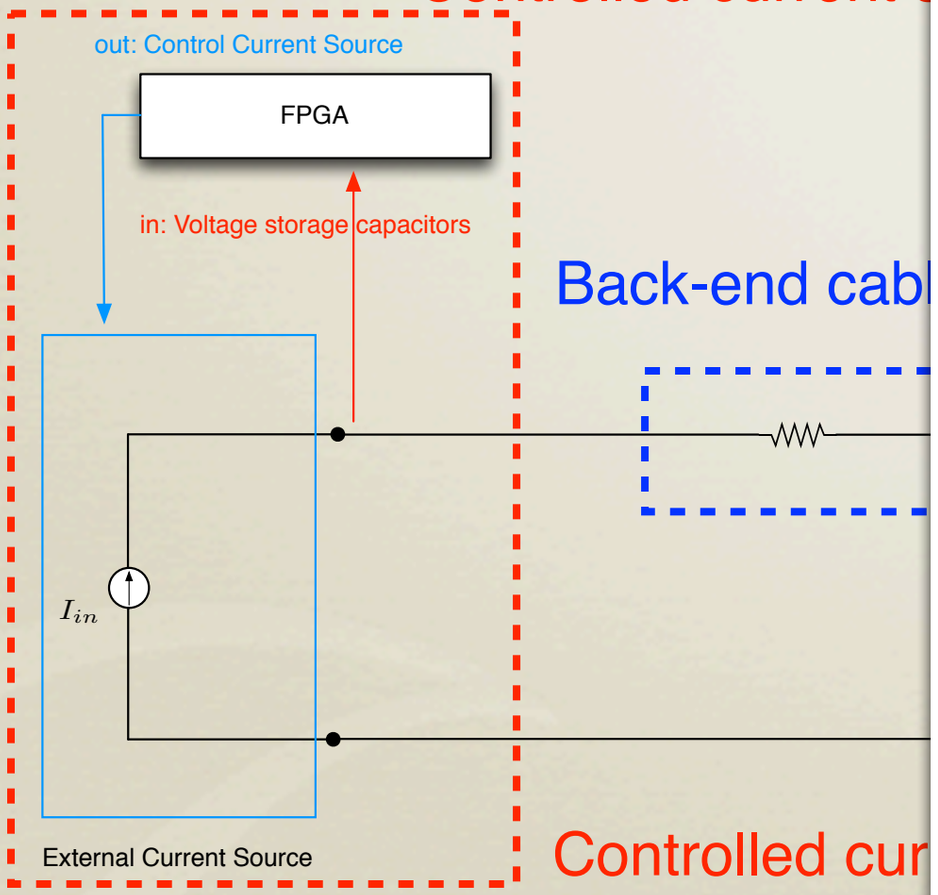
PCB implementation

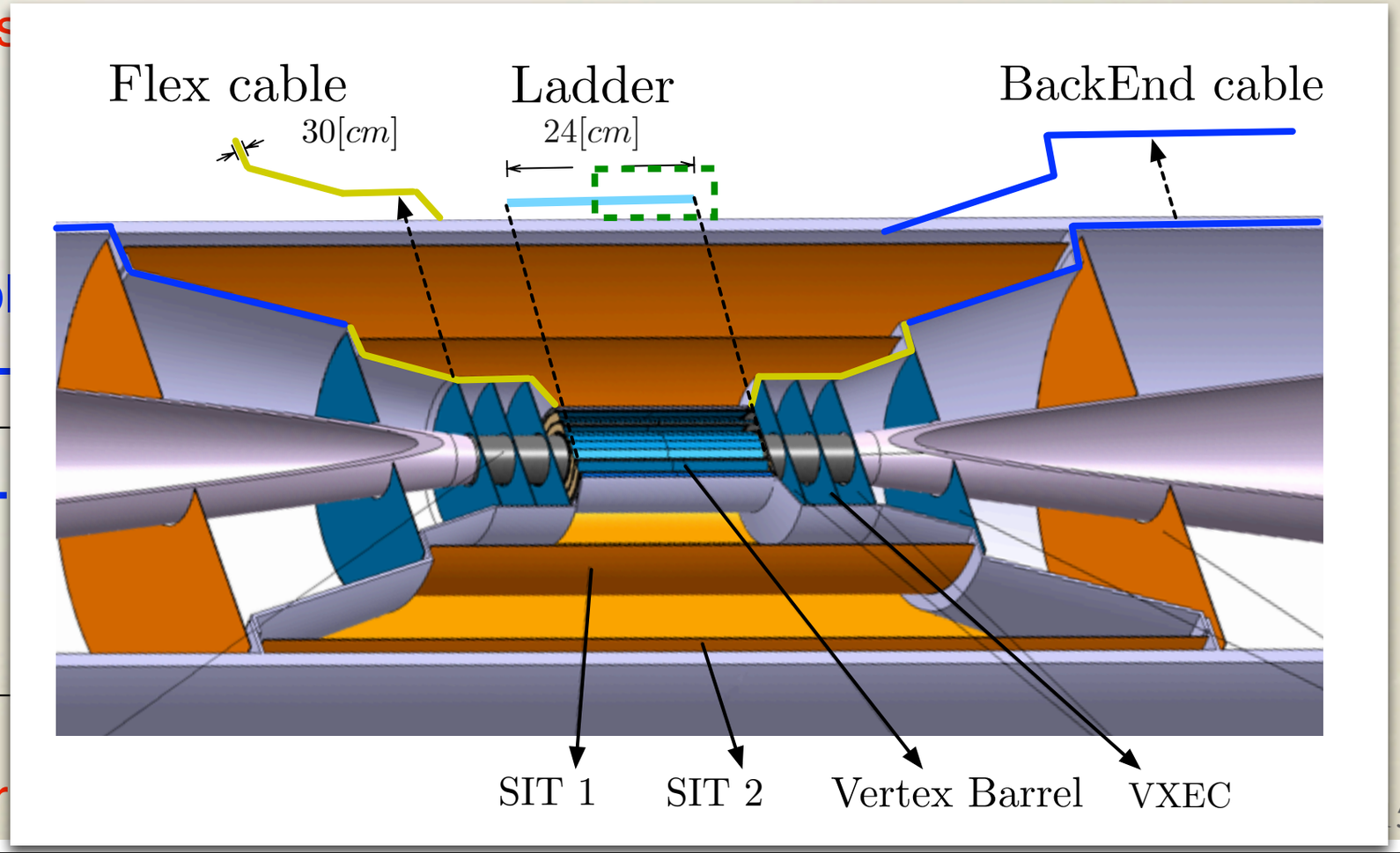


FPGA

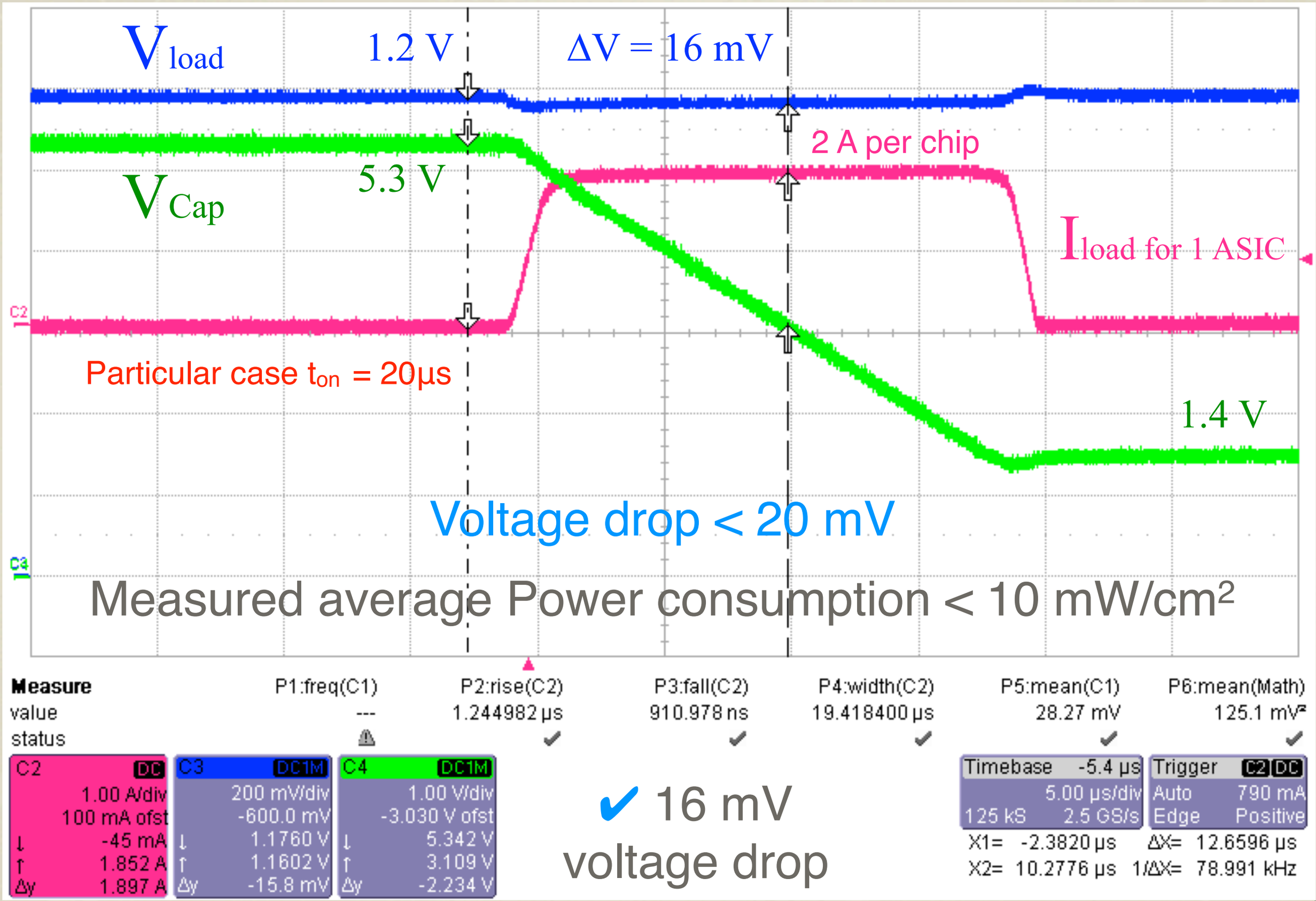
Implementation @ Lab





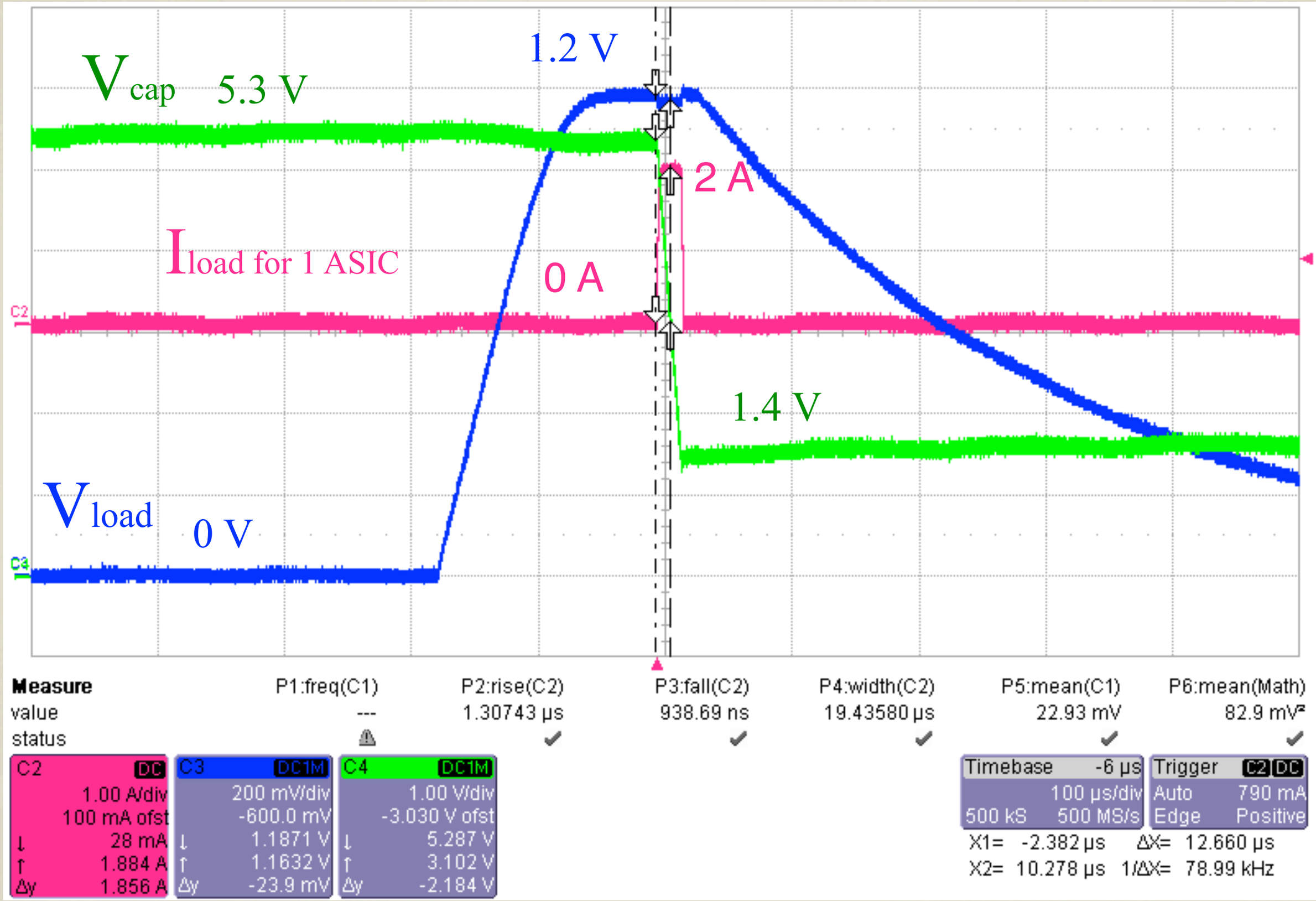


Regulation during t_{on} < 20 mV (analog)

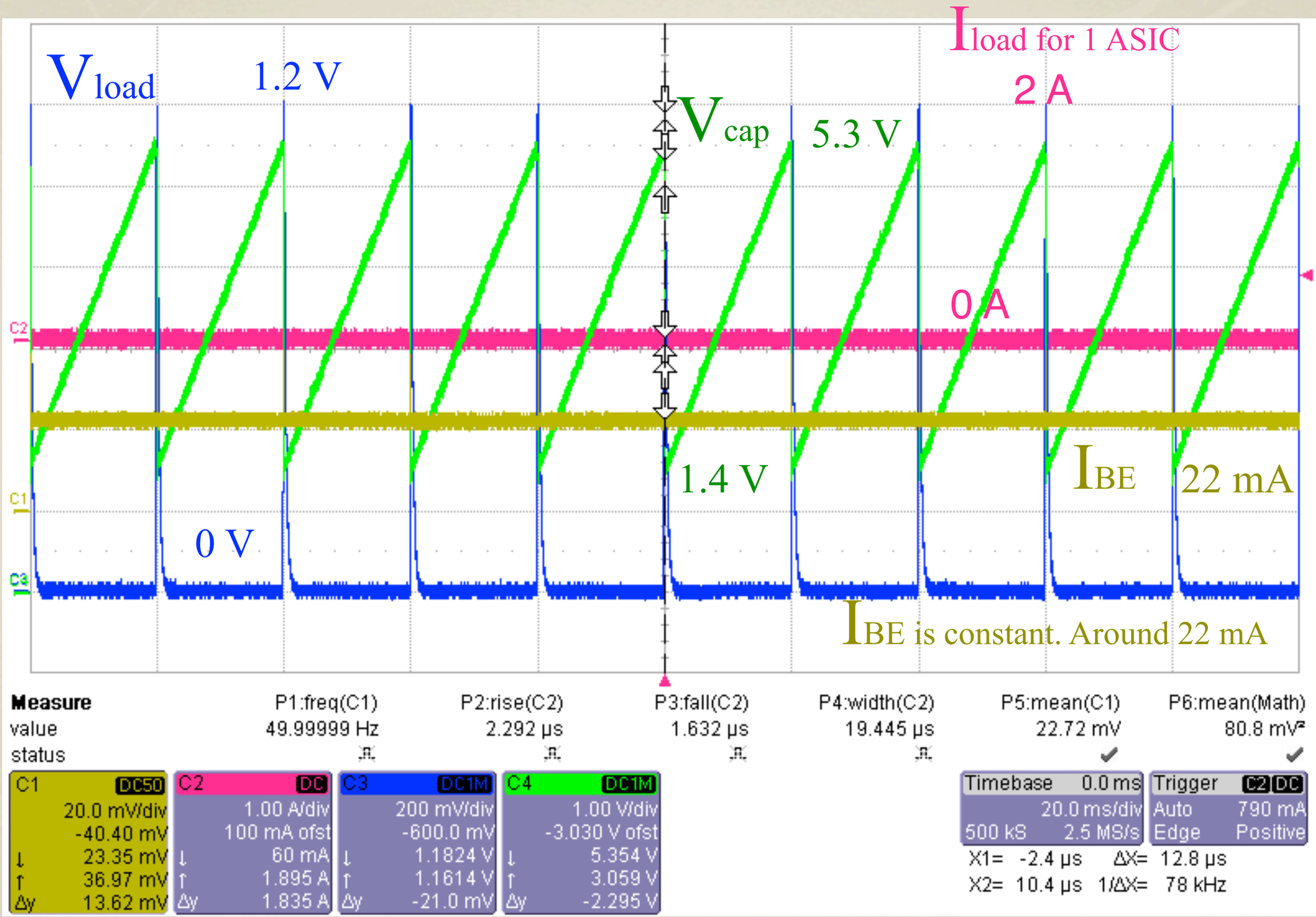


✔ 16 mV voltage drop

En/Dis voltage regulator (analog)



Measurements for same load value (analog)



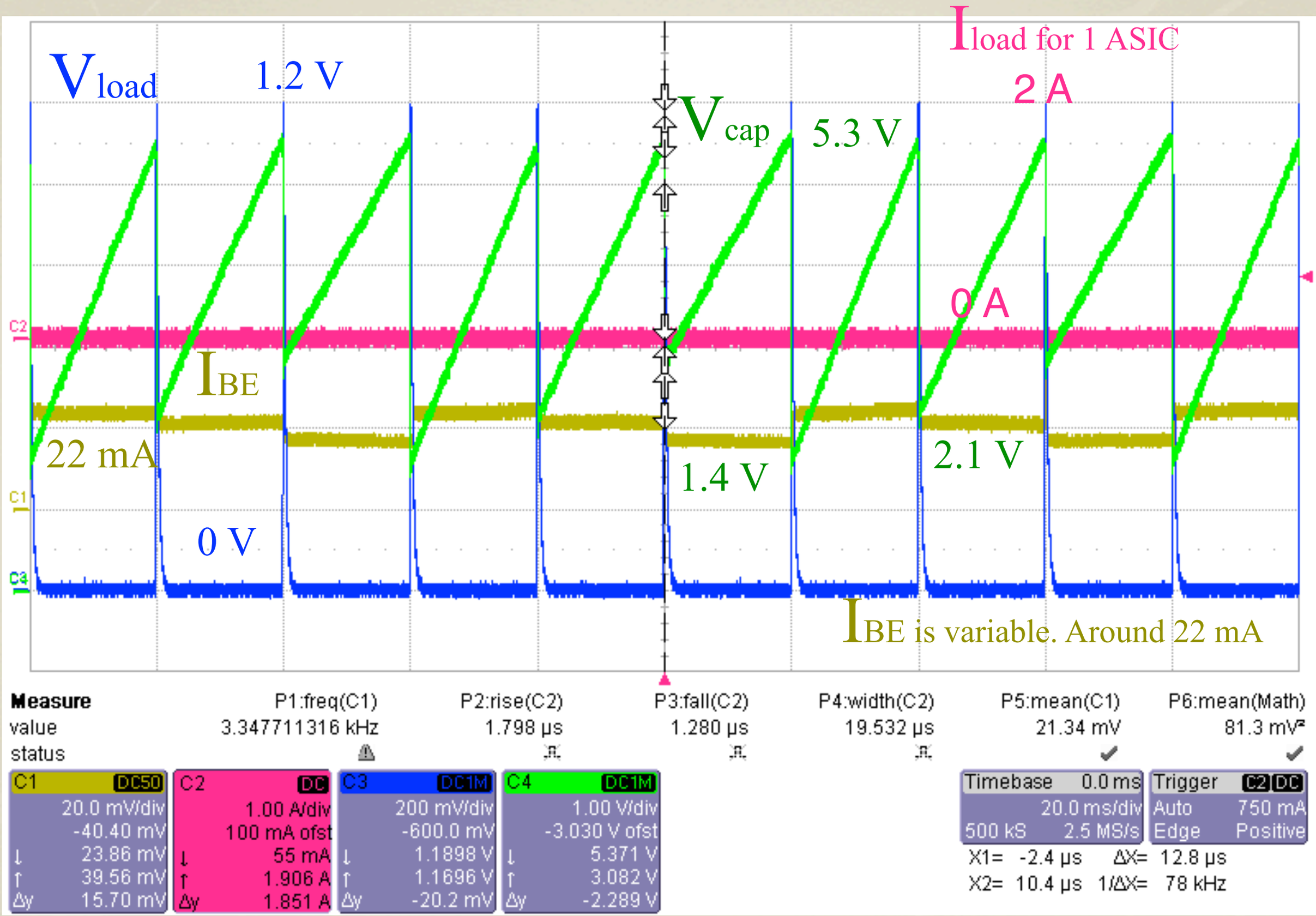
Measure	P1:freq(C1)	P2:rise(C2)	P3:fall(C2)	P4:width(C2)	P5:mean(C1)	P6:mean(Math)
value	49.99999 Hz	2.292 µs	1.632 µs	19.445 µs	22.72 mV	80.8 mV²
status					✓	✓

C1 DC50	C2 DC	C3 DC1M	C4 DC1M
20.0 mV/div	1.00 A/div	200 mV/div	1.00 V/div
-40.40 mV	100 mA ofst	-600.0 mV	-3.030 V ofst
↓ 23.35 mV	↓ 60 mA	↓ 1.1824 V	↓ 5.354 V
↑ 36.97 mV	↑ 1.895 A	↑ 1.1614 V	↑ 3.059 V
Δy 13.62 mV	Δy 1.835 A	Δy -21.0 mV	Δy -2.295 V

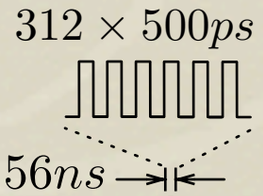
Timebase 0.0 ms	Trigger C2 DC
20.0 ms/div	Auto 790 mA
500 kS 2.5 MS/s	Edge Positive

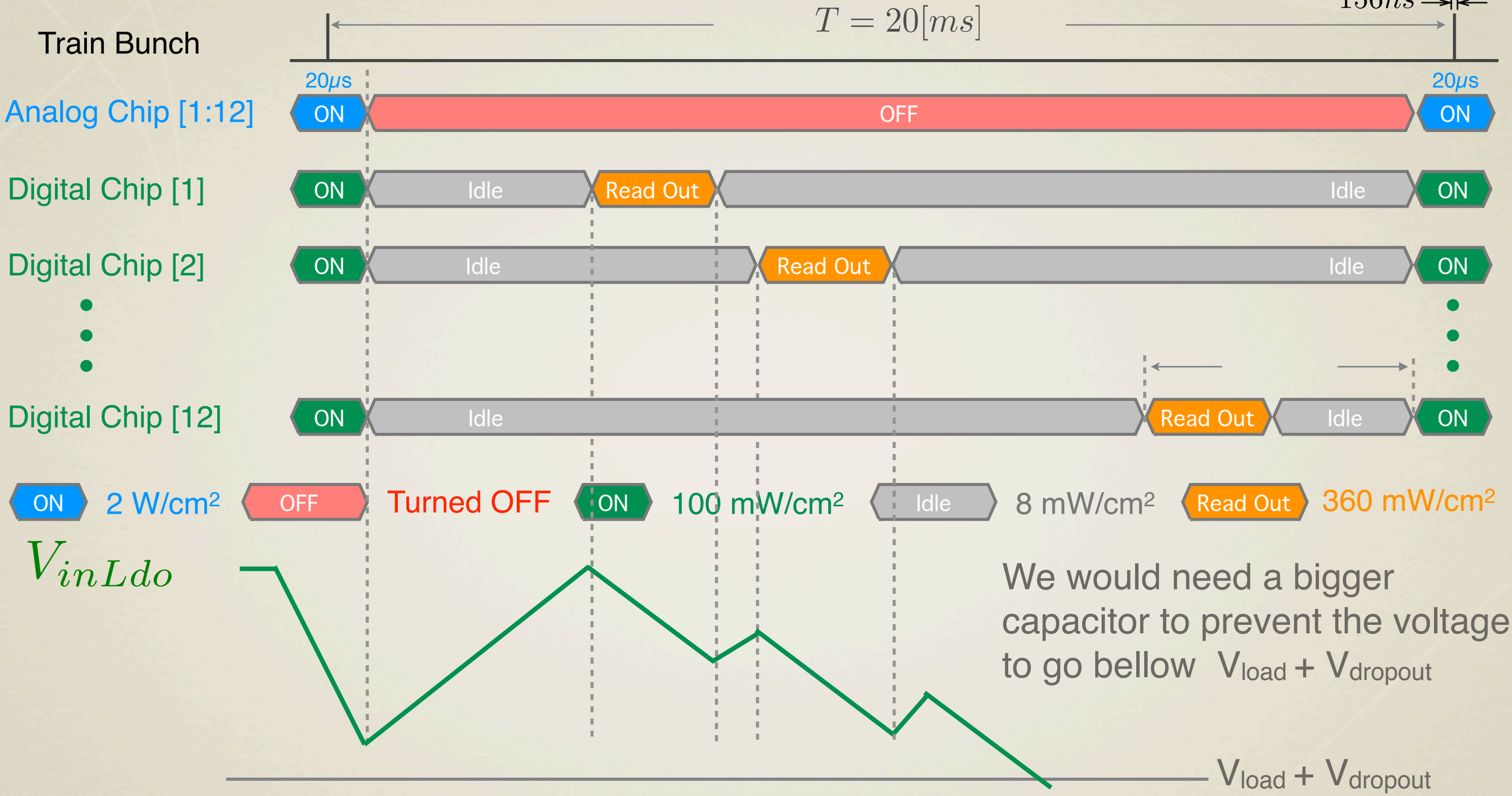
X1= -2.4 µs ΔX= 12.8 µs
X2= 10.4 µs 1/ΔX= 78 kHz

Change in the load consumption (analog)



Power consumption of Half a Ladder





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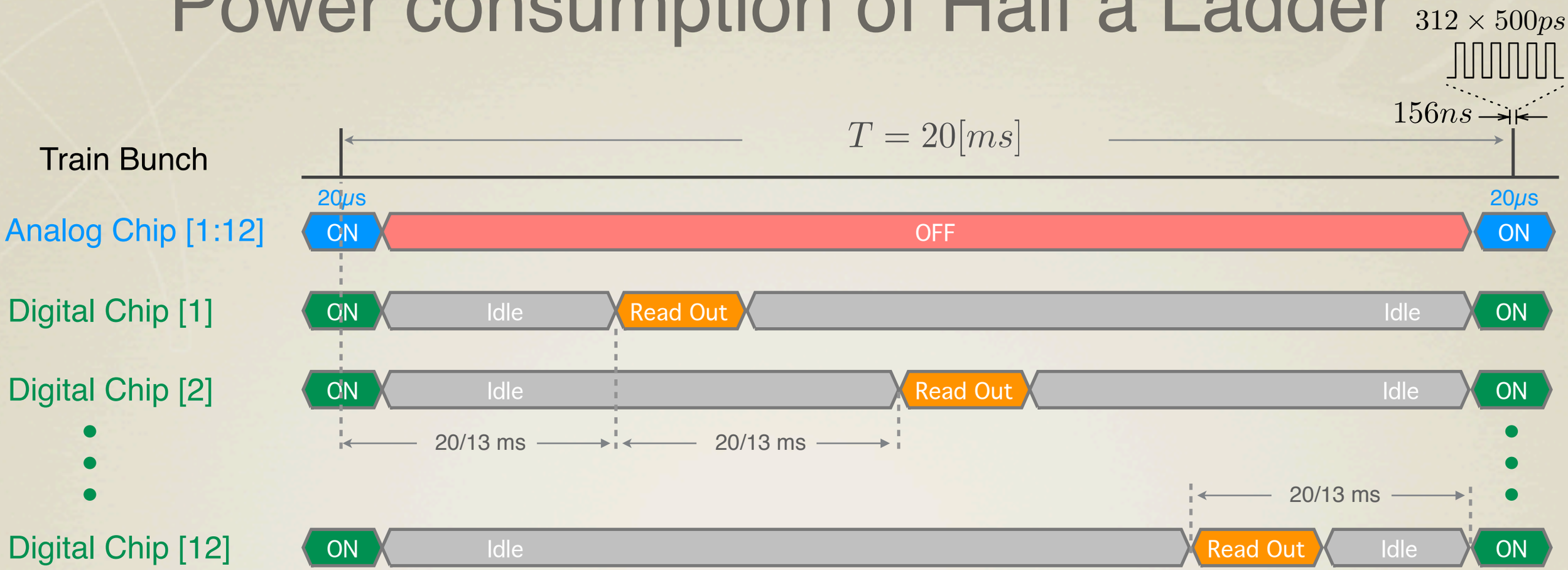


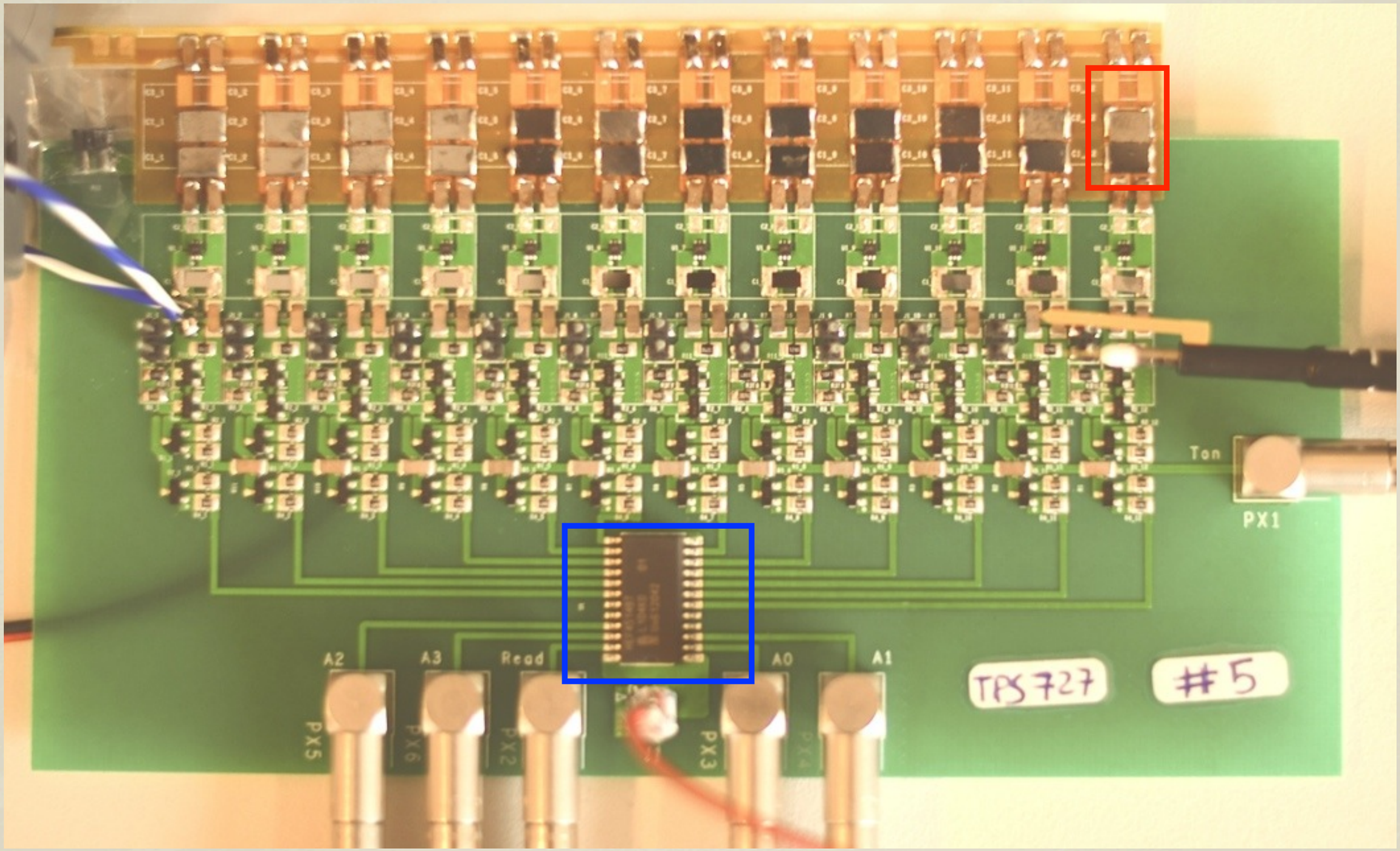
ON 2 W/cm² OFF Turned OFF ON 100 mW/cm² Idle 8 mW/cm² Read Out 360 mW/cm²

➡ One chip is readout every 20/13 ms. The time the chip needs to be read out depends on the occupancy, which maximum is 3% (300 μs). Avg power consumption= 13m W/cm²

➡ Now it can be solved similarly than for the analog part, with the difference that the time to charge the capacitor is smaller but the power consumption is lower too.

Digital Dummy Load / test board

We reduced the capacitors from 10 μF to 6.6 μF



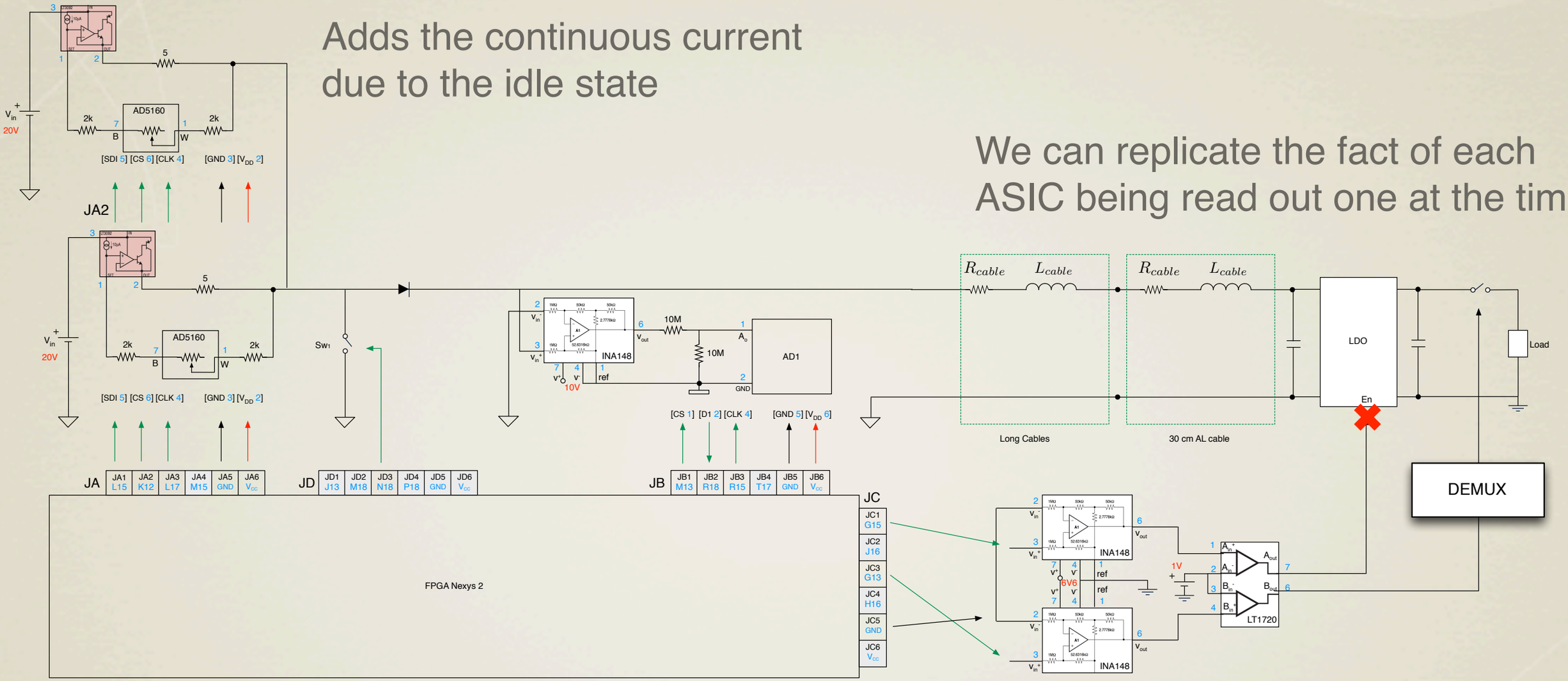
We added the possibility to switch individual MOSFETs to represent the read out of the ASICs

Power components BE and FPGA (Digital)

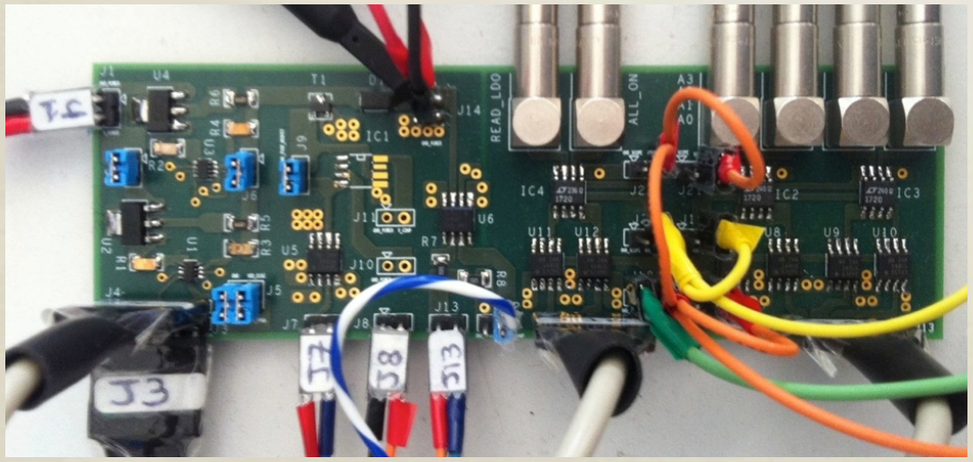
Schematic

Adds the continuous current due to the idle state

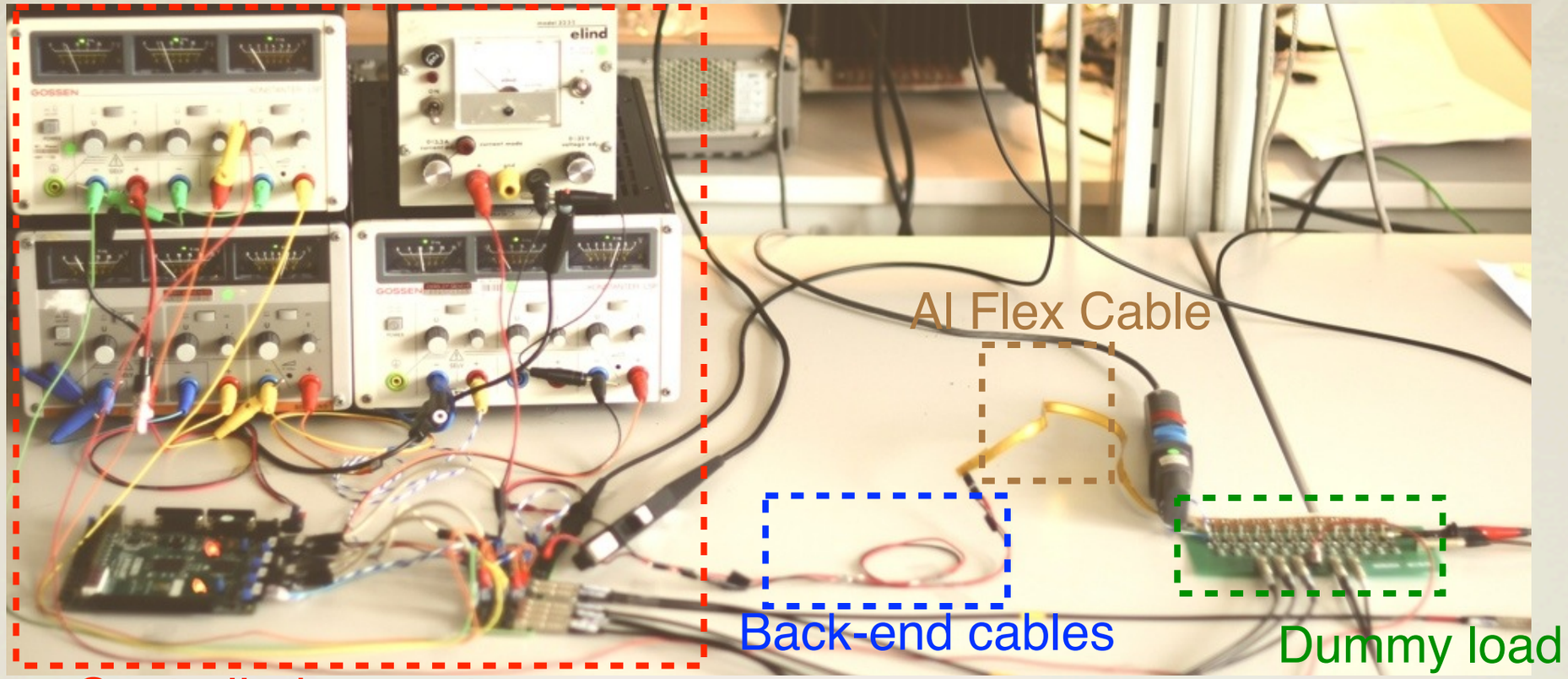
We can replicate the fact of each ASIC being read out one at the time.

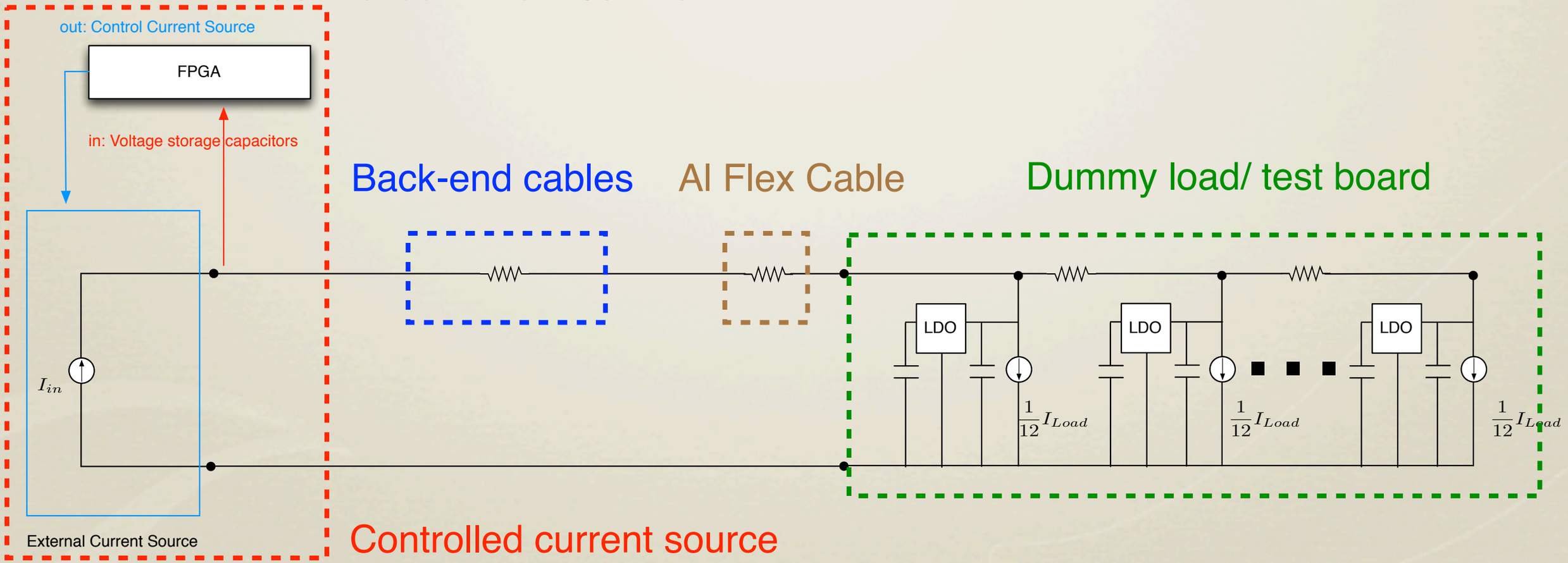


PCB implementation

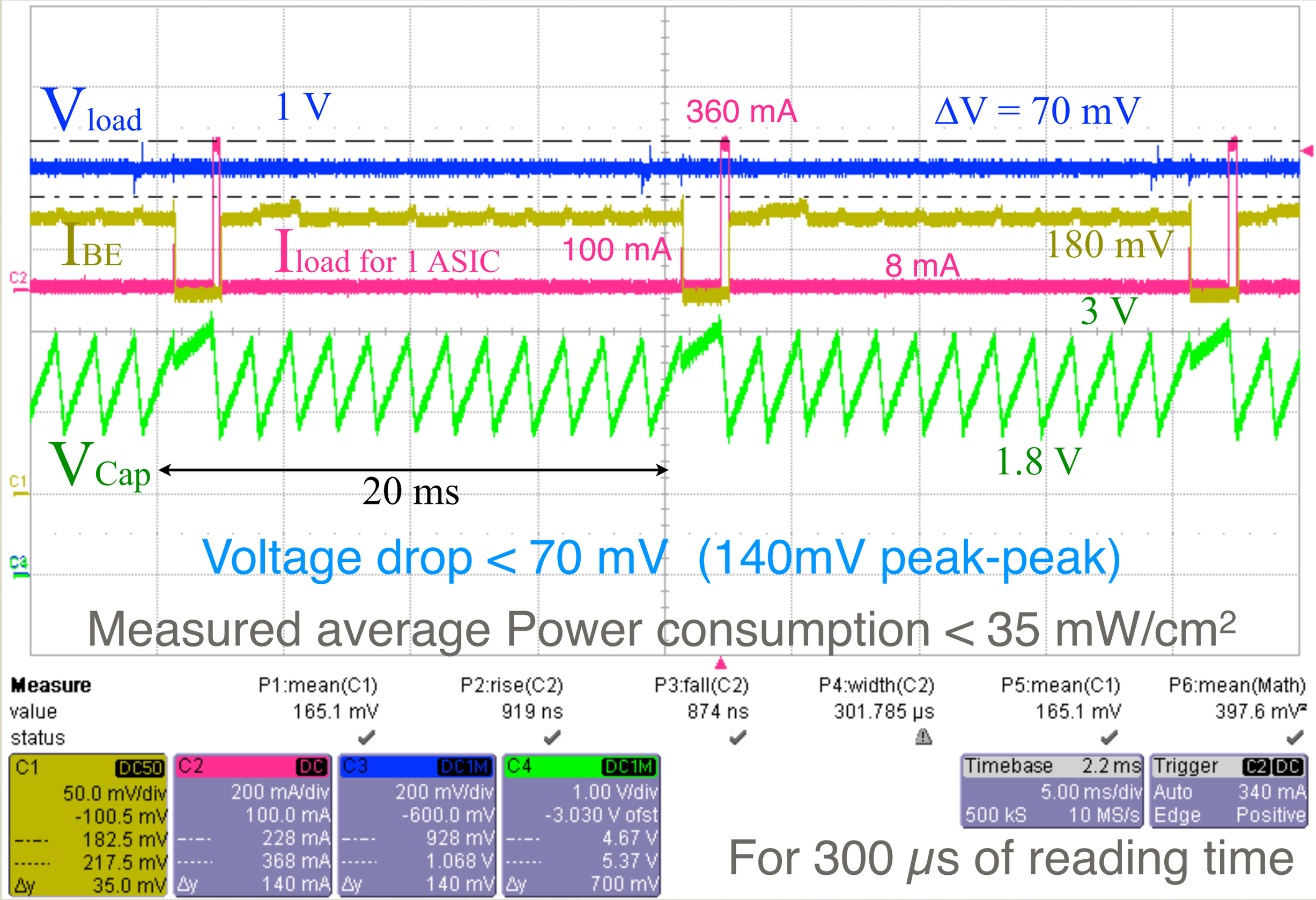


Implementation @ Lab



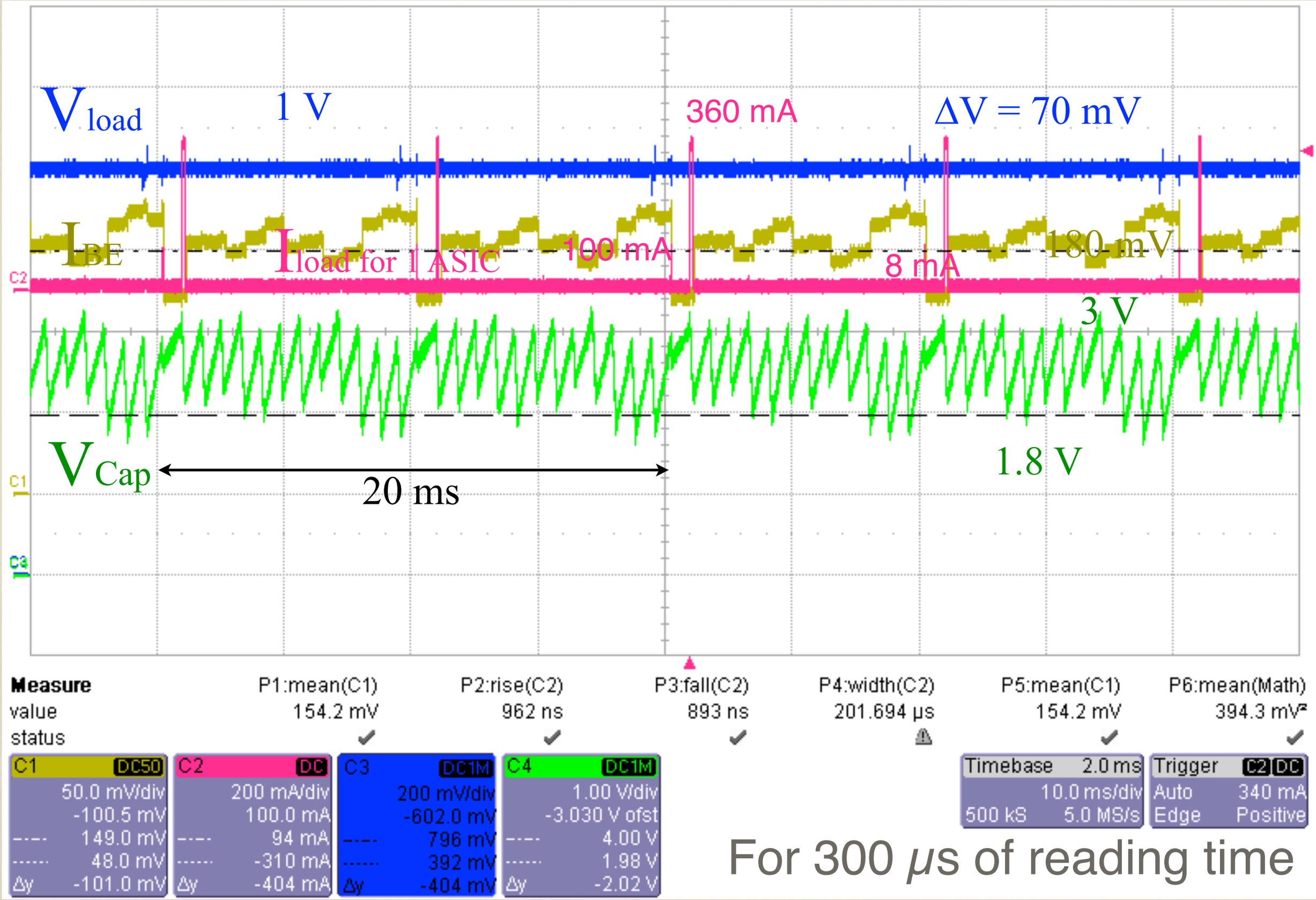


Digital results



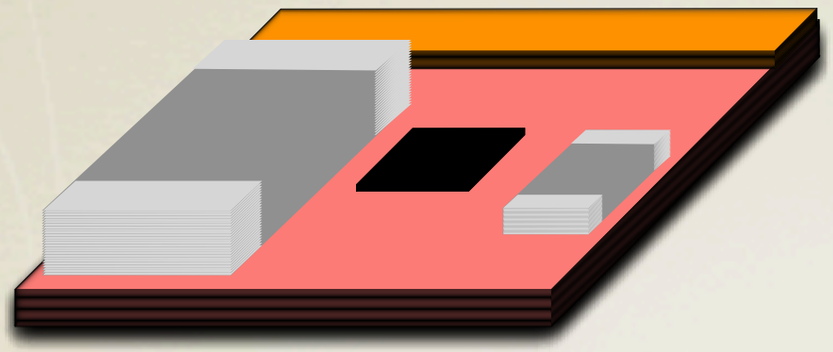
For 300 μs of reading time

Digital results



For 300 μs of reading time

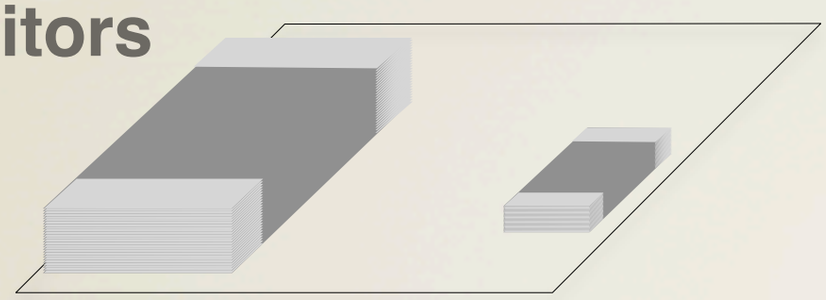
Material Budget:



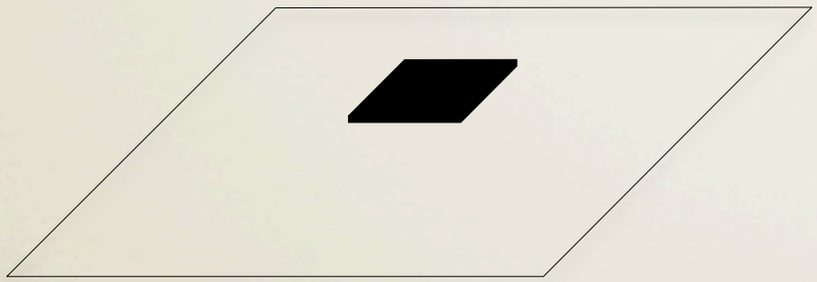
Material Budget:

Flex Cable

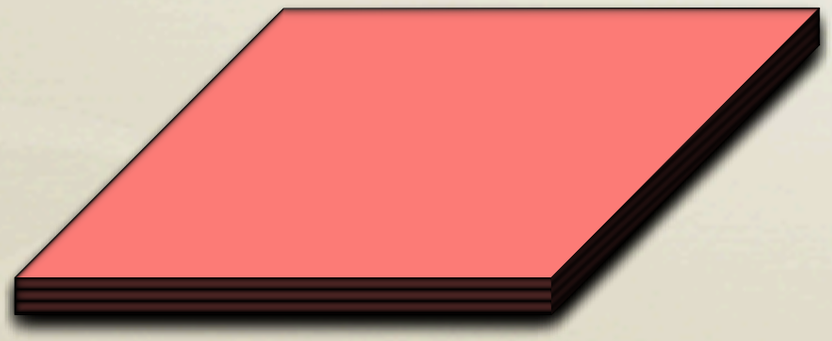
Capacitors



LDO

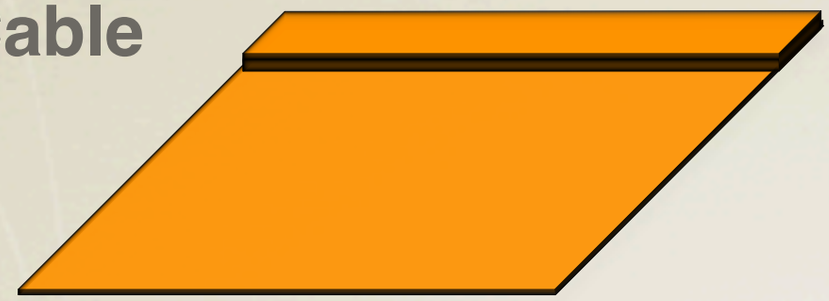


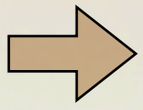
ASIC



Material Budget:

Flex Cable





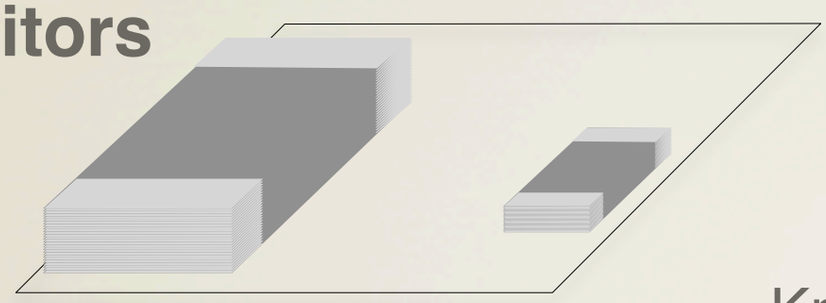
Cross-section

$h_{eq(FLEX)}$

$V_i = \text{Volume of material } i$
$A = \text{Area of the ASIC}$

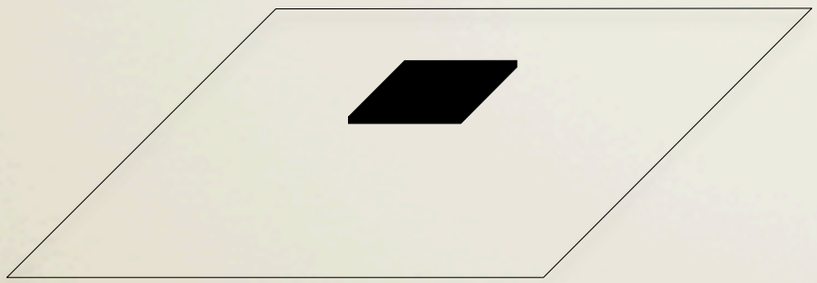
$$h_{eq(i)} = \frac{V_i}{A} \quad (mm)$$

Capacitors



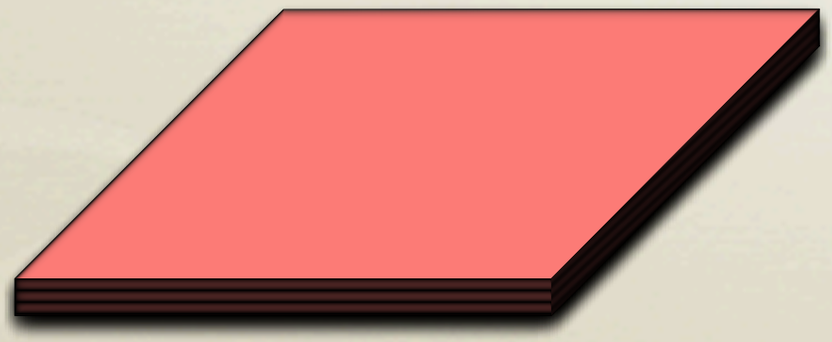
Knowing the radiation length $X_{0(i)}$ of the material in mm, we obtain the fraction of the radiation length $\%X_0$ by:

LDO



$$\%X_0 = \sum_i \frac{h_{eq(i)}}{X_{0(i)}} \cdot 100$$

ASIC



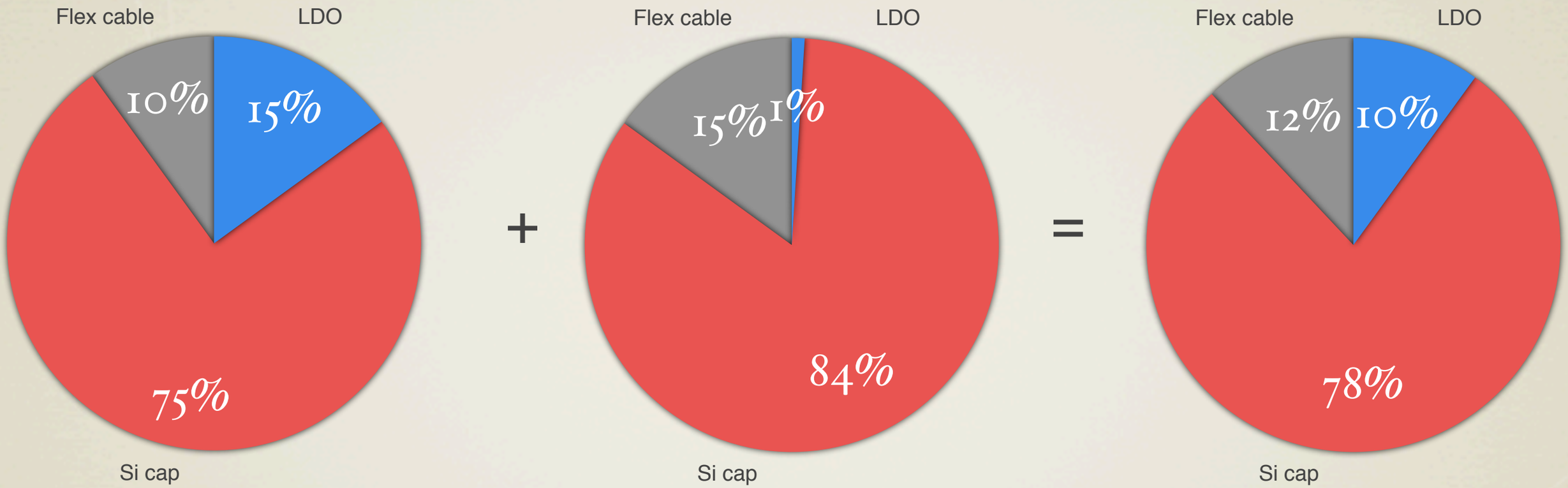
~ 0.1 %X_0

$$\%X_{0,ASIC} = \frac{0.1mm}{93.6mm} \cdot 100 = 0.1068$$

Material Budget Today

Silicon capacitors (today 25 μF/cm²):

Analog + Digital = Total

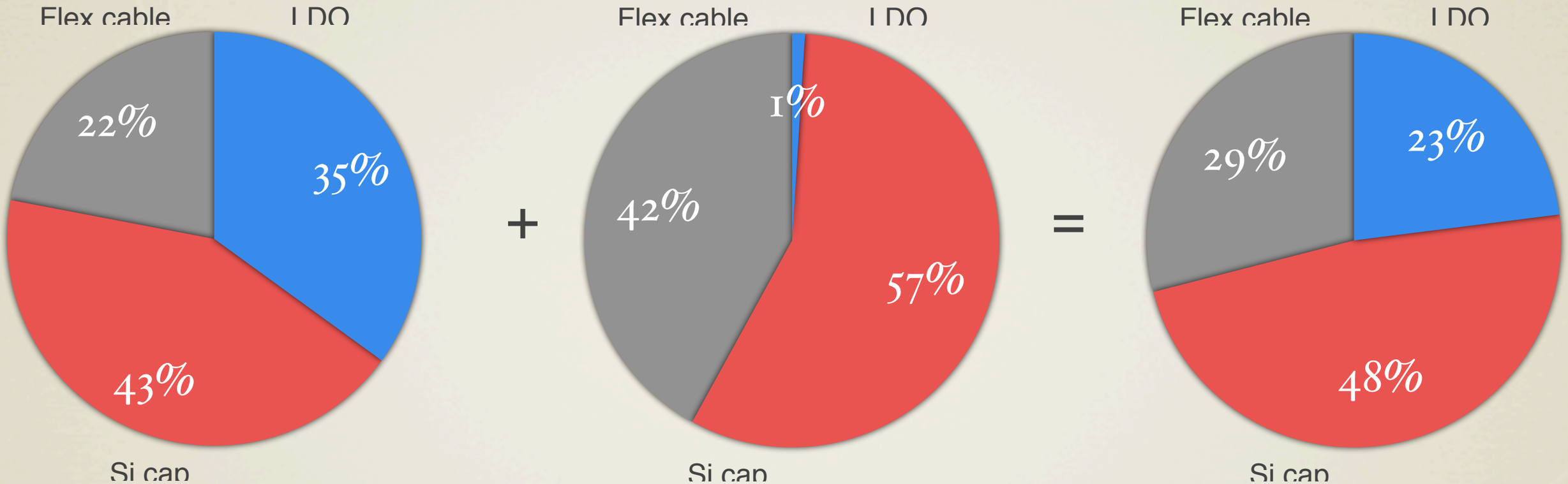


0.064 % X_0 + 0.04 % X_0 = 0.104 % X_0

Material Budget ~~Today~~ Tomorrow*

Silicon capacitors (~~today 25~~ 100 µF/cm²):

Analog + Digital = Total



0.028 % X_0 + 0.015 % X_0 = 0.043 % X_0

Flex cable & LDO contribution now is half of the total.

- ➡ LDOs will be tried to be included in CLICPix
- ➡ Flex cable material can easily be decreased. (We will produce a new al Flex)

* for IPDiA roadmap and reference, see back-up slides

Conclusions

During this talk we presented a power-pulsing scheme to power the analog and digital electronics of the future vertex barrel read-out ASIC CLICpix.

The presented scheme counted with regulation and silicon capacitors in the front-end, which were charged up using a back-end current supply of less than 50 mA for the analog part and less than 200mA for the digital one.

Some of the achieved results were:

- Good regulation as required:
  Analog voltage drop < 20 mV and Digital voltage drop < 70 mV

- Total Power losses/dissipation < 50mW/cm^2 as required.
  Analog < 10mW/cm^2 and Digital < 35mW/cm^2

- Small current (20mA to 60mA for Analog and 100mA to 200mA for Digital) through the whole cable depending on the load consumption. => Low material cables.

- Today's Material Budget of 0.104 % X0, which is expected to be less than 0.043 % X0. (after improvements of silicon capacitors technology).

We expect to decrease this contribution furthermore by redesigning the aluminum flex cable and by integrating the LDOs in the CLICPix ASIC.

Thanks for your attention :)