



PH-DT

Detector Technologies

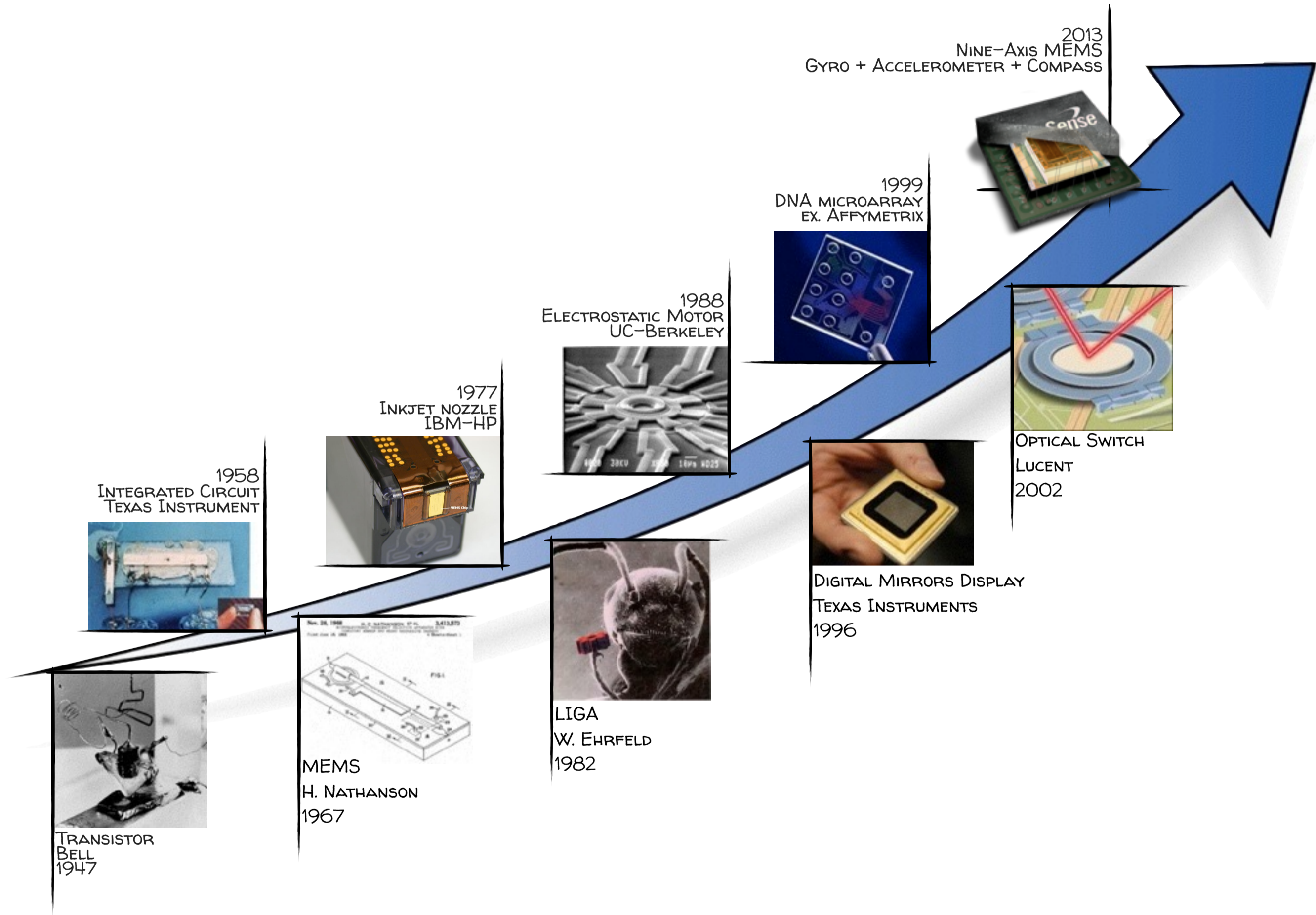
# Microfabrication in PH-DT

Alessandro Mapelli  
PH-DT-EO

FROM MICROFLUIDIC SCINTILLATION DETECTORS  
TO ON-DETECTOR COOLING SYSTEMS

PH-ESE seminar  
CERN, 5 November 2013

# Microfabrication Milestones



# Microfabrication Techniques

## BULK MICROMACHINING

MECHANICAL STRUCTURES ARE ETCHED IN THE SUBSTRATE



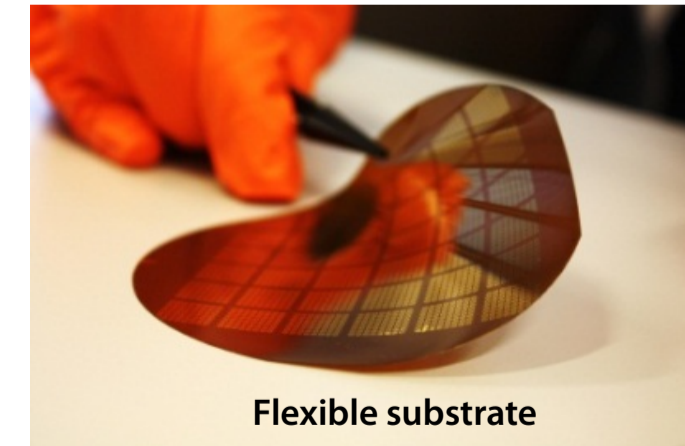
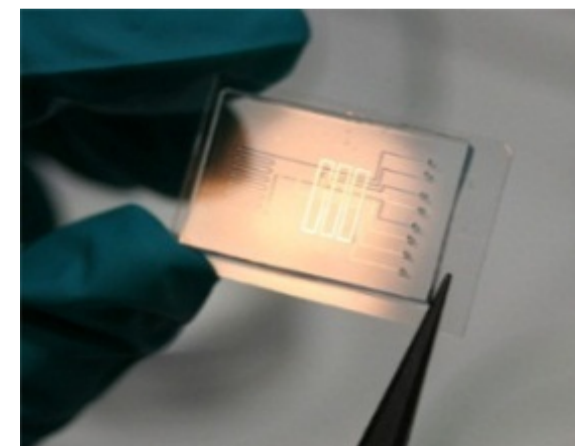
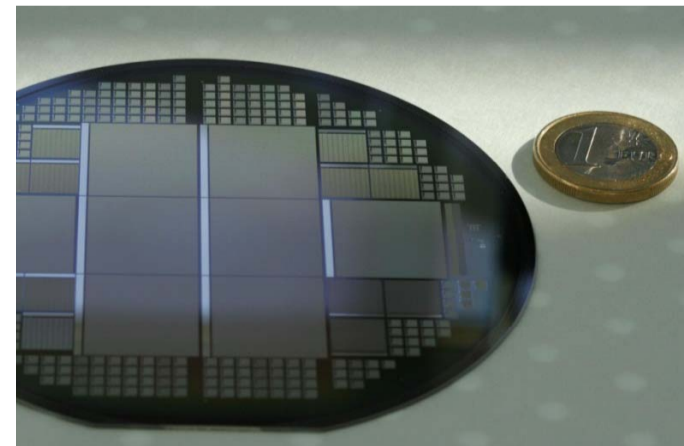
## SURFACE MICROMACHINING

LAYERS OF MATERIAL ARE DEPOSITED ON THE SUBSTRATE, PATTERNED AND SELECTIVELY REMOVED



## SUBSTRATES

ROUND WAFERS 3", 4", 6", 8", 12"..."  
SILICON, SOI, GLASS, GAAAs, SiC, Ge, POLYMERS...



2006

2007

2008

2009

2010

2011

2012

2013

MICROSCINT

MICROFLUIDIC SCINTILLATION DETECTORS

MICROHEII

HEAT TRANSFER OF SUPERFLUID HELIUM

MICROCOOL

MICROFABRICATED ON-DETECTOR COOLING SYSTEMS





microtechnologies



particle detectors



<http://directory.web.cern.ch/directory/>

## PH PHYSICS

IT Information Technology  
BE Beams  
TE Technology  
EN Engineering  
HR Human resources  
FP Finance and Procurement  
GS General Infrastructure Services

GIULIA ROMAGNOLI  
PIETRO MAODDI  
ANDREA FRANCESCON  
LUDOVIC SEREX

<http://ph-dep.web.cern.ch/ph-dep/>

ESE : Electronics System for Experiments group  
AGS : Administration and General Services  
LCD : Linear Collider Detector  
ALICE : A Large Ion Collider Experiment  
LHCb : The Large Hadron Collider Beauty experiment  
ATLAS : A Toroidal LHC Apparatus  
SFT : SoFTware design for experiments group  
CMS : the Compact Muon Solenoid experiment  
SME : Small and Medium Experiments team

## DT : DETECTOR TECHNOLOGIES

TH : Theoretical physics unit  
EDU : EDUcational group  
TOTEM : TOTal cross section, Elastic scattering and diffraction dissociation Measurement at the LHC

<http://ph-dep-dt.web.cern.ch/ph-dep-dt/>

DI: Detecior Infrastructure  
DD: Detector Development  
TP: Technology & Physics

## EO: ENGINEERING OFFICE

EM1: Engineering & Mechanics 1  
EM2: Engineering & Mechanics 2



# @EPFL

[HTTP://CMI.EPFL.CH/](http://CMI.EPFL.CH/)

© Valentin Flauraud

CLASS 100 MEMS CLEANROOM  
4" WAFERS  
(6" WAFERS)

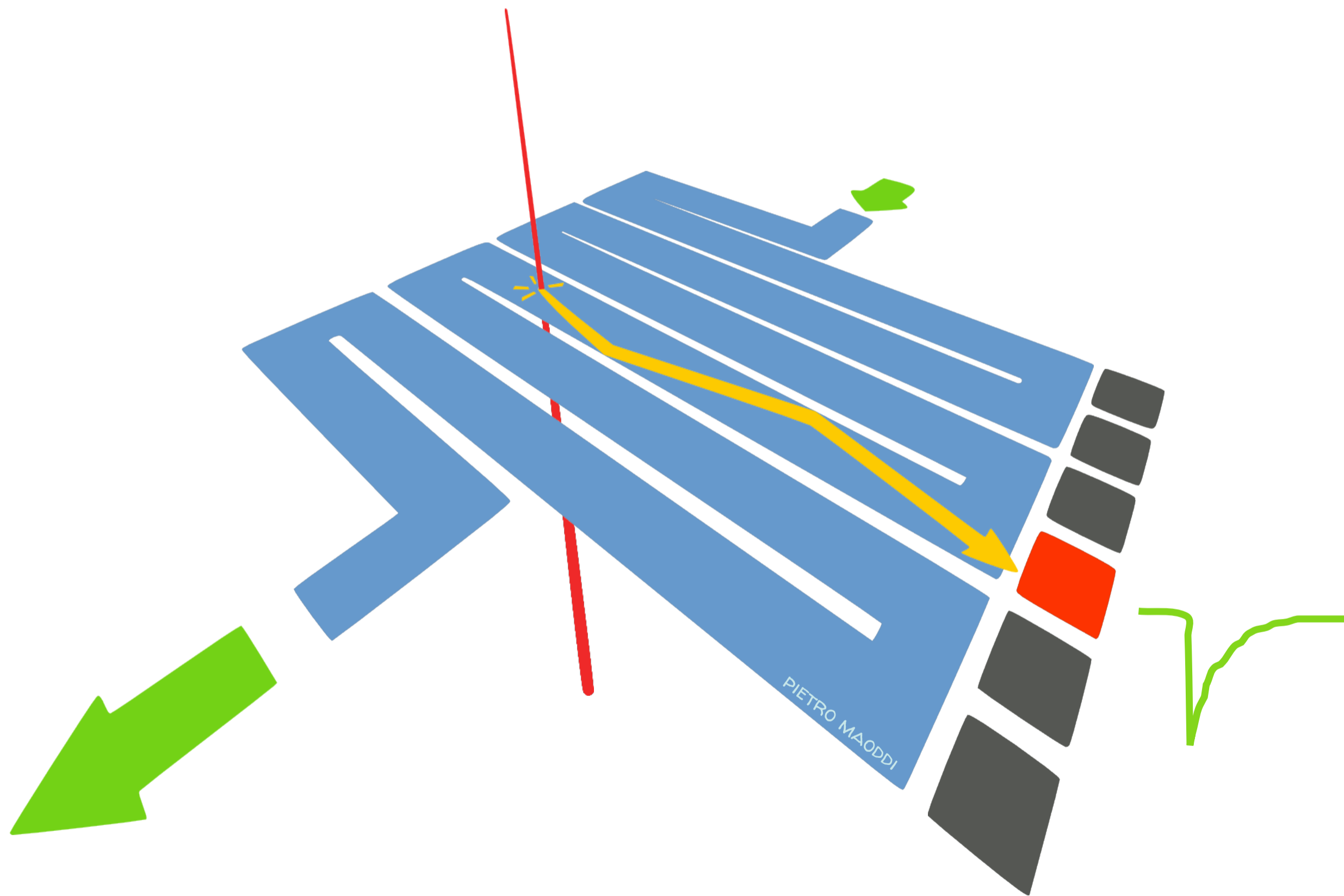
OPERATION ON 50 MACHINES  
PHOTOLITHOGRAPHY  
ETCHING  
THIN FILMS  
BONDING  
THINNING  
METROLOGY

OUTPUT  
130 PHOTOLITHOGRAPHY MASKS  
1200 WAFERS PROCESSED



# microScint

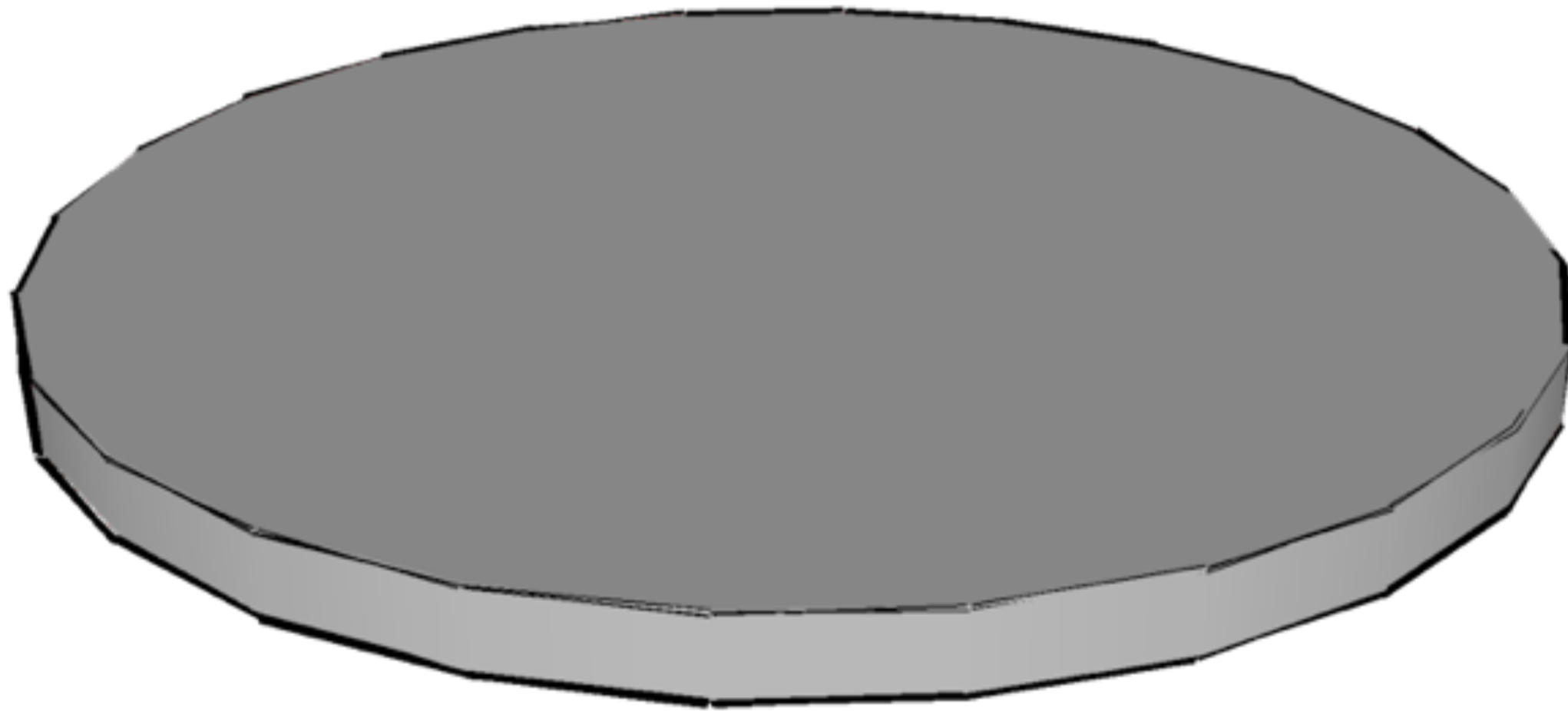
Development of a **microfluidic scintillation detector** where a single microfluidic channel defines an array of independent optical waveguides to be potentially used as single particle tracker or beam monitor.





# first prototype

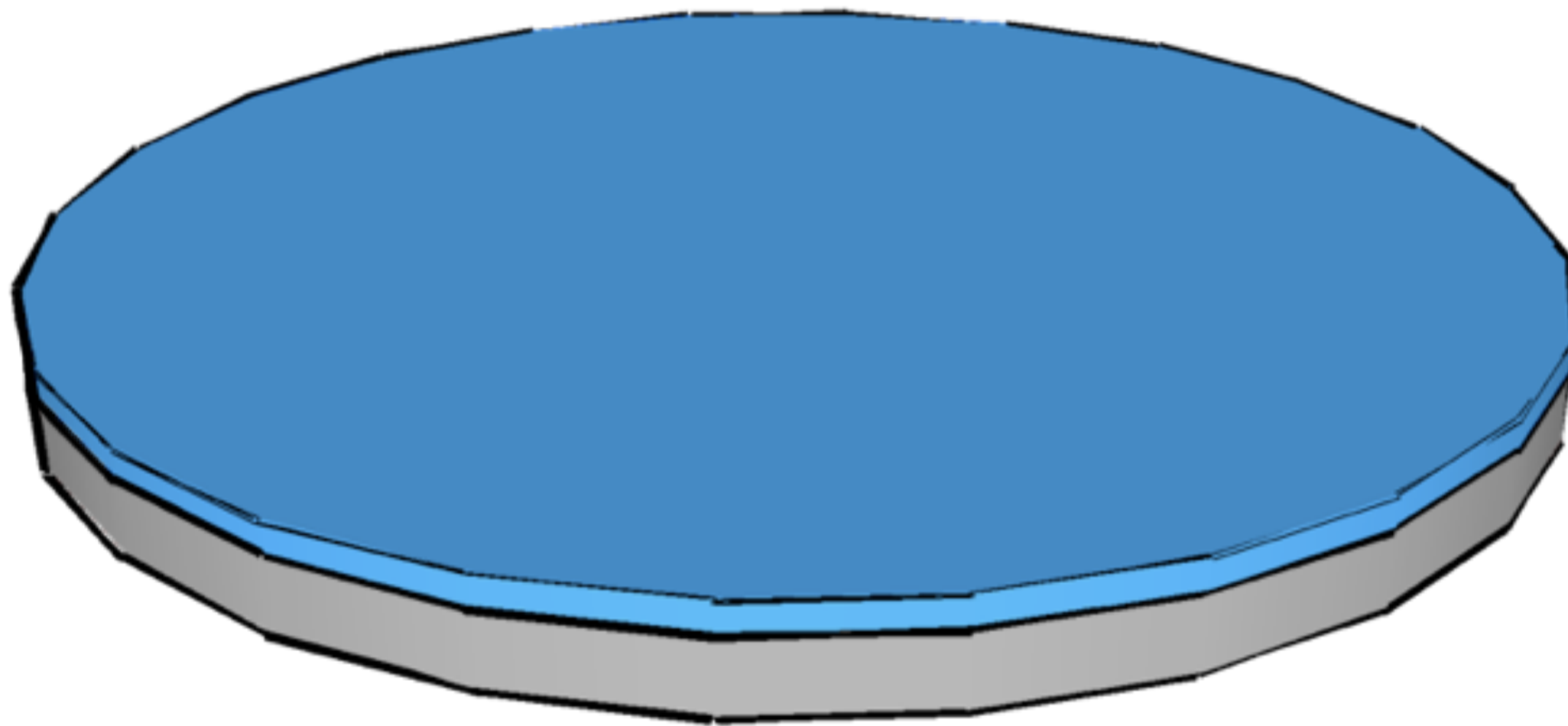
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS  
(SURFACE MICROMACHINING)



**SILICON SUBSTRATE**

# first prototype

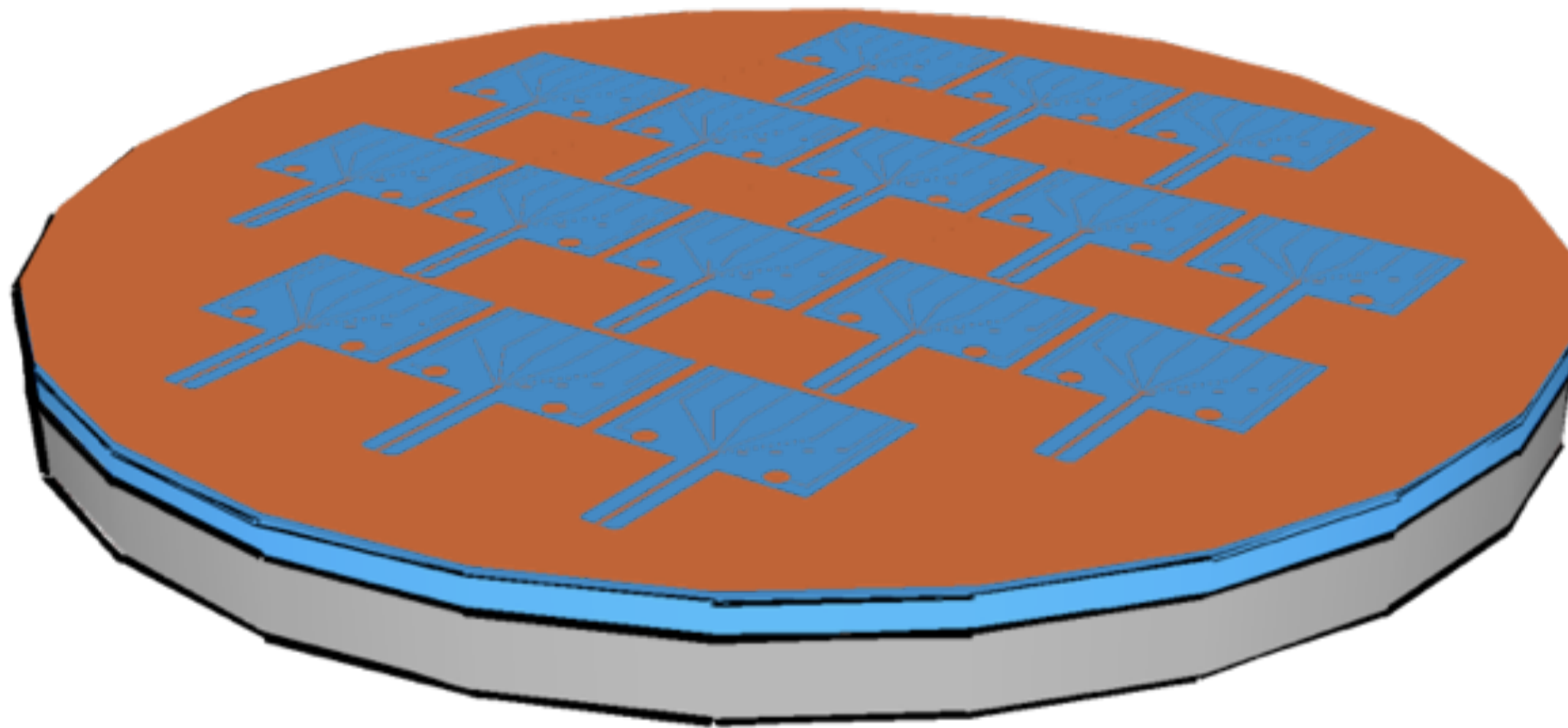
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS  
(SURFACE MICROMACHINING)



## PHOTORESIST SPIN COATING

# first prototype

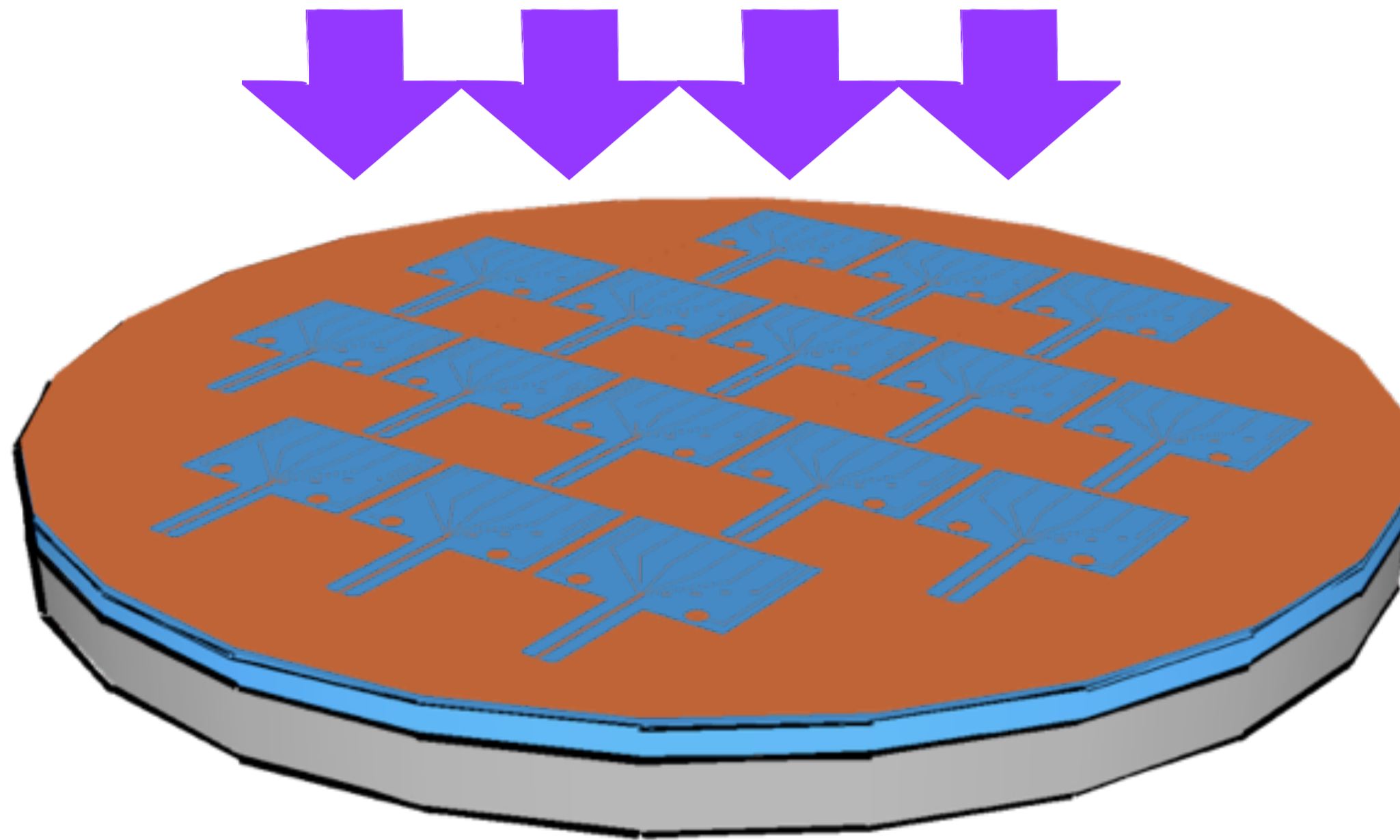
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS  
(SURFACE MICROMACHINING)



## MASK ALIGNMENT

# first prototype

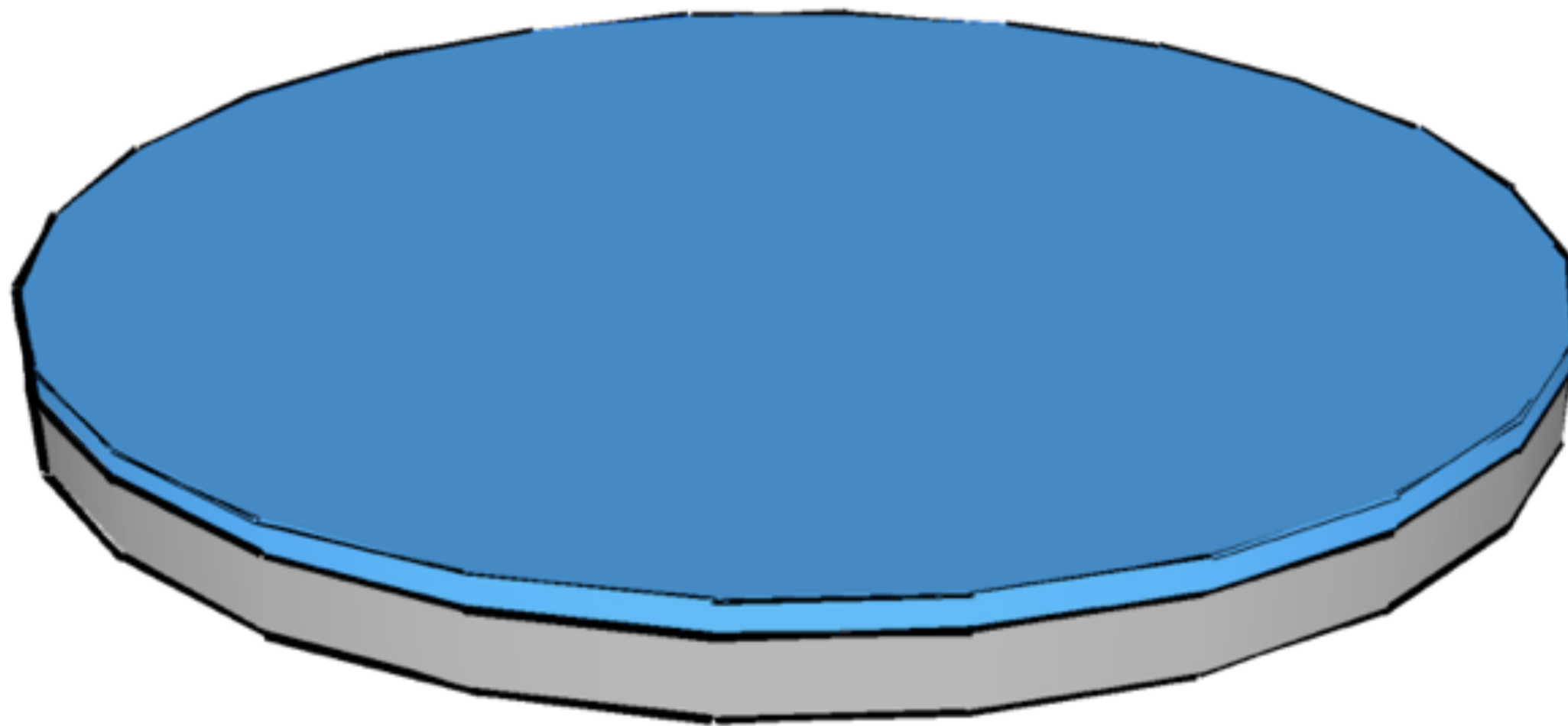
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS  
(SURFACE MICROMACHINING)



UV EXPOSURE

# first prototype

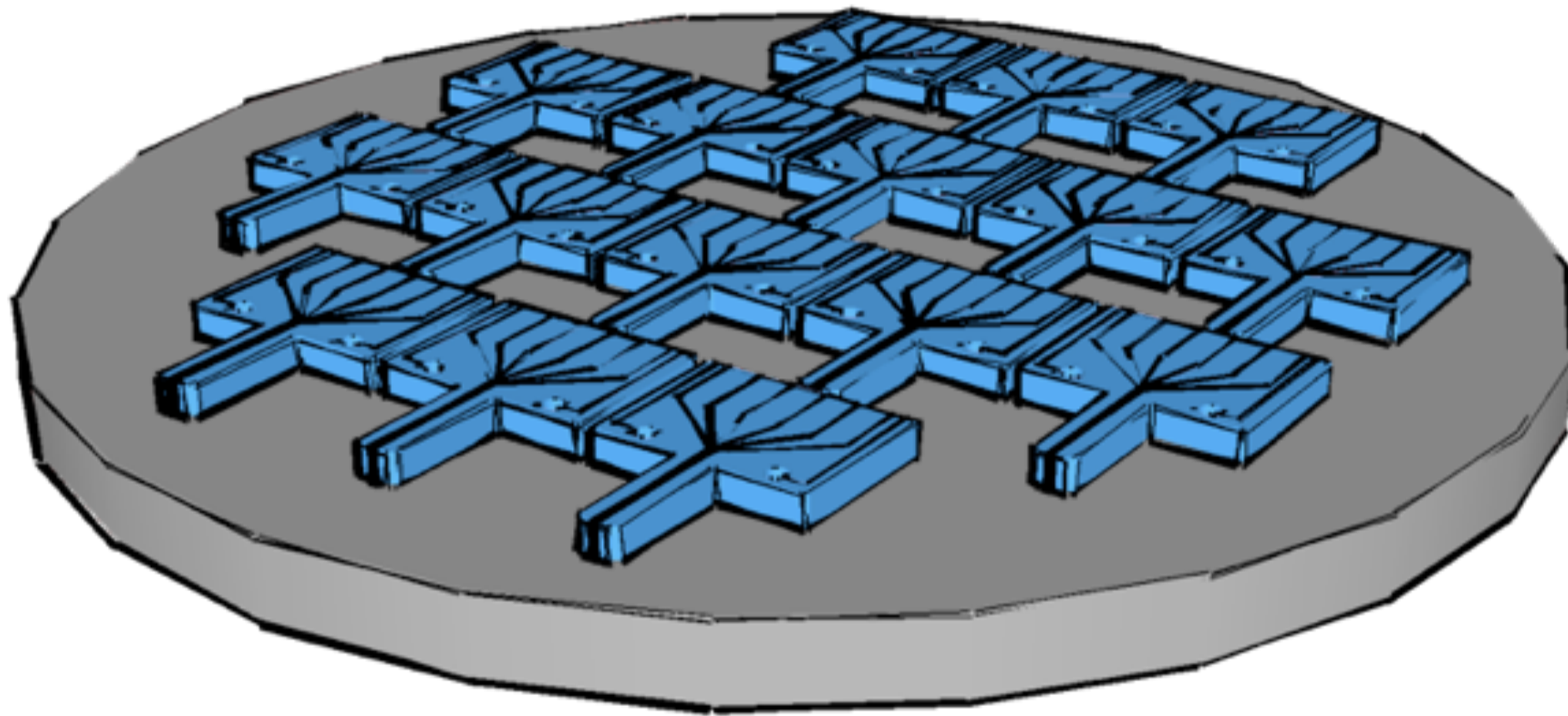
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS  
(SURFACE MICROMACHINING)



UV EXPOSURE

# first prototype

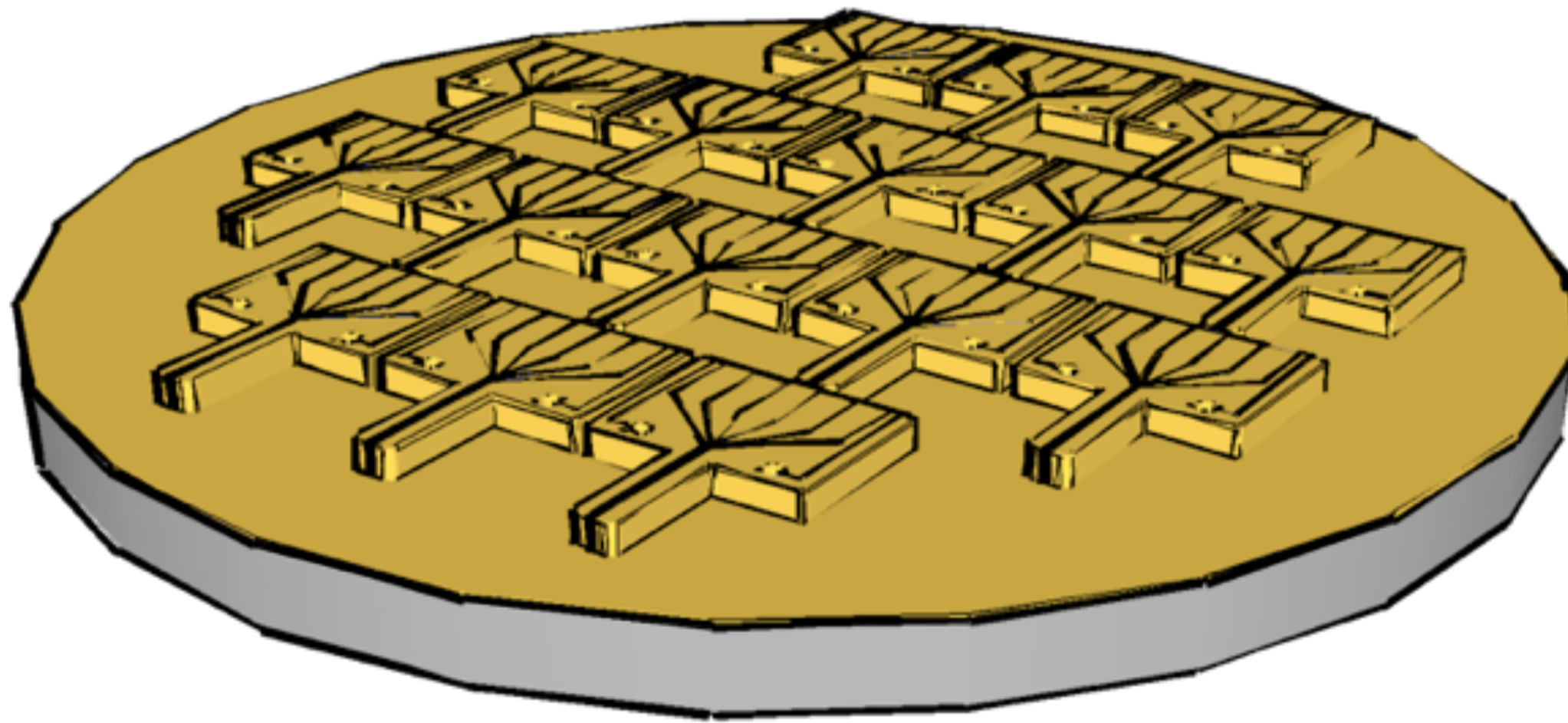
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS  
(SURFACE MICROMACHINING)



## DEVELOPMENT

# first prototype

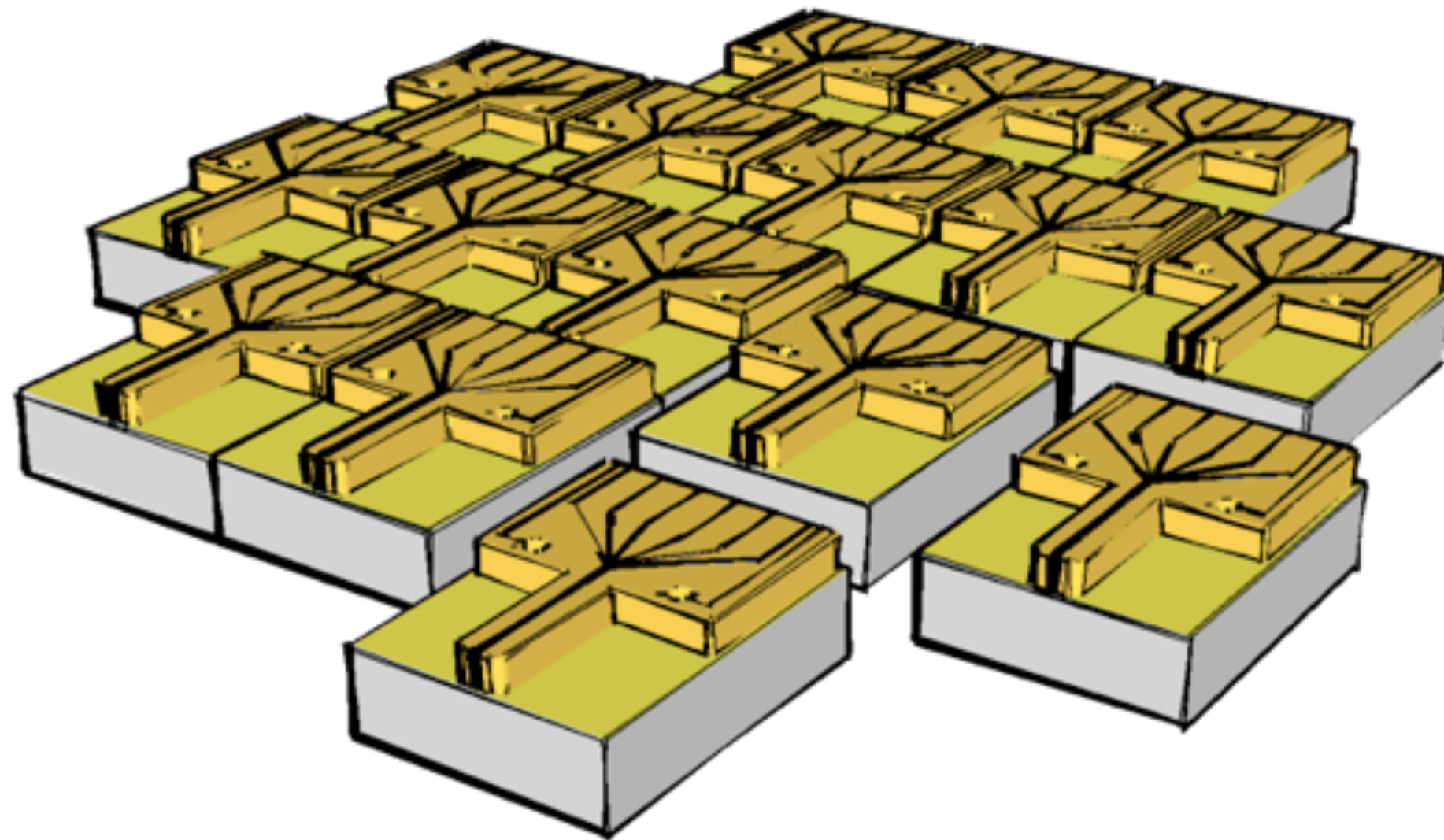
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS  
(SURFACE MICROMACHINING)



## METALLIZATION

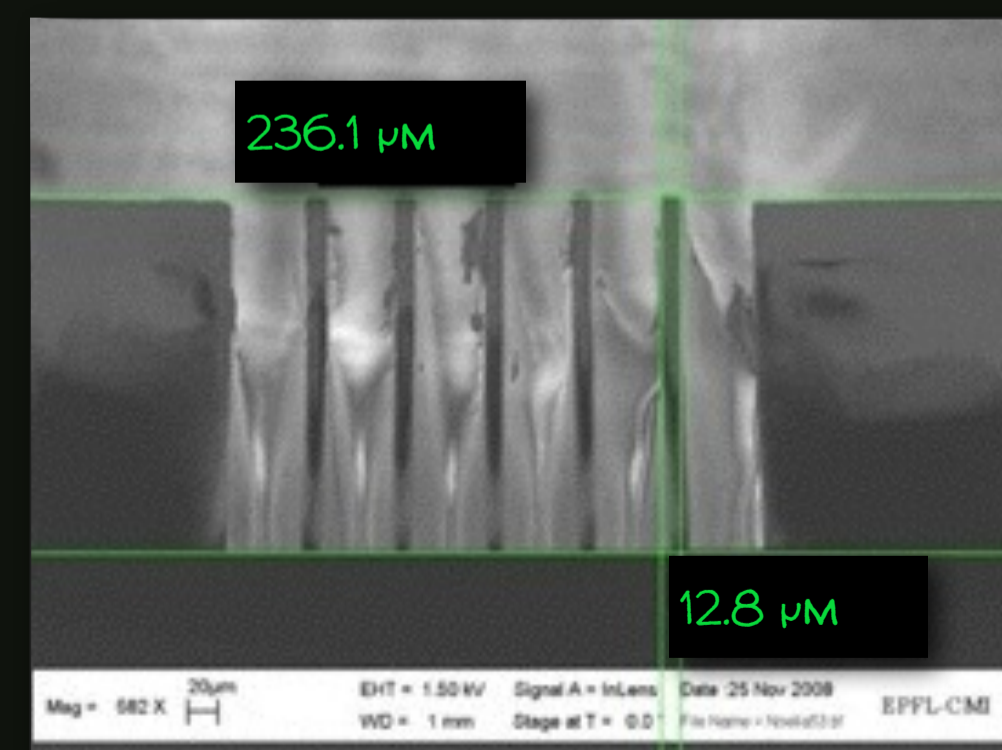
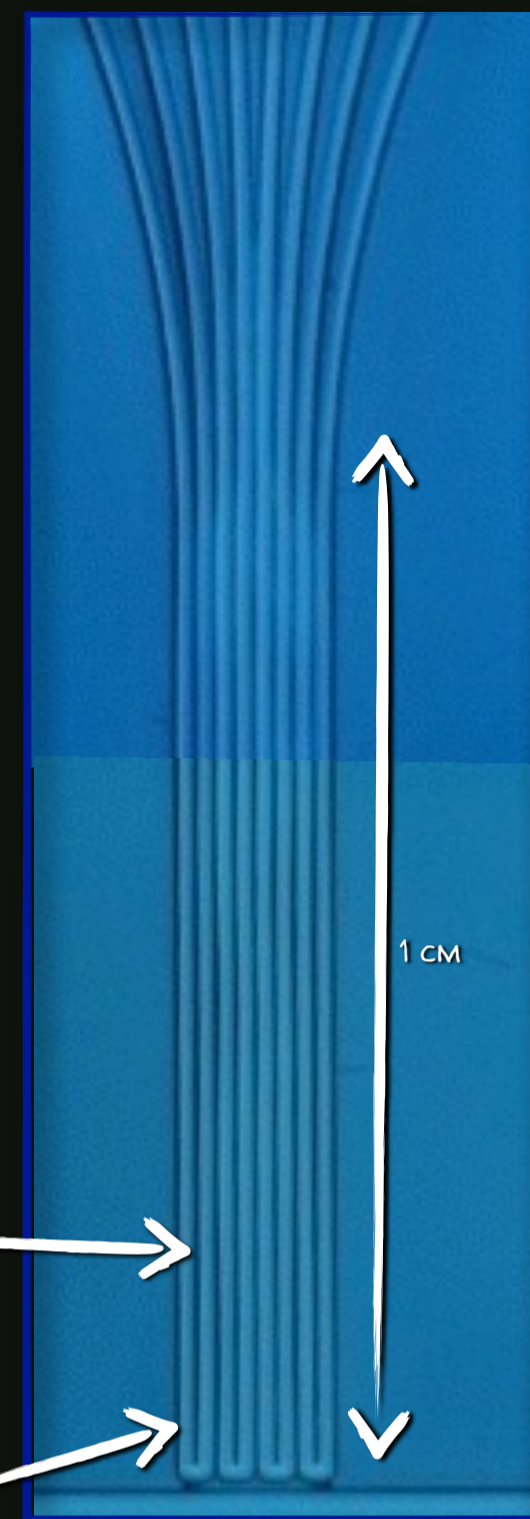
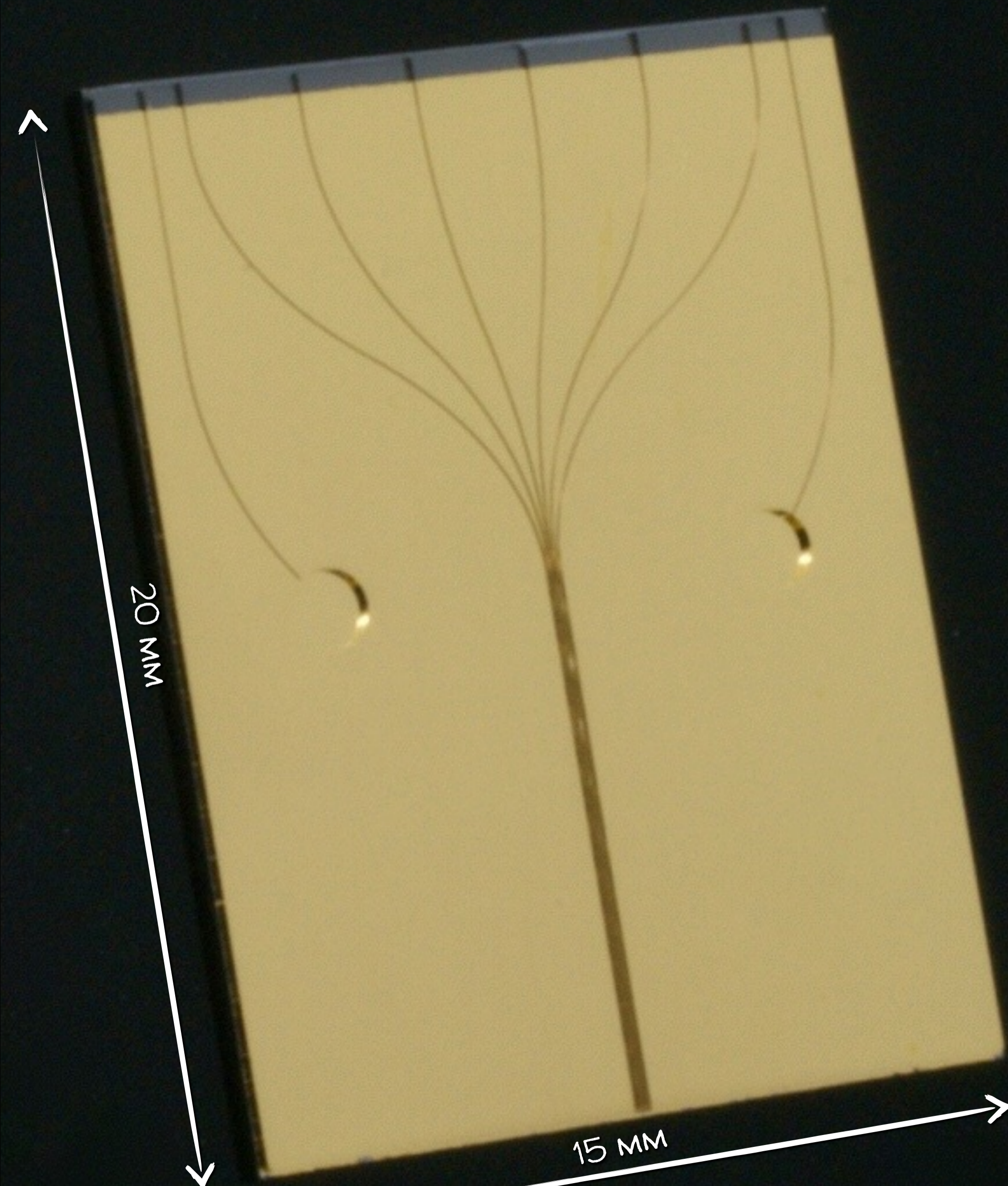
# first prototype

SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS  
(SURFACE MICROMACHINING)



**DICING**

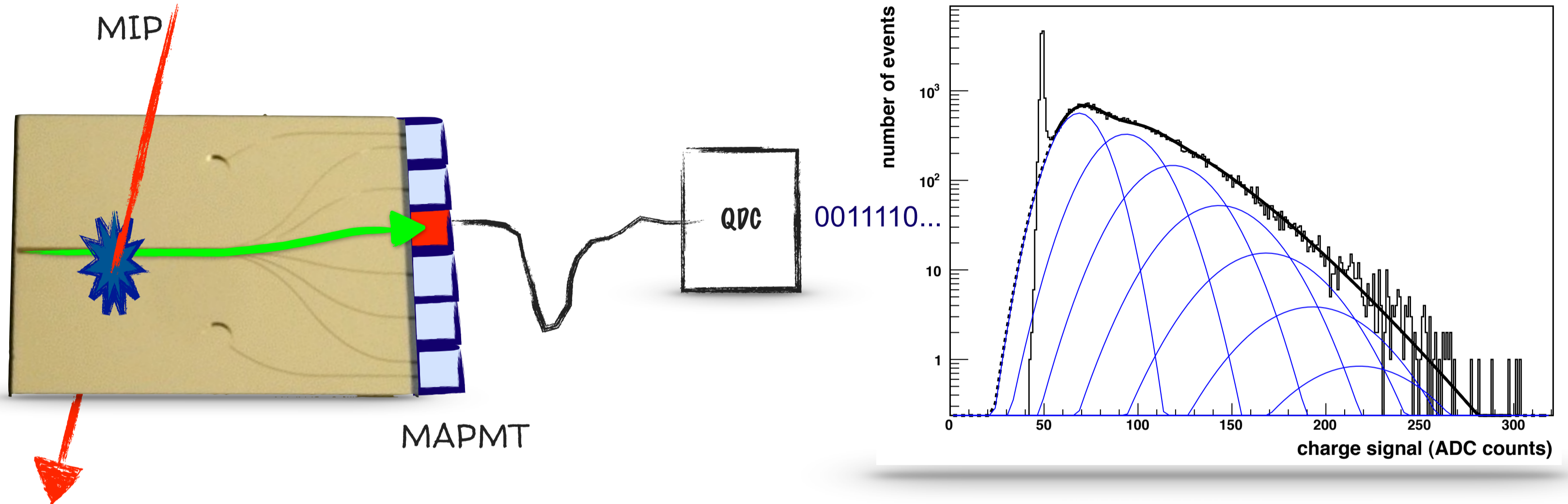




# proof of principle

## WITH 200 $\mu\text{M}$ DEEP AU-COATED SU-8 MICRO CHANNELS

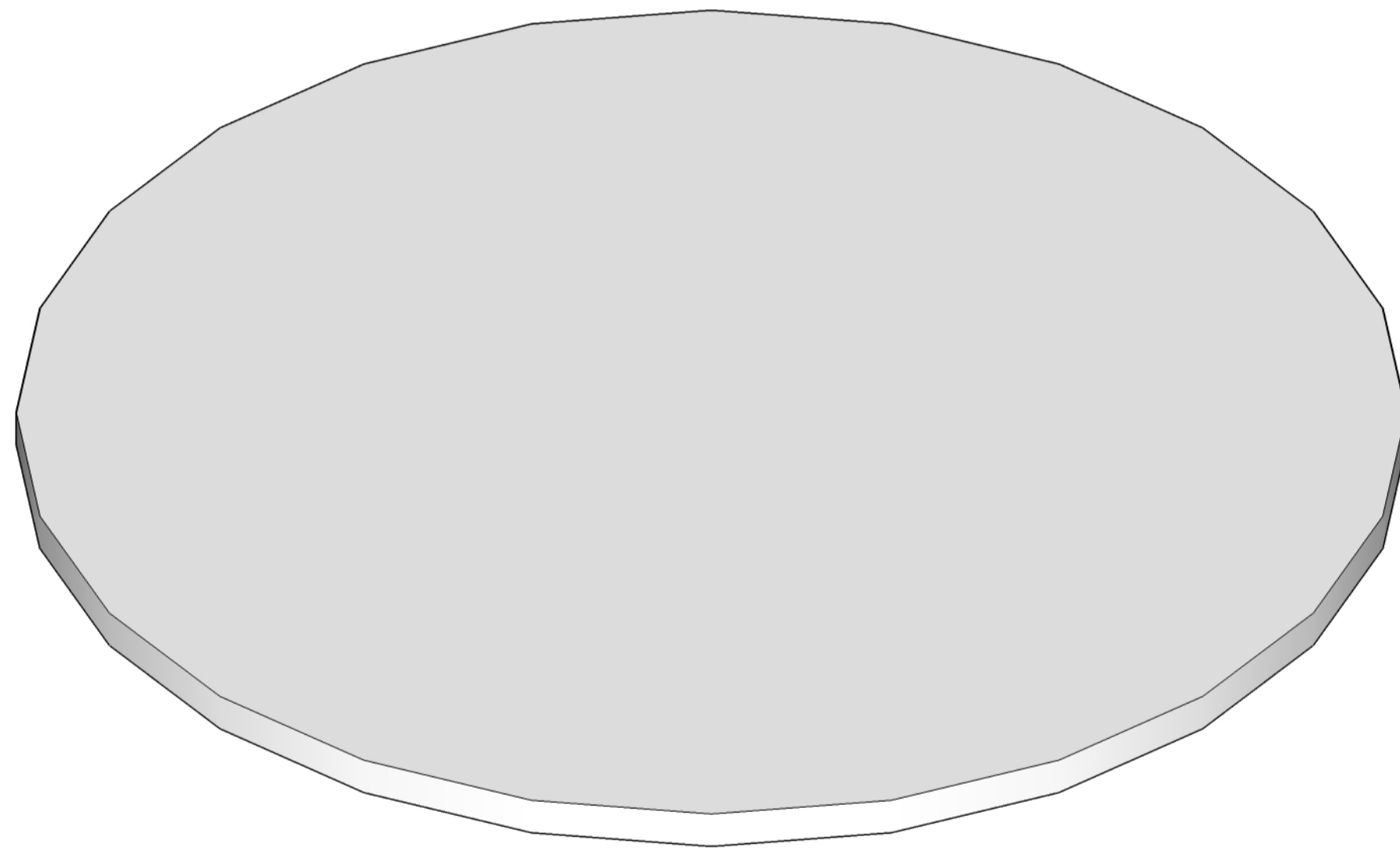
A. MAPELLI ET AL., "SCINTILLATION PARTICLE DETECTION BASED ON MICROFLUIDICS"  
 SENSORS AND ACTUATORS A 162 (2010) 272-275



	PLASTICS	MICROSCINT SU-8 AU-COAT
SCINTILLATOR	0.5 MM	0.2 MM
LIGHT YIELD	4.4 PE 9 PE/MM	1.6 PE 8 PE/MM

# second prototype

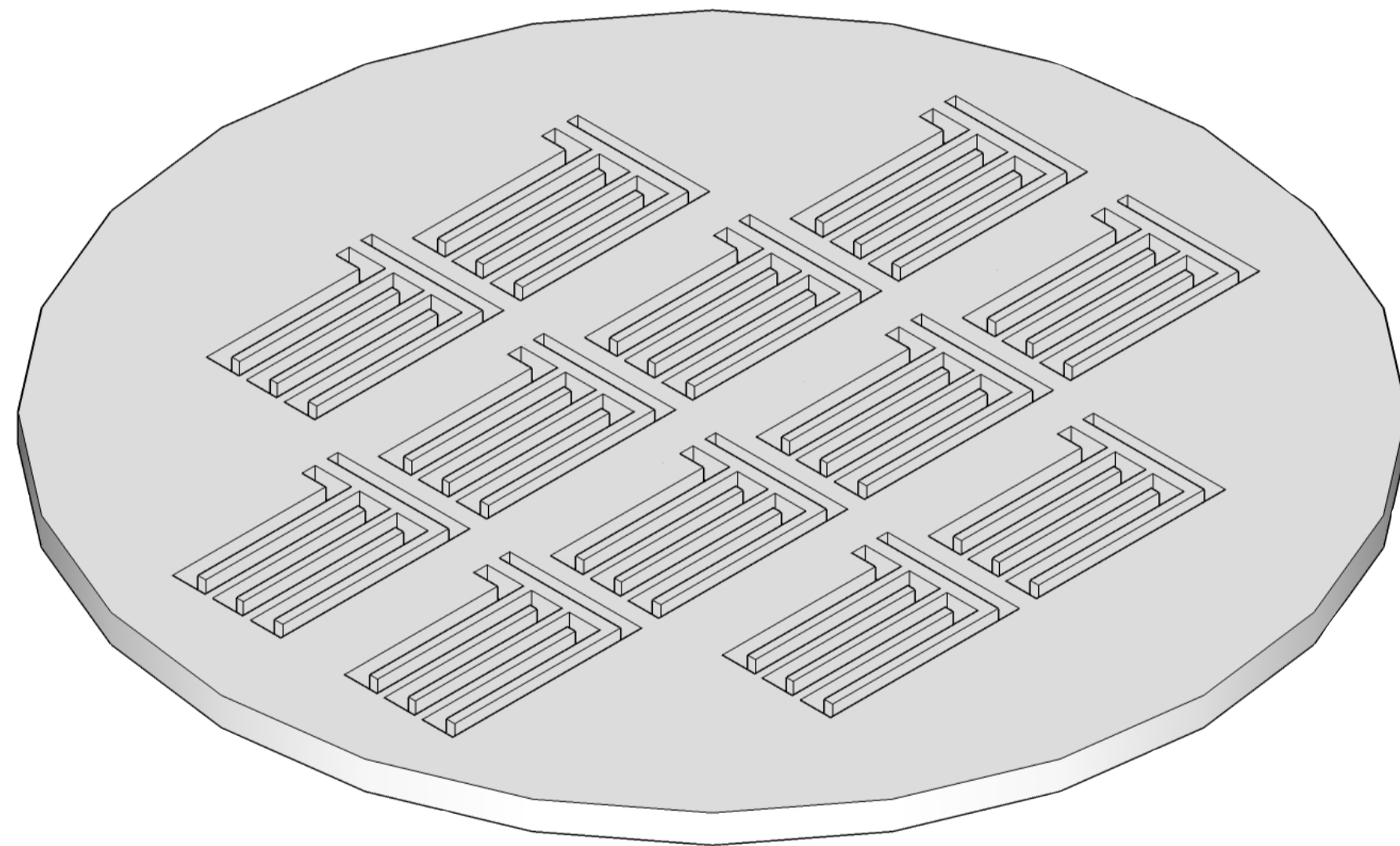
CHANNELS ETCHED IN SILICON SUBSTRATE  
(BULK MICROMACHINING)



**SILICON SUBSTRATE**

# second prototype

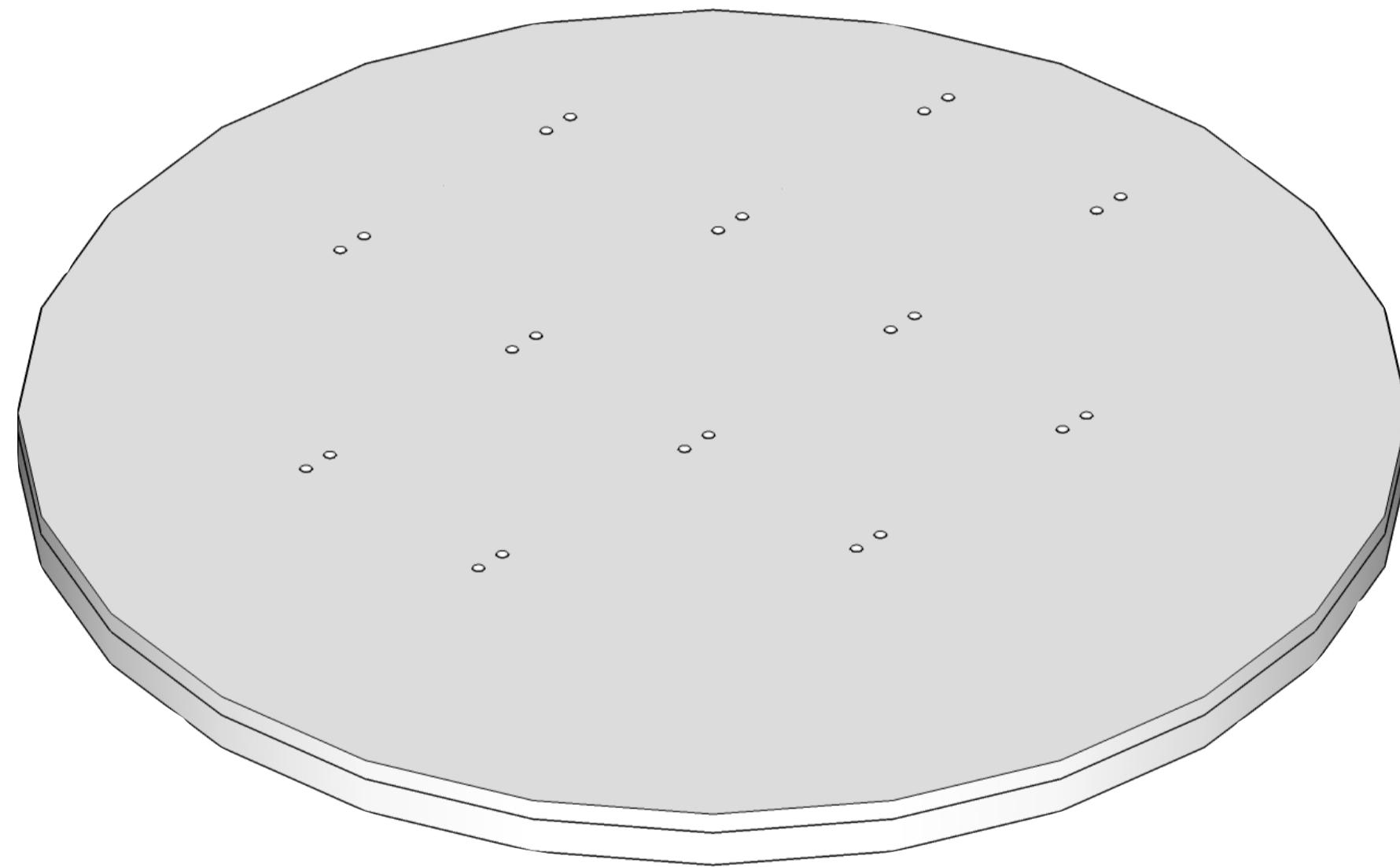
CHANNELS ETCHED IN SILICON SUBSTRATE  
(BULK MICROMACHINING)



## ETCHING

# second prototype

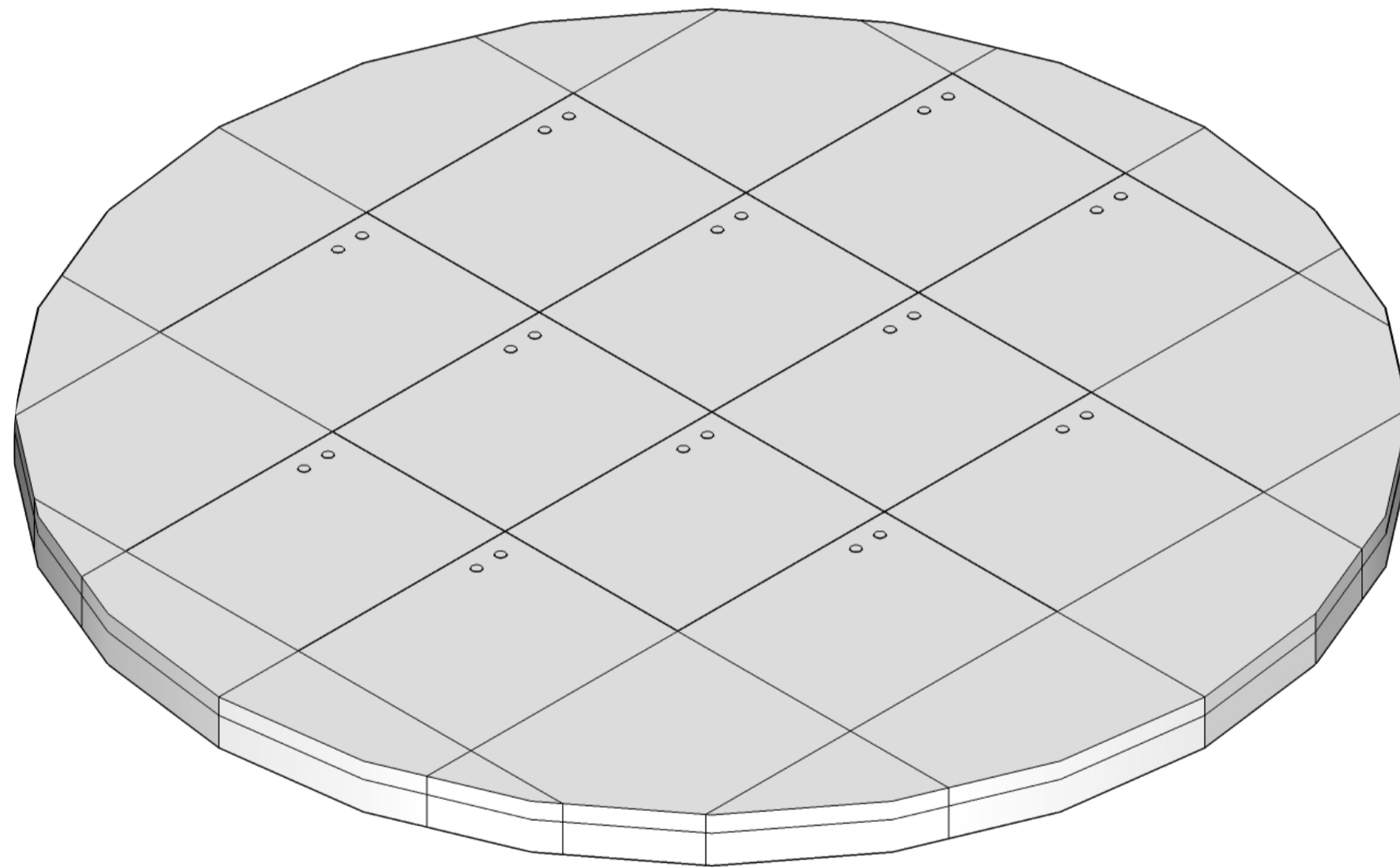
CHANNELS ETCHED IN SILICON SUBSTRATE  
(BULK MICROMACHINING)



BONDING OF SI SUBSTRATE WITH THROUGH-HOLES

# second prototype

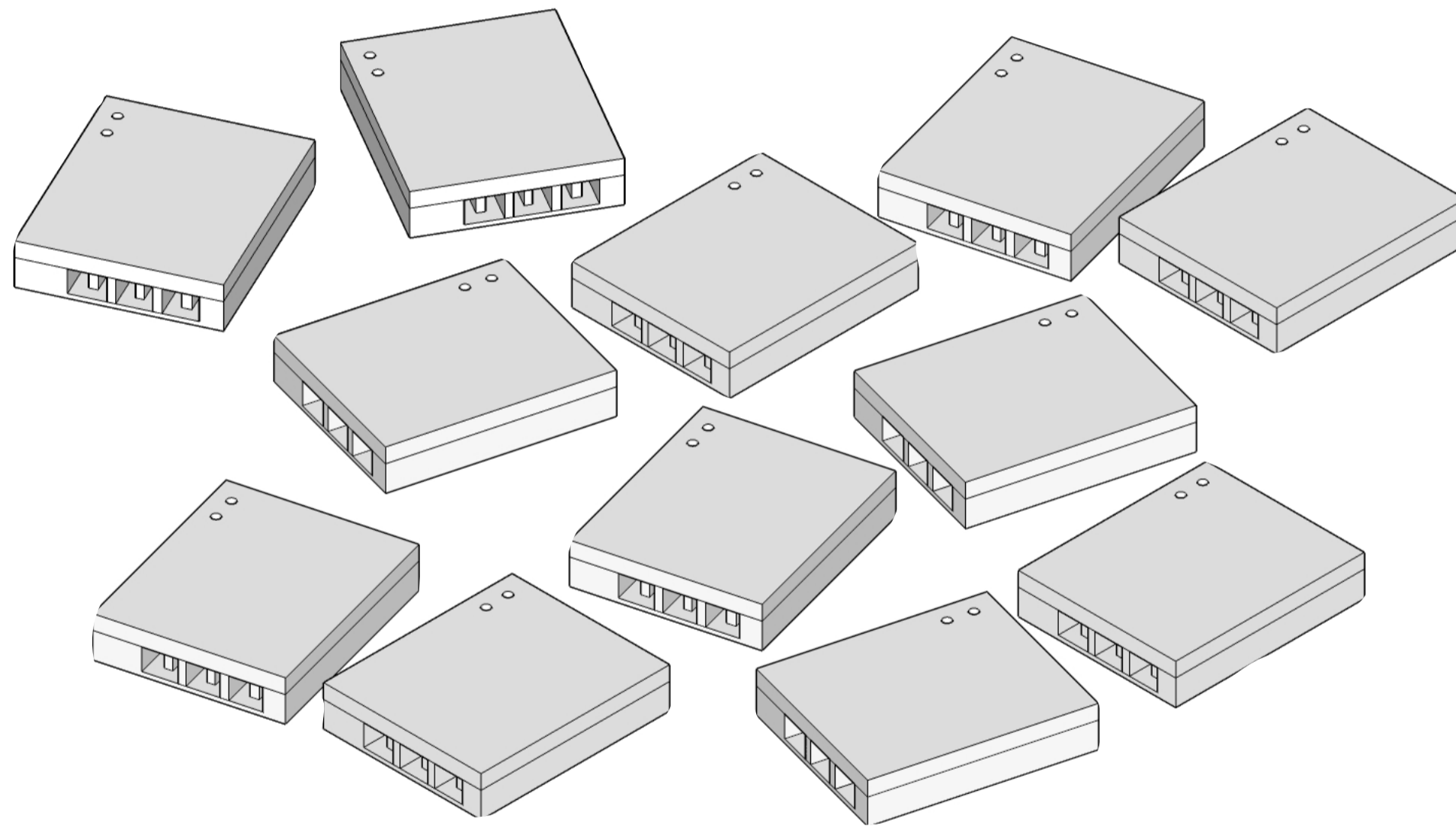
CHANNELS ETCHED IN SILICON SUBSTRATE  
(BULK MICROMACHINING)



**DICING**

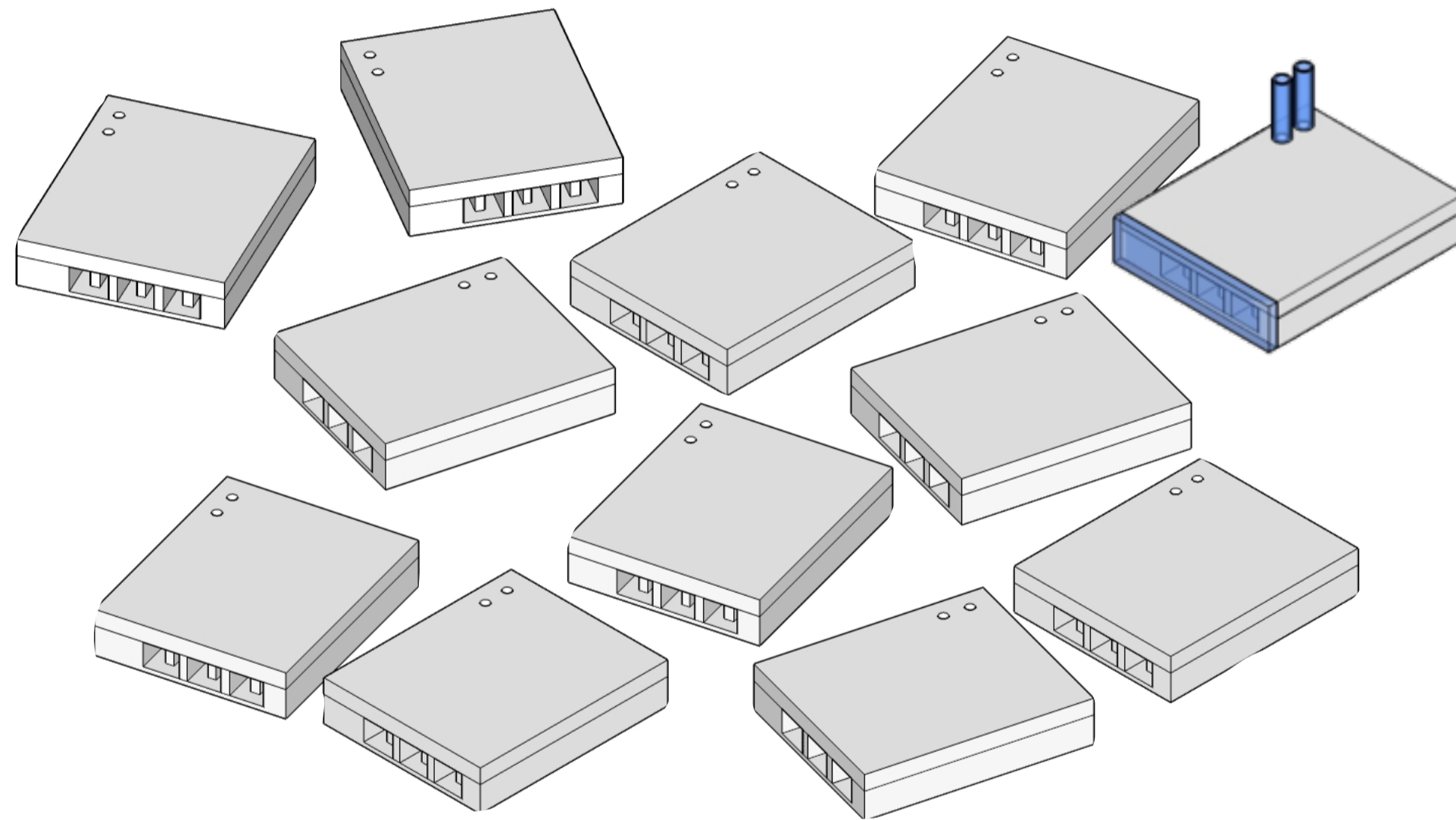
# second prototype

CHANNELS ETCHED IN SILICON SUBSTRATE  
(BULK MICROMACHINING)



# second prototype

CHANNELS ETCHED IN SILICON SUBSTRATE  
(BULK MICROMACHINING)

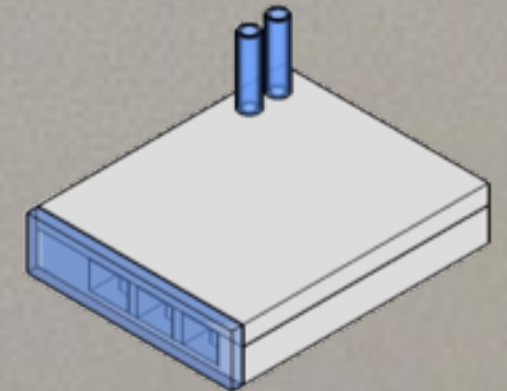
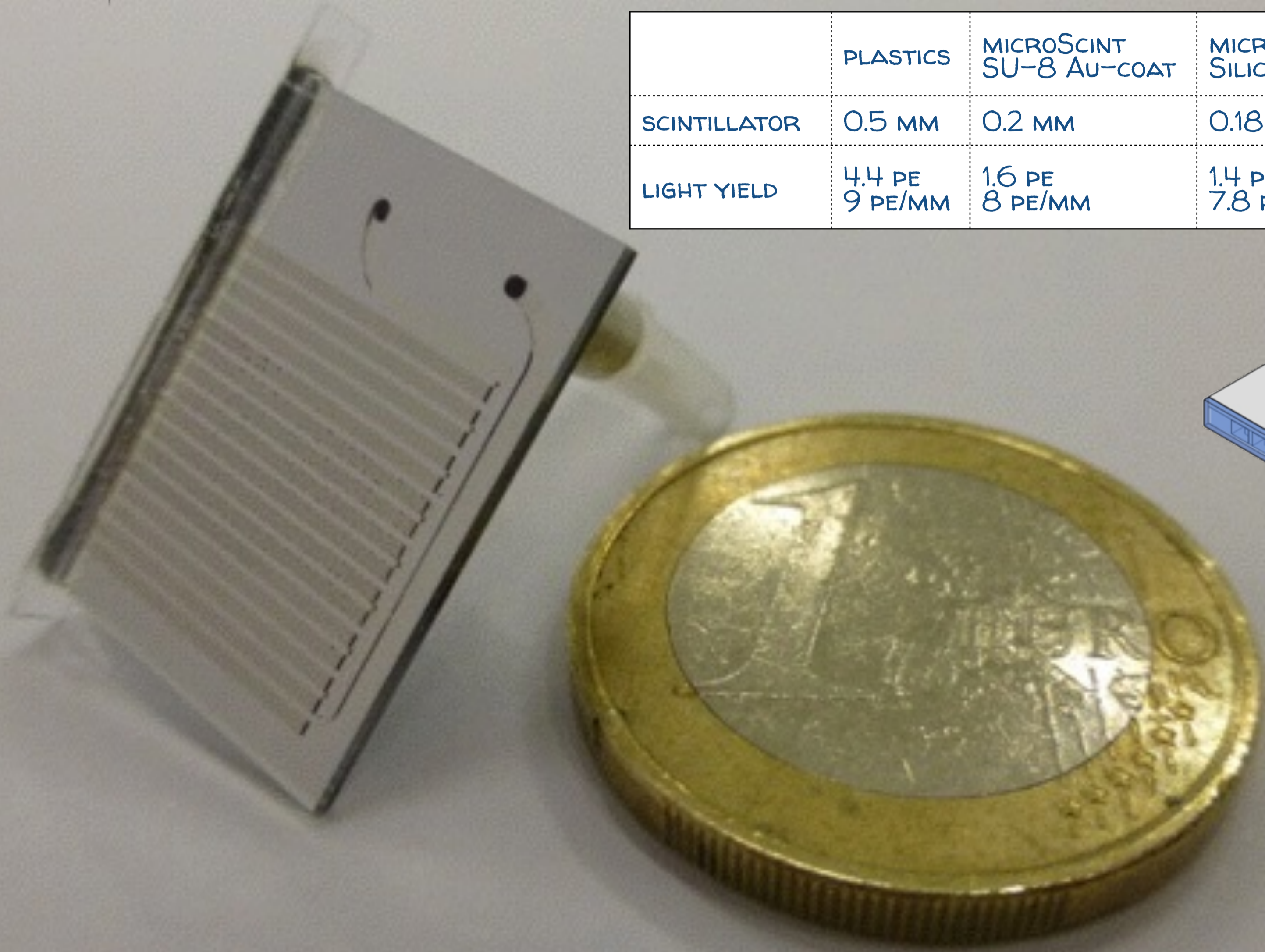


## GLUEING OF WINDOW AND TUBES

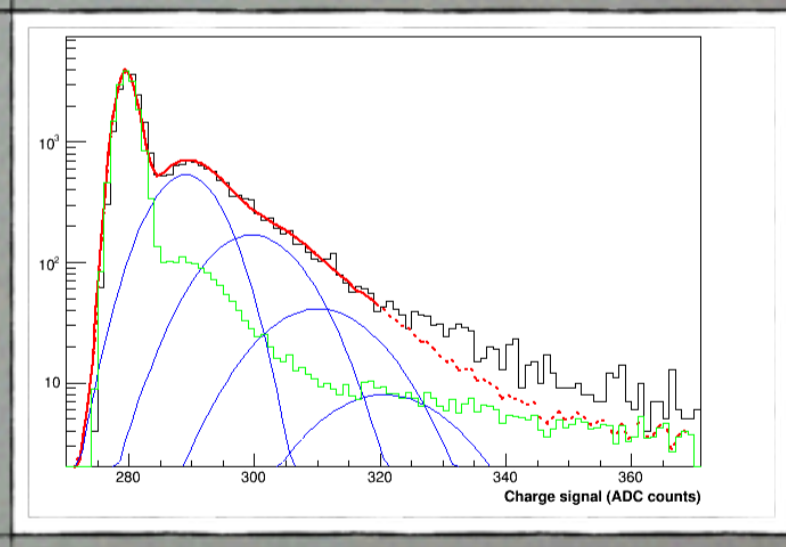
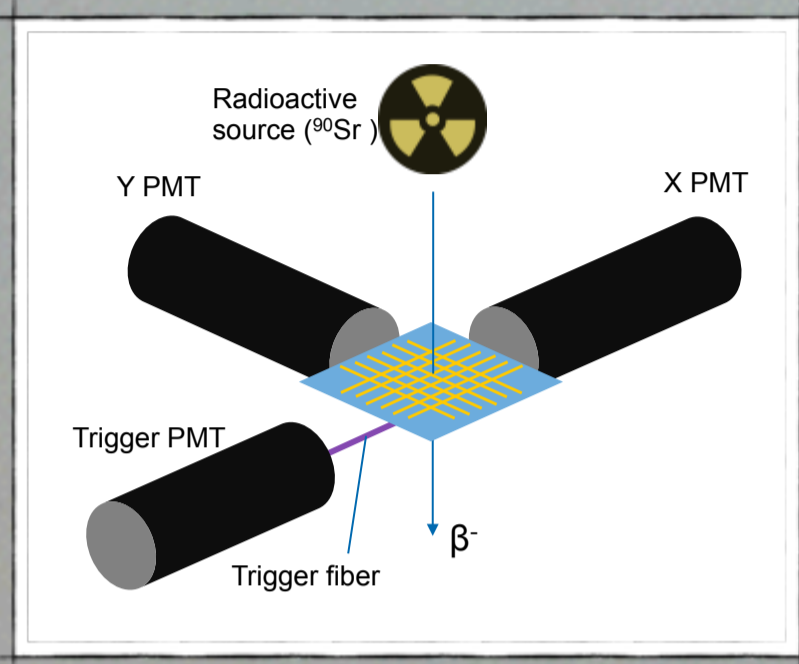
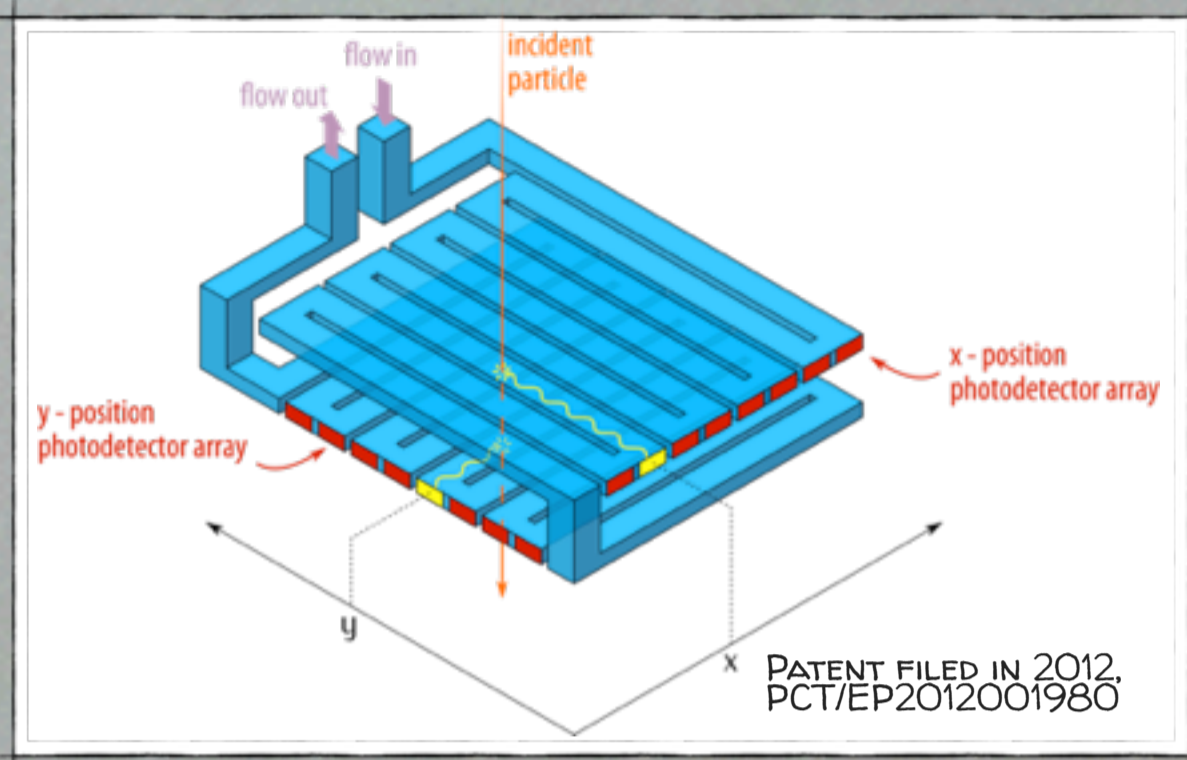


# EXPERIMENTAL CHARACTERISATION WITH PMT

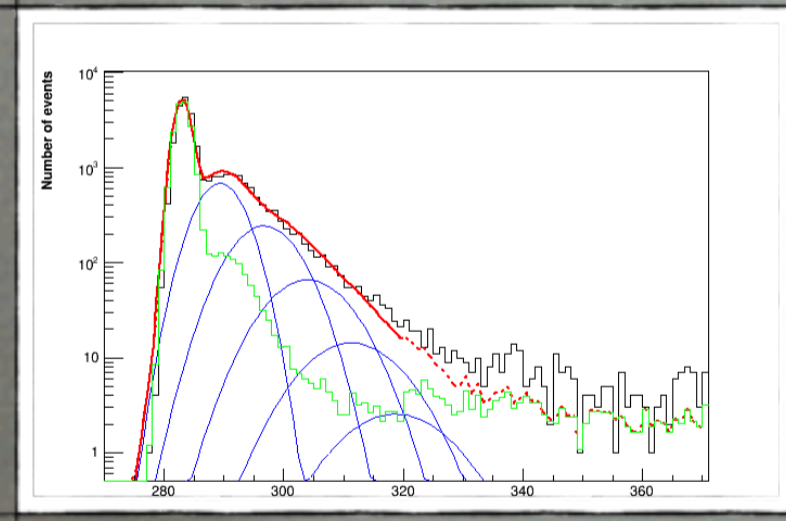
	PLASTICS	MICROSCINT SU-8 AU-COAT	MICROSCINT SILICON AL-COAT
SCINTILLATOR	0.5 MM	0.2 MM	0.18 MM
LIGHT YIELD	4.4 PE 9 PE/MM	1.6 PE 8 PE/MM	1.4 PE 7.8 PE/MM



# DOUBLE LAYER DEVICES FOR XY RECONSTRUCTION



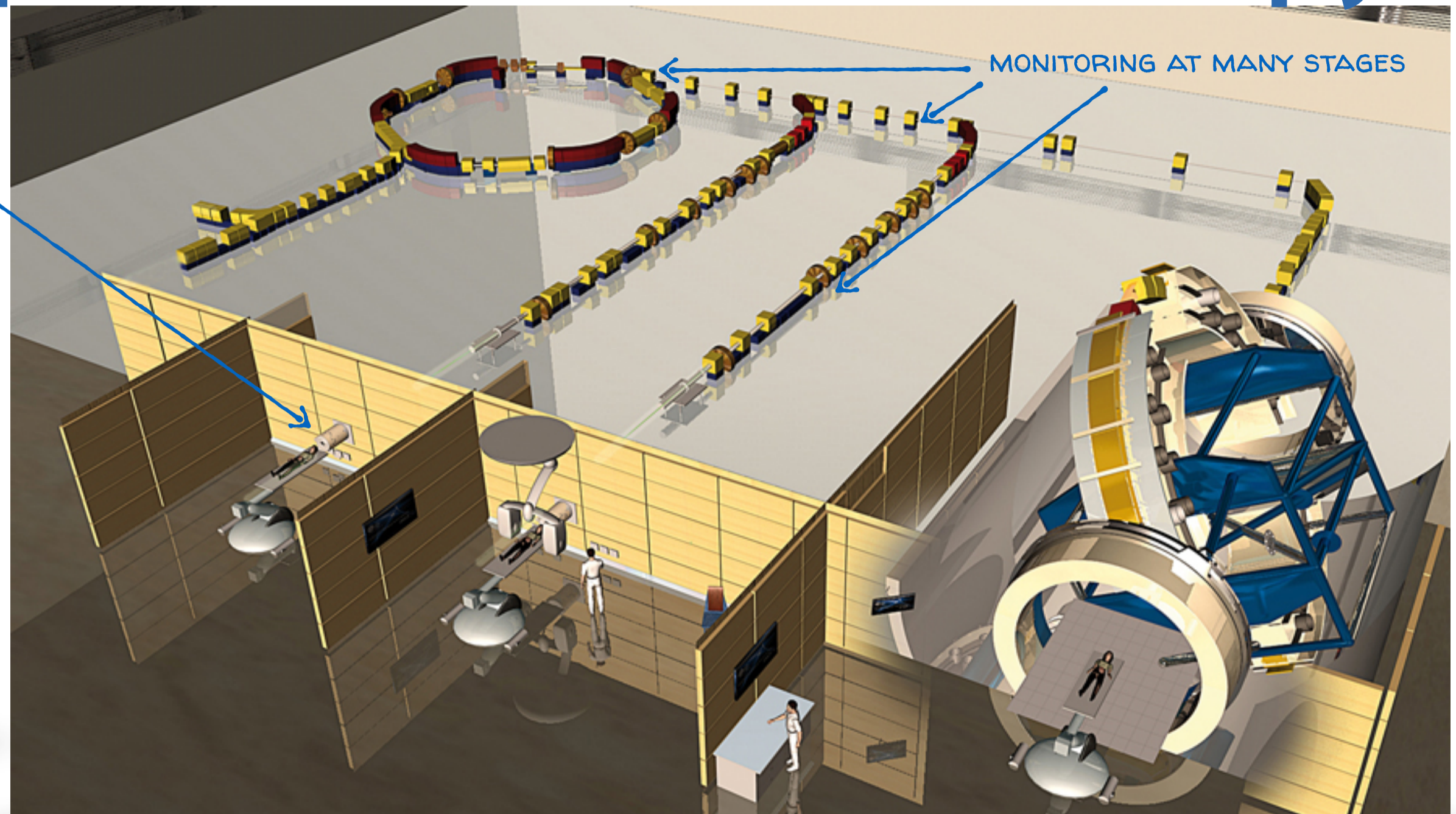
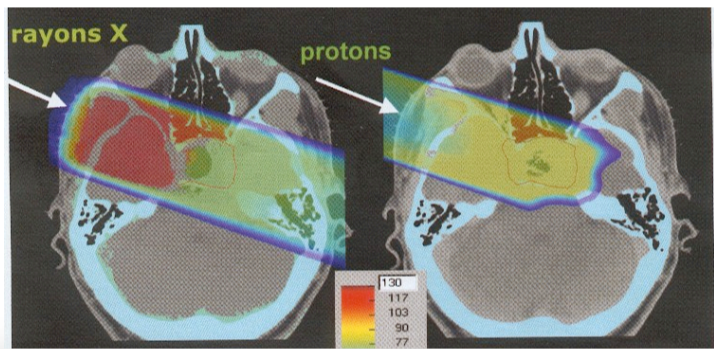
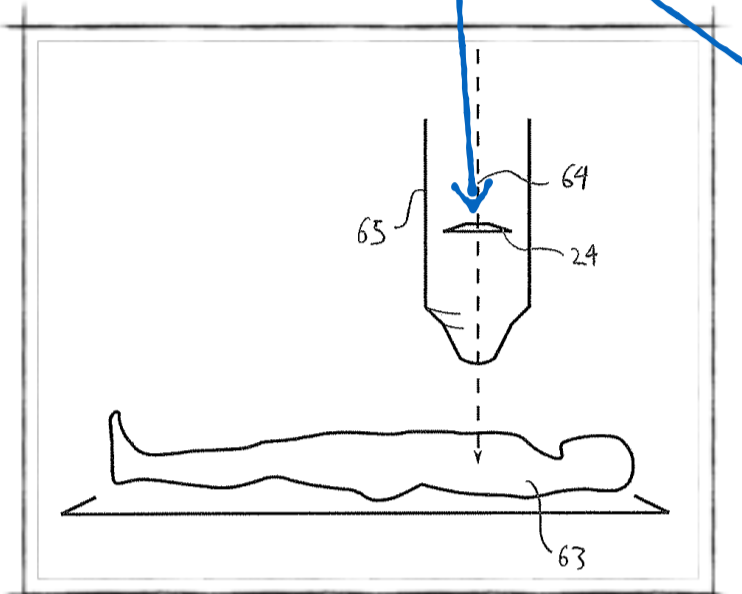
X LAYER 150  $\mu\text{m}$   
0.9 PE  
6 PE/MM



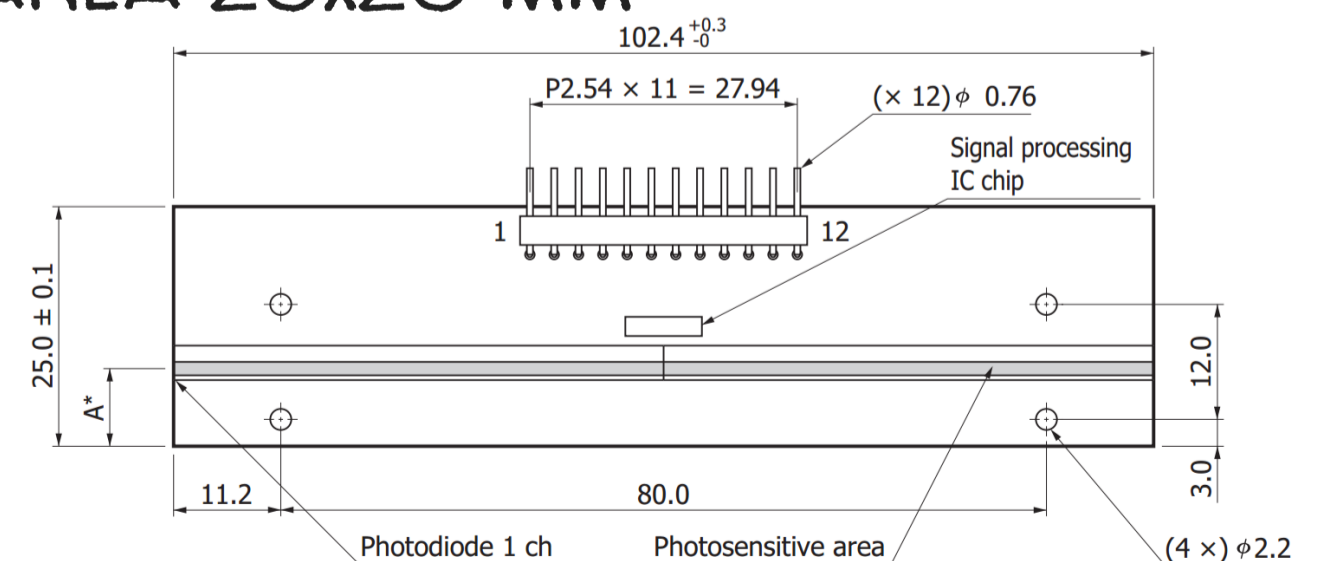
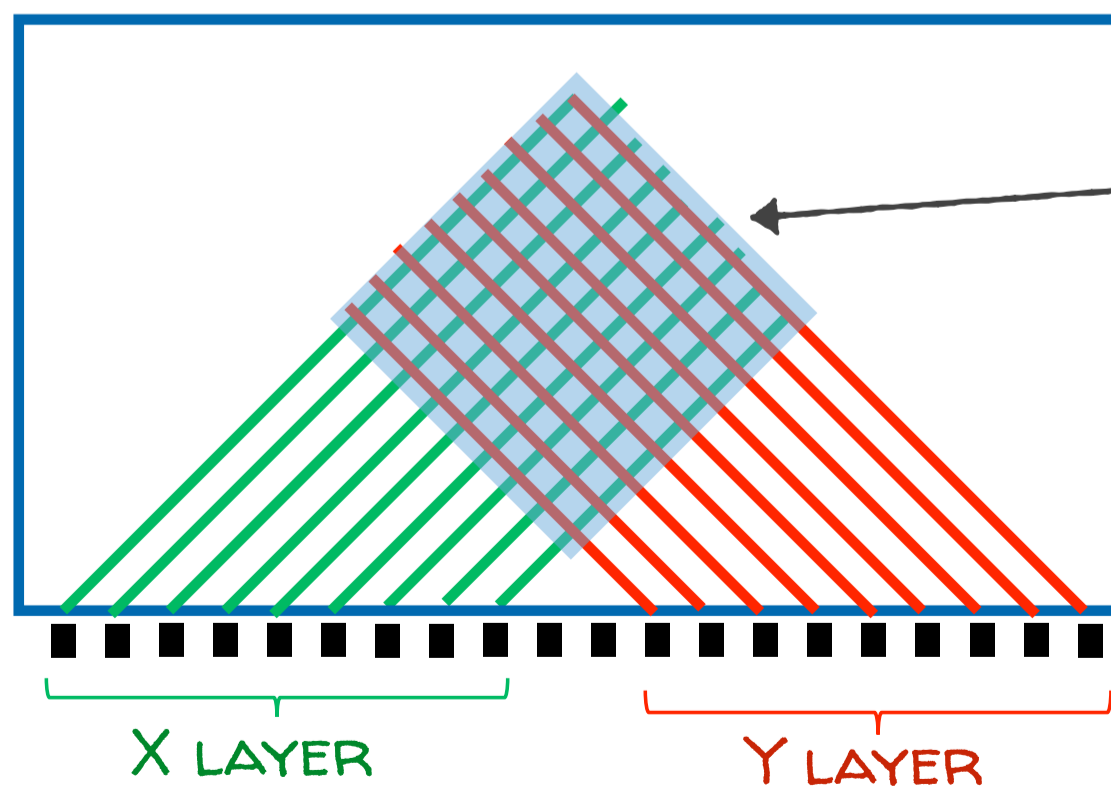
X LAYER 150  $\mu\text{m}$   
1.0 PE  
6.7 PE/MM

# beam profiler for hadrontherapy

THIN MICROFLUIDIC MONITOR



ALL SILICON DEVICE  
500  $\mu\text{m}$  THICK ( $\sim 0.5\% X_0$ )  
ACTIVE AREA 20x20  $\text{mm}^2$



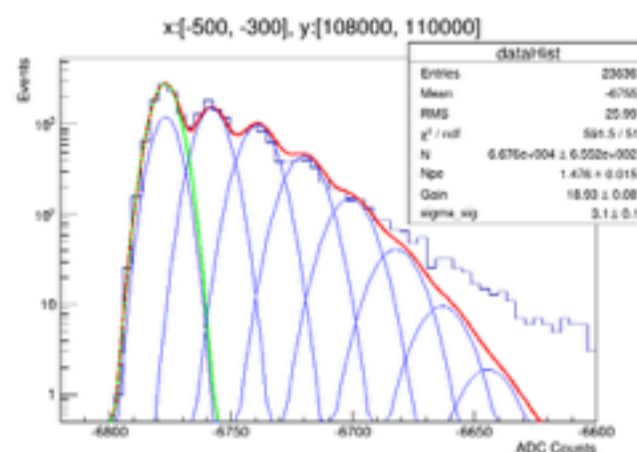
PHOTODIODE ARRAY  
HAMAMATSU S8866-128-02



# coming up!

Beam test at PSI to validate XY device read-out by photodiodes as beam monitor for hadrontherapy

SiPM readout of single layer at CERN (with Christian Joram)

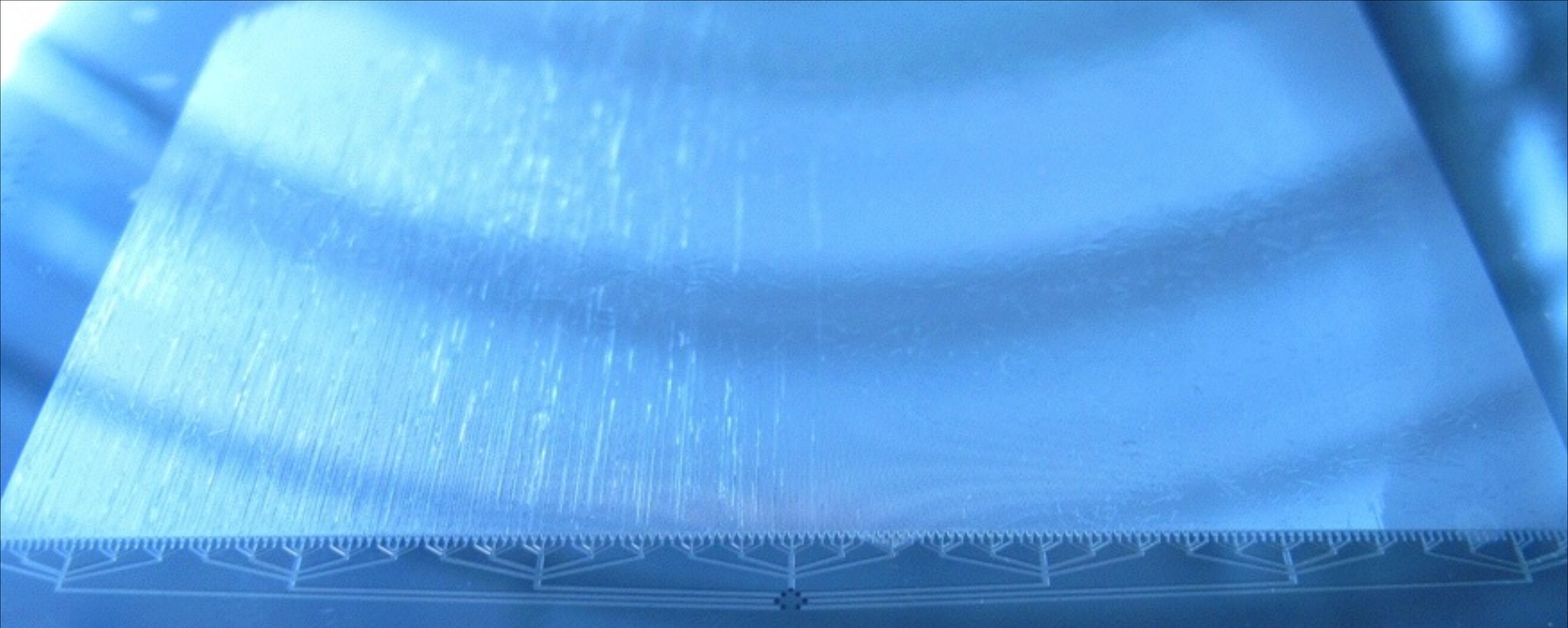


Implement SiPM readout at CERN (INFN)

Integrate **aSi photodiodes** on microfluidic devices (EPFL-PVLAB)



Large area detectors (with Rui de Oliveira)





NAI2-GTK cooling (left)  
cooling holes: 61 x 46  $\mu\text{m}$   
50 x 50 channels, pitch: 75  
Manifold: 500 / holes: 4 x 4 mm diam.  
Distributor: / holes: 7 x 17 mm diam.

# MICROCOOL

MICROFABRICATED ON-DETECTOR COOLING SYSTEMS


# microCool at TWEPP

 **EPFL** ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE 

## Micro Scale Heat Transfer for Electronics Cooling

**Prof. John R. Thome**  
Laboratory of Heat and Mass Transfer  
Faculty of Engineering Science  
Ecole Polytechnique Fédérale de Lausanne  
Lausanne, Switzerland  
TWEPP-09, Paris, Sept. 24, 2009

2009



## Microfluidic Cooling for Detector and Electronic

**A. Mapelli & P. Petagna**  
CERN PH-DT  
Reporting on behalf of  
D. Bouit, J. Daguin, L. Kottelat, A. Mapelli, J. Noel, P. Petagna – CERN PH-DT  
K. Howell – Georges Mason University / CERN PH-UFT  
G. Nuessle – Université Catholique de Louvain / CERN PH-UFT  
A. Pezous - CSEM  
P. Renaud – EPFL-LMIS4

**OUTLINE:**  
Motivations for micro-channel cooling in HEP  
Micro-technologies involved  
First possible HEP cases: the NA62 GTK  
the ALICE ITS upgrade  
the LHCb VELO upgrade  
Other ongoing R&D programmes on micro-channel cooling  
Conclusions and perspectives

2011

## Microfabricated silicon on-detector cooling systems

**Alessandro Mapelli**

 PH-DT  
Detector Technologies



TWEPP 2013  
Perugia, Italia

O. Augusto  
J. Buytaert  
J. Degrange  
R. Dumps  
A. Francescon  
K. Howell  
M. John  
J. Noel  
A. Nomerotski  
G. Nuessle  
P. Petagna  
G. Romagnoli  
M. van Stenis  
B. Verlaat

2013



# Motivation

## Issues to be addressed when designing on-detector cooling systems

1. Minimization of material budget
2. Efficient thermal management
3. Minimization of  $\Delta T$  between heat source and heat sink

## Integration of cooling and detector lay-out

The cooling has to be considered as an integral part of the detector and the experiment, therefore physicists and engineers shall collaborate from the beginning of the conceptual design of the systems, with an overall view on all subparts.

*Engineering Cooling Forum  
30 October 2008, CERN*

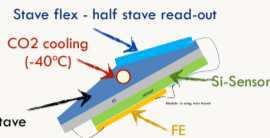
# Integrating Cooling in Support Structures.. ..or Somewhere in the Silicon?

## ATLAS IBL

### The IBL stave

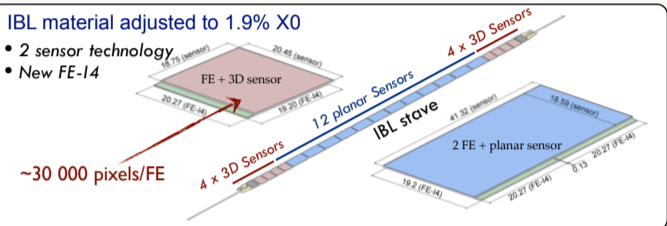
ATLAS → Inner Detector → Pixel

- Composed of 14 staves
- 60 cm of active length (Z) or 11 coverage of 2.5
- Average radius of 34mm with a 9mm envelop
- Hermeticity ensure with an overlap of 1.8° between staves



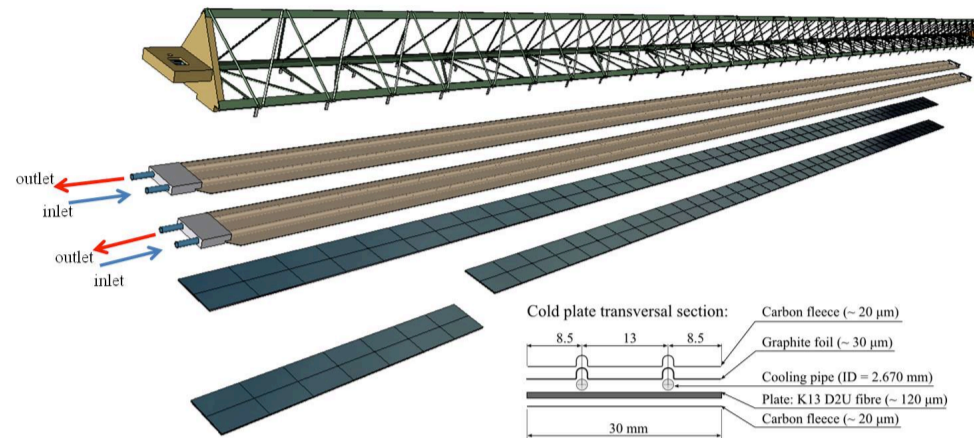
IBL material adjusted to 1.9% X<sub>0</sub>

- 2 sensor technology
- New FE-14

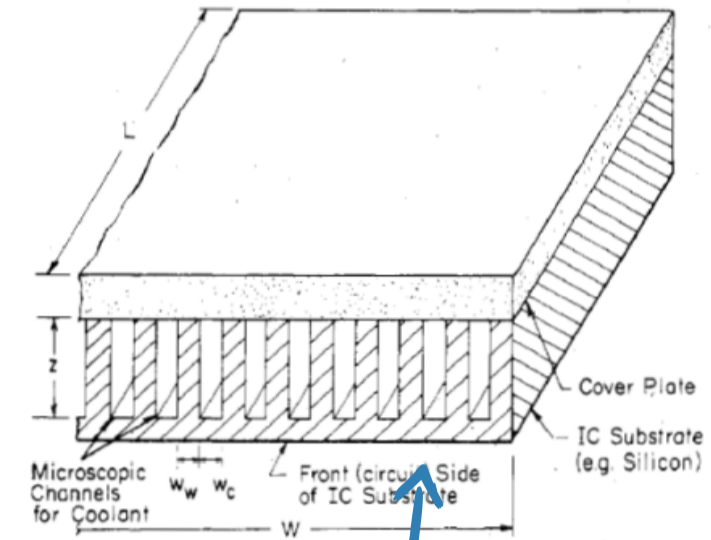


from J. Bilbao <http://indico.cern.ch/sessionDisplay.py?sessionId=6&confId=208719#20130125>

## ALICE ITS Upgrade

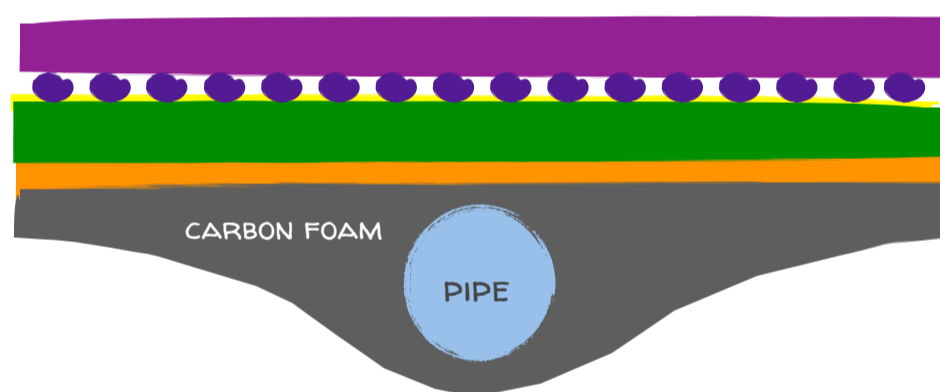


ALICE ITS Upgrade Outer Barrel Stave

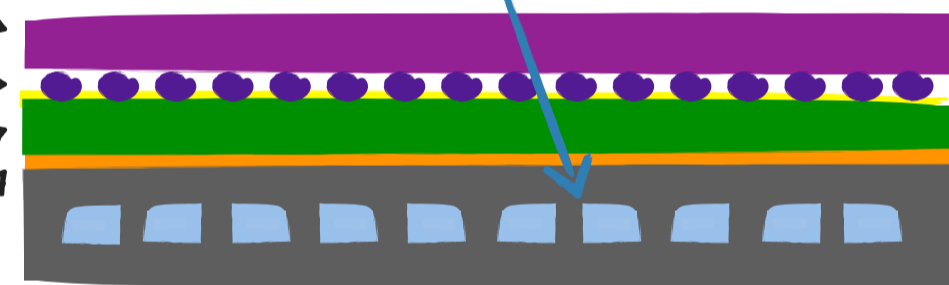


D.B. Tuckerman and R.F.W. Pease. IEEE Elec. Dev. Letters. Vol. 2. 5. 1981

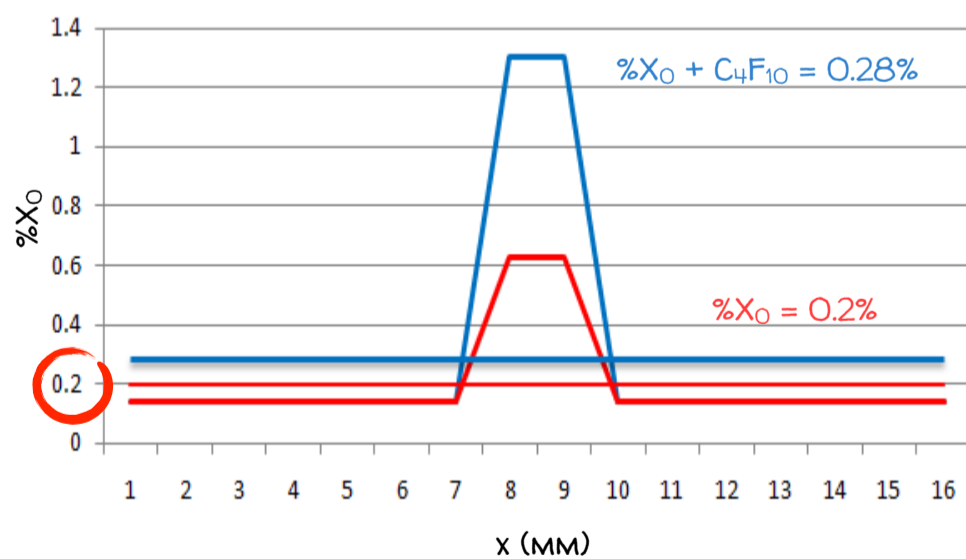
## IN-MECHANICS APPROACH



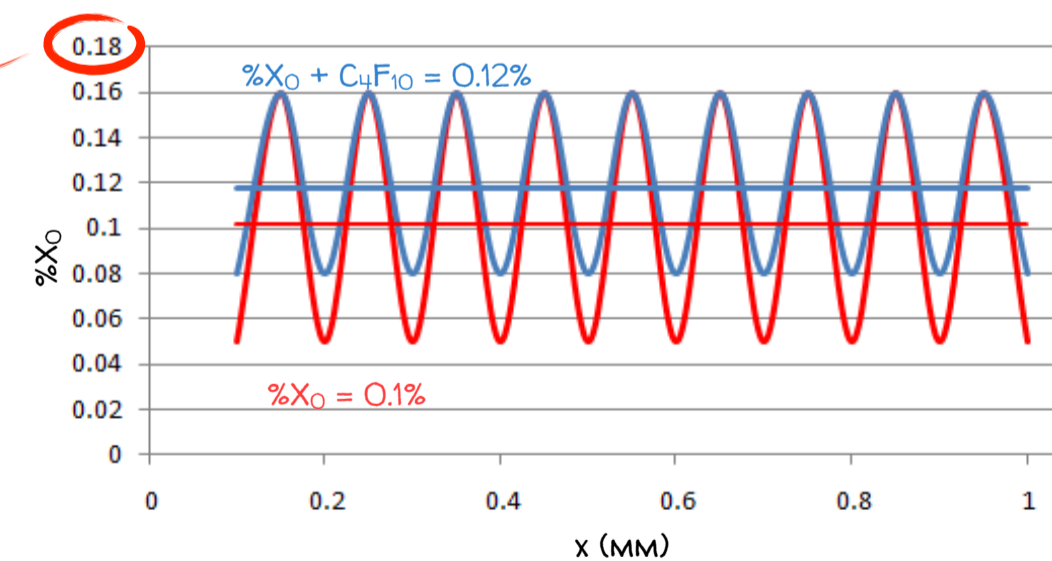
## SILICON COOLING MICROCHANNELS



NO CTE MISMATCH



X<sub>0</sub> calculations by Claudio Bortolin



10°C

$\Delta T$  between heat source and heat sink for power dissipations of  $\sim 1\text{W}/\text{cm}^2$   
(currently installed systems  $\sim 15^\circ\text{C}$ )

5°C



# Silicon Microfluidic Cooling

OUT OF THE HEP WORLD

IBM Research - Zurich



## Direct Liquid jet impingement

Arrayed jets, distributed return

Biological vascular systems are optimized for the mass transport at low pressure

Cooling of up to  $350 \text{ W/cm}^2$

Direct Liquid Jet-Impingement Cooling with Micron-Sized Nozzle Array and Distributed Return Architecture, T. Brunswiler et al., IThERM 2006

ATP focus topic August 2010

© 2009 IBM Corporation

A new technology for stacking several layers of microprocessors, which is being developed at EPFL in collaboration with ETHZ and IBM Research, could boost the performance of computer chips by a factor 10. The team estimates that the first 3D chips will be implemented in supercomputers by 2015 with a novel internal cooling system fully operational by 2020, for even further improvements.

### Today's microchips

Cores - At present, processors in computers consist of 2-16 cores.

Cables - The cores are placed next to each other and communicate via interconnect cables.

- The interconnect network consumes a lot of energy.
- The interconnect network generates a significant amount of heat which could damage the chip.
- Heat and energy consumption limit the evolution of multicore technology.

### Tomorrow's 3D microchips

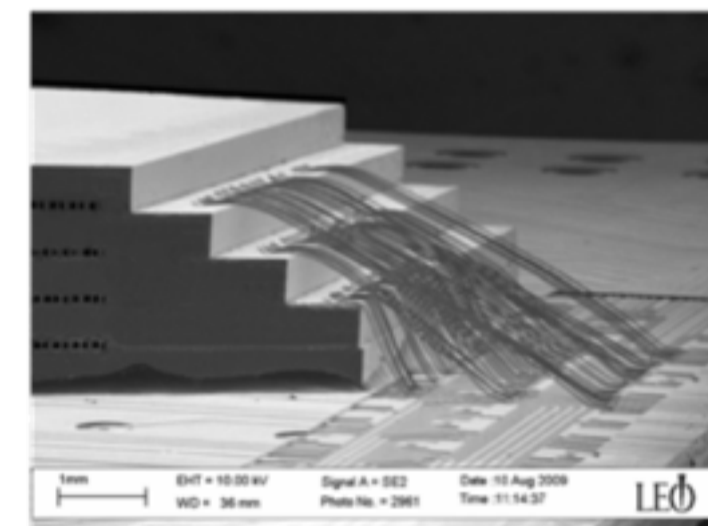
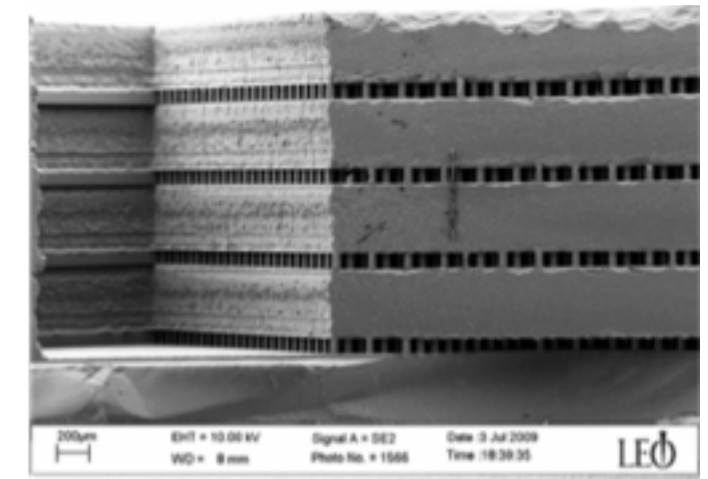
Cores - The cores are no longer placed side-to-side but stacked vertically.

Cables - 100 connections per mm<sup>2</sup> link the cores over their entire surface. Advantages:

- Data transfer between the cores is many times faster.
- The processor consumes less energy.
- The processor generates less heat.

Channels - As thin as a human hair (50 microns), the channels filled with the coolant (water or refrigerant) traverse the 3D microchip to maintain the optimal operating temperature.

Reference: EPFL, LTM, John R. Thome  
Infograph: Pascal Cotery, pascal@salut.ch



Processors should not reach more than 85°C

1. MICRO CHANNELS High performance micro channel coolers are attached directly to the backside of the processor. In the cooler, water is distributed by a network of very fine channels for efficient heat removal.

2. HEAT EXCHANGER The heat removed from the data center is delivered to a second circuit.

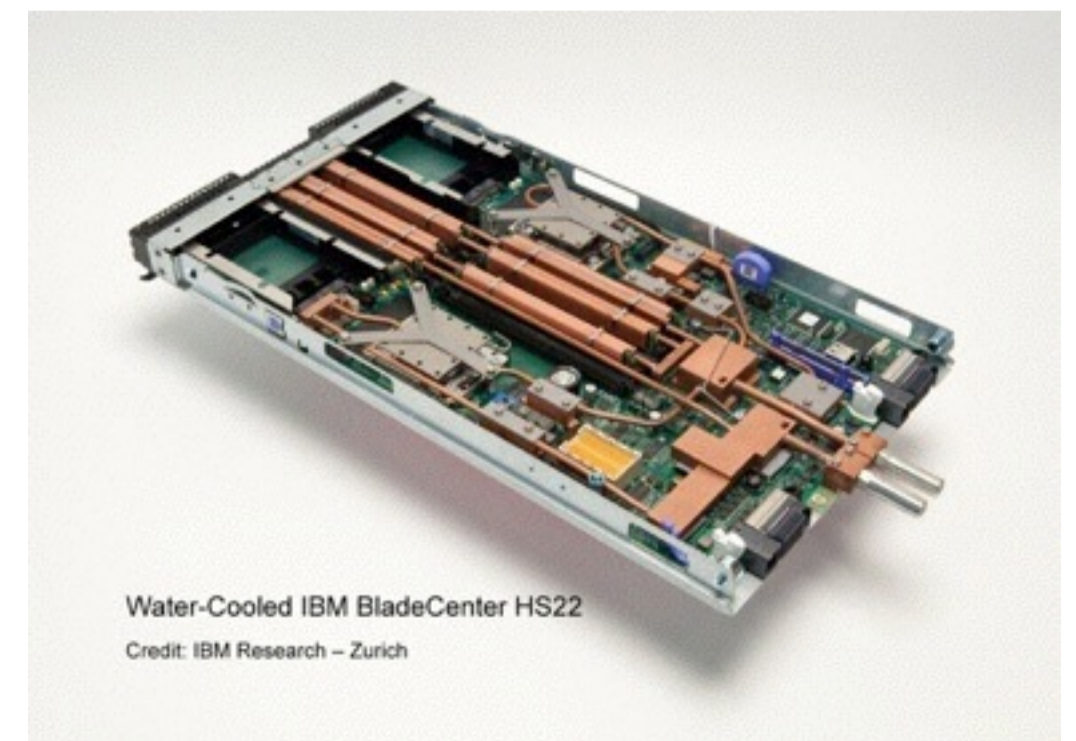
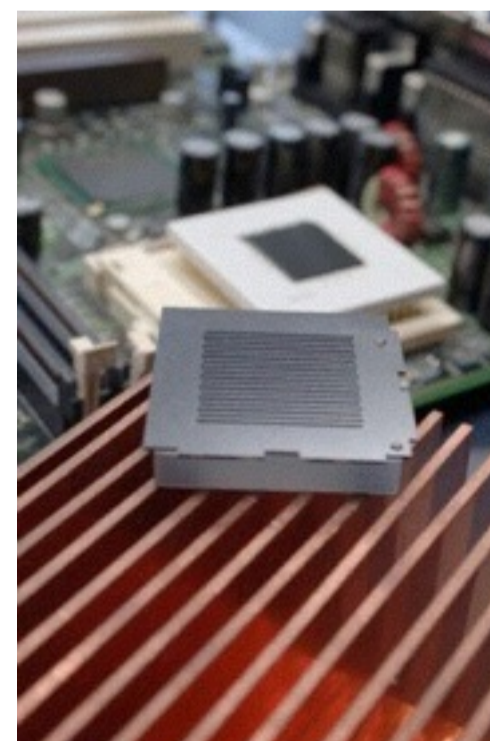
3. DIRECT REUSE OF WASTE HEAT The heat removed from the data center can directly be repurposed for a second usage, e.g. for heating of buildings.

Water pump

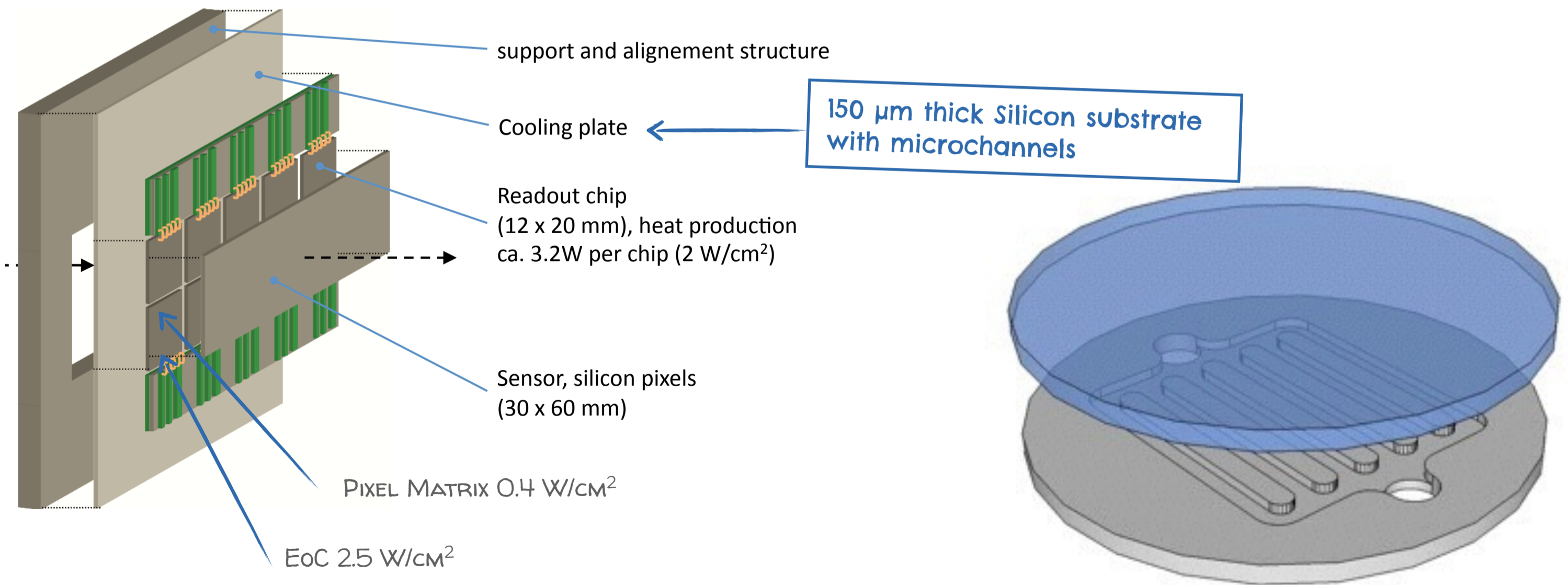
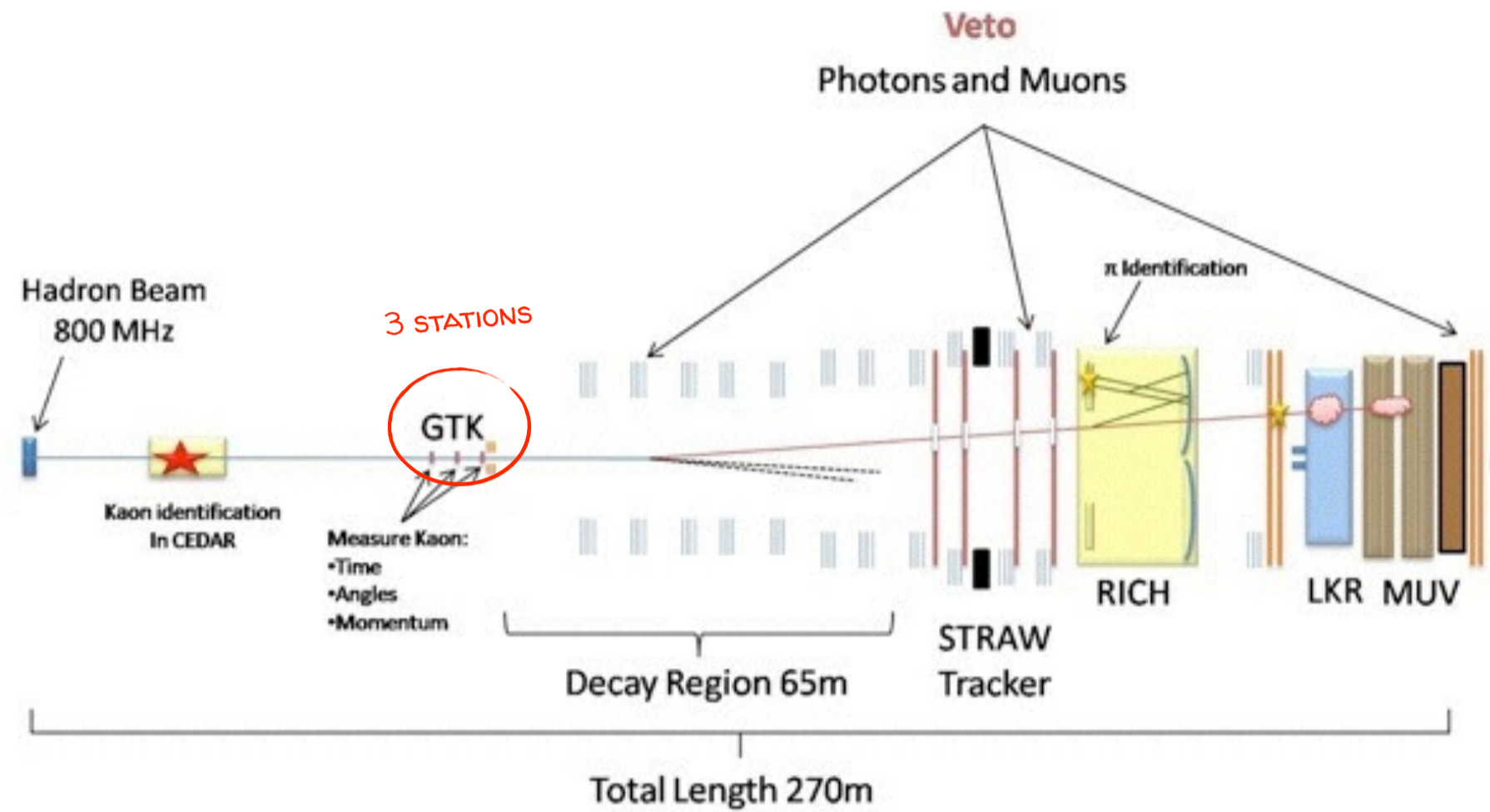
Under floor heating

CHIP COOLING Heating power Today's chips dissipate 10 times the heat of a typical hotplate. For optimal operation, chips must be cooled below 85°C.

Source: IBM Zurich Research Laboratory



# NA62-GTK



# Silicon Cooling Plate

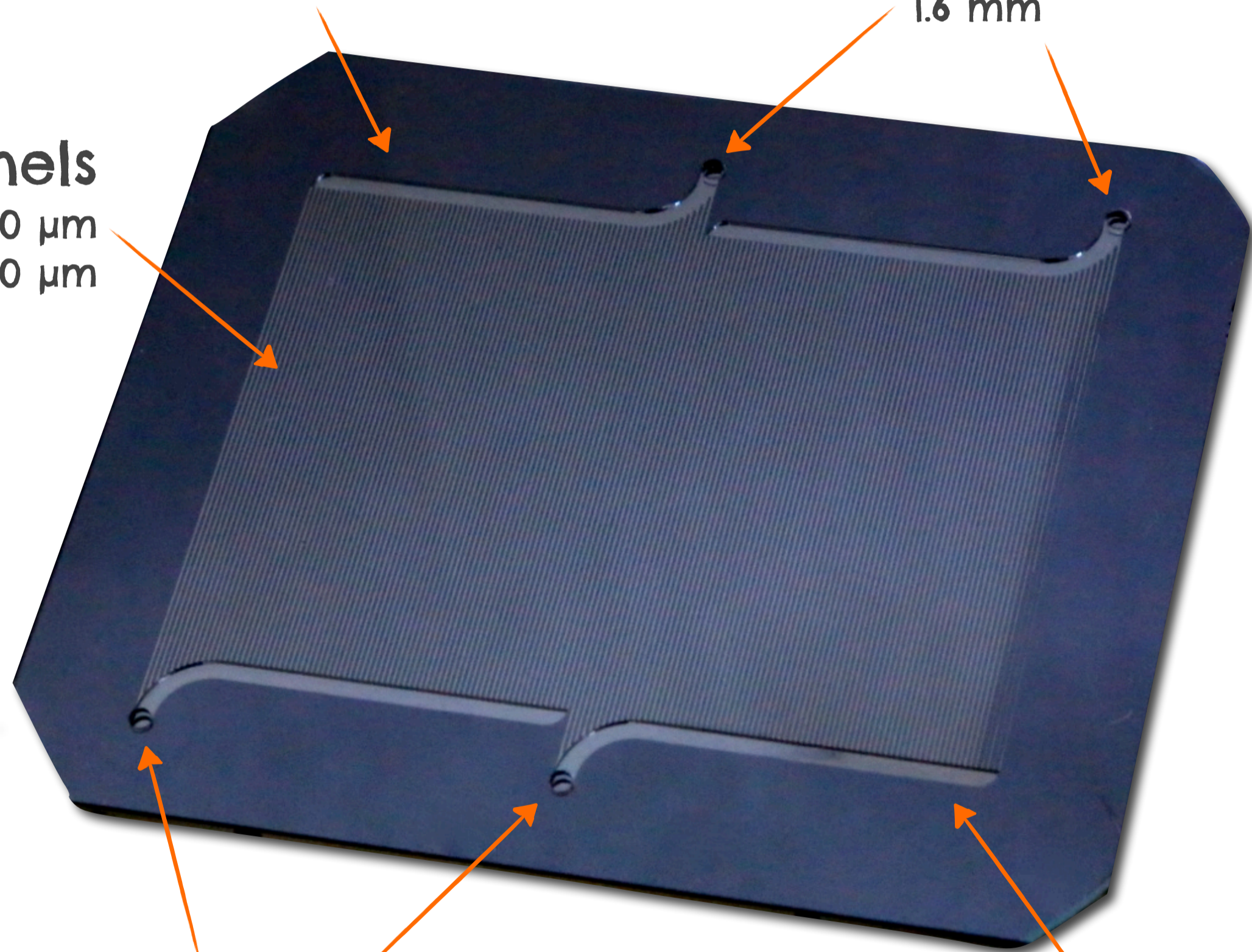
**distribution manifolds**  
280  $\mu\text{m}$  deep

**fluidic inlets**  
1.6 mm

**150 microchannels**  
200 x 70  $\mu\text{m}$   
pitch 400  $\mu\text{m}$

**fluidic outlets**  
1.6 mm

**recollection manifolds**  
280  $\mu\text{m}$  deep



# Microfabrication

Prototypes fabricated at EPFL by PH-DT.

Six pre-production modules outsourced to IceMOS.



Si wafer



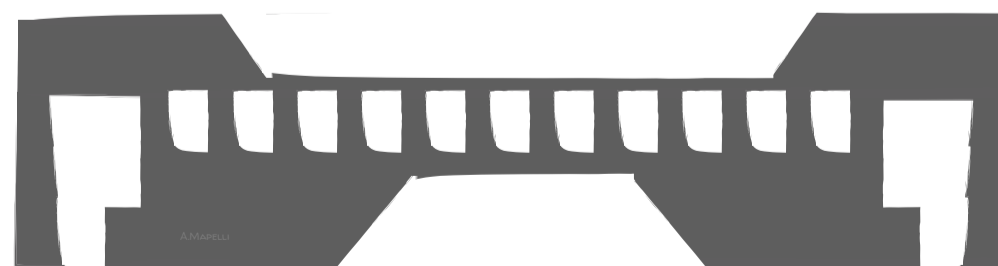
Plasma etching of channels & manifolds



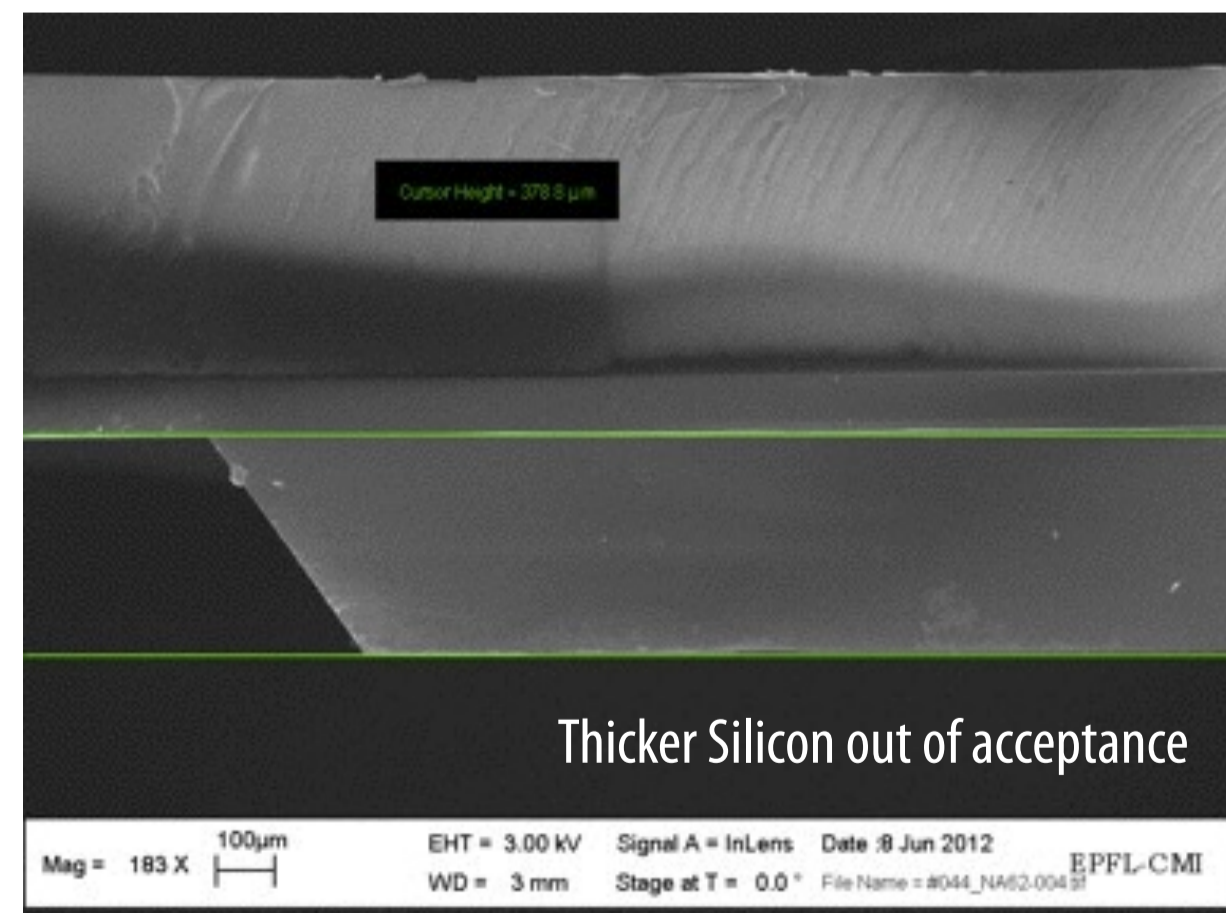
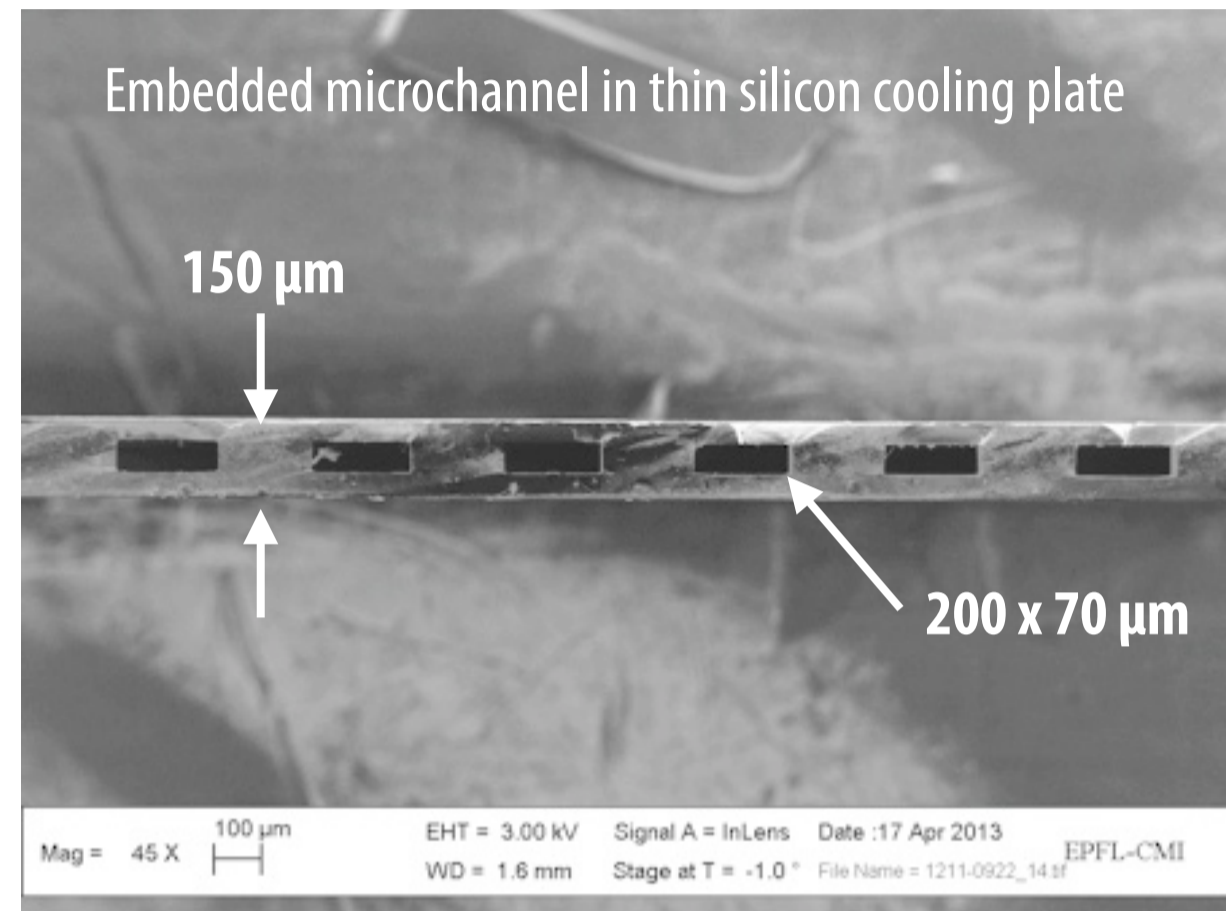
Bonding of Si cover



Plasma etching of fluidic openings

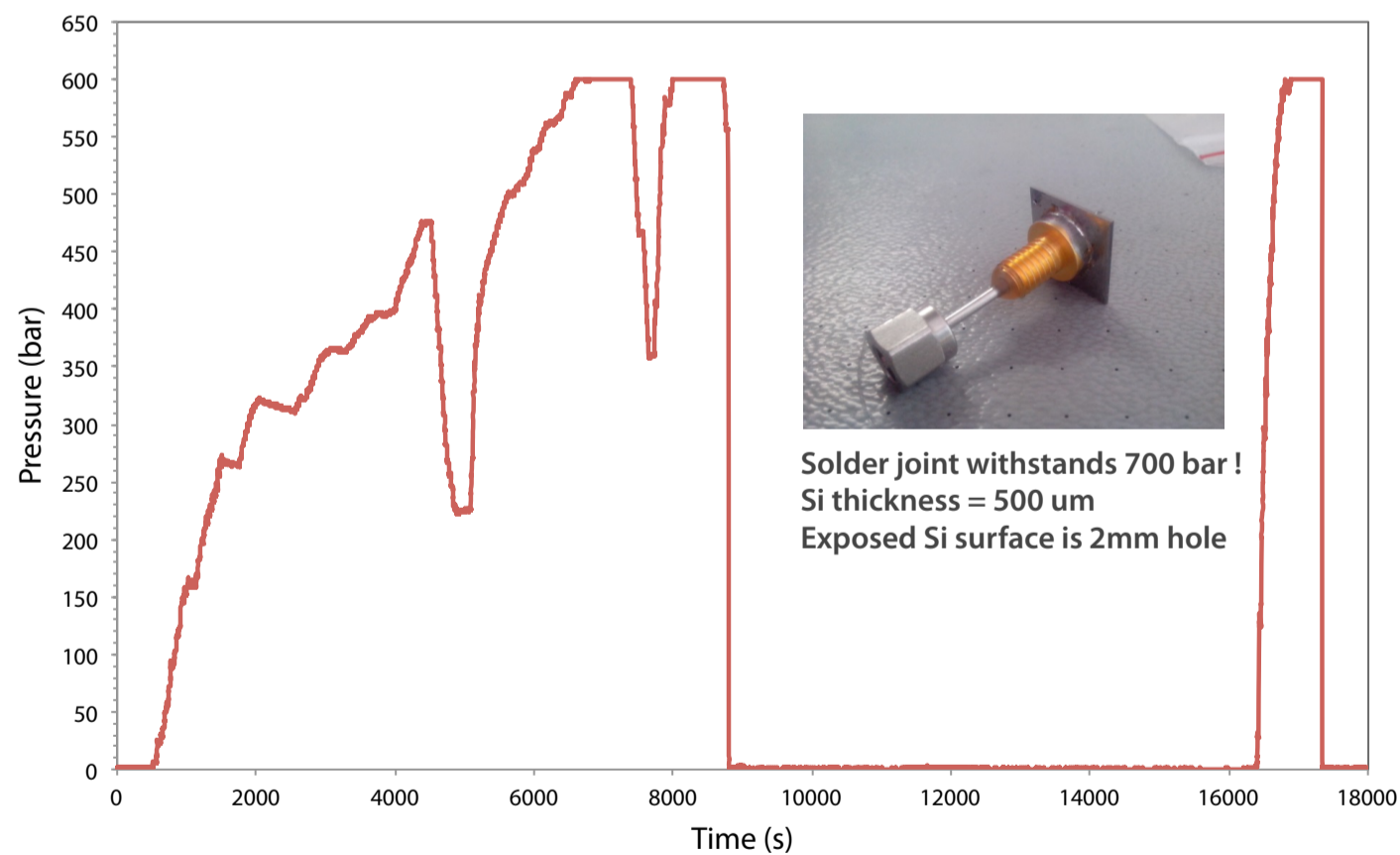
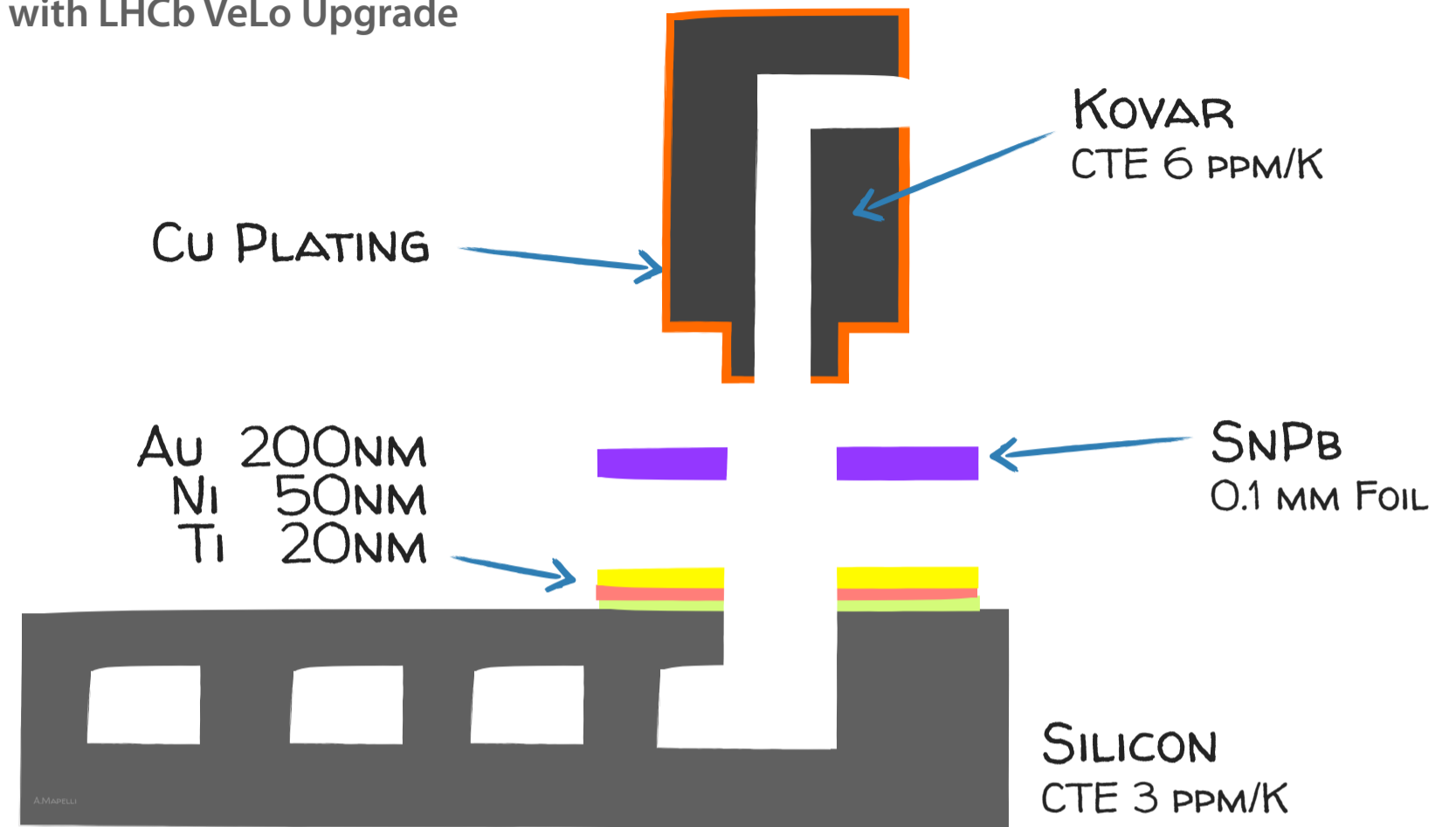
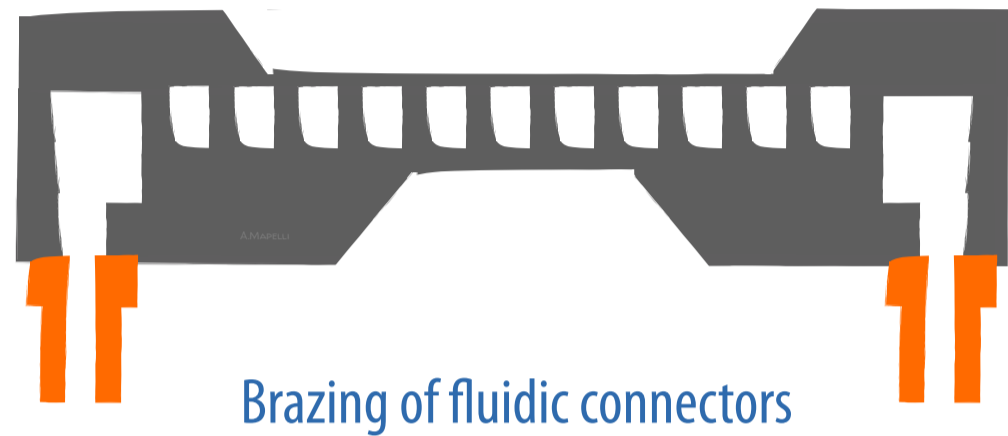


Wet etching of acceptance

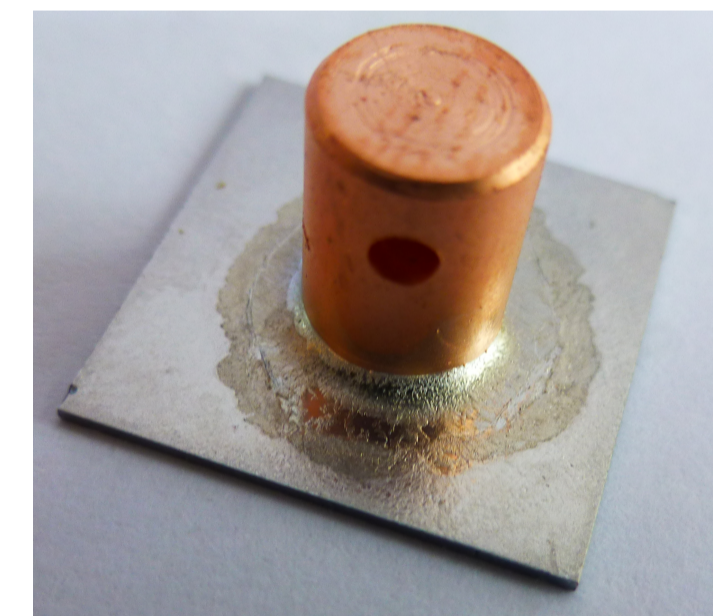


# Fluidic Connectors

Common development with LHCb VeLo Upgrade

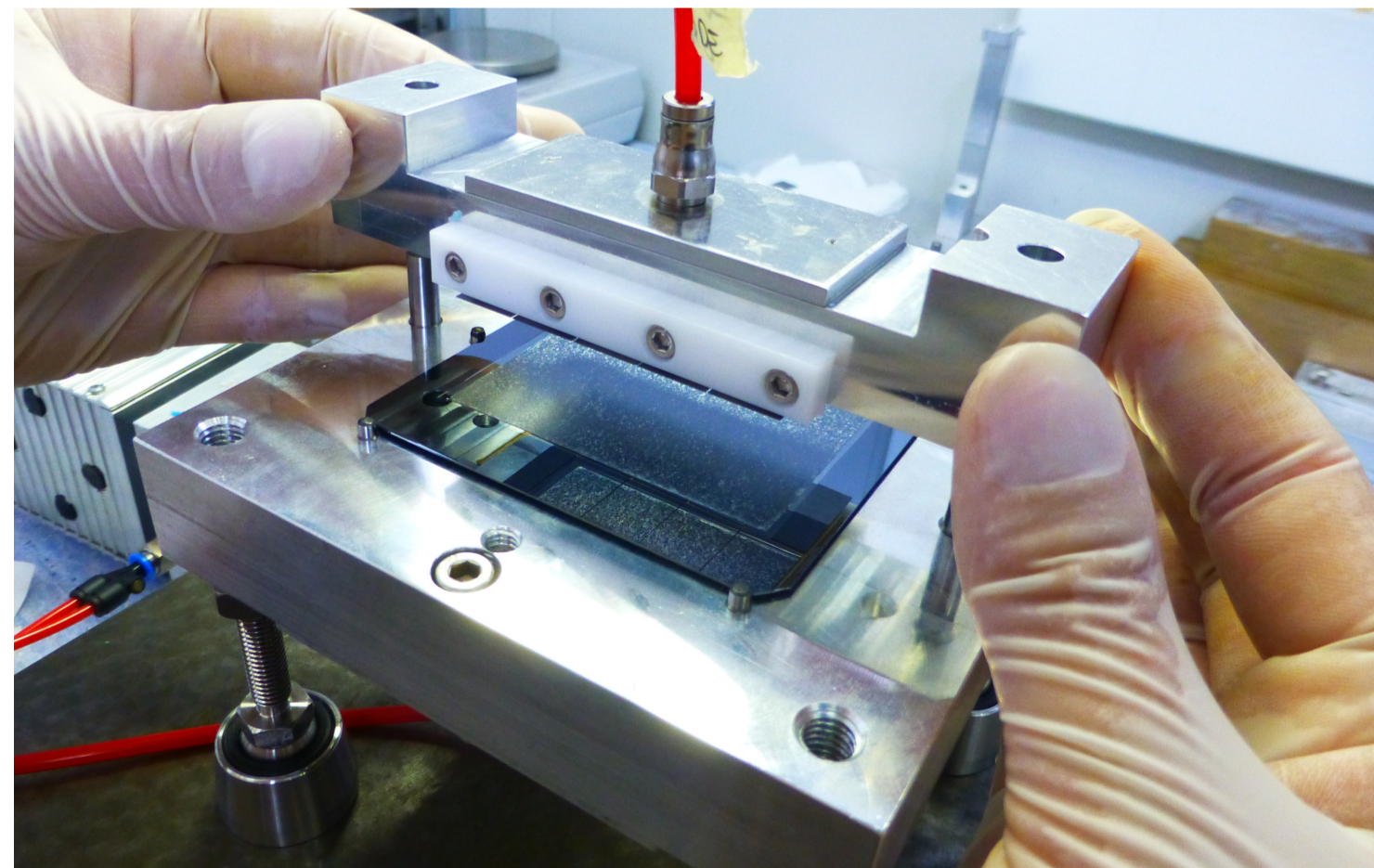
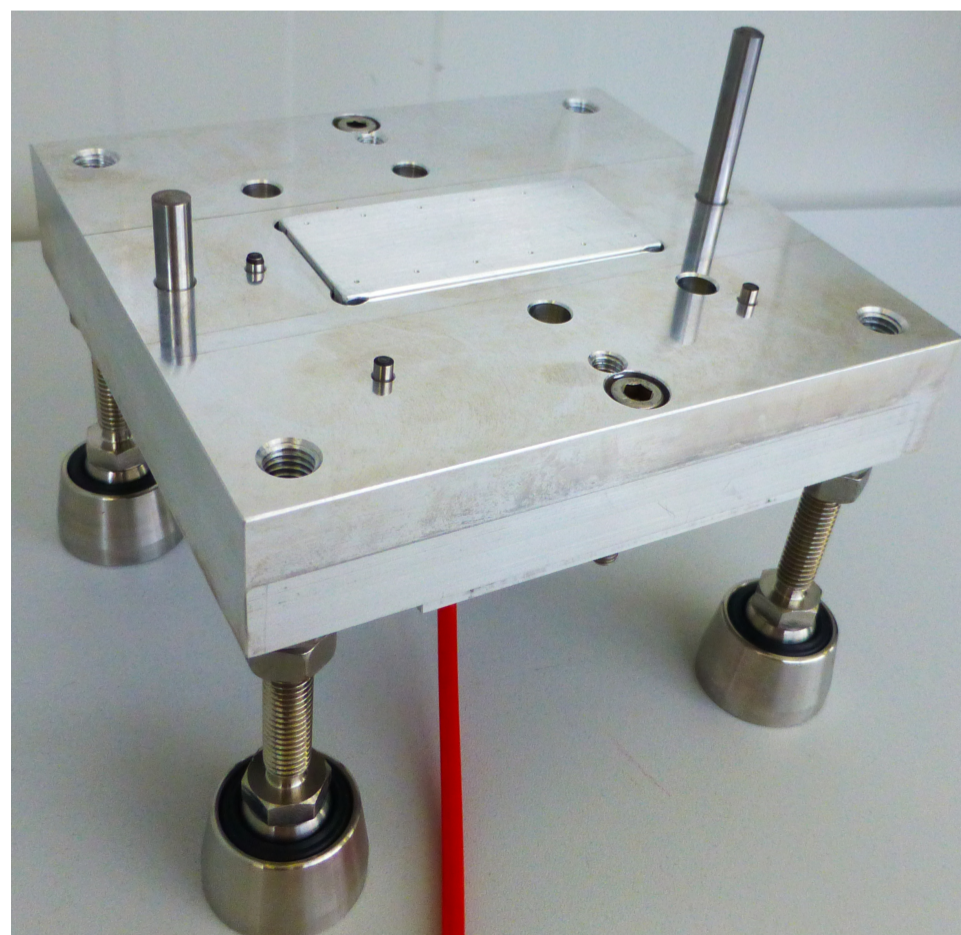
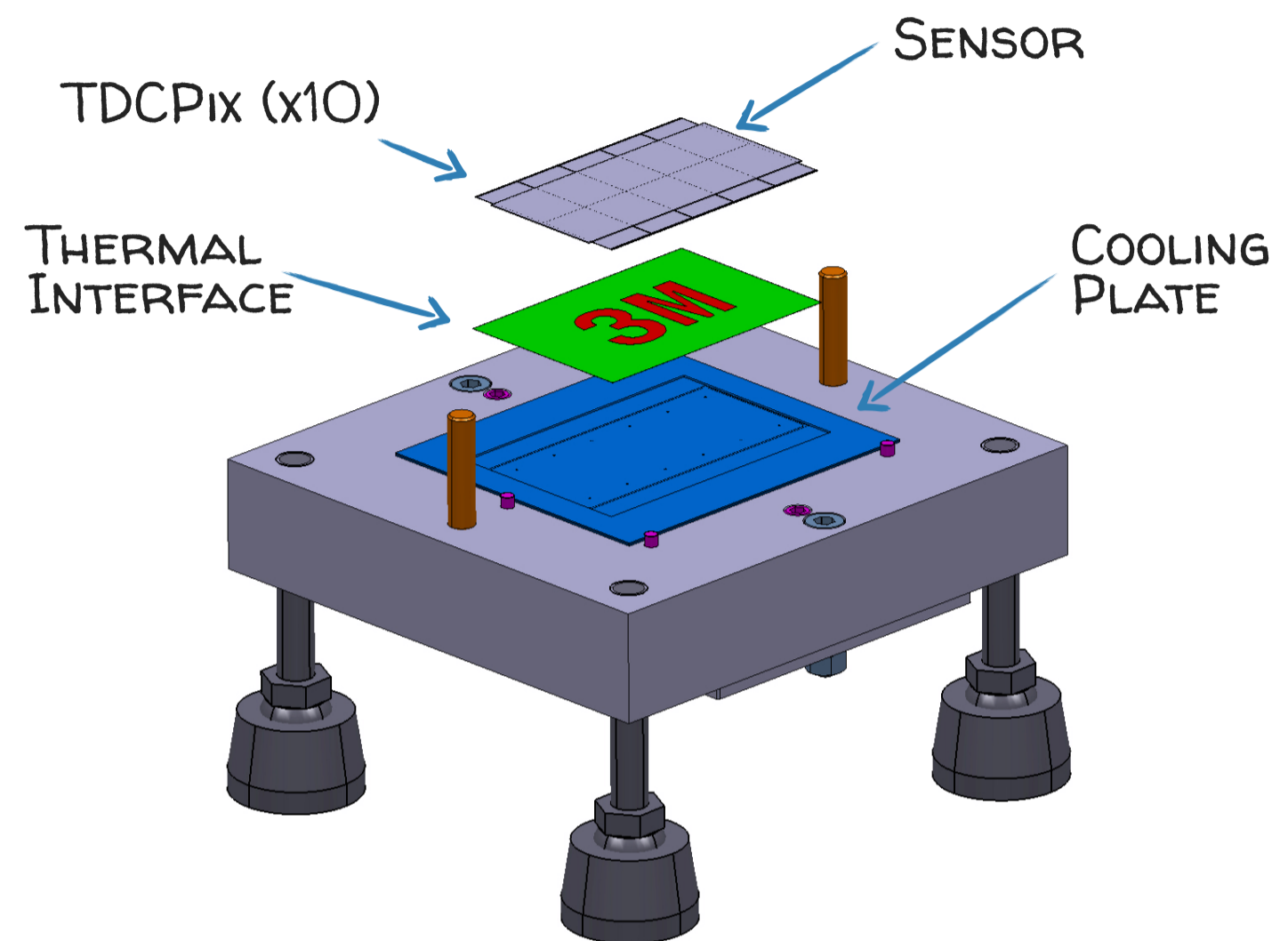
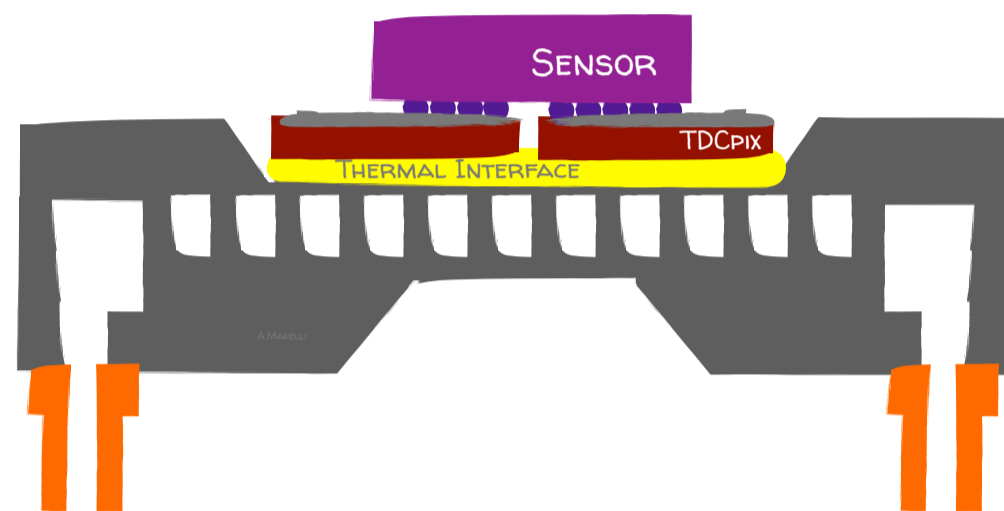


Limitation of the test set-up read-out at 600 bars  
Limitation of the pump 700 bars  
**No failure of the solder joint**



preliminary prototypes  
size reduction and different geometries under study

# Assembly to Sensor/TDCPix

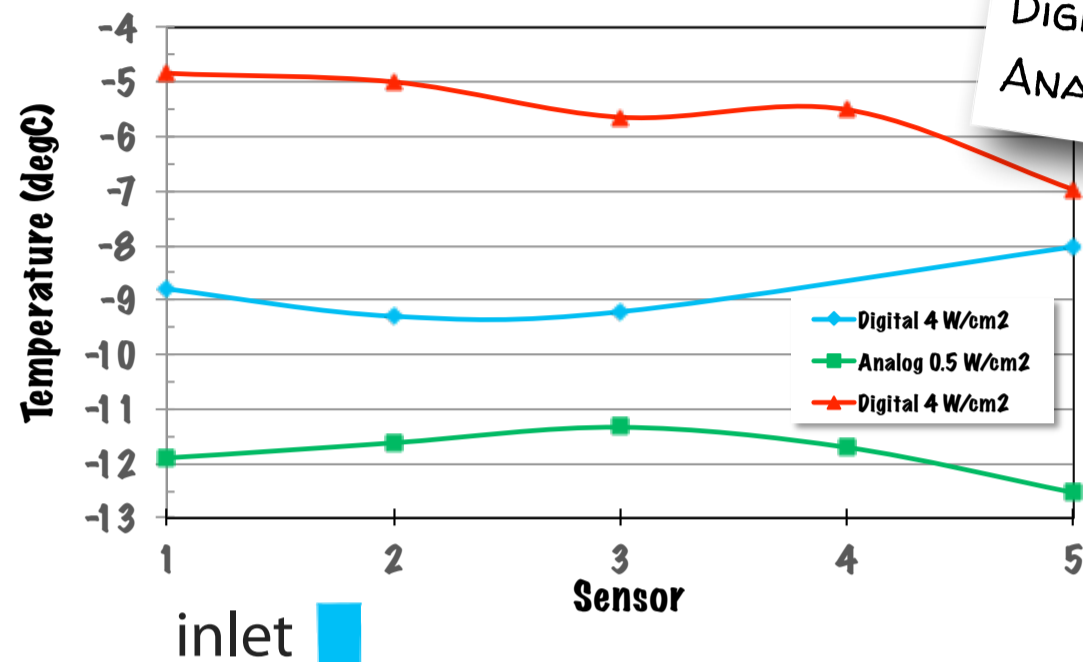


# Experimental Validation

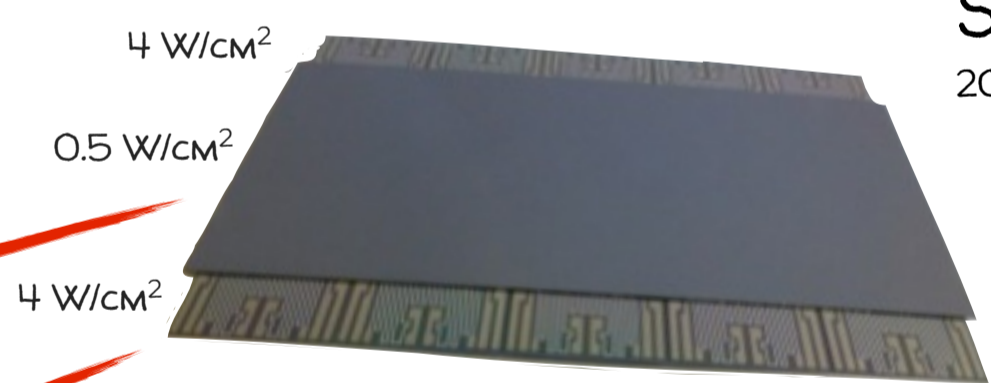
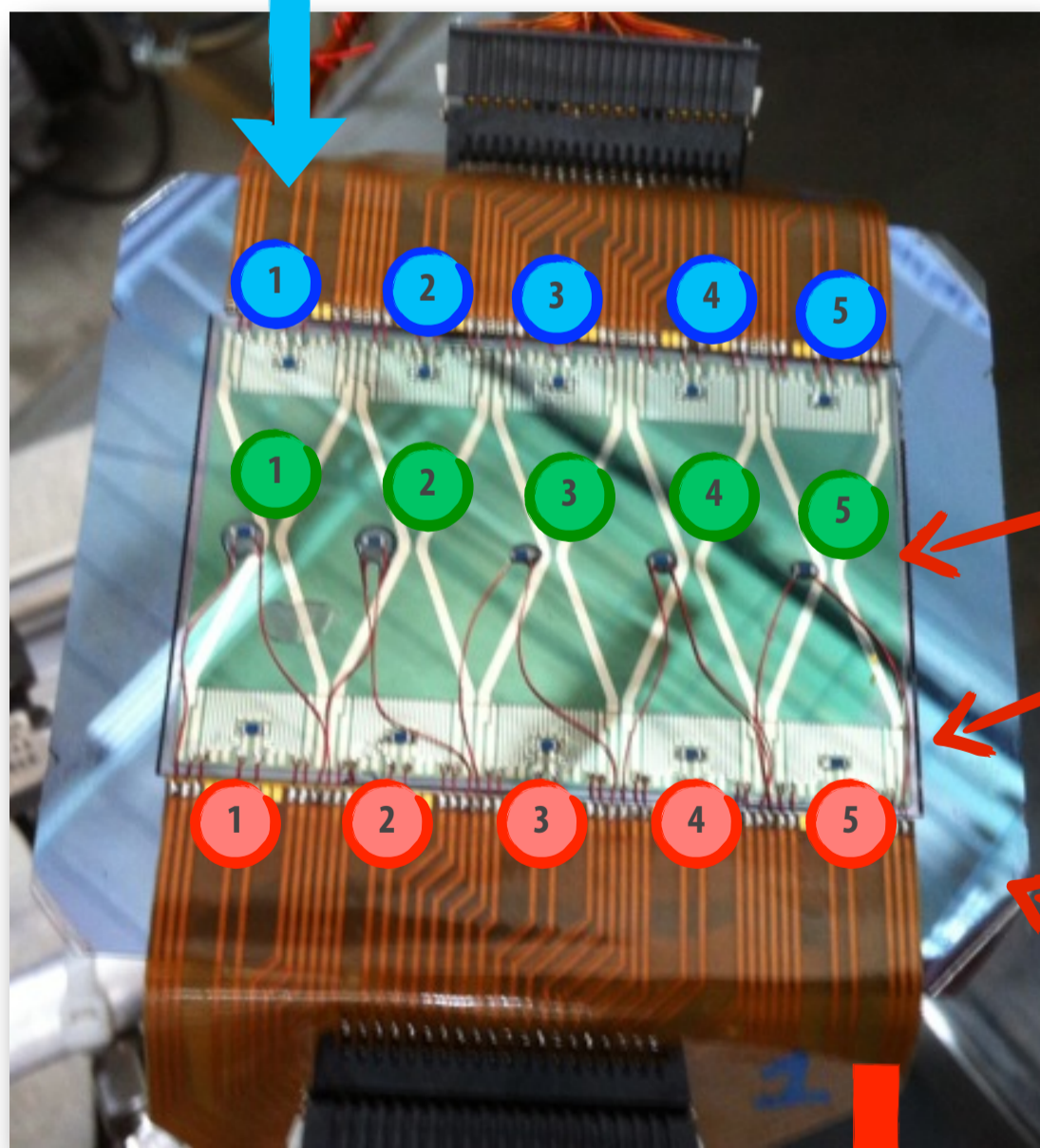
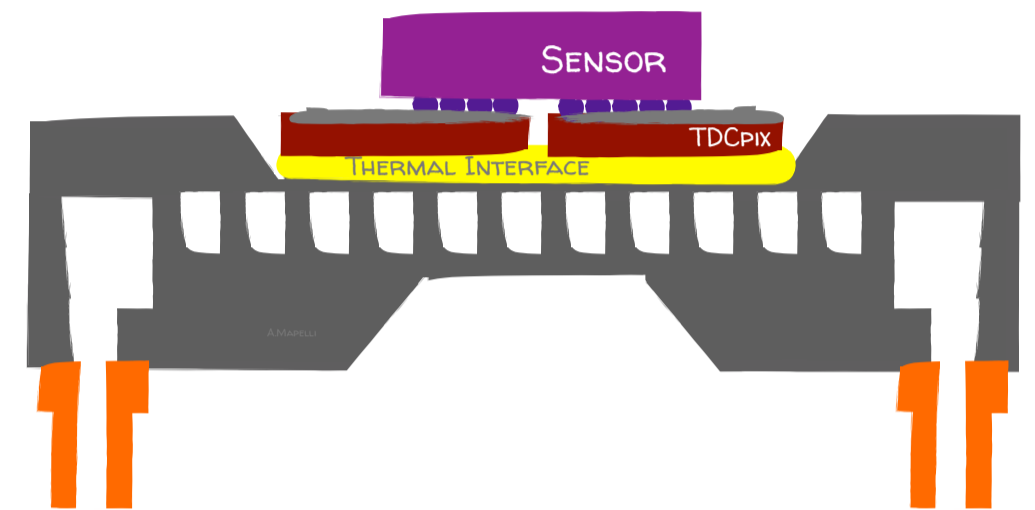
## Liquid Cooling C<sub>6</sub>F<sub>14</sub>

Nominal Power Dissipation 24 W

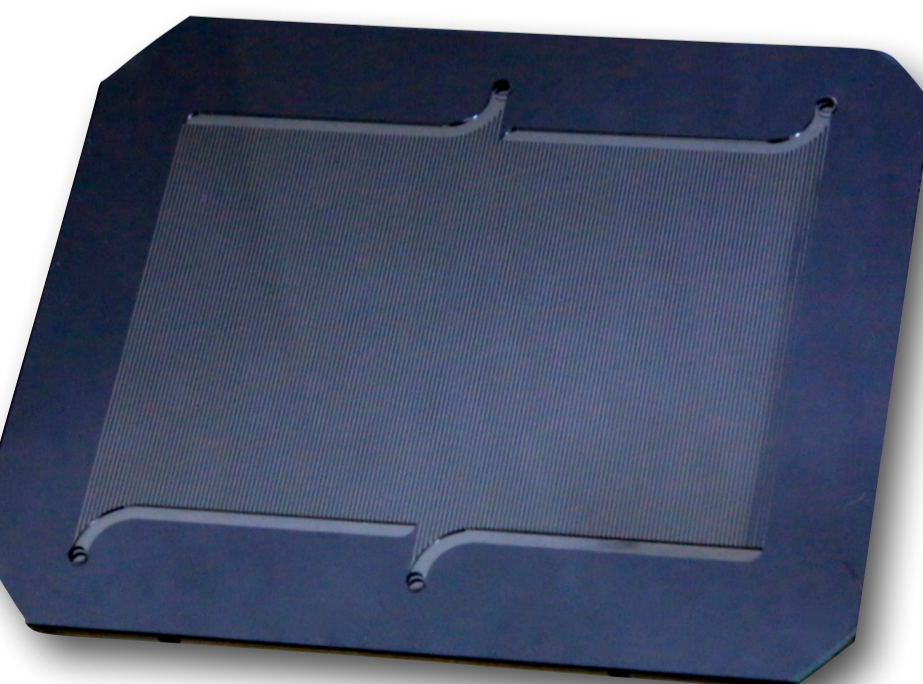
Results presented for extreme scenario 48 W



C<sub>6</sub>F<sub>14</sub>: 7G/s, -19°C AT INLET  
 DIGITAL POWER 38 W  
 ANALOG POWER 10 W



**SENSOR DUMMY**  
 200 μm THICK SI

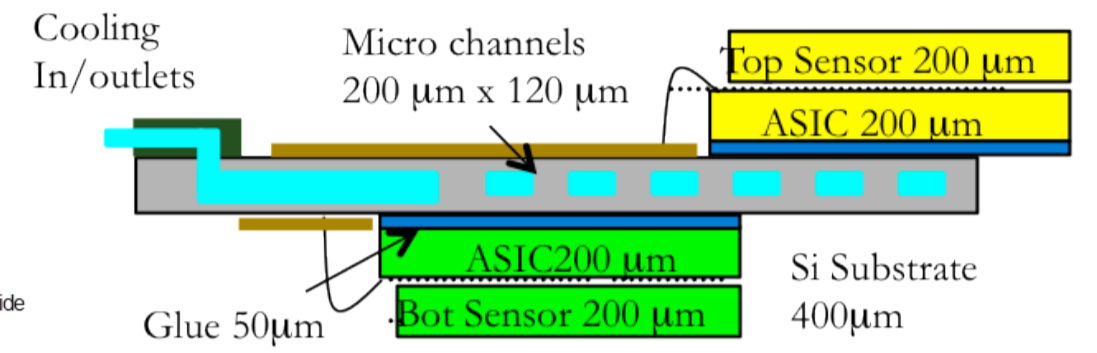
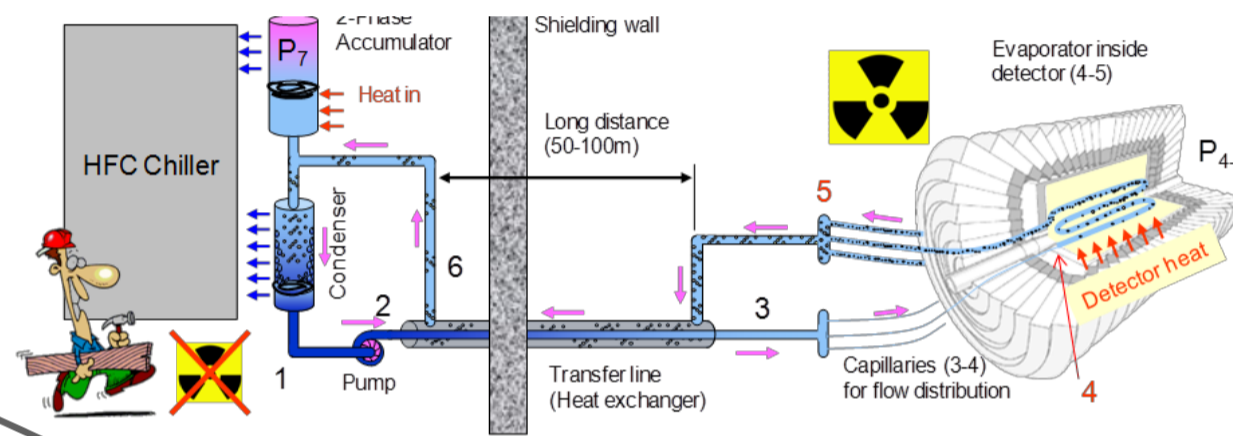
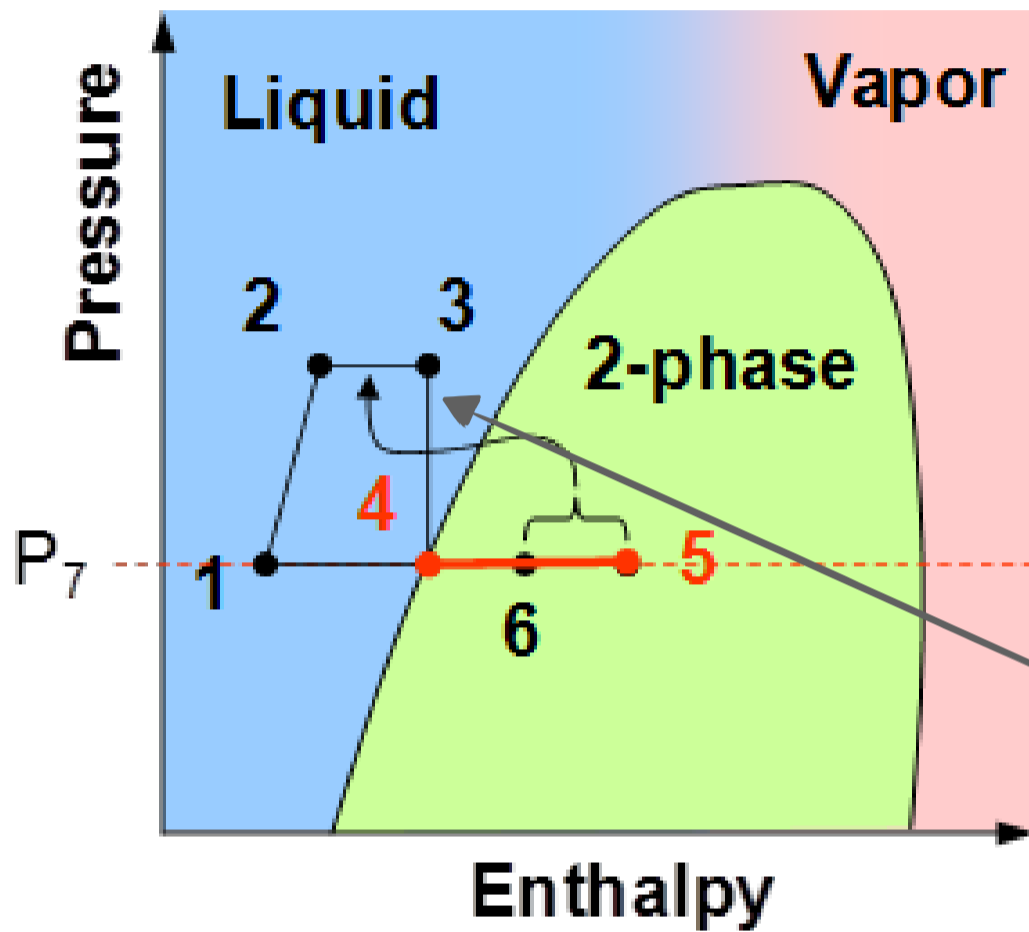


**COOLING PLATE**  
 150 μm THICK SI

**TDCPIX DUMMIES**  
 100 μm THICK SI  
 20 METAL LINES TO SIMULATE POWER DISSIPATION OF ANALOG AND DIGITAL PARTS OF 10 TDCPIX CHIPS

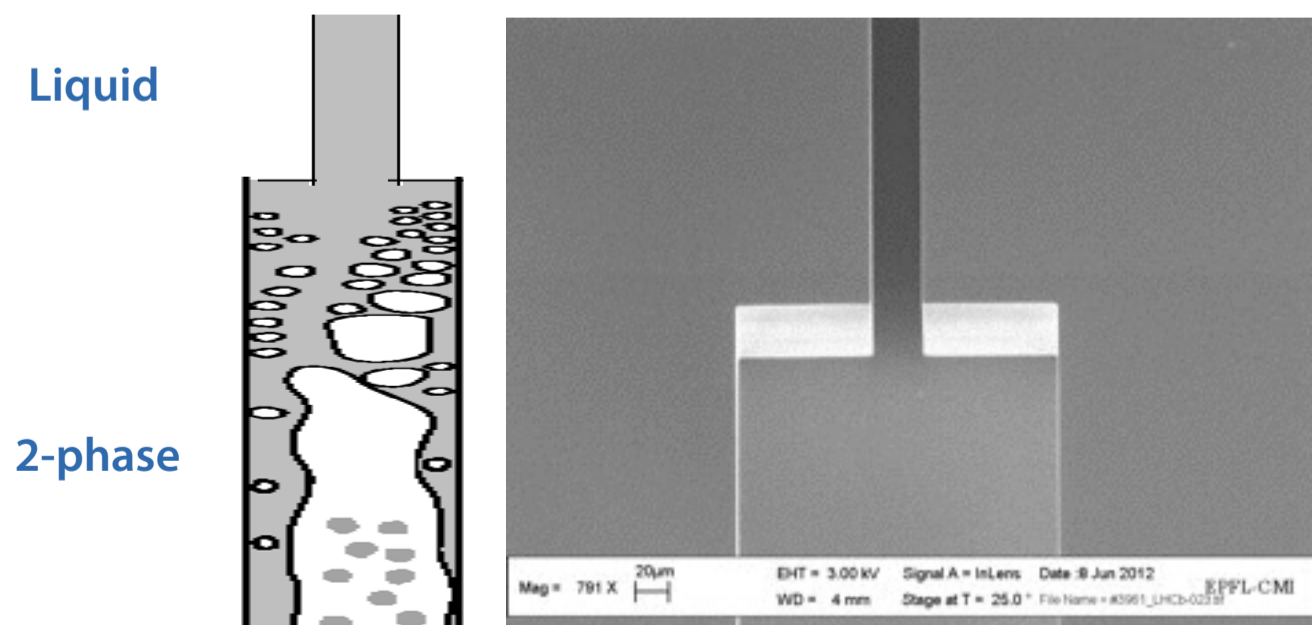
# LHCb VeLo Upgrade

## Evaporative CO<sub>2</sub> in silicon microchannels



Inlet Outlet

Inlet restrictions  
30 x 60 µm



Transition from inlet restrictions  
to evaporative microchannels



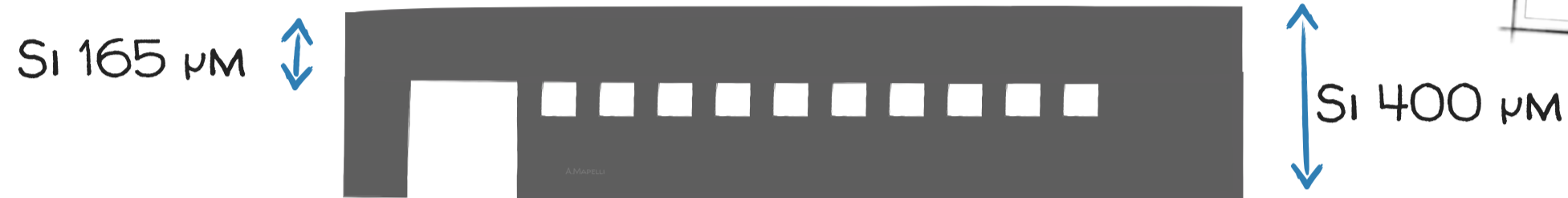
Microchannels  
200 x 60 µm



# pressure resistance

1. operating pressure at low temperature ~15 bar
2. pressure at room temperature start-up ~60 bar
3. validation pressure with safety factor ~150 bar

SAMPLES PRODUCED BY LETI-3S

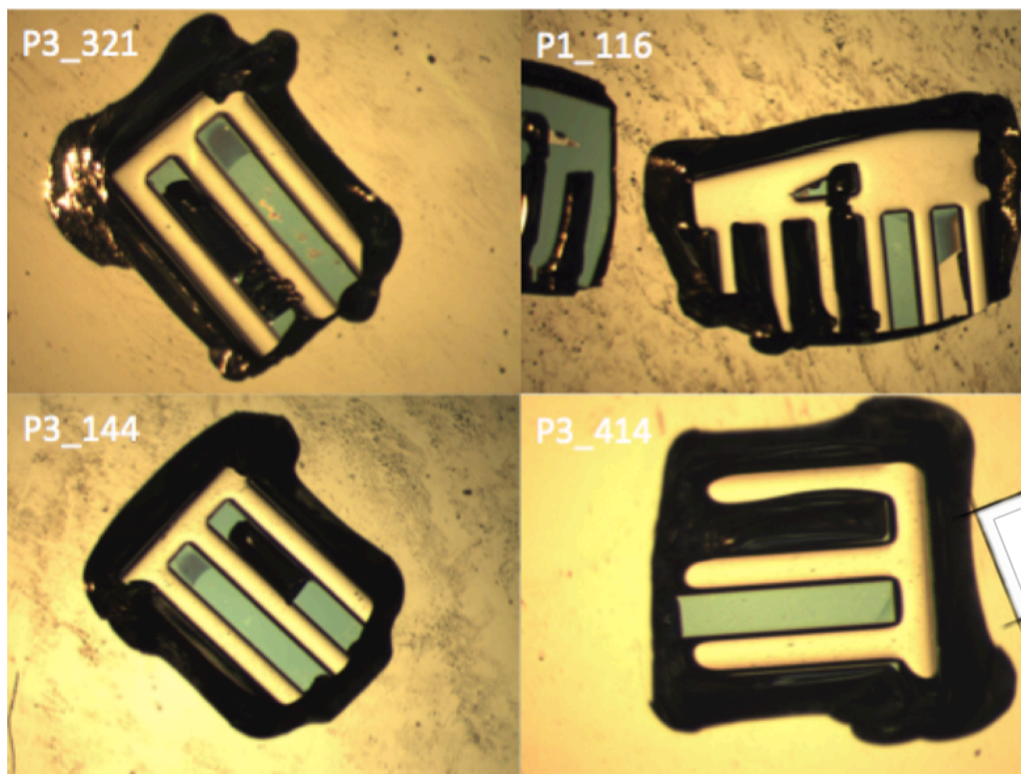
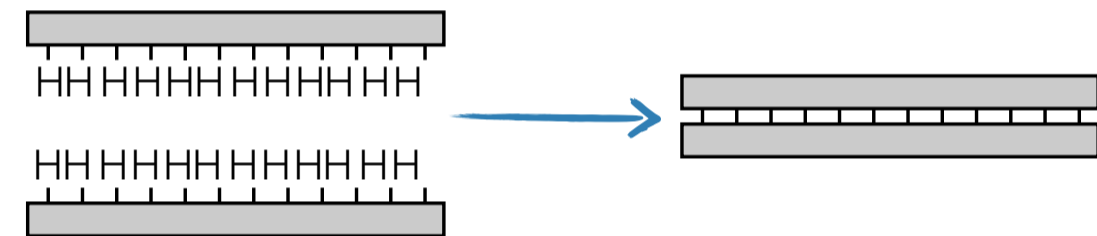


## Hydrophilic Bonding



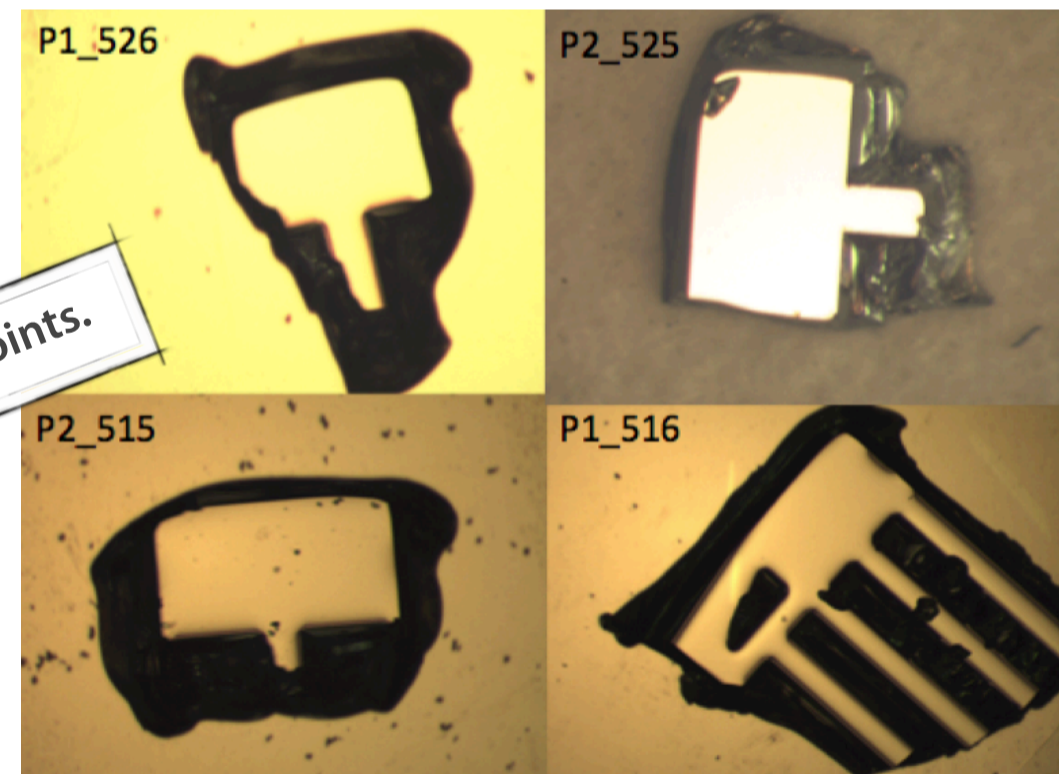
vs.

## Hydrophobic Bonding



Round 1

Manifolds are the weak points.



## Delamination + Si Rupture

Rupture at 400 bars due to delamination

Round 2

with improved connector over manifolds (R. Dumps)

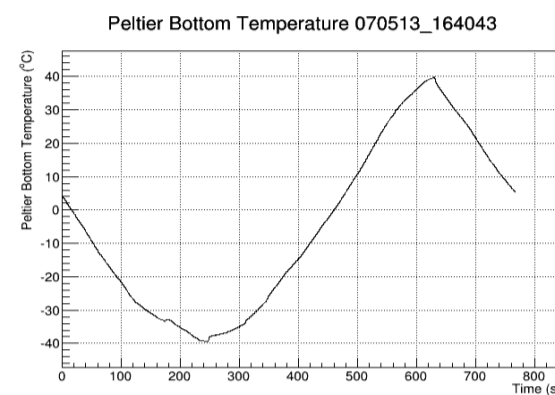
## No Delamination

**Hold 700 bars**

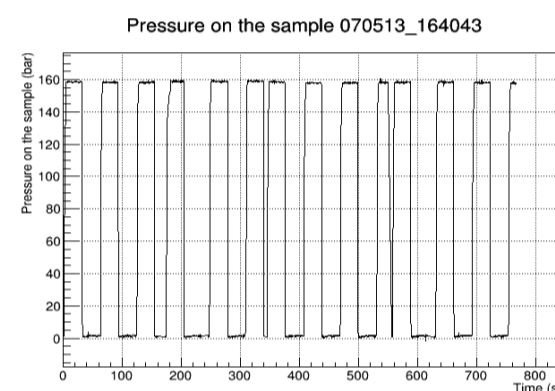
Limitation of pump

# long term cycling and qualification

- 14 pressure cycles during each temperature cycle

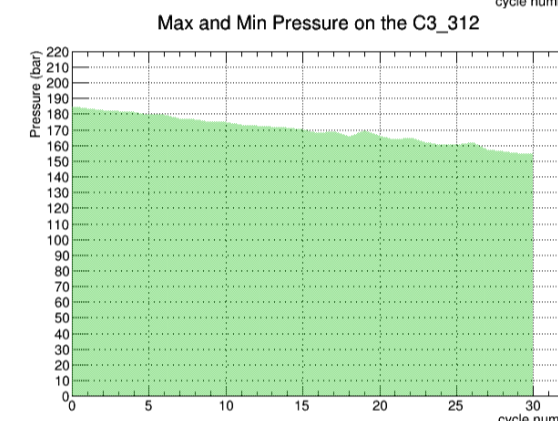
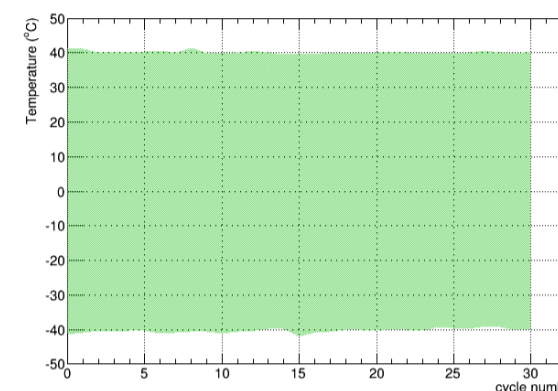


80°C range  
[-40°,40°]

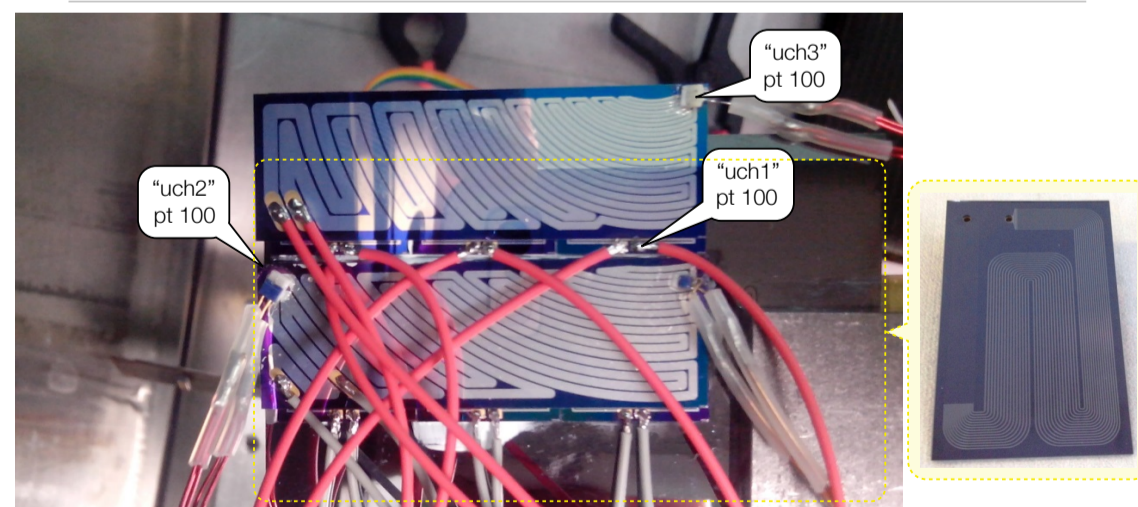


170 bar  
[0,185max]

Max and Min Temperature Pressure on the C3\_312 → ~7 hours



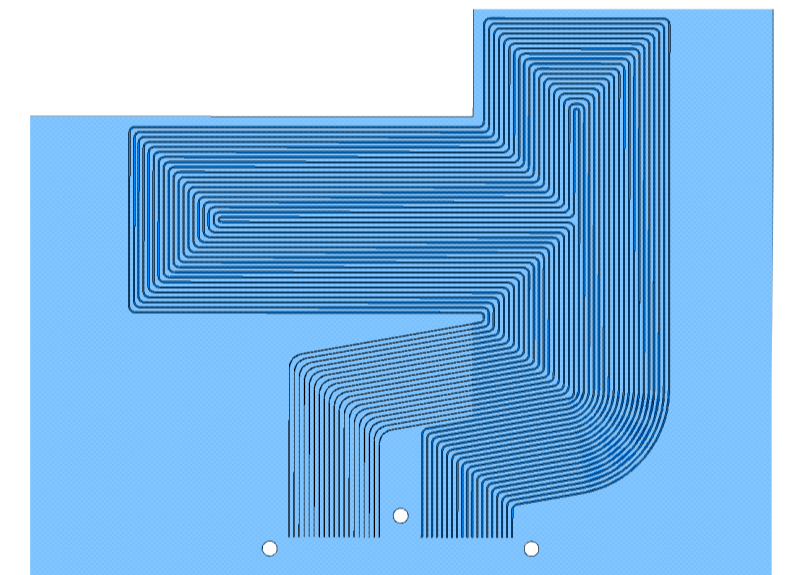
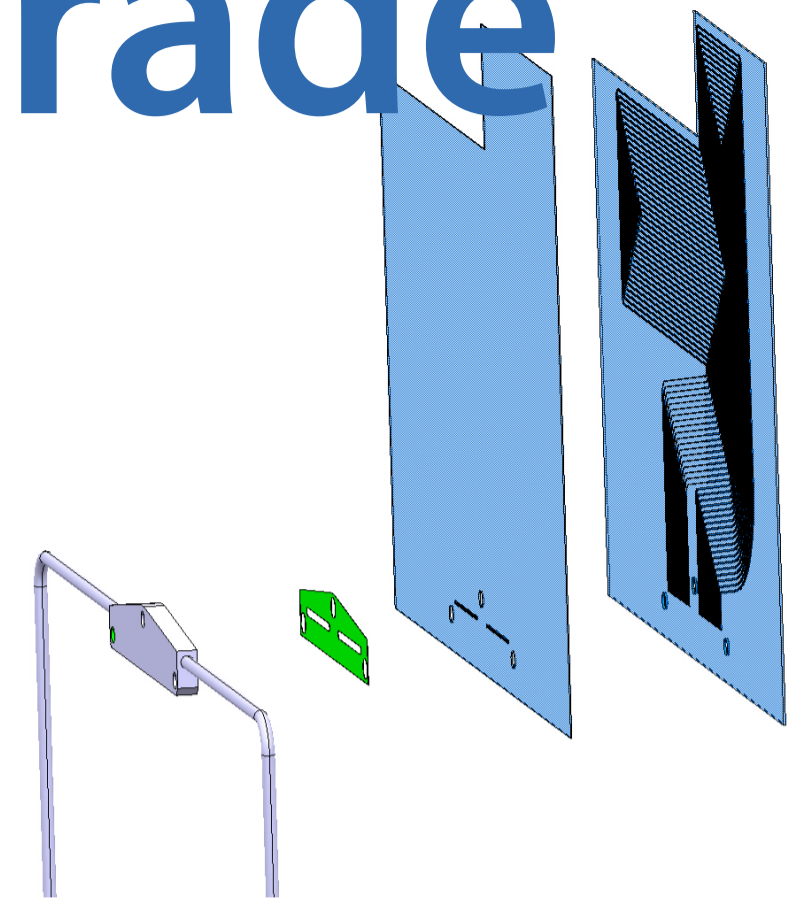
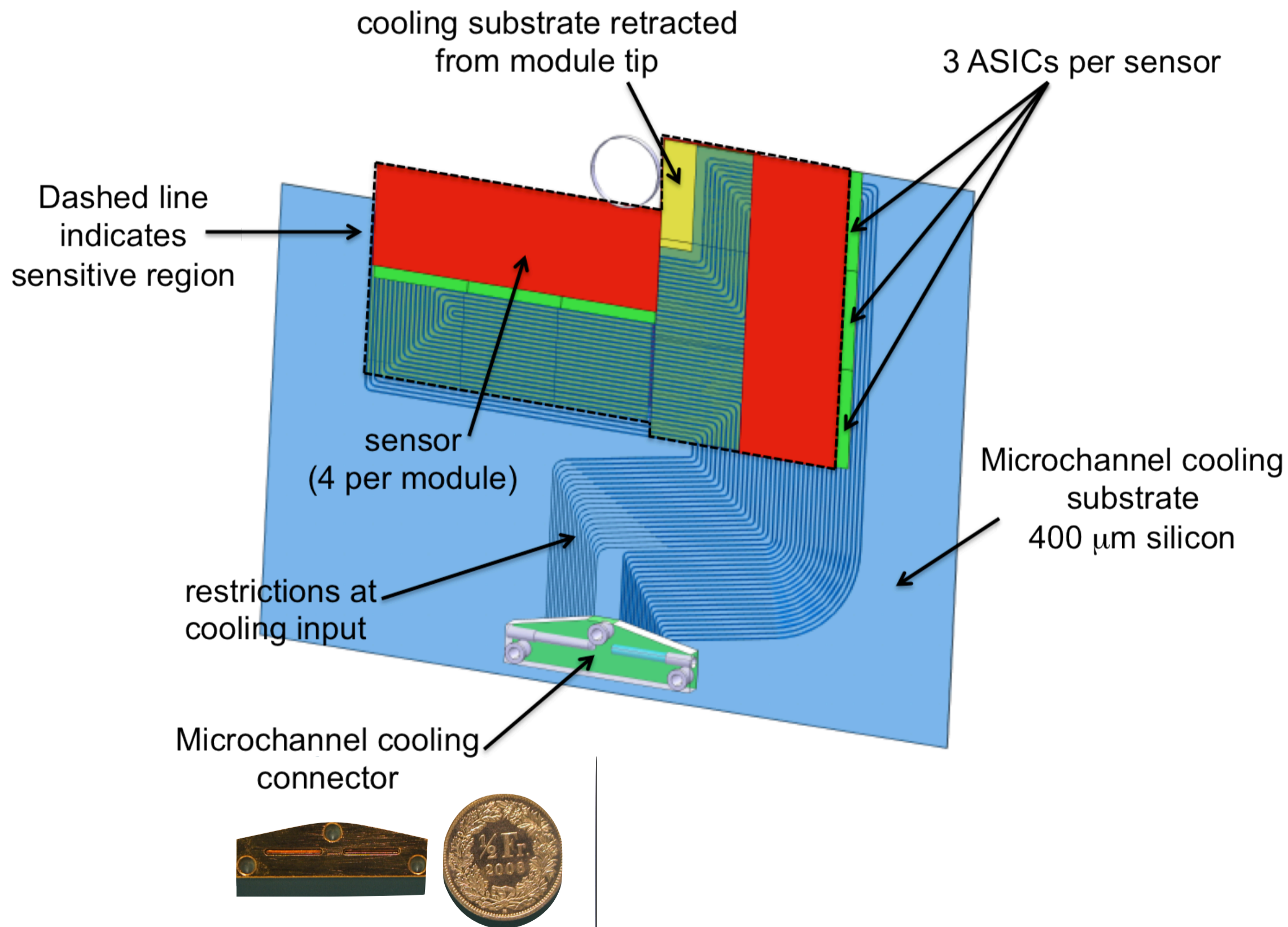
Example of sample tested over 30 cycles



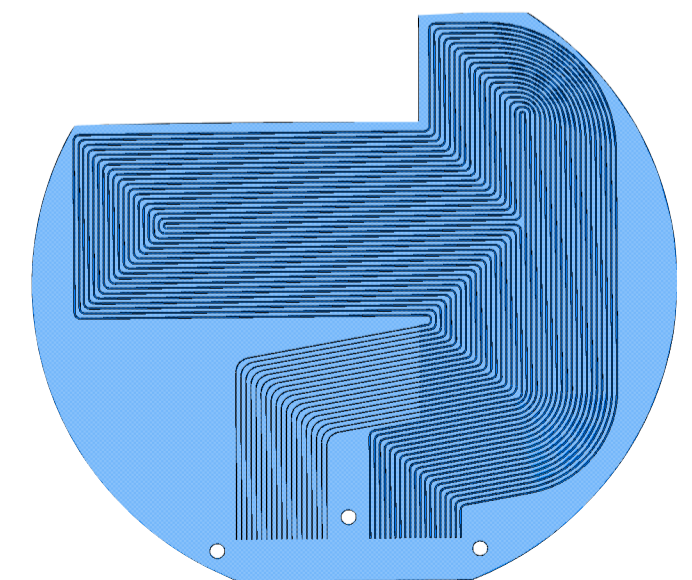
Required heat-sinking demonstrated with a 1/2 module mockup

# LHCb VeLo Upgrade

final design



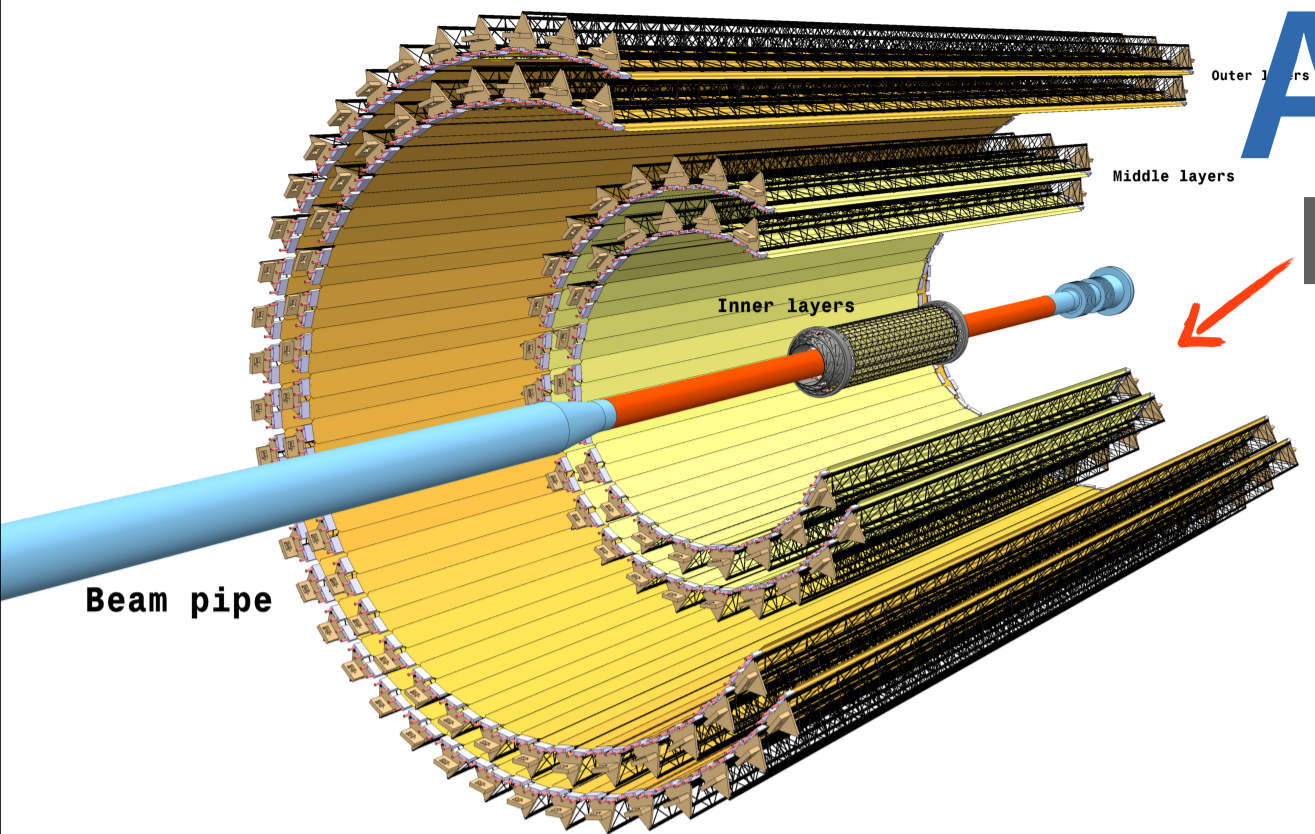
Fabrication by CEA Leti-3s



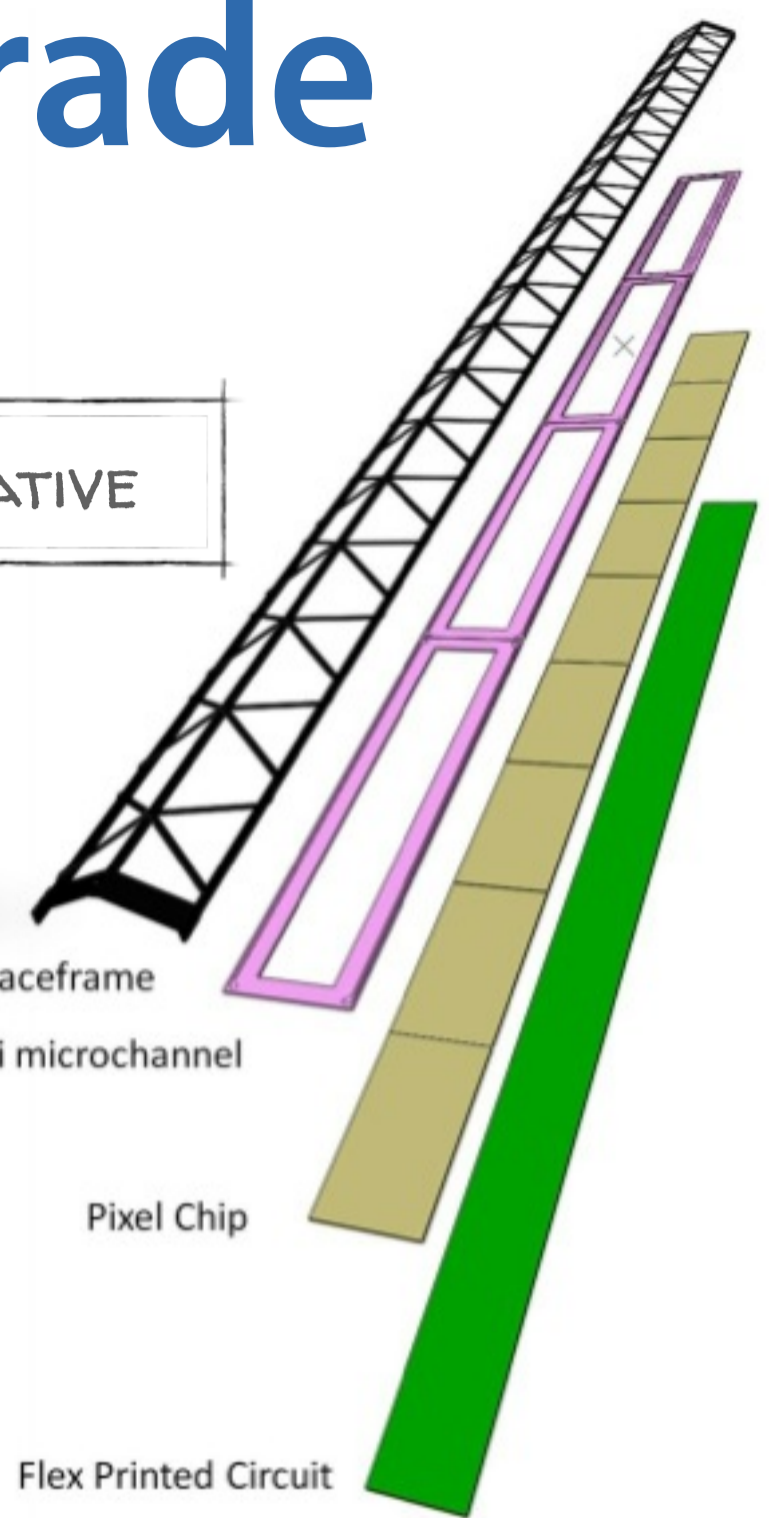
Prototyping at EPFL on 4" wafers

# ALICE ITS Upgrade

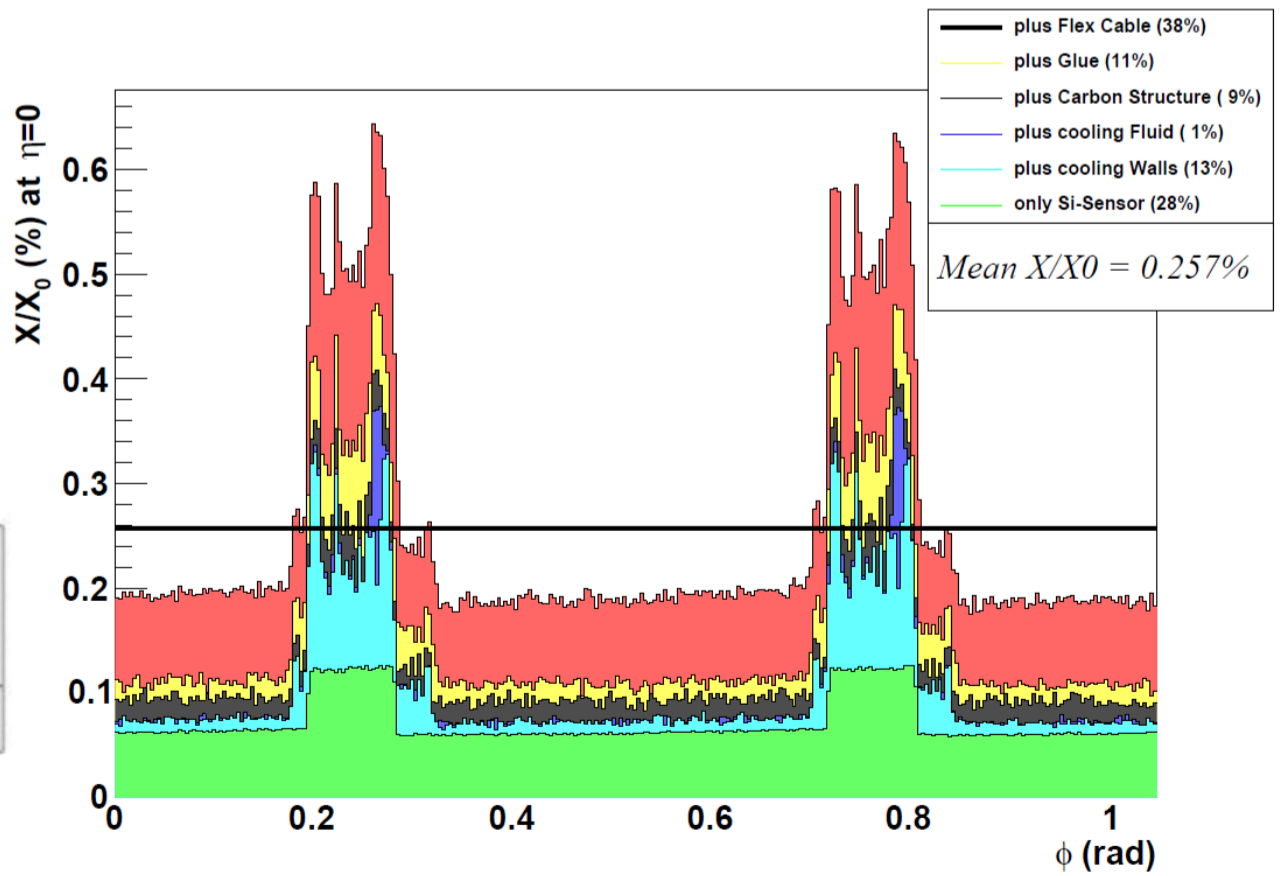
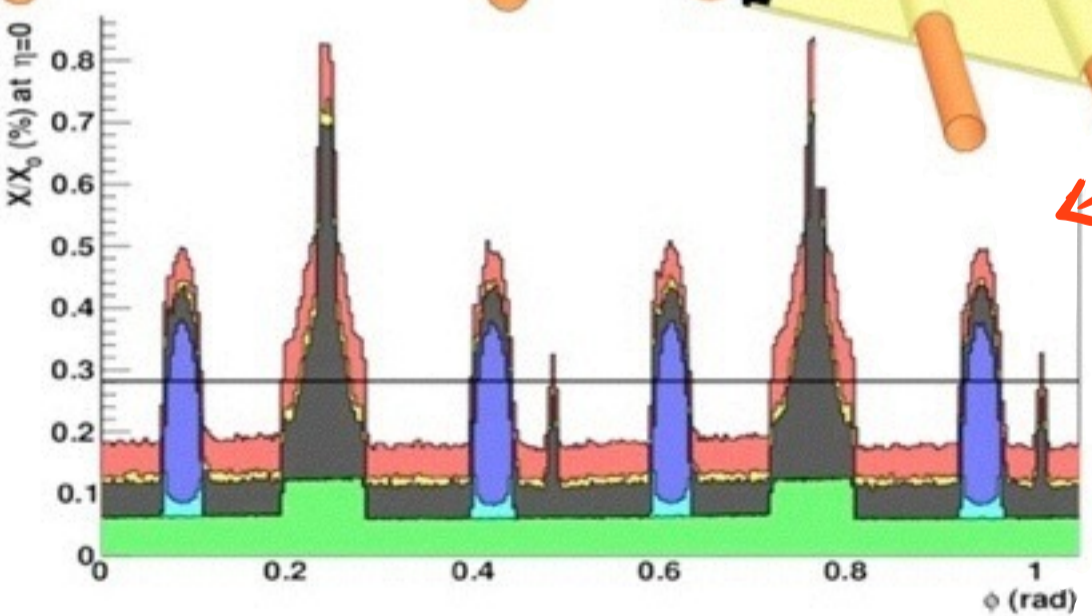
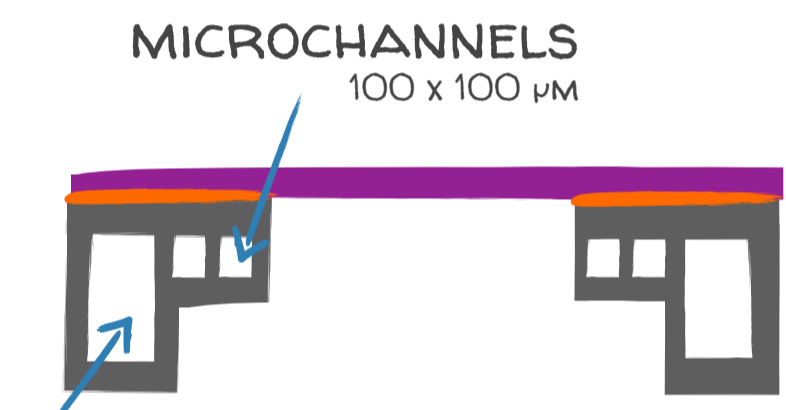
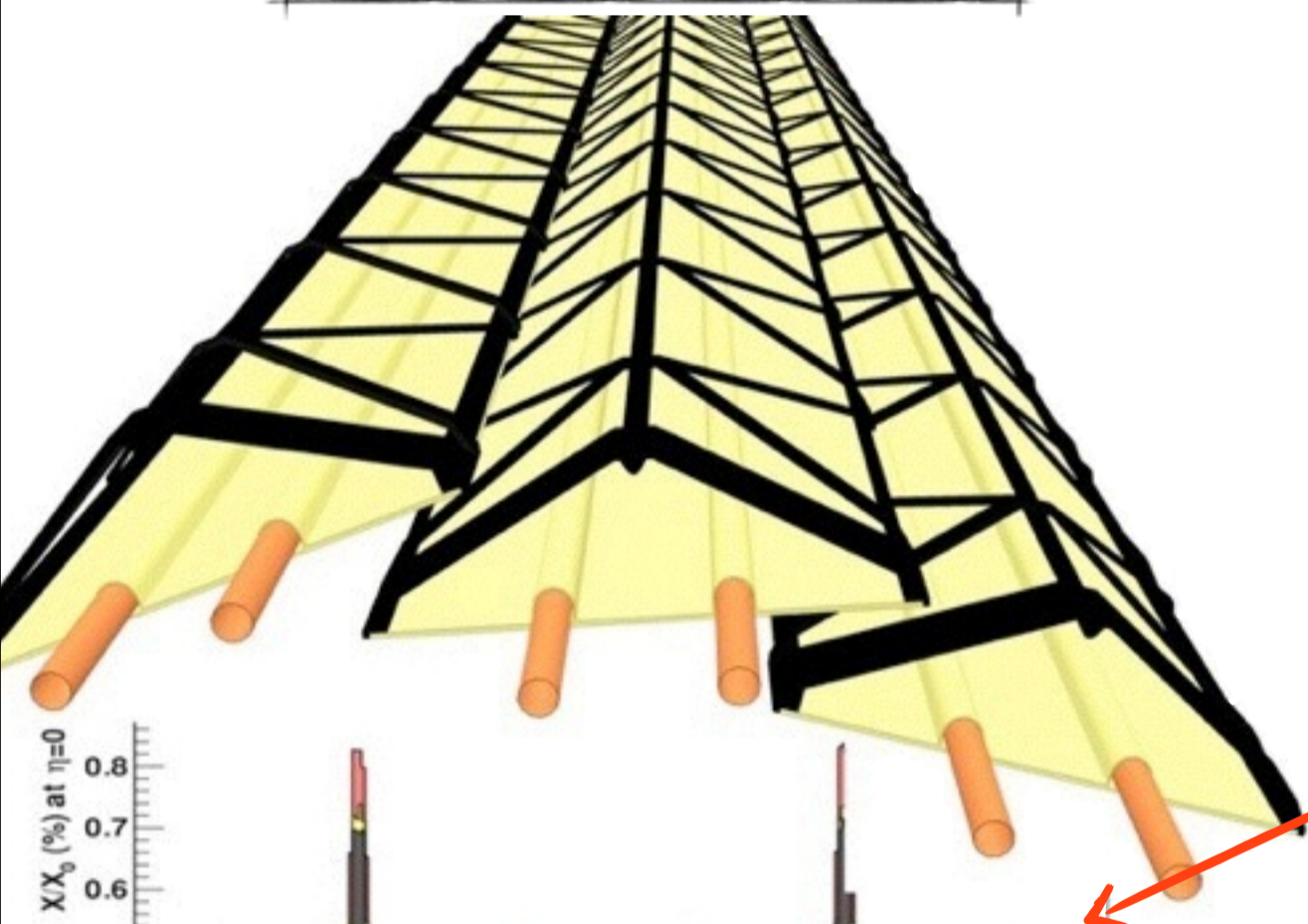
## Inner Layers



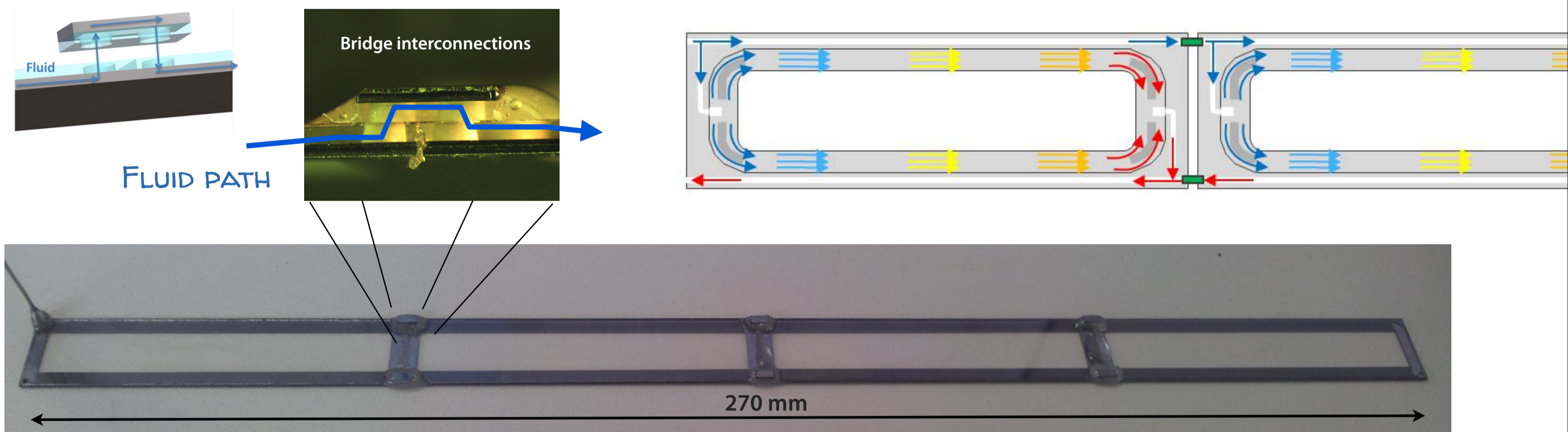
SILICON ALTERNATIVE



BASELINE SOLUTION  
*C. Gargiulo et al.*



# ALICE ITS Upgrade

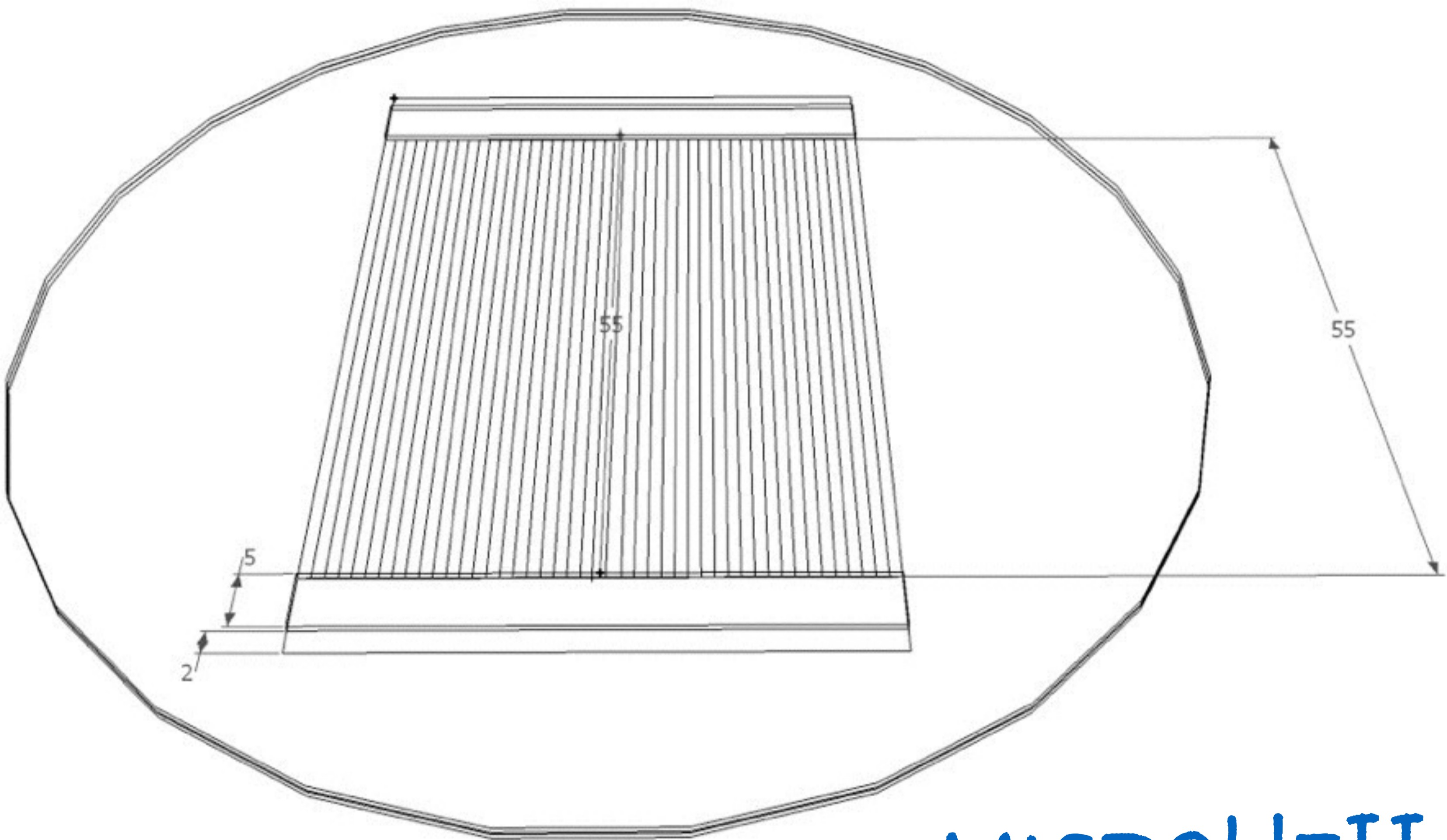


4 frames are required for a stave from 4" wafers.  
Only 2 frames required with single interconnection from 6" wafers (TMEC, Thailand).



9x silicon dummy chips with thin metal film (heater) glued on top of the stave.  
Thermo-fluidic preliminary tests have started demonstrating the principle of operation.

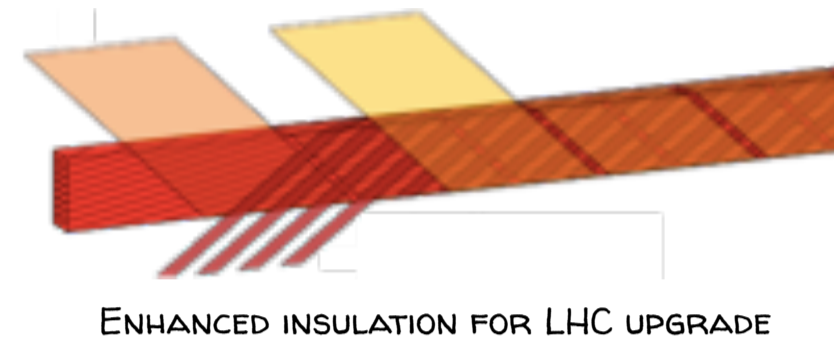
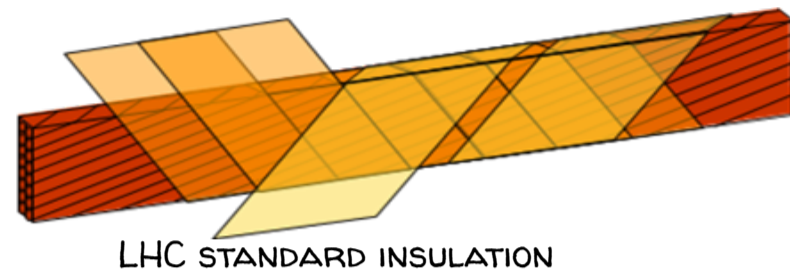
# HEAT TRANSFER OF SUPERFLUID HELIUM



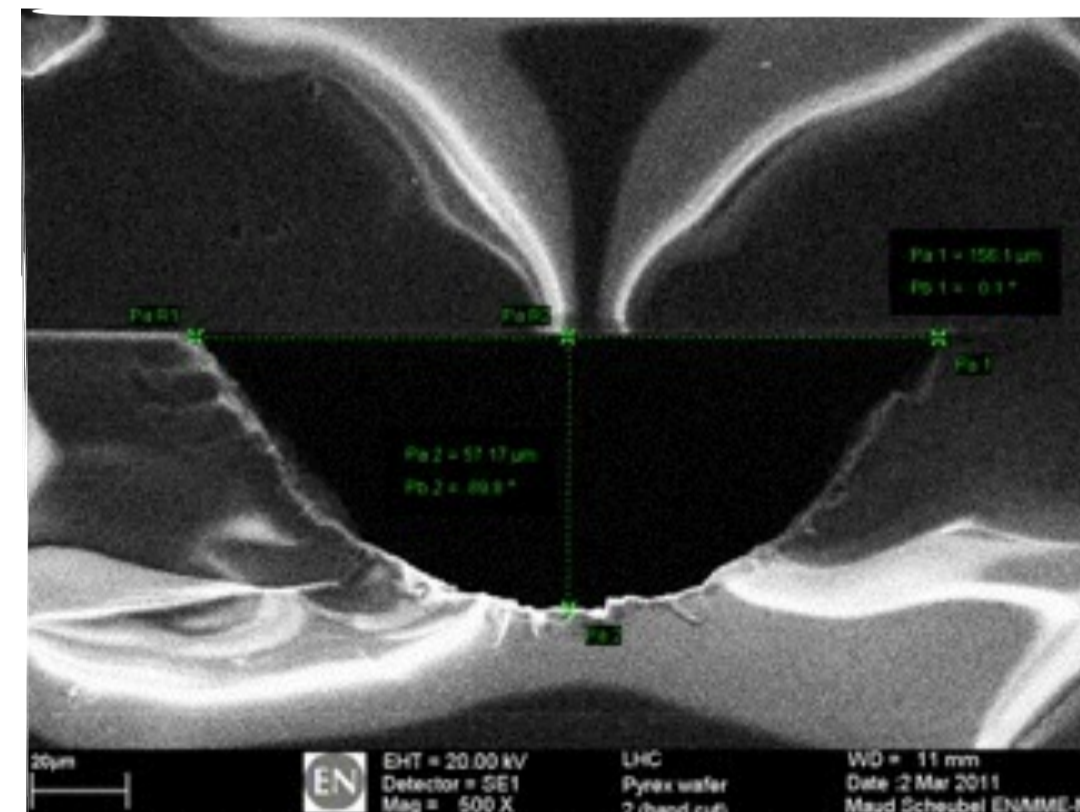
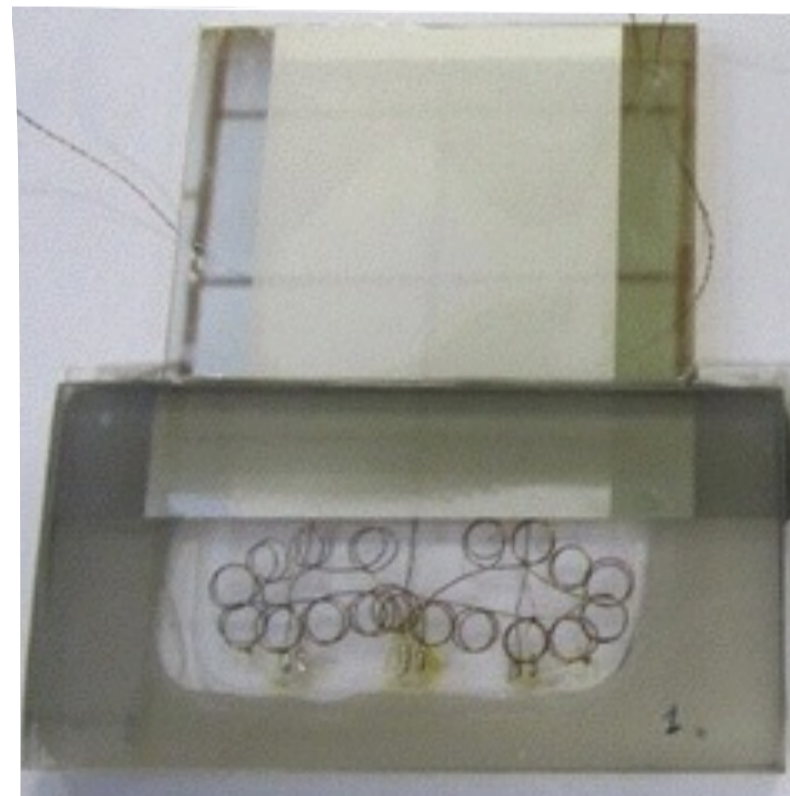
MICROHEII

# STUDY THE HEAT TRANSFER OF SUPERFLUID HELIUM II IN MICROCHANNELS

## THERMALLY-ENHANCED INSULATION OF LHC MAGNETS



Sample	MEMS technique	Number of channels	Characteristic dimensions ( $\mu\text{m}$ )	Total Channels Area ( $\text{mm}^2$ )	Length (mm)
1	Sandblasting	158	$\Phi_{\text{equivalent}} = 100.4$	1.25	55
2	HF etching	172	$17.15 \times 75.1$	0.22	55
3	DRIE etching	1000	$\sim 15.8 \times 24$	0.38	55



P. P. GRANIERI, ET AL., "STEADY-STATE HEAT TRANSFER THROUGH MICRO-CHANNELS IN PRESSURIZED HE II"  
AIP CONF. PROC., 1434 (2012) 231-238

# Conclusions

Microfabricated devices provide many advantages and potential applications for HEP.

Within the PH-DT group, microfabrication techniques have been successfully used for

- the development of novel particle detectors (microScint)
- alternative ways of integrating services (microCool)
- the investigation of heat transport of Hell channels (microHell)

A great effort still has to be undertaken to study and develop reliable connectivity solutions both in-plane and out of plane.



