

# VMM Update

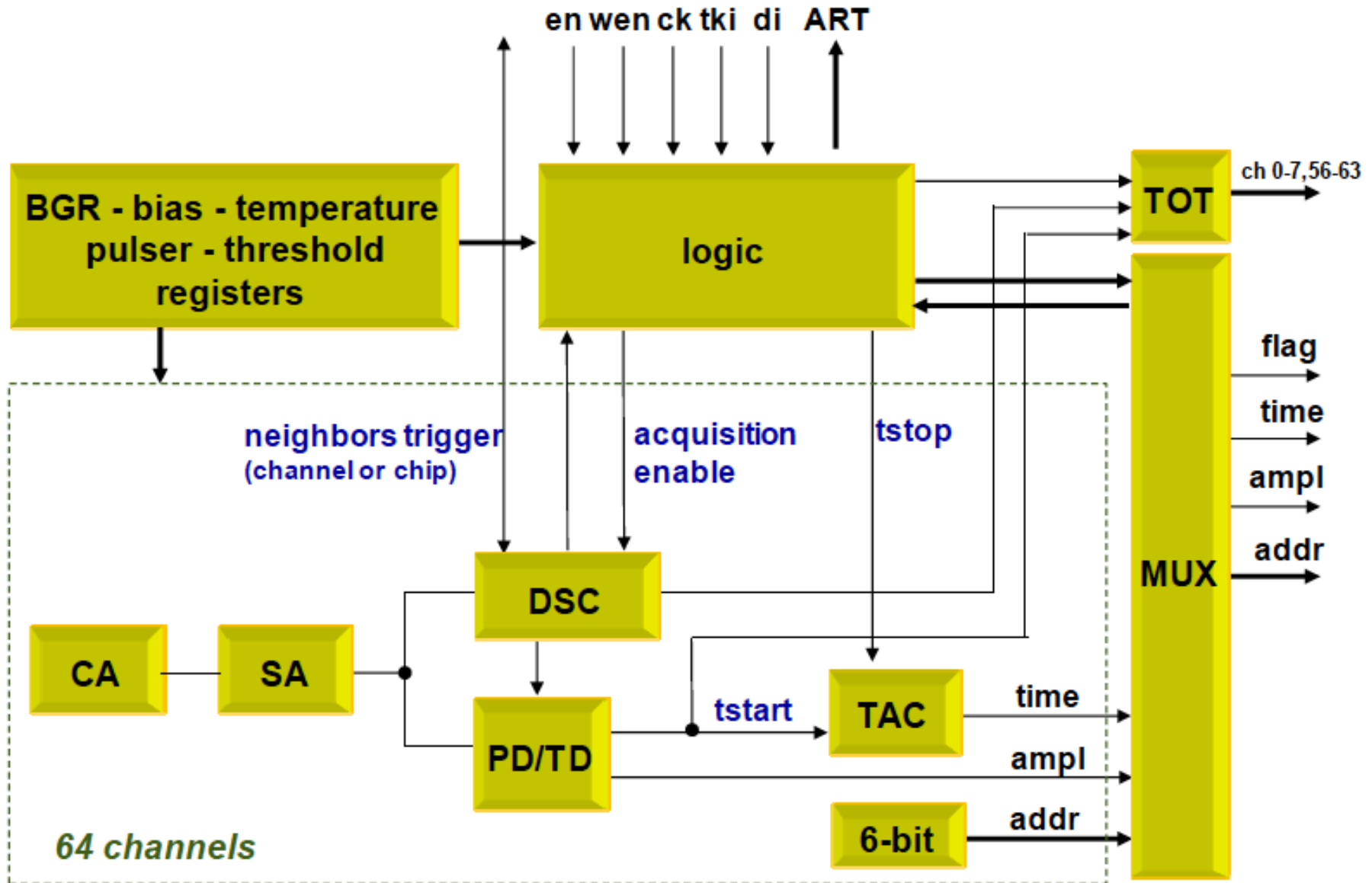
## Front End ASIC for the ATLAS Muon Upgrade

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BNL

# Design Parameters/Features

- Dual Polarity
- Adjustable Gain (0.5 – 9.0 mV/fC)
- Adjustable peaking Time (25-200 ns)
- Address in Real Time (Fast OR in effect - Mmegas Trigger)
- Prompt digitized (6-bit) Amplitude, Time-over-threshold, time-to-peak (TGC Trigger)
- Peak Detector, Time Detector (<1 ns)
- Discriminators with sub-hysteresis
- Neighbor enable logic (channel to channel and across lcs)
- Sparse readout w/smart token passing,
- Threshold trim, built-in calibration, channel mask, analog monitor, temp. sensor, 600 BGR, 600 mV LVDS

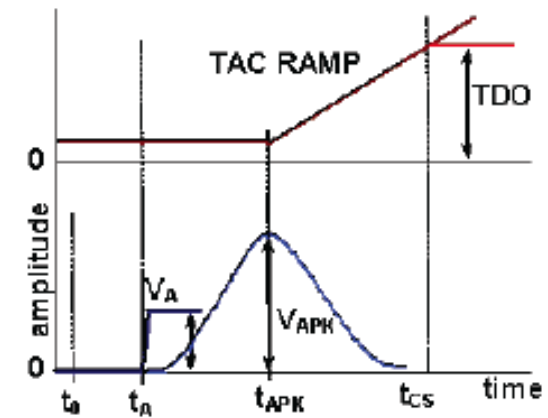
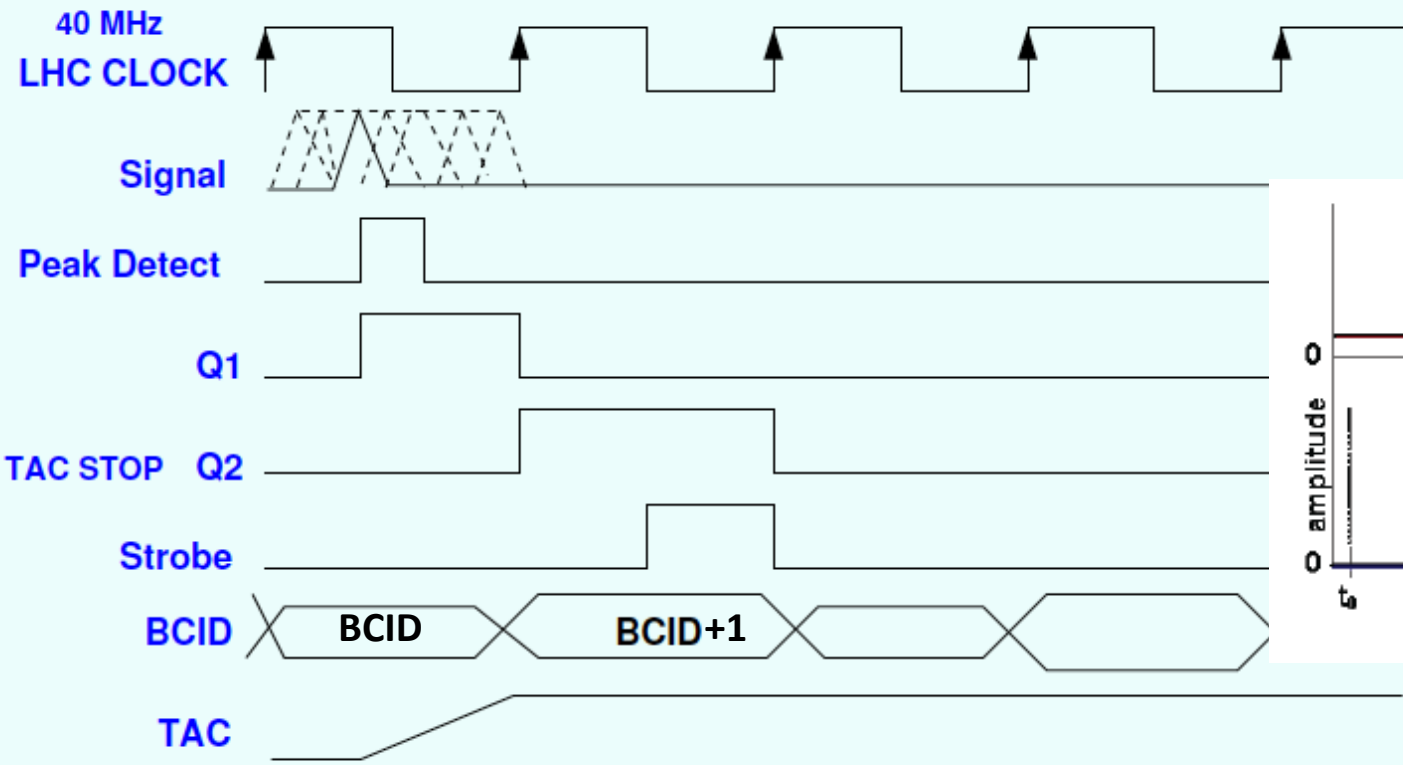
# VMM1, First Version, 64 channels, fully functional analog front end, Amp, Timing analog multiplexer outputs



# Signal Processing Concept

- Discriminators → Data driven front end
  - Zero suppression
- Neighbor Logic (channel to channel and across chips) allows processing below threshold signals
- Peak Detector provides signal amplitude
- Peak timing with negligible time walk and excellent resolution
- Discriminators with sub-hysteresis feature allow trigger at a few mV above baseline

# Timing



Start of live spill triggers 40 MHz clock

Time to Analog converter starts at "peak found", marks the hit time wrt leading edge of BCID

TAC stops at rising edge of BCID+2 (125 ns ramp)

TAC amplitude digitized by 8-bit ADC

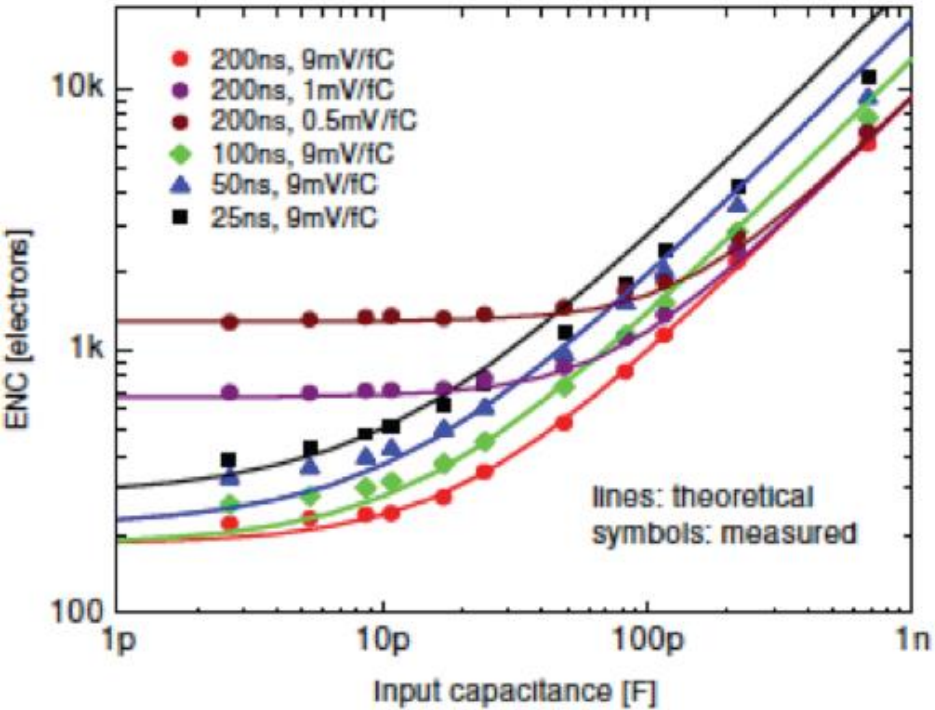
HIT time =  $BCID \times 25 + ADC \times 125 / 256$  [nsec]

BCID and ADC are stored in buffer

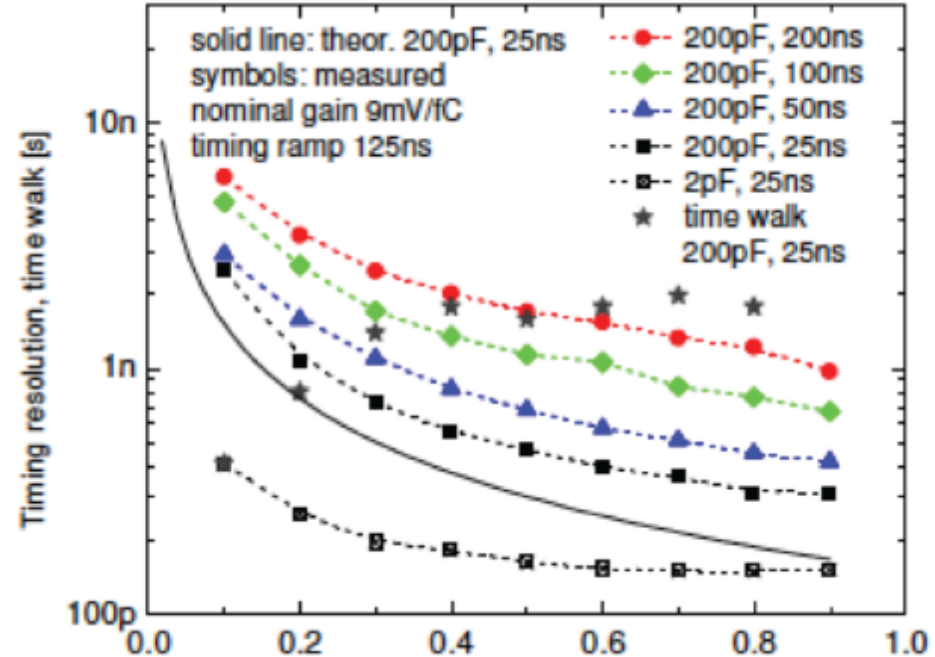
Process repeated for subsequent hits

10/15/13 Could do away with ramp, have, e.g., 200 MHz clock and just record BCID count (5 ns resolution)

# Examples of VMM1 performance

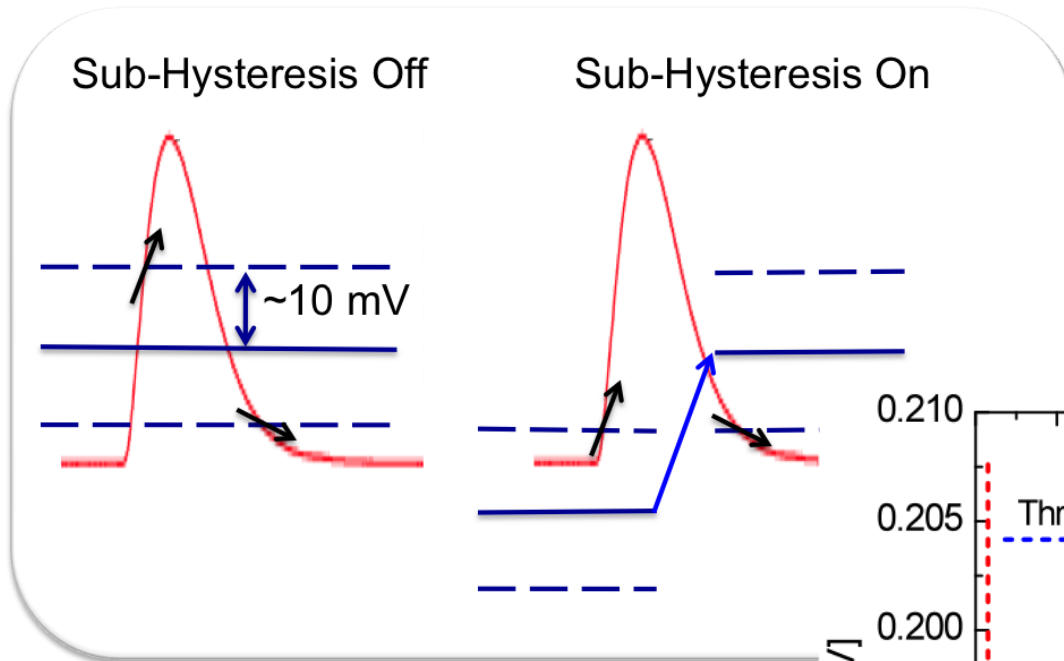


ENC as a function of input capacitance  
 $< 1\text{fC}$  even with fast shaping (25 ns) and  
 large input capacitance (200 pF)

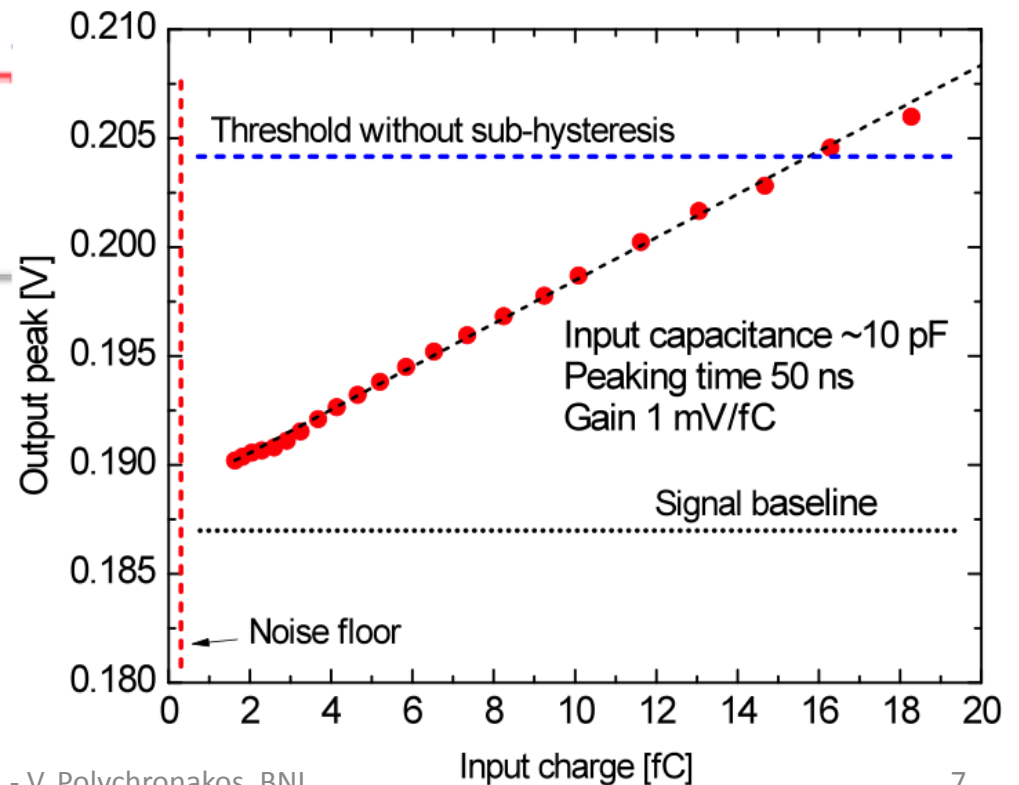


Time resolution as a function of  
 amplitude  $\sim$  ns resolution and timewalk

# Sub-hysteresis allows trigger at very low Amplitudes



Allows setting trigger threshold at 1 or 2 primary electrons

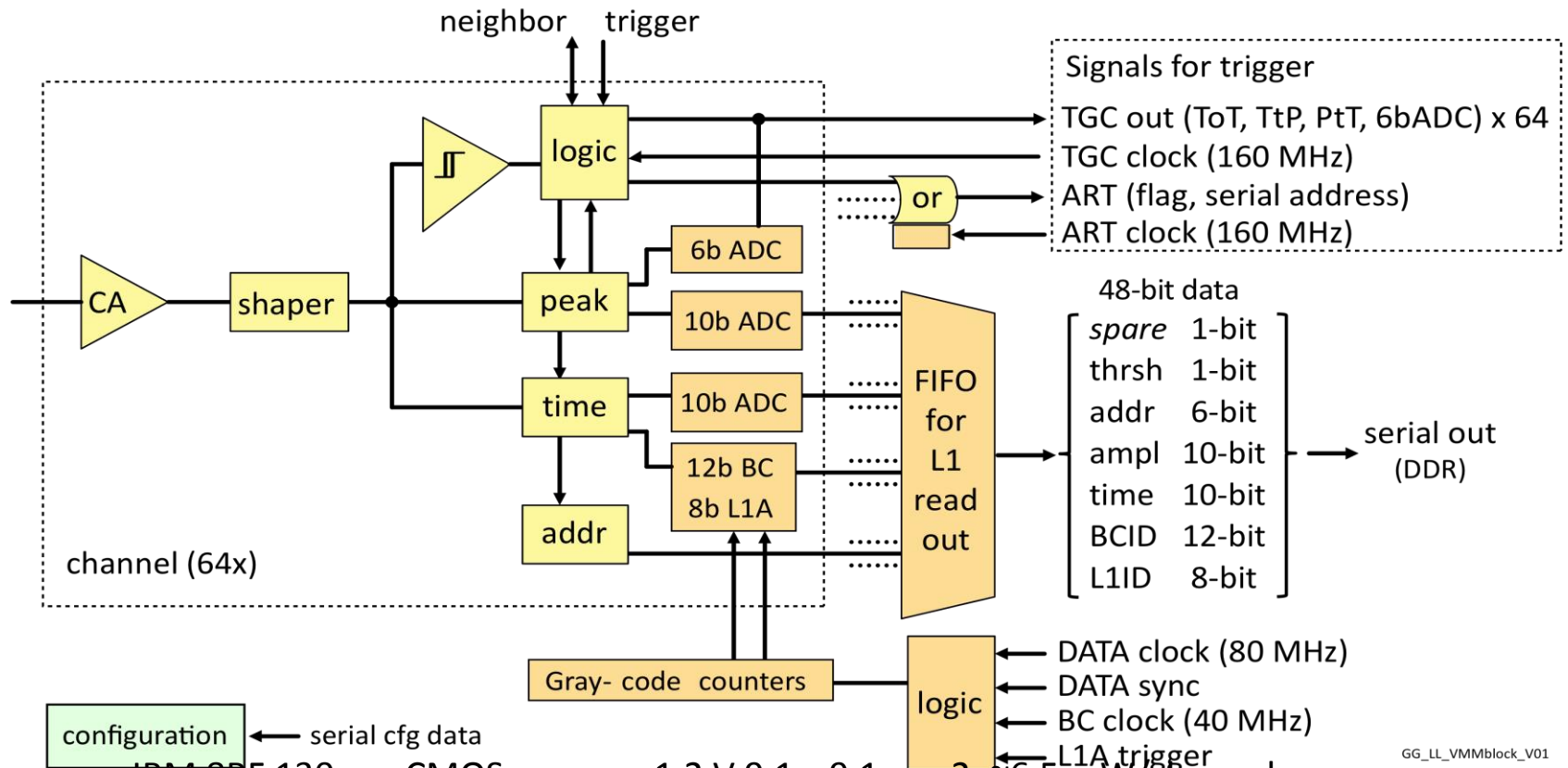


# The Second version of the ASIC (VMM2)

G. De Geronimo, BNL Instr. Div.

- Fixes issues (mostly minor) of the first version
- Includes 10-bit digitizers for amplitude and timing (200 ns)
- Includes a 6-bit Amplitude digitizer at ~40 ns conversion time
- Includes 4 word buffer, simultaneous read/write, can continuously be read out at both phases of 200 MHz clock in DDR mode → 800 Mbps

VMM Architecture



IBM 8RF 130 nm CMOS process, 1.2 V 9.1 x 9.1 mm<sup>2</sup>, ~6.5 mW/channel

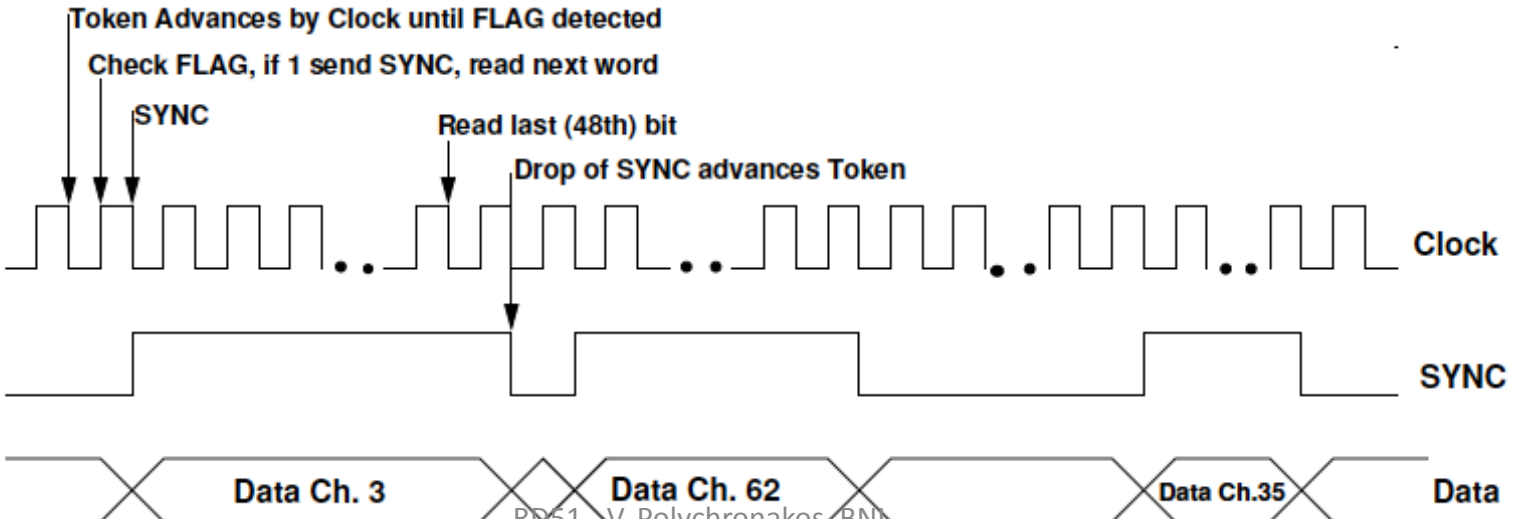
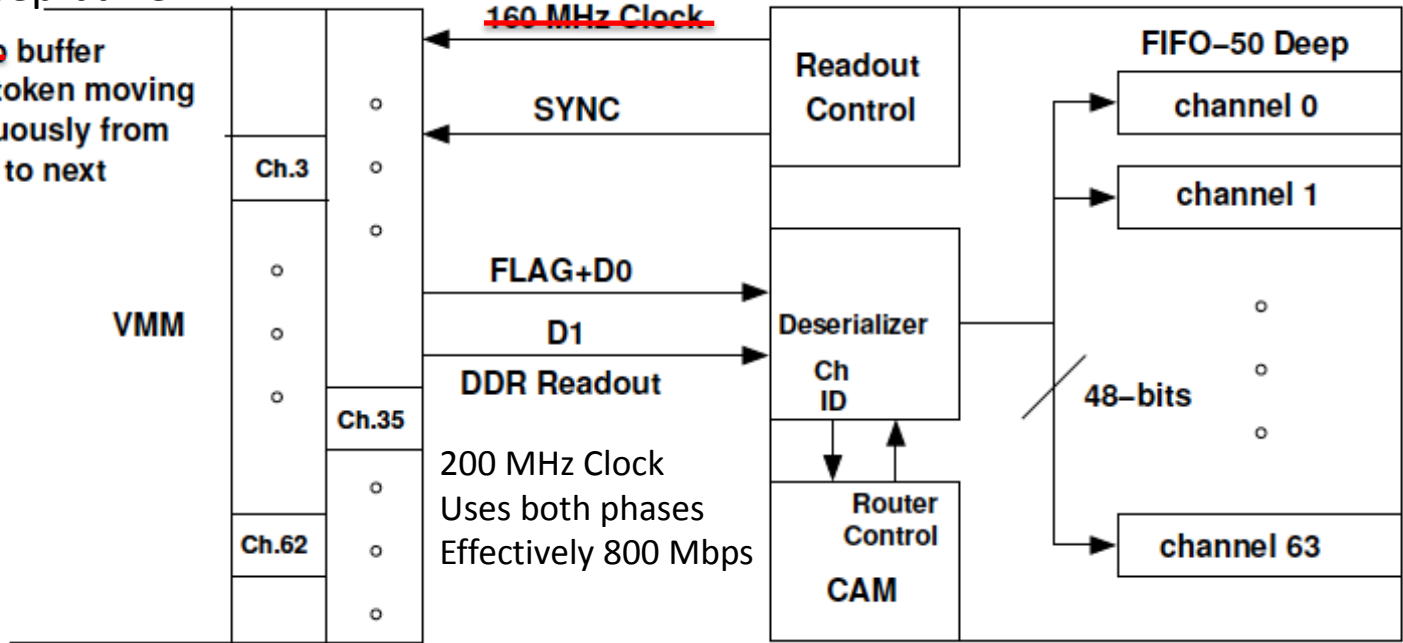
GG\_LL\_VMMblock\_V01



# VMM2 Readout (May be modified in final version)

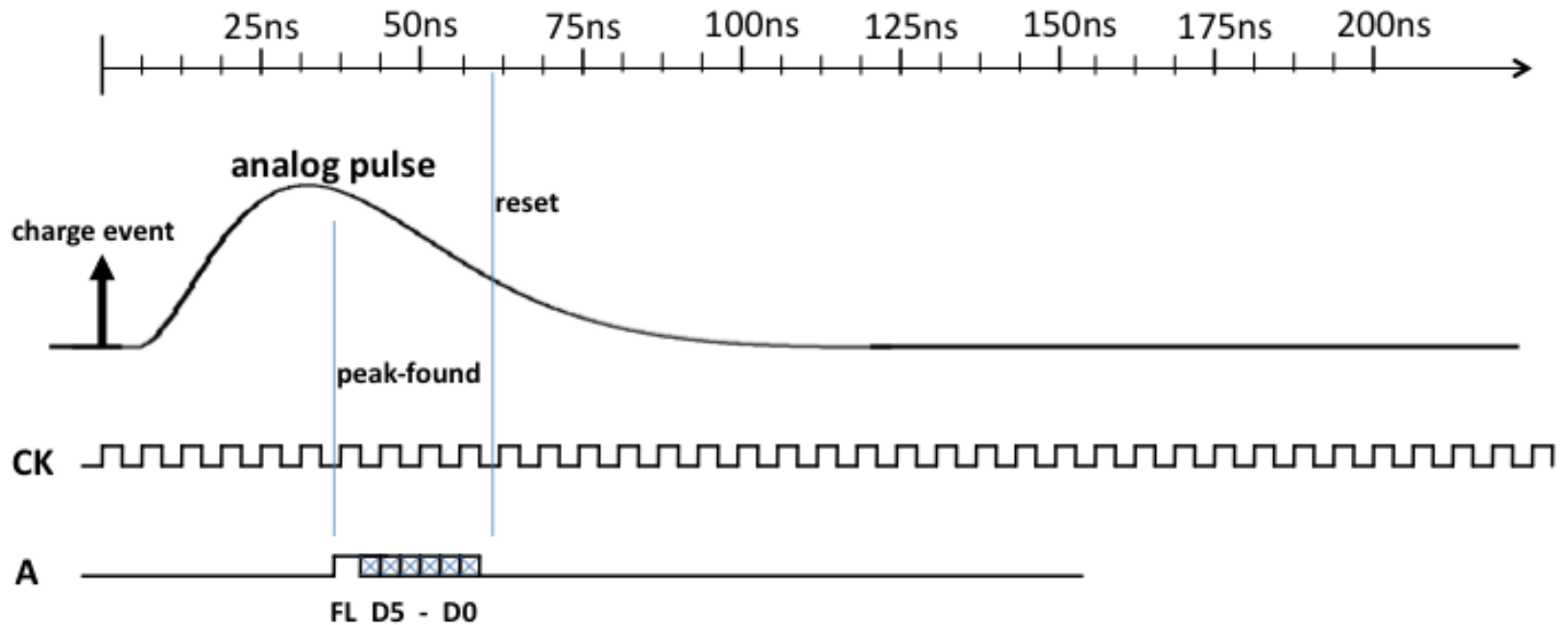
4-deep buffer

~~2-deep~~ buffer  
Smart token moving continuously from 1 word to next



# Trigger Feature 1- Address in Real Time (ART)

## VMM1 ART SERIALIZER - v2



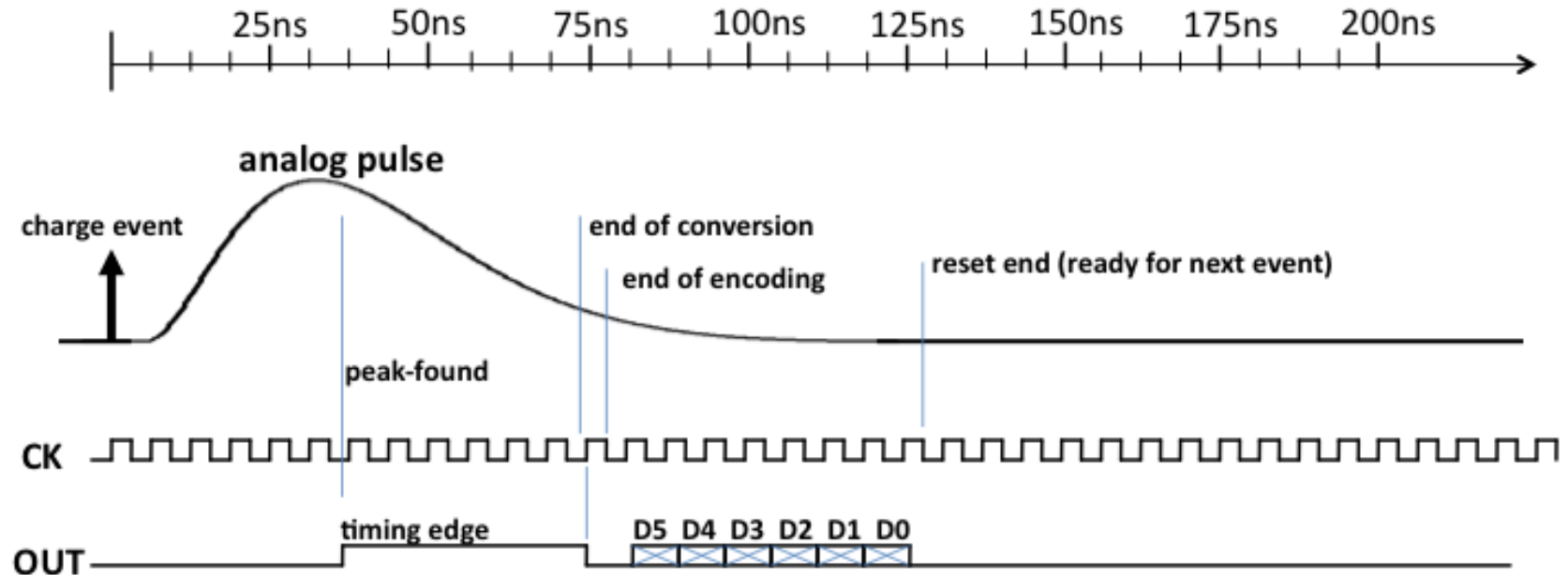
**Assumes 160 MHz clock provided externally**  
**ART serialized in one line A**  
**Data D5-D0 shifted at each clock edge**  
**LVDS 600mV +/- 150mV**

At every bunch crossing ART provides the 6-bit address of the channel with the earliest signal above threshold

Can be used as a fast OR

# Trigger Feature 2- Prompt 6-bit amplitude per Channel

## VMM1 FAST DIGITIZER PER CHANNEL



**Assumes 160 MHz clock provided externally**  
**Conversion starts at pulse, ends ~50ns after peak**  
**Dead time from charge event ~125ns**  
**LVDS 600mV +/- 150mV**

# Summary, Schedule - Availability

- VMM2 design completed about a month ago
- Layout, simulations in progress, expect to be completed end of November (next MOSIS MPW run)
- VMM is a very large chip (~ 100 sq.mm), cost 230 k\$US/40 samples!
- Decided to go for a dedicated run (450 k\$US) sharing the wafer with a smaller BNL ASIC which will reduce the cost by ~ 100 k
- The cost above includes processing of 6 wafers, ~800-1000 chips
- Chips available ~May 2014 if submitted in early December
- Package in BGA 350 pins (21x21 mm<sup>2</sup>)
- In the process of applying for Commerce Department export license
- What remains for the final version is SEU mitigation logic and final decision on digital buffer size and management
- Several Readout boards for ATLAS under development, SRS compatible hybrid under discussion