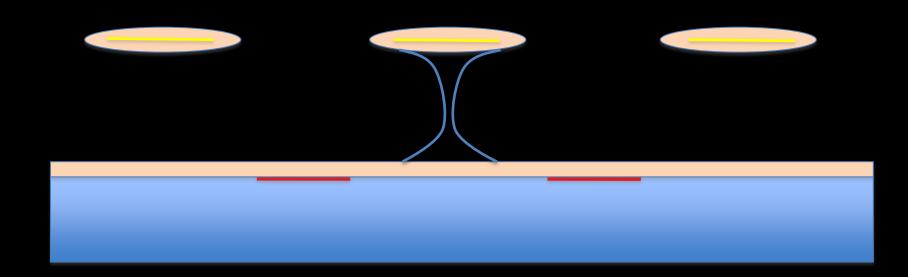
GridPix:

- the all-ceramic InGrid
- TimePix-3
- the Quad Focus chamber
- Q64

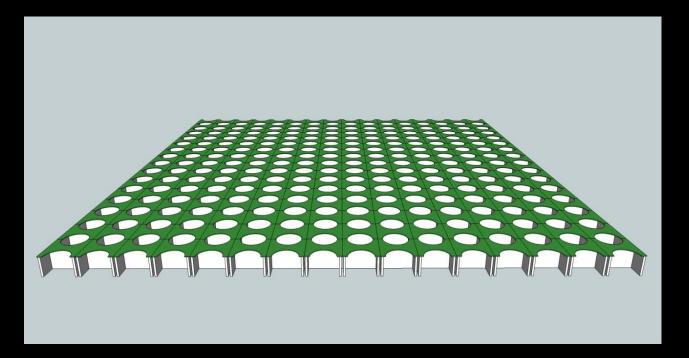
Harry van der Graaf Nikhef/TU-Delft

RD51 Workshop WG 1, CERN, Oct 16, 2013

The all-ceramic InGrid: Yevgen Bilevych & Hong Wah Chan @ IZM-Berlin



- Double Discharge Protection (like RPCs)
- thermal expansion coefficient as Si: cryogenic applications
- no outgassing (LAr & LXe TPCs)

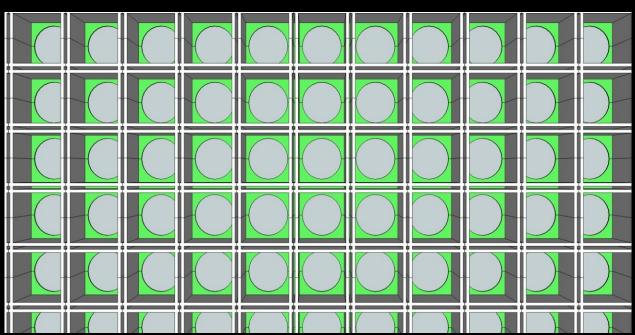


First:

all-ceramic Micromegas

Discrete component to be mounted on TimePix (-3!) chip

Later: intergration: all-ceramic InGrid

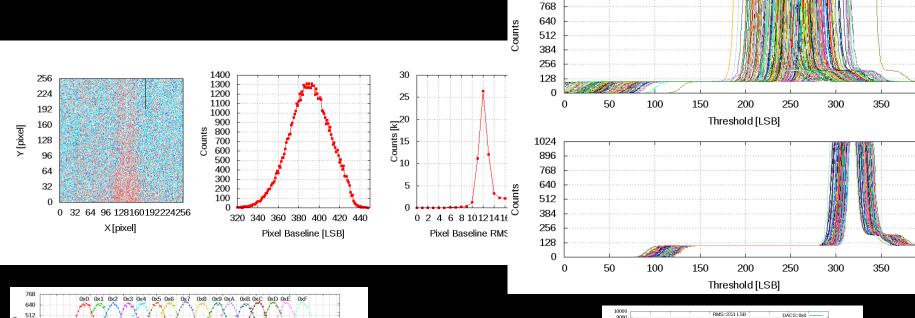


Apper	ndix A: Flo	ow chart		Deep reactive-ion etching (DRIE). DRIE etching allows high aspect ratio structures to be etched. The width of the trenches will be 2-3 μm. In this design a double square wall will be formed.
				Low pressure chemical vapor deposition Silicon Nitride (LPCVD SiN). LPCVD SiN has a high conformity, which will fill up the trenches nicely when a layer of 1.5 µm is deposited.
	II	II		Aluminum deposition. A thin layer of aluminum is deposited for the lateral conductivity of the grid.
	T	T	П	Aluminum patterning. The aluminum is patterned, so that no aluminum is exposed when the grid holes are opened.
	T	II	T	Plasma-enhanced chemical vapor deposition (PECVD) SiN. The aluminum is covered by PECVD SiN. This layer will prevent sparks.
Γ	T	T	T	Grid patterning. The grid holes are opened by plasma etching.
		П		Photoresist + dicing foil. Photoresist and dicing foils are applied to the surface of the grid. The wafer can be diced at this stage.

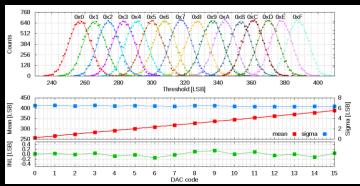
TimePix-3 CERN Medipix Consortium

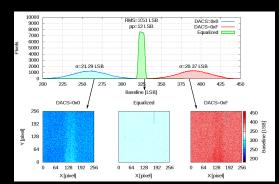
Engineering run: wafers received @ CERN in Sept 2013

Seems to work perfectly!



1024 896

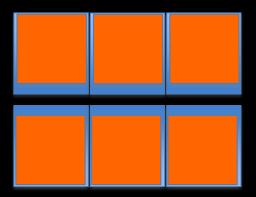




400

GridPix on Single TimePix-3 chip under construction!

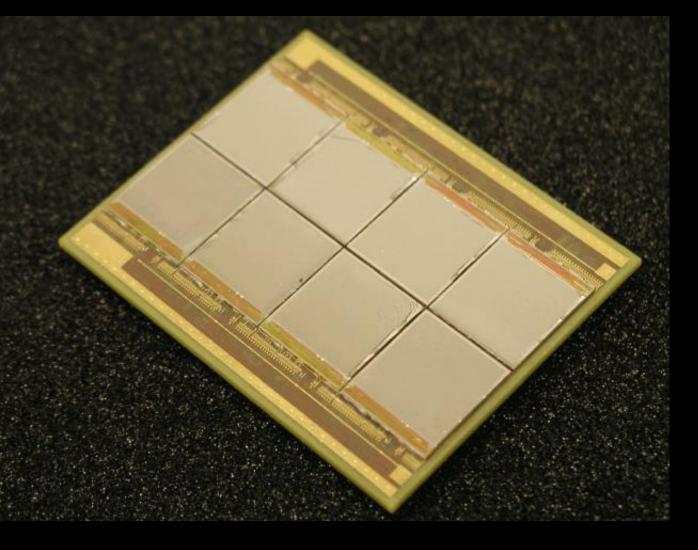
The QuadFocus chamber



GridPix: best tiling now

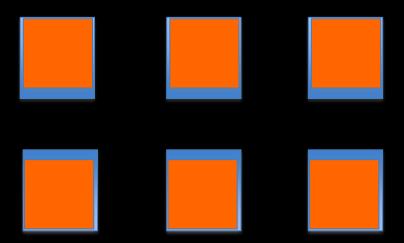
For TPC readout: dead regions due to non-perfect tiling

- perfect tiling possible with Si-Medipix ReLaXd at the cost of through-vias
- dead regions acceptable for some tracking TPCs
- for ILC TPC: no urgency to minimize dead regions



Octopuce: attempt to minimize dead regions

- very hard to exchange broken chips (and we will have broken chips)
- uncontrolled distortion of drift field



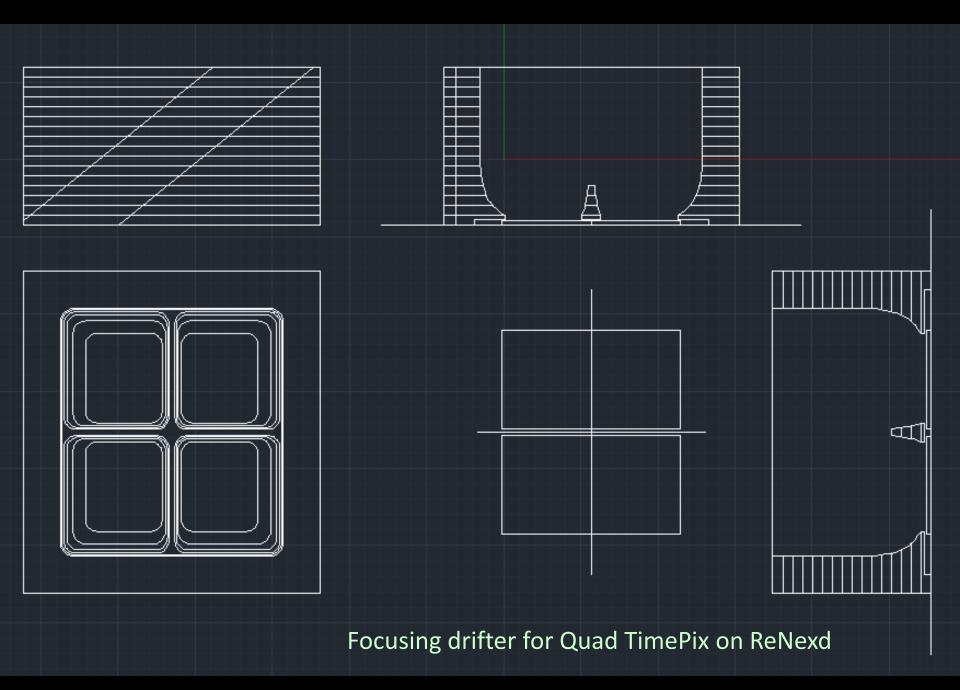
Strong focusing

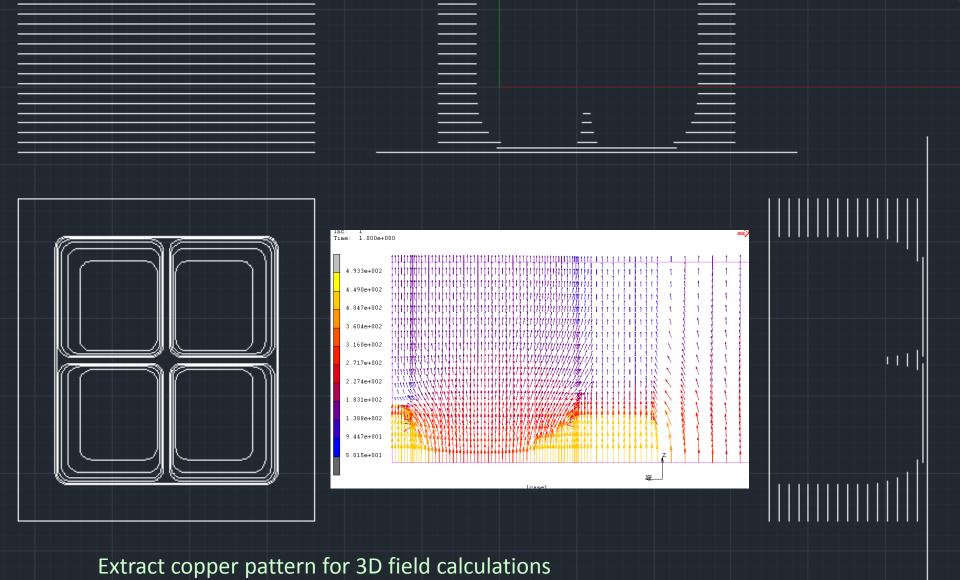
-cover only 25 of fiducial surface with active pixel chip

- saves \$\$
- saves power, thus cooling, thus radiation length

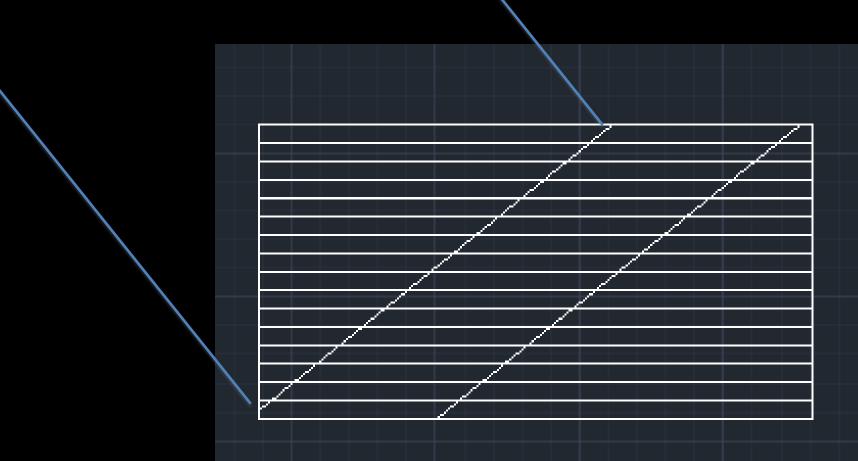
But:

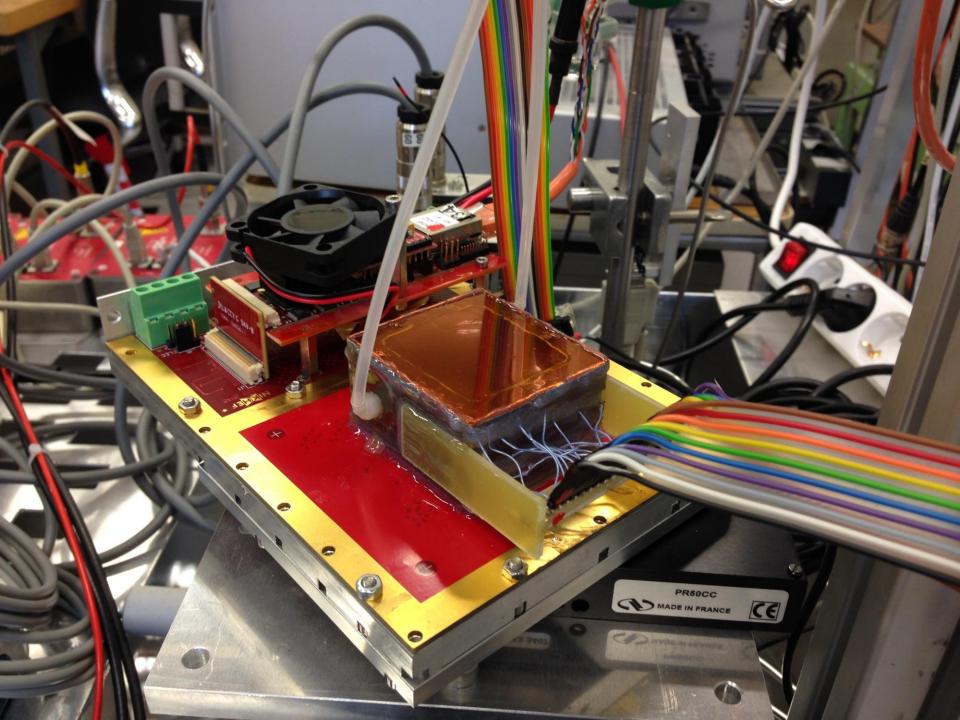
- •larger effective pixel pitch (256 x 256 pixels @ 55 μm x 55 μm)
- → 110 µm x 110 µm Moore'sLaw: smaller pixels in future
- region of amplified diffusion
- •in B-field: E x B effect: amplified (coupled) diffusion

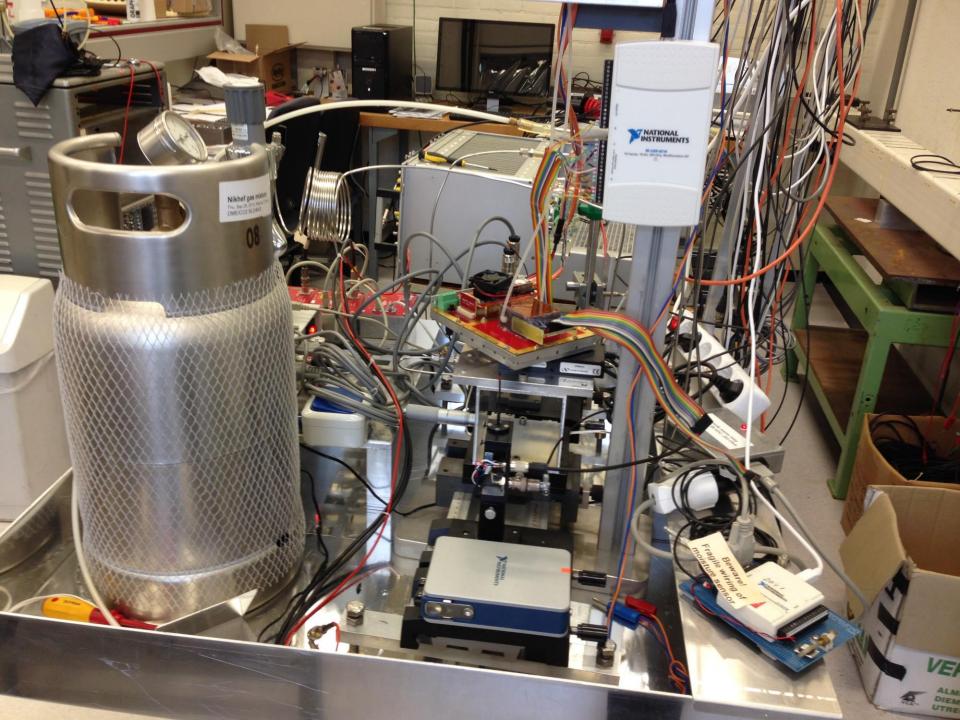




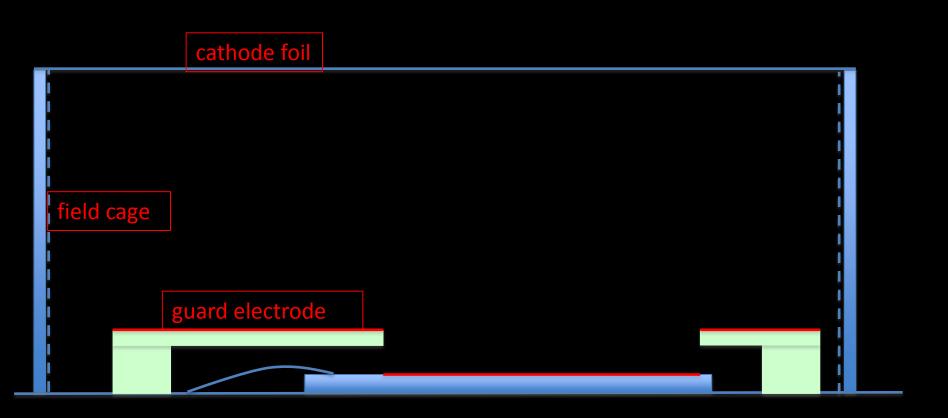
Flat Cable with 16 leads: external potential settings

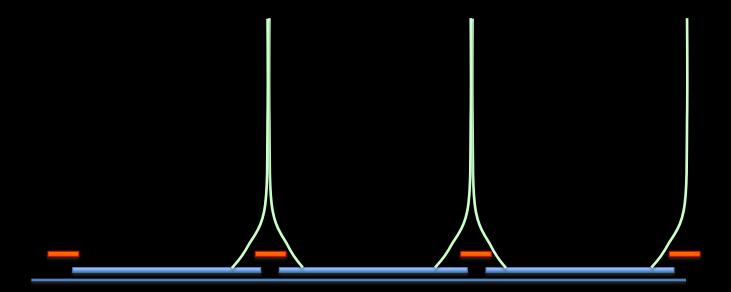




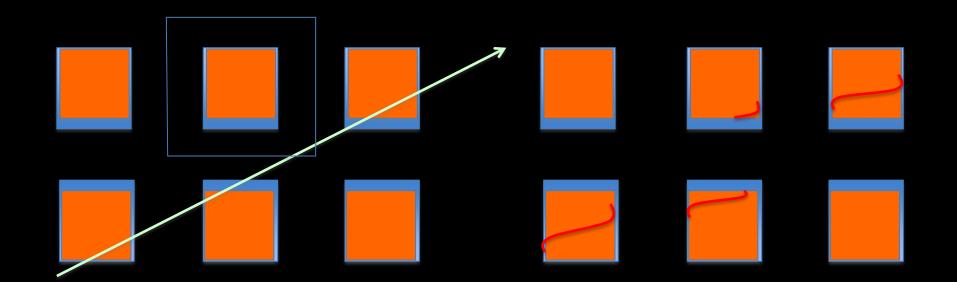


The Q64 chamber





Focus drift field by means of guard electrode to avoid dead regions



Autocalibration

- -get initial $f(X,Y) \rightarrow (X',Y')$ from 3D e-field
- -make scatter plots of residuals
- -modify f(X,Y) until residuals are minimized

Basic correction: X' = C X, Y' = C Y + E x B effect

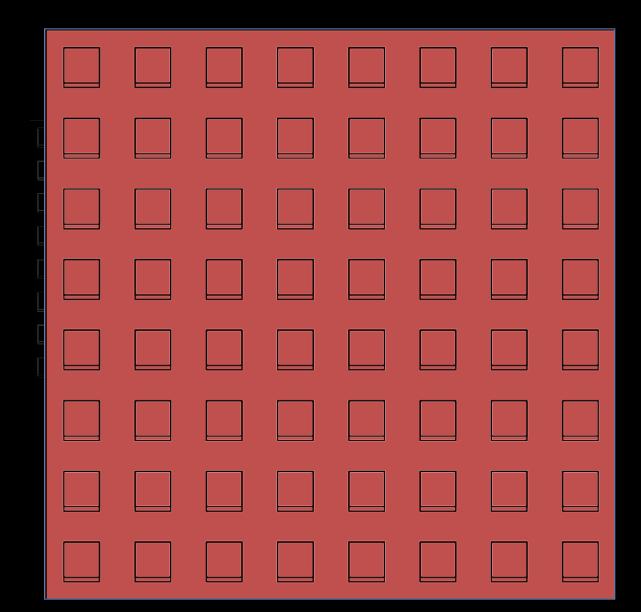
Performance

- requires knowledge of local vectors E, B
- effective pixel size related to electron diffusion
- E x B effect, allthough correctable, may worsen resolution

Plans

- Quad Focus Drifter under construction (finished)
- 2x Sci 30 mm x 40 mm to be constructed
- Chamber support + rotator (around Z axis) ready
- HV distribution box (16 channels!) ready
- Testbeam @ DESY in Oct 2013
 - Data analysis, Monte Carlo simulation, correction procedure

Q64: an assembly of 16 Quads



work: pcb focusing electrode cooling (ReLaXd) field cage wall focusing electrode GridPix ReLaXd unit . cooling elements