Linac4 Low Level RF

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CERN AB-RF

Outline

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  - Feeding two tanks from a single klystron

1. Tank Controller

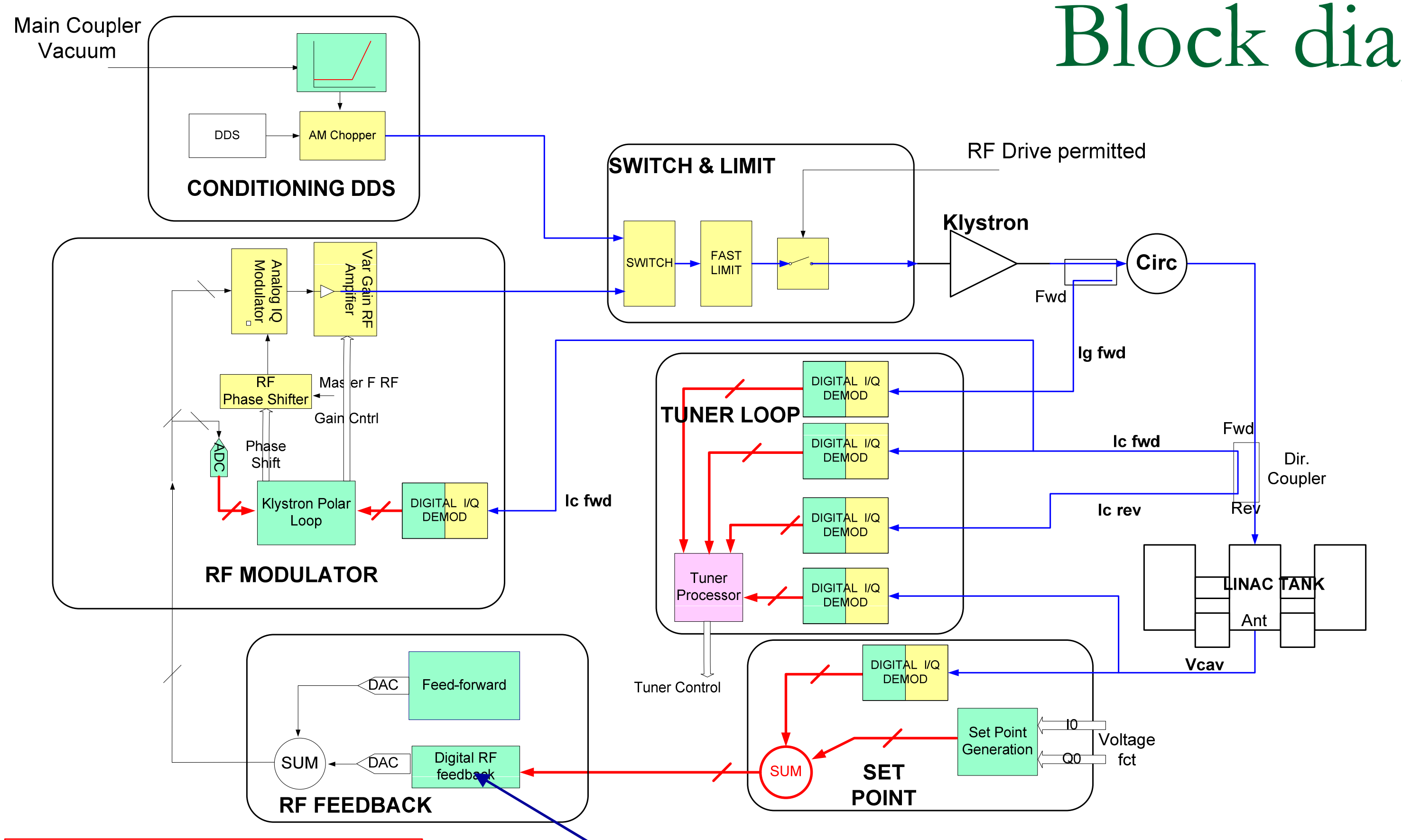
Functionalities

- A **Tuner Loop** to keep the structure on resonance
- An **RF Feedback**, and a **Feedforward** (Iterative Learning) to keep the accelerating voltage at the desired value in the presence of beam transient
- A **Klystron Polar Loop** to compensate the variation of klystron gain and phase shift caused by High Voltage (HV) supply fluctuations (HV droop)
- A **Conditioning System** monitoring the Main Coupler Vacuum while feeding the Line with Frequency Modulated bursts of RF power of increasing amplitude
- A **Klystron Drive Limiter** that prevents from driving the klystron over the saturation limit during loop transients.

Developments

- In 2002, design started for a VME Linac Controller meant for both present and future CERN hadron Linacs: R. Garoby, I. Kozsar, T. Rohlev (on leave from SNS), J. Serrano. The card includes RF feedback, Tuning, Klystron Loop and Iterative Learning (feed-forward).[1]
- In 2003 development started for the VME cards for the LHC LLRF. T. Rohlev joined the Design team and adapted the RF Front-End at 400.8 MHz (Digital IQ demodulators).
- The “PS Linac” card was commissioned on Linac3 in 2004-2005. It followed the “all-in-one-card” philosophy while a modular system was preferred for the LHC
- The LHC LLRF is presently being commissioned
- We propose to adapt the modular LHC system to Linac4: Modularity makes it possible to install and commission the system function by function. Large parts of firmware and software will be re-used.

Block diagram



Linac Module Servo Controller.
Simplified Block Diagram

Signals:

Digital: → Digital I/Q pair: ⇸

Analog baseband: → Analog I/Q pair: ⇸

RF @ 352.2 MHz →

Technology:

DSP 🟪

CPLD or FPGA (35.22 MHz) 🟩

Analog RF 🟨

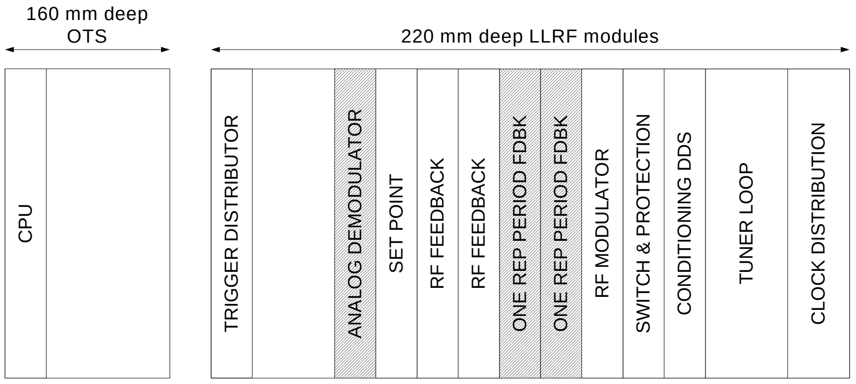
Multi-notch filter to deal with the parasitic resonances (non-accelerating modes) of the multi-cell tank [2]

1 Tank Controller per tank

1 Klystron per Tank

Platform

- Same crates as LHC LLRF:
  - 4 slots 160 mm deep (CPU) with extended VME interfacing (32 bits D, 48 bits A)
  - 15 slots 220 mm with reduced VME interfacing (16 bits D, 24 bits A) for custom LLRF cards (10 slots used)
  - EMC qualified crates
- Special J2 backplane:
  - Linear +-6V, +- 12 V P.S. for RF and Analog circuitry
  - (Slow) clock distribution (up to 35.2 MHz) plus rep rate pulse
  - JTAG for reprogramming FPGAs
  - Serial distribution of functions
  - Interlock lines
  - A series of hardware timings


160 mm deep OTS

220 mm deep LLRF modules

CPU

TRIGGER DISTRIBUTOR

ANALOG DEMODULATOR

SET POINT

RF FEEDBACK

RF FEEDBACK

ONE REP PERIOD FDBK

ONE REP PERIOD FDBK

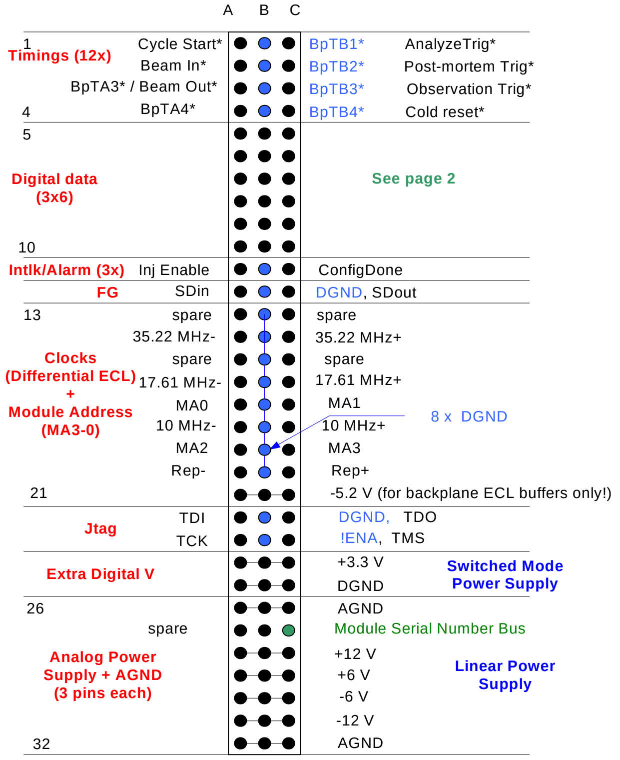
RF MODULATOR

SWITCH & PROTECTION

CONDITIONING DDS

TUNER LOOP

CLOCK DISTRIBUTION


A B C

1 Timings (12x) Cycle Start* — BpTB1* AnalyzeTrig*

Beam In* — BpTB2* Post-mortem Trig*

BpTA3* / Beam Out* — BpTB3* Observation Trig*

4 BpTA4* — BpTB4* Cold reset*

5

Digital data (3x6) — See page 2

10

Intlk/Alarm (3x) Inj Enable — ConfigDone

FG SDin — DGND, SDout

13 spare — spare

35.22 MHz- — 35.22 MHz+

Clocks (Differential ECL) + Module Address (MA3-0)

spare — spare

17.61 MHz- — 17.61 MHz+

MA0 — MA1

10 MHz- — 10 MHz+

MA2 — MA3

Rep- — Rep+

8 x DGND

21 — -5.2 V (for backplane ECL buffers only!)

Jtag TDI — DGND, TDO

TCK — !ENA, TMS

Extra Digital V — +3.3 V, DGND — Switched Mode Power Supply

26 — AGND

spare — Module Serial Number Bus

Analog Power Supply + AGND (3 pins each) — +12 V, +6 V, -6 V, -12 V — Linear Power Supply

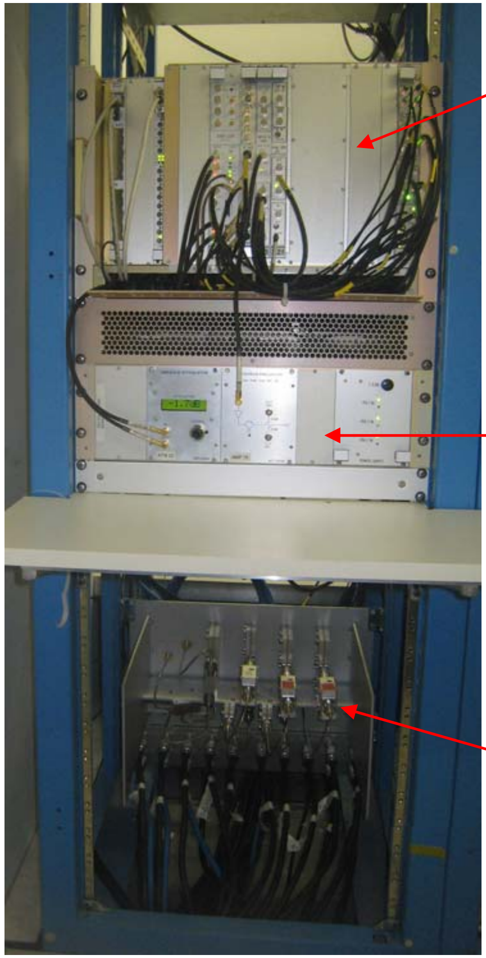
32 — AGND

LINAC LLRF backplane
Lower connector: 3 x 32 pins
version 9/16/2006

Diagnostics

- Important signals (~30/controller) are stored for monitoring
- Two sets of memory
  - Post-Mortem memory: Free-running, stopped by specific machine-wide post-mortem trigger, fixed sampling rate. Meant to correlate acquisitions after a fault.
  - Observation: Piloted by operator that sets sample rate and triggers the acquisition. Meant for monitoring during operation.
- Built-in Network Analyzer
  - Excitation memories to inject signals (step, sine-wave, white noise,…) coupled with observation memories implement a Signal Analyzer
- Fully remote controlled

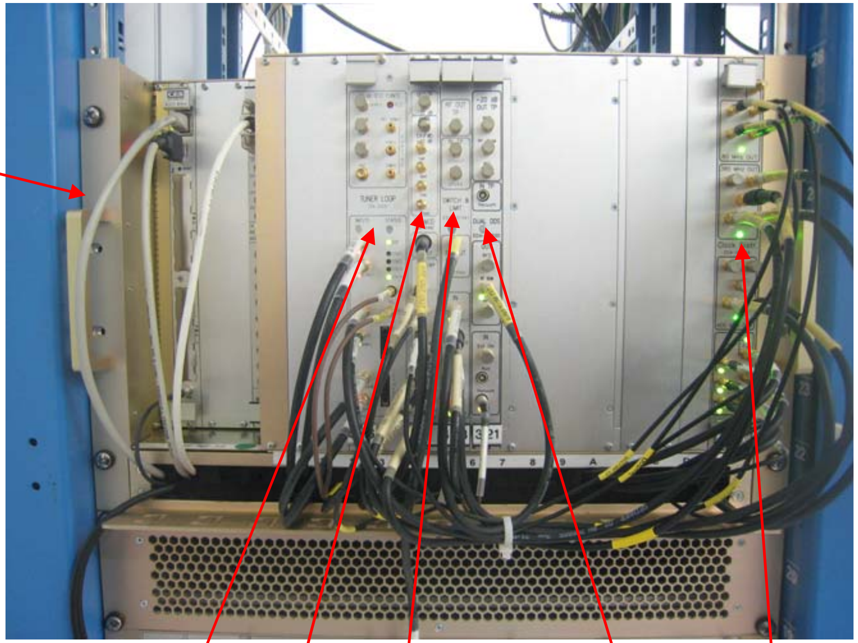
Implementation



Cavity Controller VME crate

Antenna calibration and 100 mW pre-driver

RF cable splitting



Switch&Limit

Clock Distri

Tuner Control

Conditioning DDS

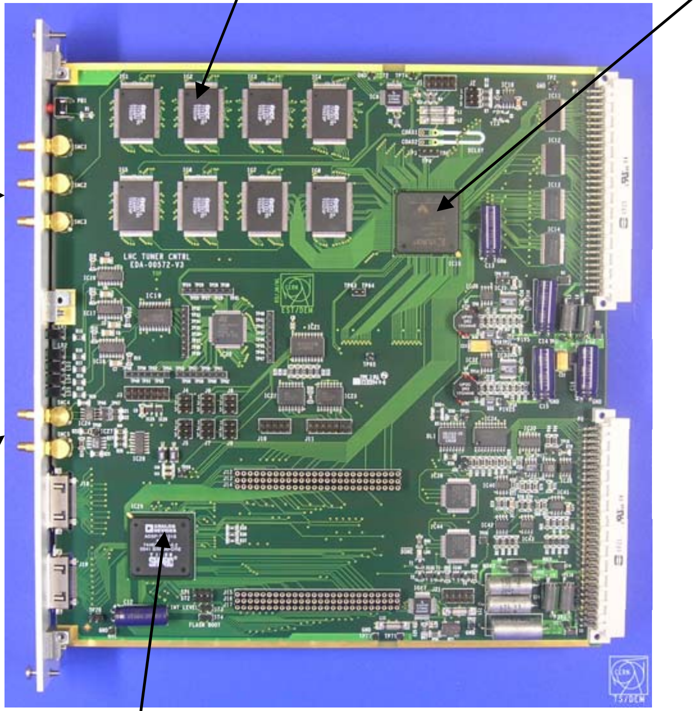
RF Modulator

One rack per RF tank in the LLRF Faraday Cage

Example of VME cards

Logging memories

FPGA



TP

In/Out

DSP

Tuner Control card

TP

In/Out

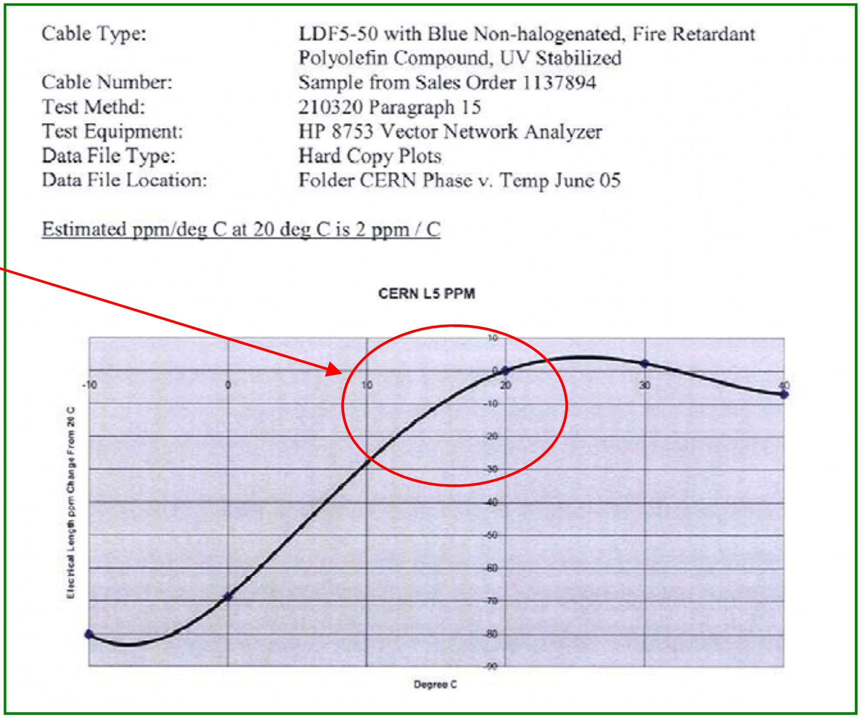
RF Front-end

Conditioning DDS

2. Reference clocks

Goal: keep tank field within 1 degree of Set Point

- The strong RF feedback imposes a fixed phase at the end of the Antenna return cable in the air conditioned Faraday cage
- All antenna return cables are equal length (~50 m), thermally cycled 7/8” Flexwell. Thermal coefficient $\Delta L/L$ = 3 ppm/degree C
- Phase drift in cavity field can be caused by:
  - Difference in temperatures sensed by cables: Assuming 5 degrees C over 50 m length we get *ΔT= 2.5 ps*
  - Differences in thermal coefficients between cables: Assuming 1 ppm/degree C and 10 degrees temperature change in the building we get *ΔT= 1.7 ps*
- Summing it up we get a total phase drift of cavity field of 4.2 ps = 0.5 degrees @ 352.2 MHz



Cable Type: LDF5-50 with Blue Non-halogenated, Fire Retardant Polyolefin Compound, UV Stabilized
Cable Number: Sample from Sales Order 1137894
Test Methd: 210320 Paragraph 15
Test Equipment: HP 8753 Vector Network Analyzer
Data File Type: Hard Copy Plots
Data File Location: Folder CERN Phase v. Temp June 05

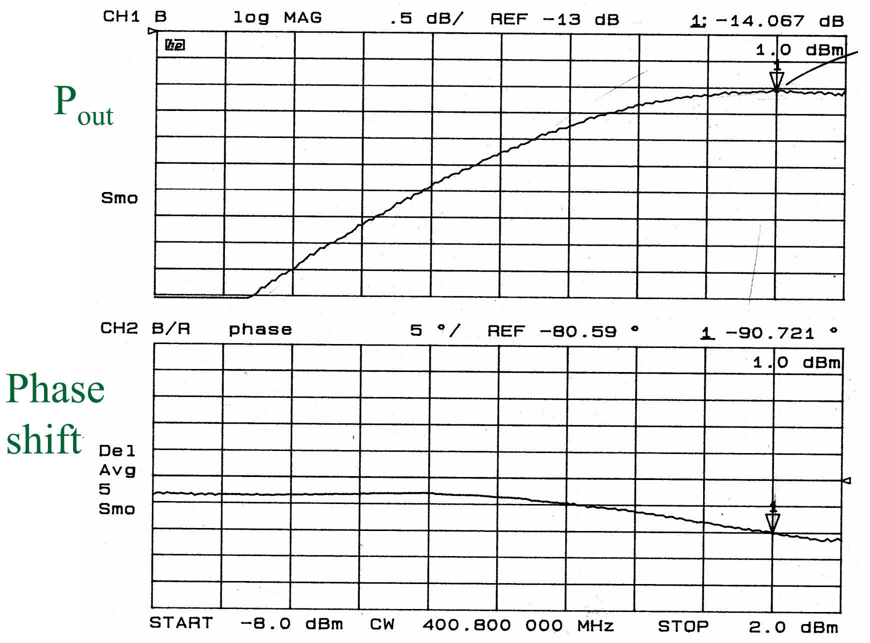
Estimated ppm/deg C at 20 deg C is 2 ppm / C

Measured by ANDREW on a sample of the 7/8” cables installed in the LHC

3. Open questions

Saturated klystron

- The LLRF counts on a strong RF feedback (Field stability)
- At saturation there is zero small-signal gain. LLRF is helpless.
- Linac4 proposal: only 10 % power budget for phase and amplitude control = saturation – 0.46 dB. This reduces the gain to ¼ (linear) the unsaturated value
- For comparison: LHC klystrons saturate at 300 kW. In operation we require 150 to 200 kW

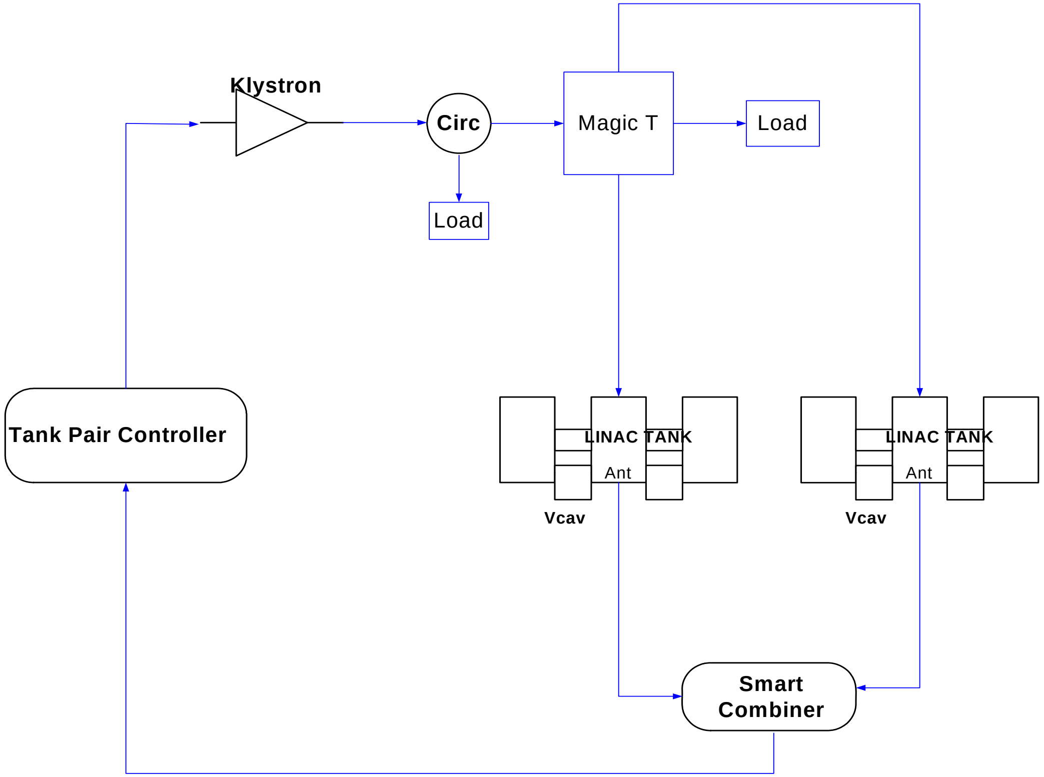


LHC Klystron CW @ 400.8 MHz

Derating in dB	**Gain loss**	**Operating point in % of Pmax**
-0.5 dB	**-11 dB**	89 %
-1 dB	-6.7 dB	79 %
-1.5 dB	-4 dB	71 %
-2 dB	-3.2 dB	63 %
-3 dB	-2.6 dB	50 %

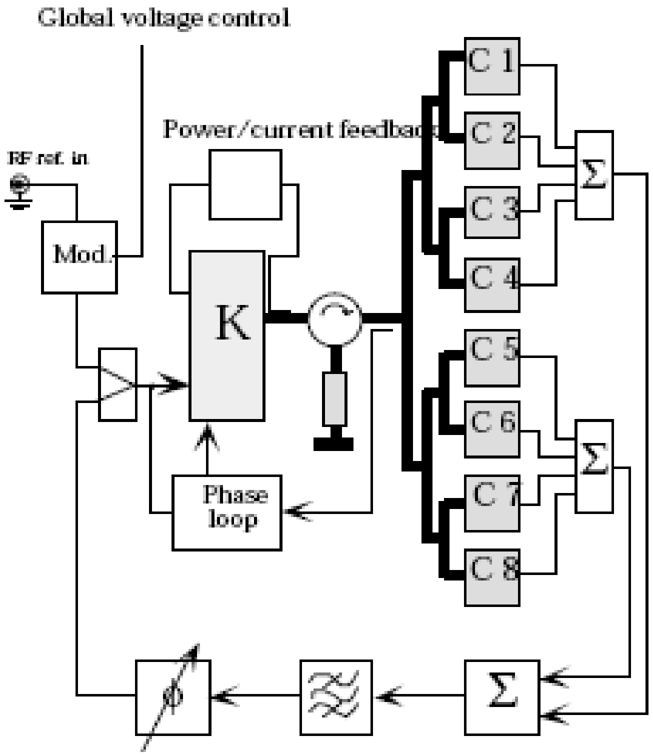
One klystron for two tanks

- For PIM5 to PIM12 we plan to feed two PIMs from a single 2.5 MW klystron
- In the future it is planned to replace 2 LEP klystrons by 1x 2.5 MW
- No individual control of the field in the two PIMs of a pair.
- RF feedback has to deal with 2 families of parasitic modes (close but not equal).
- Problem caused by imperfect isolation of the two cavity feeds (cross-talk in magic-T)



LEP Vector-Sum Feedback

- This so-called "Vector Sum Feedback" was tested in LEP. Not successful. [3]
- *"On the topic of the SNS RF system, we use one klystron - one cavity. We do share high voltage power supplies but each cavity has its own klystron."* Mark Crofford, private communication.



Reproduced from [3]

References

- [1] J. Broere, I. Kozsar, R. Garoby, A. Rohlev, J. Serrano, All Digital IQ Servo-System for CERN Linacs, EPAC 2004
- [2] D. Boussard , H.P. Kindermann, V. Rossi, RF Feedback applied to a multicell superconducting cavity, EPAC 88
- [3] E. Peschard, RF System for High Intensity, Chamonix 1996

Thank you…

Additional material if questions arise

RF feedback Theory

- RF Feedback theory [6],[7]
  - Minimal cavity impedance (with feedback) scales linearly with T

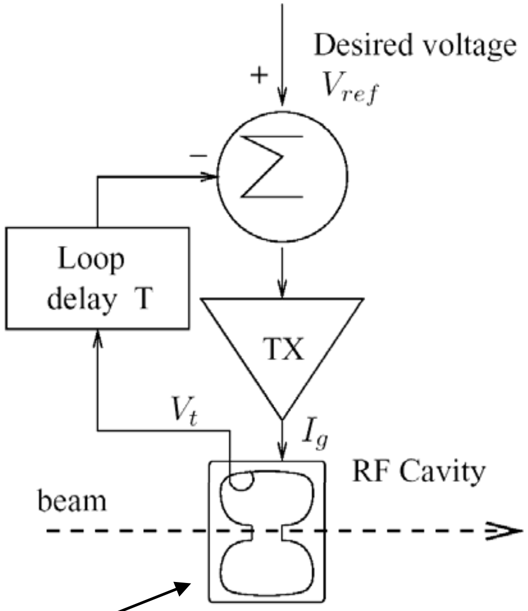
$$\boxed{R_{\min} = \frac{2}{\pi}\frac{R}{Q}\omega_0 T}$$

  - Achieved for a gain value proportional to Q

$$\boxed{G_{opt} \approx \frac{Q}{\omega_o T}}$$

  - Achievable fdbk BW inversely proportional to T

$$\boxed{\Delta\omega = \frac{1.3}{T}}$$



assumed single-cell