WP.3 – Microelectronics and interconnect technologies for particle physics experiments

WP.3-Task.1 – Microelectronics Technologies and enabling Tools

1. Introduction

The scale and the performances required for the construction of modern particle physics experiments demand the massive application of advanced microelectronics technologies. These technologies are necessary to design low power circuits for the signal treatment of particle sensors and are indispensable to reduce the cost of large multi-million channel detectors. As the telecommunication revolution has been made possible by the miniaturization of portable phones, so the availability of multi-channel, low cost and low power integrated circuits allows physicist and engineers to design revolutionary new sensors for the detection of products of particle collisions at high luminosity accelerators. Application-specific integrated circuits (ASICs) designed for particle physics experiments often have to survive in the very harsh radiation environments generated by high luminosity accelerators. Commercial technologies and standard design styles are generally not directly suited for these applications. Therefore special design techniques and methodologies have to be developed and maintained. In view of the efforts and investments involved, this requires a high level of organization and support within the particle physics engineering community.

The main objective of this task is to provide the infrastructure to make specific modern deep-submicron microelectronics technologies available to the largest possible group of users in the particle physics community. Besides assessing the technologies and adapting the design methodologies for our specific needs, this task includes the access to tools, the training and the support for design engineers within a growing community. It also comprises the coordination of common submissions for prototype productions in the form of HEP specific multi-project wafer (MPW) runs.

2. Organization participation

Participant acronym	CERN	INFN Italy	IN2P3 France	CNM Spain	RAL UK	Bonn Germany	Cracow	Nikhef	PSI
Estimated person-months per participant:	24	24	?	36	6	12	12	12	?

3. Objectives

- Evaluation, qualification and characterization of a restricted but well selected family of advanced CMOS and BiCMOS technologies for users in the particle physics community
- Monitoring of parameters of technologies under irradiation and development of optimised design methodologies
- Making available a standard set of Computer Aided Engineering tools and training of designers in using the appropriate design methodologies
- Organize a common computing infrastructure to house, maintain and verify large designs implemented as collaborative efforts
- Coordination of multi-project wafer submission for prototype developments
- Organization of users meeting with engineers from HEP community with the objective of exchanging information specific to designs for particle physics experiments

4. Description of work

The electronics requirements for future particle experiments at SLHC, ILC, CLIC, B-physics or neutrino experiments have many similarities in addition to numerous experiment-specific and detector-specific

demands. The individual detector systems count up to tens of millions of independent sensitive elements. In general this requires low-mass analog and digital electronics systems, with high sensitivity, high speed, dense channel concentration and low power consumption. Individual requirements on signal shaping, timing characteristics, sensitivity, dynamic range and radiation hardness may vary rather widely. In addition, special technologies are needed for the implementation on-detector power distribution circuits. ASICs with the required functionality typically comprise up to 128 channels per chip.

Within this task, requirements will be collected from the various future experiment collaborations with the aim of selecting a small number of commercially available technologies that are expected to fulfil the needs. These will include advanced CMOS technologies, for applications where size and power are the most critical requirements, as well as BiCMOS technologies, where performance is the driving parameter, and finally high-voltage CMOS technologies for specific powering applications. These technologies will be evaluated, qualified and characterized for their suitability for particle physics applications. Particular emphasis will be put on their performance under irradiation. In this context, optimised design methodologies will be developed, implemented and tested.

The resulting design methodologies will be publicly made available to the microelectronics designers in the particle physics community at large. These designers will be given access to a standardised set of Computer Aided Engineering (CAE) tools for the selected technologies. These CAE tools will comprise standard commercial modules, complemented with specific add-on modules (from enhanced simulation models to modified design rule checks). Dedicated training courses will be organised for users to guarantee an optimal use of the tools and they will be given technical support for their design activities. In addition the coordination of multi-project wafer submissions for prototype developments will be part of this task.

List of Deliverables for the task
(typically 1 per task per year)

Deliverables of task 1	**Person month estimate**	**Description/title**	**Nature**[1]	**Delivery month**[2]
D3.1.1		Qualification of 130 nm CMOS technology, and supply of corresponding CAE tools	R	M12
D3.1.2		Organization of Annual User's Meeting	R	M6 M18 M30 M42
D3.1.3		Qualification of 130 nm BiCMOS technology, and supply of corresponding CAE tools	R	M24
D3.1.4		1st Report on training, support and submissions	R	M24
D3.1.5		2nd Report on training, support and submissions	R	M36
D3.1.6		Qualification of more advanced CMOS technology, and supply of corresponding CAE tools	R	M36

List of Milestones for the task

Milestones	**Description/title**	**Tasks involved**	**Delivery month**[2]	**Means of verification**
M2.1	Selection of a more advanced CMOS technology for qualification			M24

[1] Nature: R=Report, P=Prototype, D=Demonstrator, O=Other
[2] Counted from the starting date