WP.3-Task.2 – Shareable IP blocks for HEP

1. Introduction

The design of ASICs implies the balanced integration of various individual functional design blocks (IPs) into a complex circuit. The availability of libraries with well-proven functional blocks can greatly accelerate the ASIC design and its likelihood of success. Due to the specificity of the circuits for particle physics, in particular the required radiation hardness properties, commercially available design blocks are normally not appropriate. Designers in the particle physics community will greatly profit from the creation of a library of IPs for all designers. The objective of this task is to provide a framework in which functional blocks of medium and high complexity, designed within the particle physics community, are made available within this community, thus minimizing the project costs and lowering their risks. This task, which includes the design and qualification of an initial set of blocks, is naturally related to Task 3.1, which provides the underlying silicon technologies.

2. Organization participation

Participant acronym	CERN	U-Bonn	INFN Italy (Bari, Genova, Padova, Bergamo)	Barcelona Univ + CNM	Nikhef	AGH Cracow	Munich
Estimated person-months per participant:	12	?	24	12	12	12	6

3. Objectives

- Creation and coordination of a framework for the design of low and medium complexity microelectronics blocks to be made available to the community
- Design, functional and performance qualification of a balanced set of blocks using the technologies of Task 3.1
- Distribution and documentation of the library of functional blocks
- Organization of regular Microelectronics Users Group meetings to exchange information, plan and coordinate actions related to the creation of a shared library of macro blocks.

4. Description of work

All the objectives below are meant to be implemented initially in a common 130 nm CMOS technology, their porting to a more advanced nm CMOS technology will be examined later in the evolution of the project depending on requests from users.

List of Deliverables for the task
(typically 1 per task per year)

Deliverables of task 1	**Person month estimate**	**Description/title**	**Nature**[1]	**Delivery month**[2]

D3.2.1	12	Report on first set of macro blocks	R	M12
D3.2.2	12	Report on first set of macro blocks	R	M24
D3.2.3	12	Report on first set of macro blocks	R	M36
D3.2.4	12	Report on first set of macro blocks	R	M48

List of Milestones for the task

Milestones	**Description/title**	**Tasks involved**	**Delivery month[2]**	**Means of verification**

Attachment: Examples of macro blocks

This is a non-exhaustive list of macro blocks of potential common interest.

- Design of a radiation tolerant *IO pad* library adapted to the selected technology; including drivers for a C4 type bump-bonding.
- Depending on irradiation results of the base technology, a full digital library realized with special layout techniques may be necessary. This requires a large investment in characterization, documentation, verification etc.
- Design of a general purpose *rad-tolerant configurable SRAM* block.
    - A *multi-port SRAM* block derived from the macro above.
    - A *FIFO* macro block could be derived from this basic macro.
- Design of timing macro blocks including:
    - A low-jitter *DLL* macro with resolution in the 10's of ps.
    - A high speed *PLL* macro with a 40 MHz standard LHC input clock frequency and outputs in the several GHz range
    - A *medium speed PLL macro* with a selectable 40-80-160 MHz input and a selectable 160-320-480-640 MHz output at the lowest possible power,
- Design of a general purpose *e-link* port macro in CMOS to interface front-end ASICs to a general purpose high speed fiber optic based serial link.
- Design of a temperature and voltage independent *bandgap* reference macro.
- Design of a standard 8 and 10 bit biasing (i.e. slow) *Digital to Analog Converter* (DAC)
- Design of *Single-Event-Upset (SEU) robust flip-flop* and storage elements for general purposes digital design applications.