ATLAS LAr Phase-I Upgrade Technical Design Report

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for the ATLAS Collaboration

Outline

- Motivations
- Proposed implementation
- Expected Performance
- System Architecture and Design Requirements
- Project organization, costs, milestones and resources

ATLAS Upgrade Plans

2009 2010 2011 2012 **2013 2014 LS1** 2015 2016 2017 **2018 LS2** 2019 2020 2021 **2022 2023 LS3** .. 2030

"Phase-0" upgrade: consolidation
$\sqrt{s}$ = 13~14 TeV, 25ns bunch spacing
$\mathcal{L}_{inst} \simeq 1 \times 10^{34}$ cm^{-2}s^{-1} ($\mu \simeq 27.5$)
$\int \mathcal{L}_{inst} \simeq 50$ fb^{-1}

"Phase-I" upgrades:
ultimate luminosity
$\mathcal{L}_{inst} \simeq 2\text{-}3 \times 10^{34}$ cm^{-2}s^{-1} ($\mu \simeq 55\text{-}81$)
$\int \mathcal{L}_{inst} \gtrsim 350$ fb^{-1}

"Phase-II" upgrades:
$\mathcal{L}_{inst} \simeq 5 \times 10^{34}$ cm^{-2}s^{-1} ($\mu \simeq 140$) w. leveling
$\simeq 6\text{-}7 \times 10^{34}$ cm^{-2}s^{-1} ($\mu \simeq 192$) no level.
$\int \mathcal{L}_{inst} \simeq 3000$ fb^{-1}

ATLAS has devised a 3 stage upgrade program to optimize the physics reach at each Phase

- New Insertable pixel b-layer (IBL)
- New Al beam pipe
- New pixel services
- New evaporative cooling plant
- Consolidation of detector elements (e.g. calorimeter power supplies)
- Add specific neutron shielding
- Finish installation of EE muon chambers staged in 2003
- Upgrade magnet cryogenics

- New Small Wheel (nSW) for the forward muon Spectrometer
- *High Precision Calorimeter Trigger at Level-1*
- Fast TracKing (FTK) for the Level-2 trigger
- Topological Level-1 trigger processors
- Other Trigger and DAQ upgrades

- All new Tracking Detector
- Calorimeter electronics upgrades
- Upgrade part of the muon system
- Possible Level-1 track trigger
- Possible changes to the forward calorimeters

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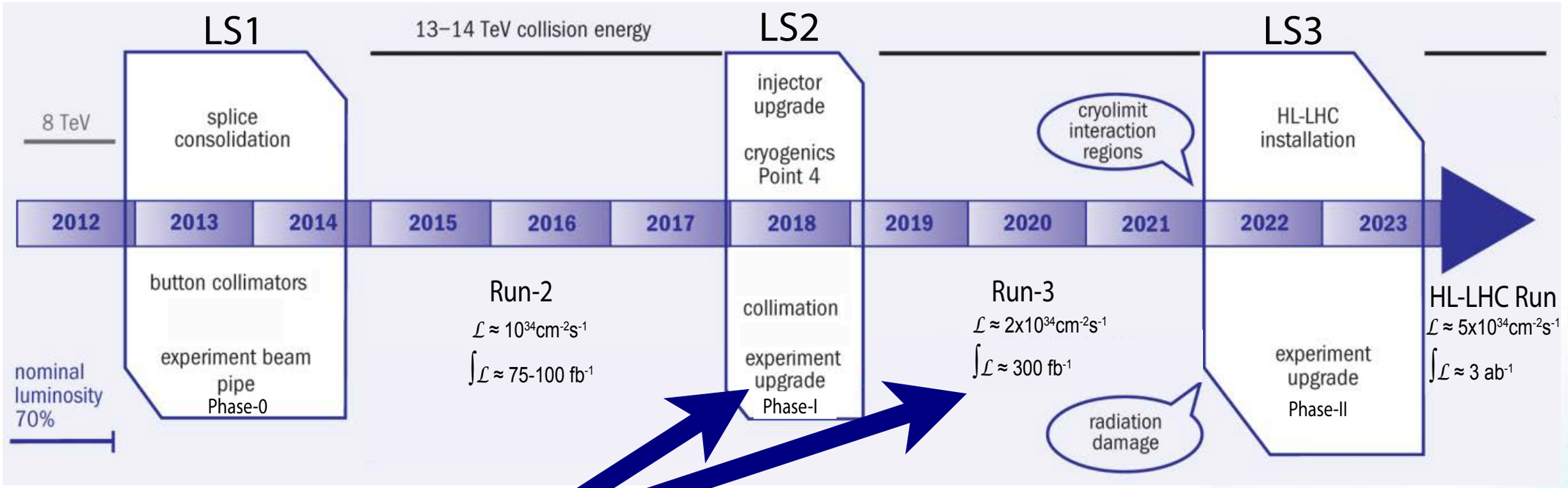
In Phase-I the ATLAS program focuses on the upgrade of the trigger sub-systems to provide better handles against increasing pileup

Assumed LHC Upgrade Scenario



- $\mathcal{L}_{inst} \simeq 2x10^{34}cm^{-2}s^{-1}$
- No reason to believe that the actual instantaneous luminosity couldn't be even higher
- **For upgraded systems in Phase-I ATLAS requirements:**

- $\mathcal{L}_{inst} \simeq \mathbf{3x10^{34}cm^{-2}s^{-1}}$
- 25ns bunch spacing
- $<\mu> \simeq 80$
- L1 Trigger Bandwidth: 100kHz max.
- L1 Delay: $\lesssim 3\mu s$ max (at the detector).
- Forward compatibility with HL-LHC operations and Phase-II upgrade programs.

Why do we need the LAr Phase-I Upgrades?

based on Run-1 trigger

	Offline p_T Threshold [GeV]	Rate [kHz]
EM18VH	25	130
EM30	37	61
2EM10	2x17	168
EM total		**270**

- Using L1 selection as in Run-1 simply impossible
- (100 kHz limit)

- Projected rates at $\mathcal{L}_{inst} \approx 3 \times 10^{34} cm^{-2} s^{-1}$ with the existing L1 calorimeter trigger system
- QCD jet background dominates L1 EM rates
  - Inclusive EM rates expected to grow linearly with $\mathcal{L}_{inst}$.
  - Rates for di-EM triggers determined by accidentals from Minimum Bias events

Why do we need the L1 Calo upgrade?

- Projected rates at $\mathcal{L}_{inst} \approx 3 \times 10^{34} cm^{-2} s^{-1}$

- Bandwidth for EM objects benchmarked at about 20% of the overall L1 trigger bandwidth
  - (similarly to Run-1)

based on Run-2 trigger

	Offline p_T Threshold [GeV]	Rate [kHz]
EM30VHI	38	14
EM80	100	2.5
2EM15VH I	2x22	2.9
		18

- Stronger isolation requirements
- Yet thresholds increase significantly
- Loss of acceptance in many physics channels (with W/Z in particular)

➡ **Need better jet rejection capability**

Phase I Upgrades?

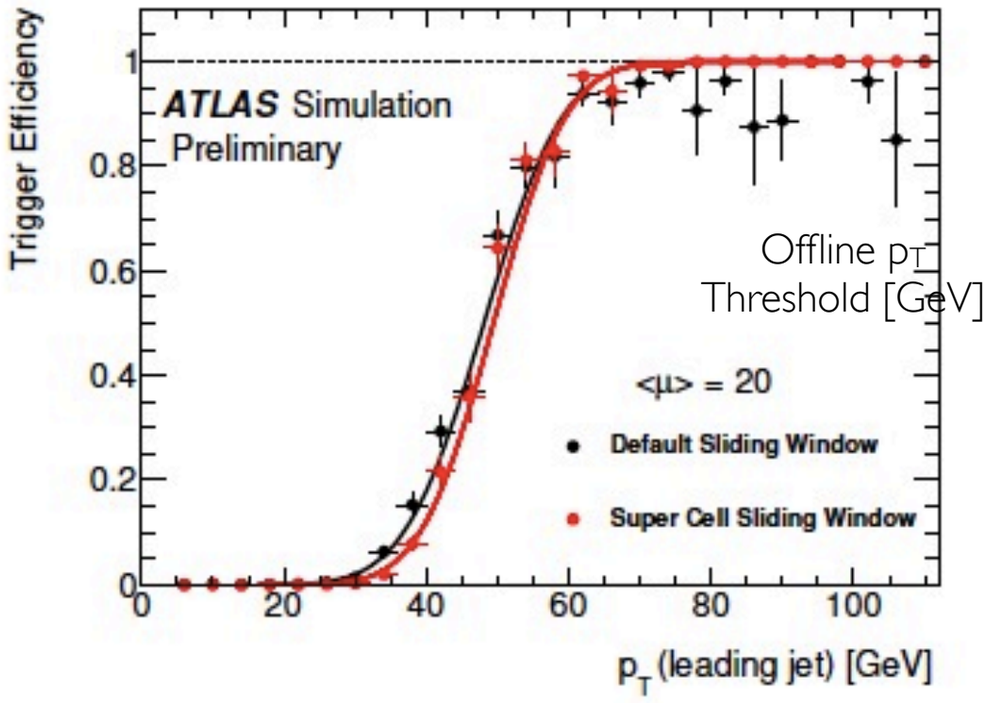
Similar for EM+**μ**, **τ**, Jet and E_T^{miss} Triggers

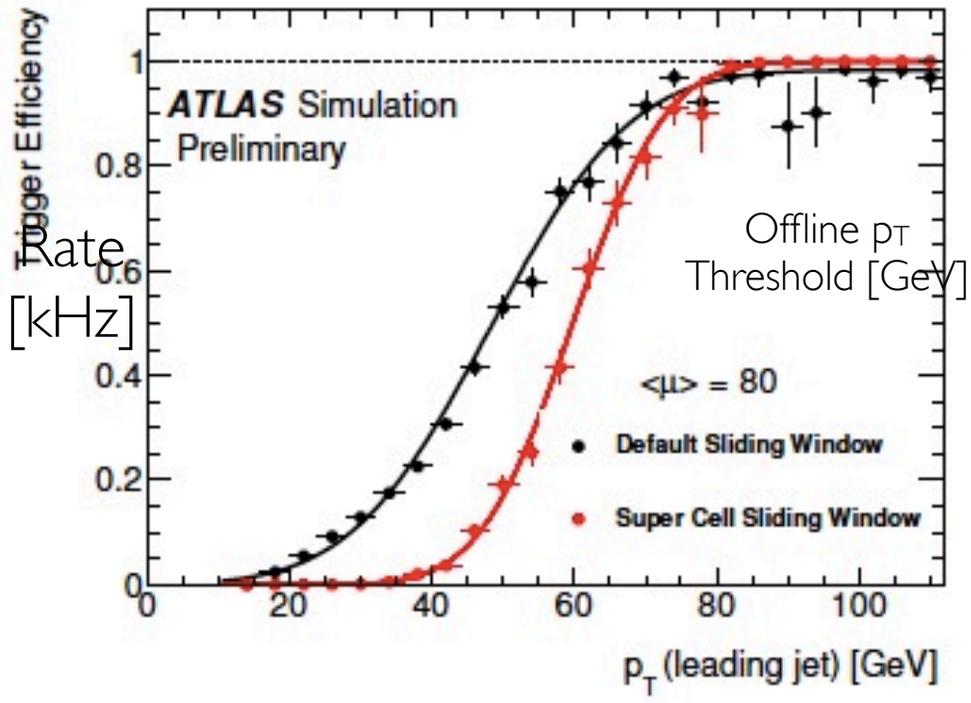
(**This is an example** - see Rainer's presentation)

- Projected rates at $\mathcal{L}_{inst} \simeq 3 \times 10^{34} cm^{-2} s^{-1}$

based on Run-1 trigger	Offline p_T Threshold [GeV]	Rate [kHz]	based on Run-2 trigger	Offline p_T Threshold [GeV]	Rate [kHz]
EM10VH_MU6	17,6	22	EM15VH_MU10	22,12	3.0
			EM10H_2MU6	17,2x8	2.5
TAU40	100	52	TAU80V	180	4.7
			2TAU50V	2x110	3.8
2TAU11I_TAU15	30,40	147	2TAU20VI_3J20	2x50,60	5.2
2TAU11I_EM14VH	30,21	60	2TAU20VI_ EM18VHI_3J18	50,25,60	2.8
			TAU15VI_MU15	40,20	3.8
TAU15_XE35	40,80	63	TAU20VI_ XE40_3J20	50,90,60	4.4
Tau total		**238**			**20**
J75	200	34	J100	200	7.0
4J15	4x55	87	4J25	4x60	3.3
			J75_XE40	150,150	8.3
XE40	120	157	XE90	250	10
Jet/E_T^{miss} total[a]		**306**			**25**

Similar for EM+μ, τ, Jet and E_T^{miss} Triggers





Rate [kHz]

Rate [kHz]

$10^{34}cm^{-2}s^{-1}$

Figure 14. The trigger efficiency as a function of the highest p_T offline jet for $\langle\mu\rangle = 20$ (a) and $\langle\mu\rangle = 80$ (b) in simulated QCD dijet events. The performance of the default sliding window algorithm (black points) is compared to that of the sliding window algorithm based on Super Cells (red points) for jets within $|\eta| < 2.5$.

Significant degradation with pileup of the turn-on curve requiring much higher offline threshold (black curves)

			5	90,60	4.4
					20
				200	7.0
4J15	4x55	87	4J25	4x60	3.3
			J75_XE40	150,150	8.3
XE40	120	157	XE90	250	10
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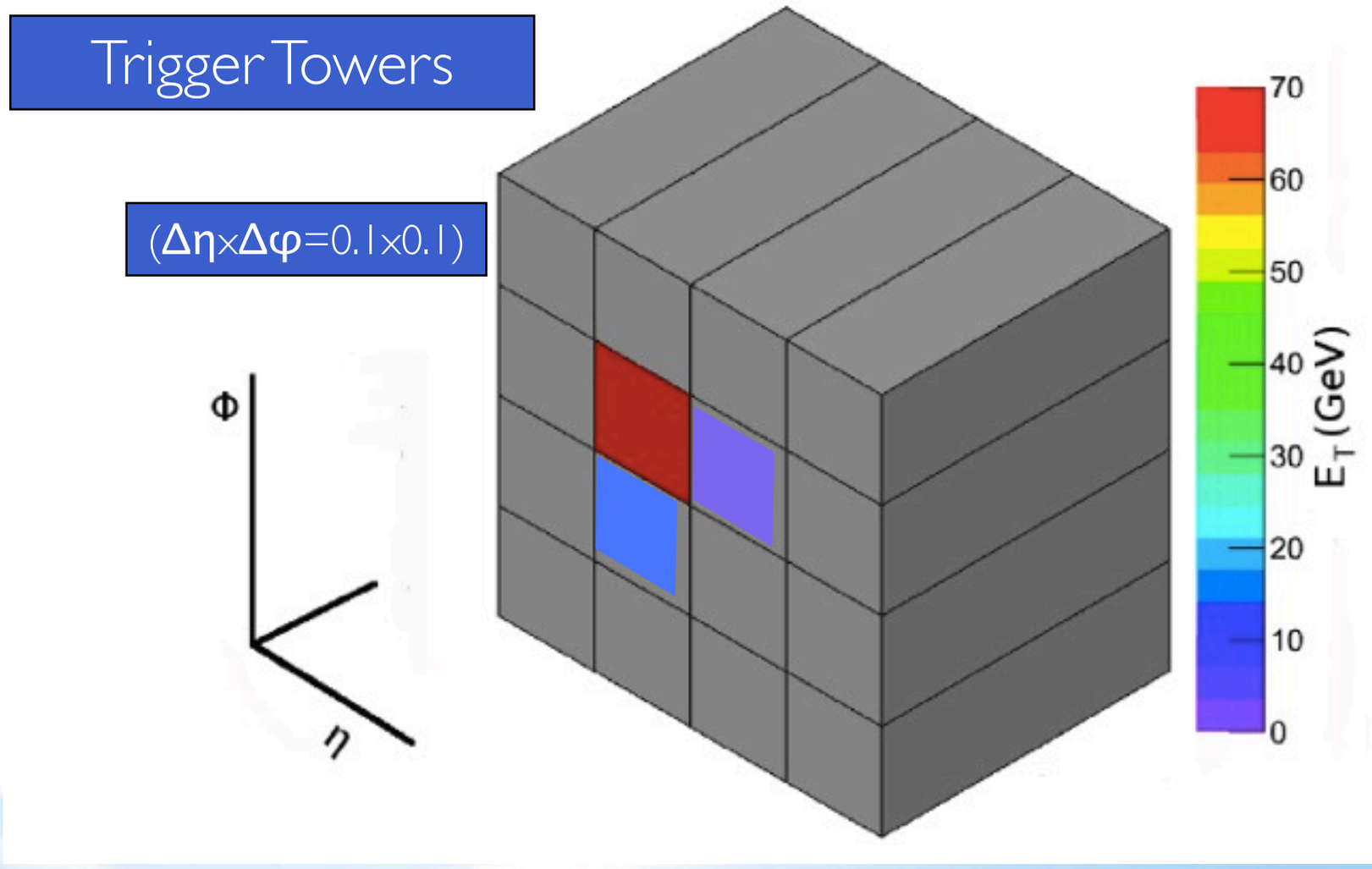
How to improve?

- Clustering and isolation with the existing Trigger Towers are significantly degraded by pileup because:
  - large area in **Δη,Δφ** (and pileup noise is correlated)
  - limited resolution (1 GeV E_T) available

Trigger Towers

(Δη×Δφ=0.1×0.1)



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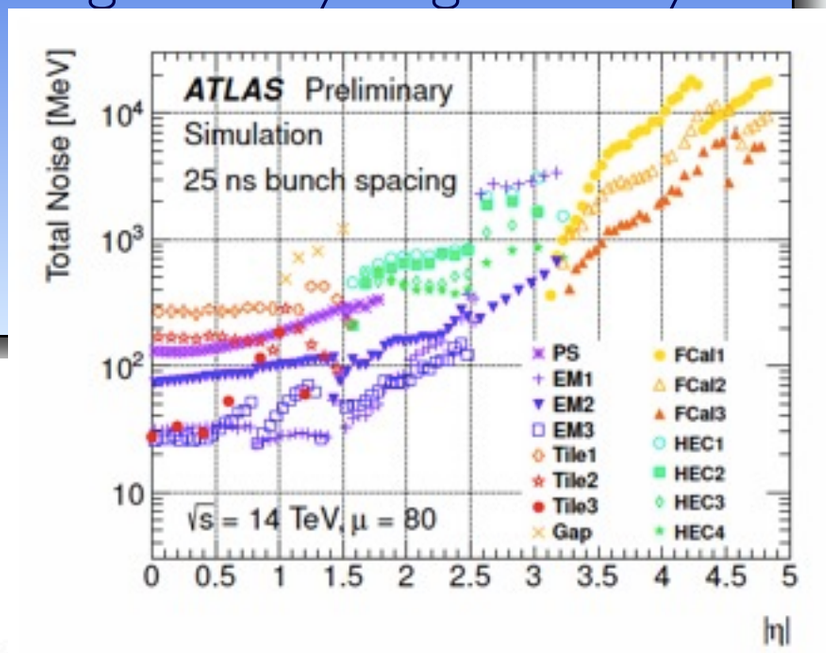


Trigger Towers

(Δη×Δφ=0.1×0.1)

Φ

EM Cluster
(Δη×Δφ=0.1×0.2 or 0.2×0.1)

EM Core
(Δη×Δφ=0.2×0.2)

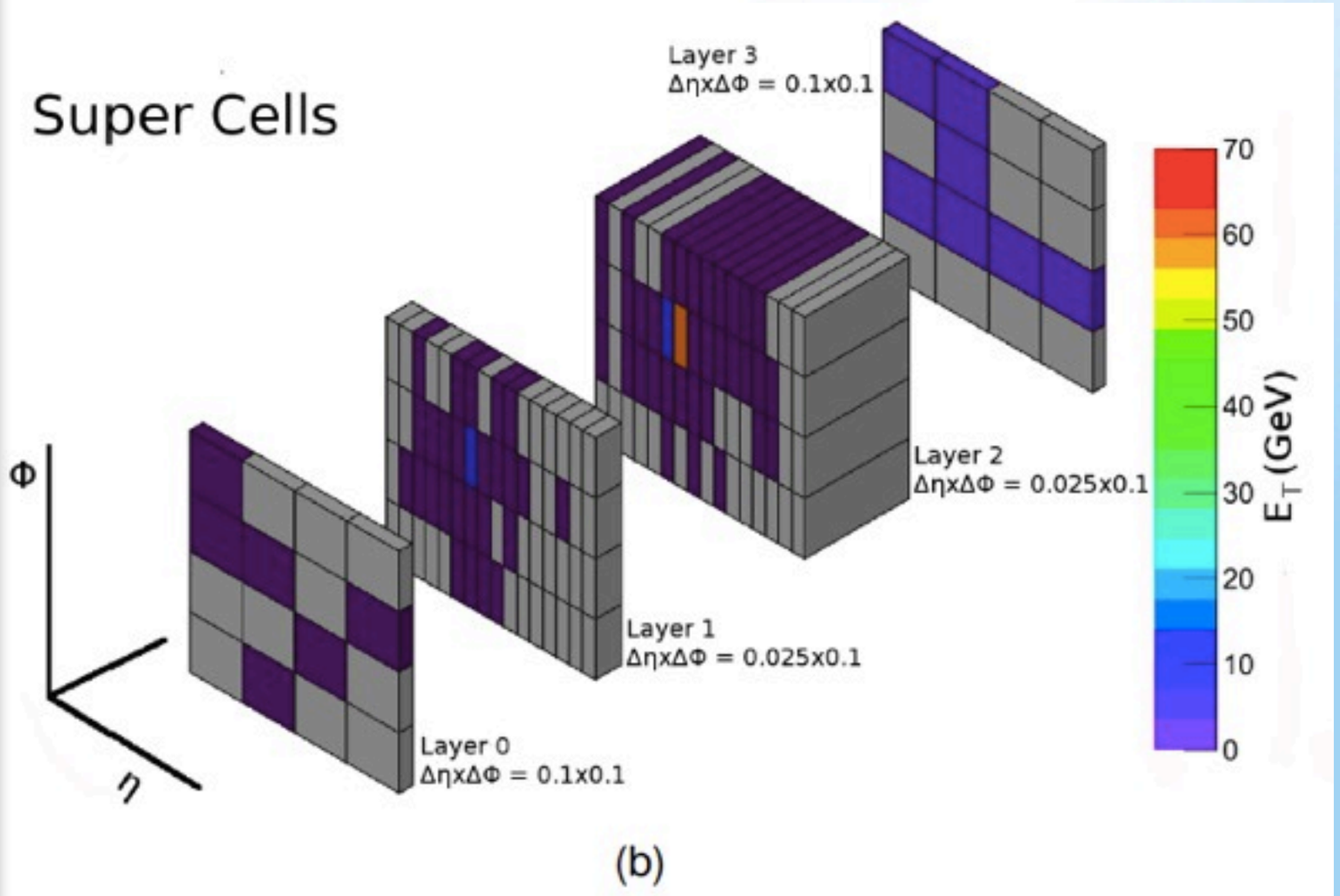
Isolation Ring
(Δη×Δφ=0.4×0.4)

E_T (GeV)

How to improve?

- Supply shower shape information already at Level-1
- Apply rejection algorithms similar to those ones used in the offline reconstruction

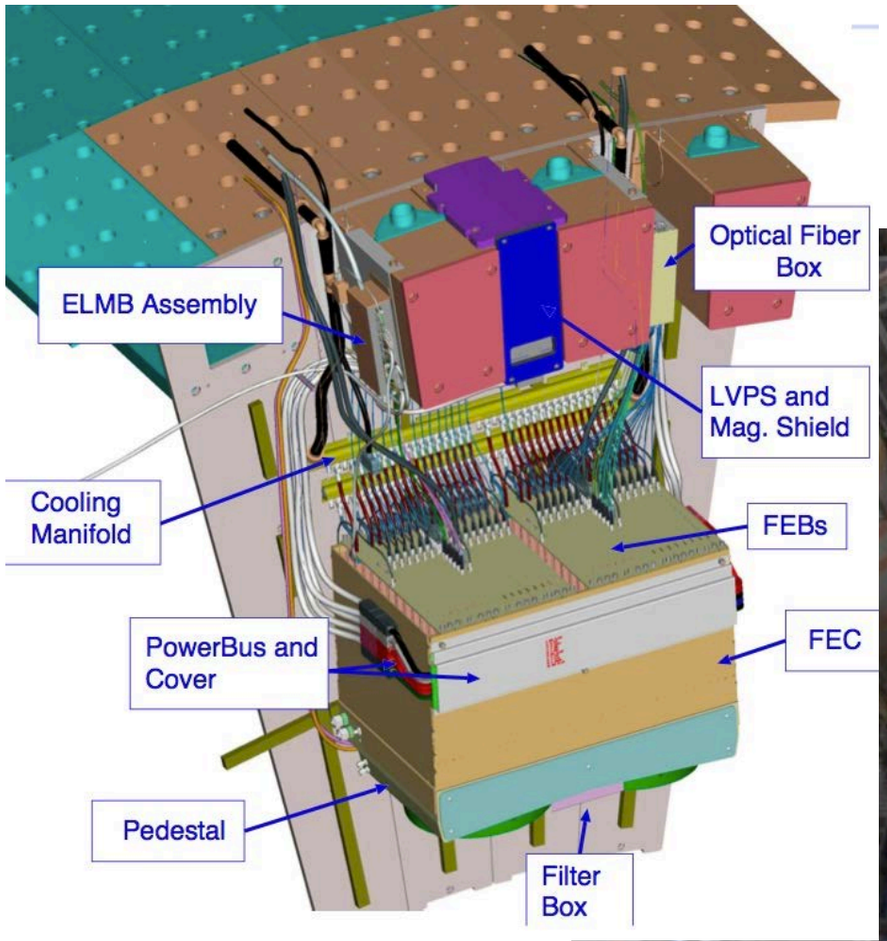
- Higher granularity in **η** (in the 1st and 2nd layer of the EM calorimeter)
- Layer information
- Finer quantization scale:
  - least significant bit: 125 MeV in the 2nd layer and 32 MeV elsewhere
- Possibility to use global event quantities to e.g. correct for pileup fluctuations event-by-event

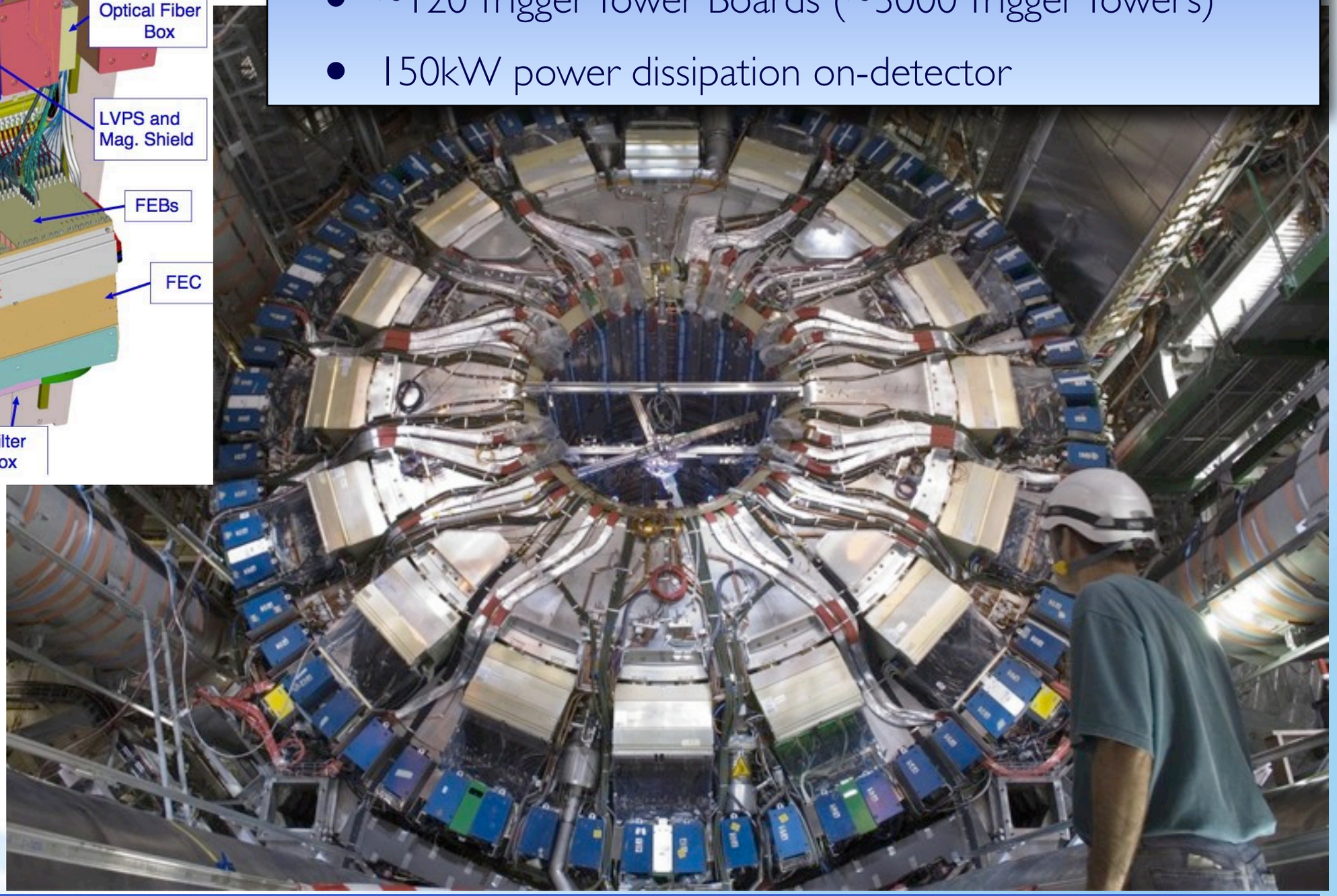


(b)

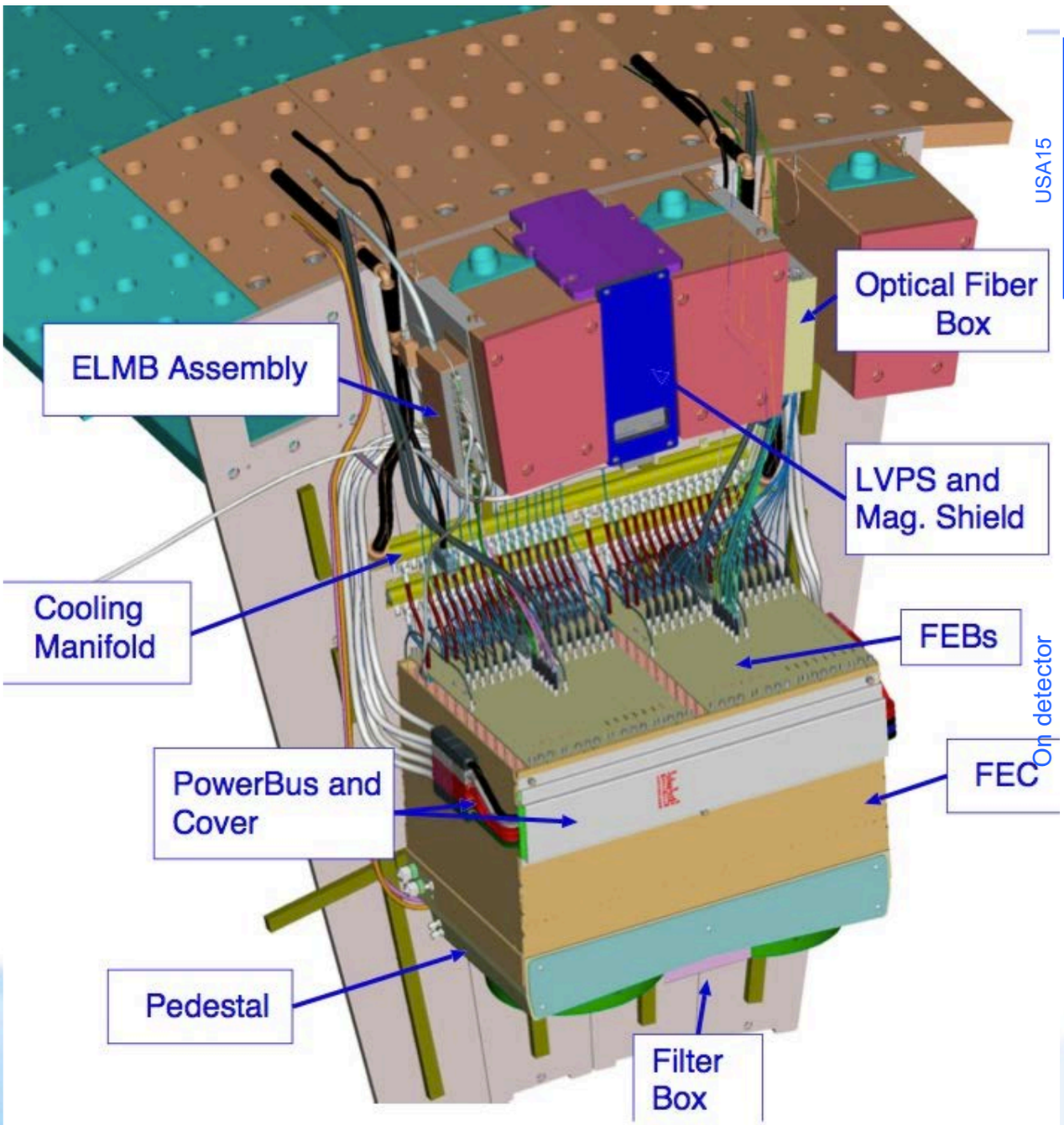
Present LAr Readout

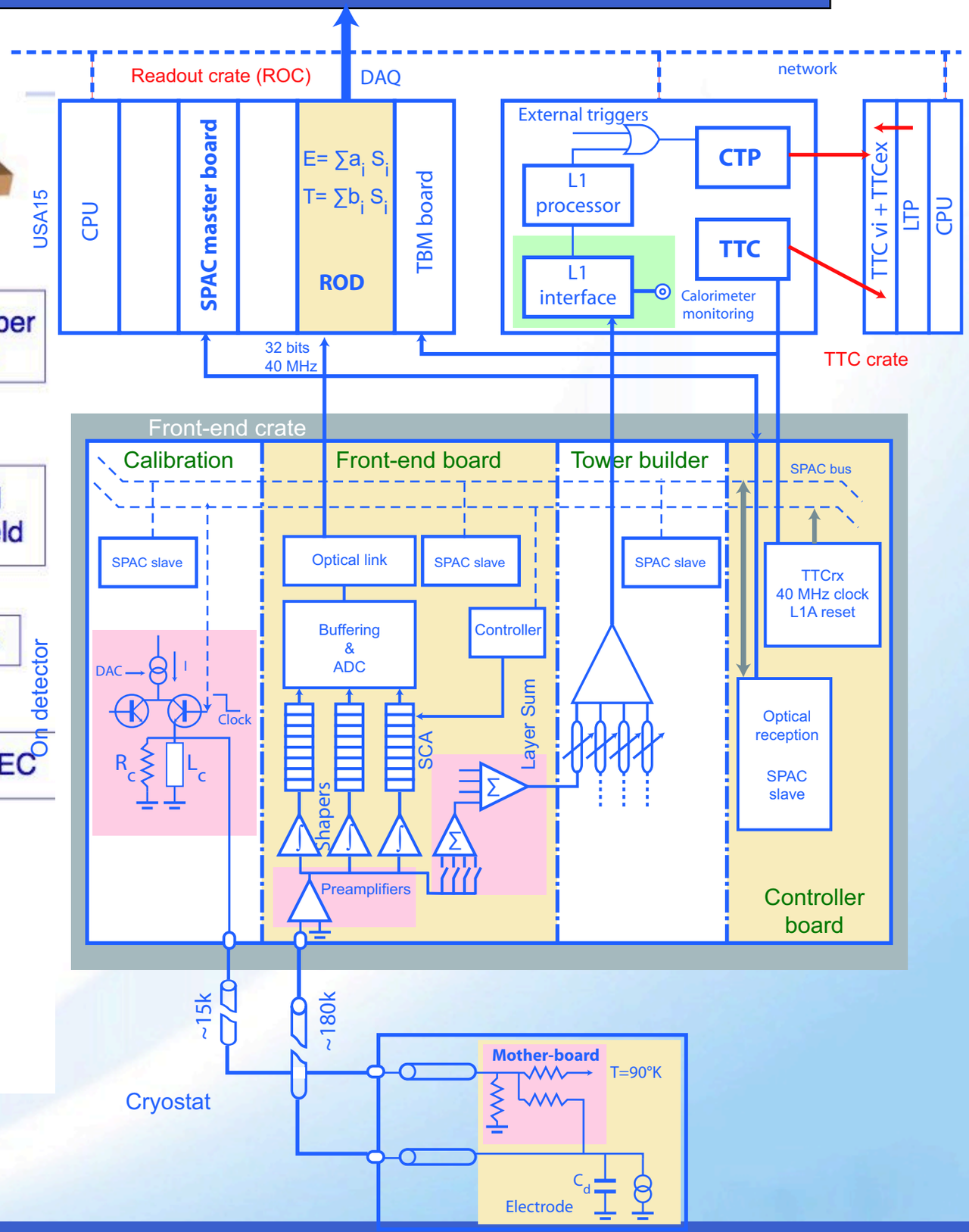
- 58 Front-End crates
- ~1500 Front-End Boards (~180k channels)
- ~120 Trigger Tower Boards (~3000 Trigger Towers)
- 150kW power dissipation on-detector





Present LAr Readout





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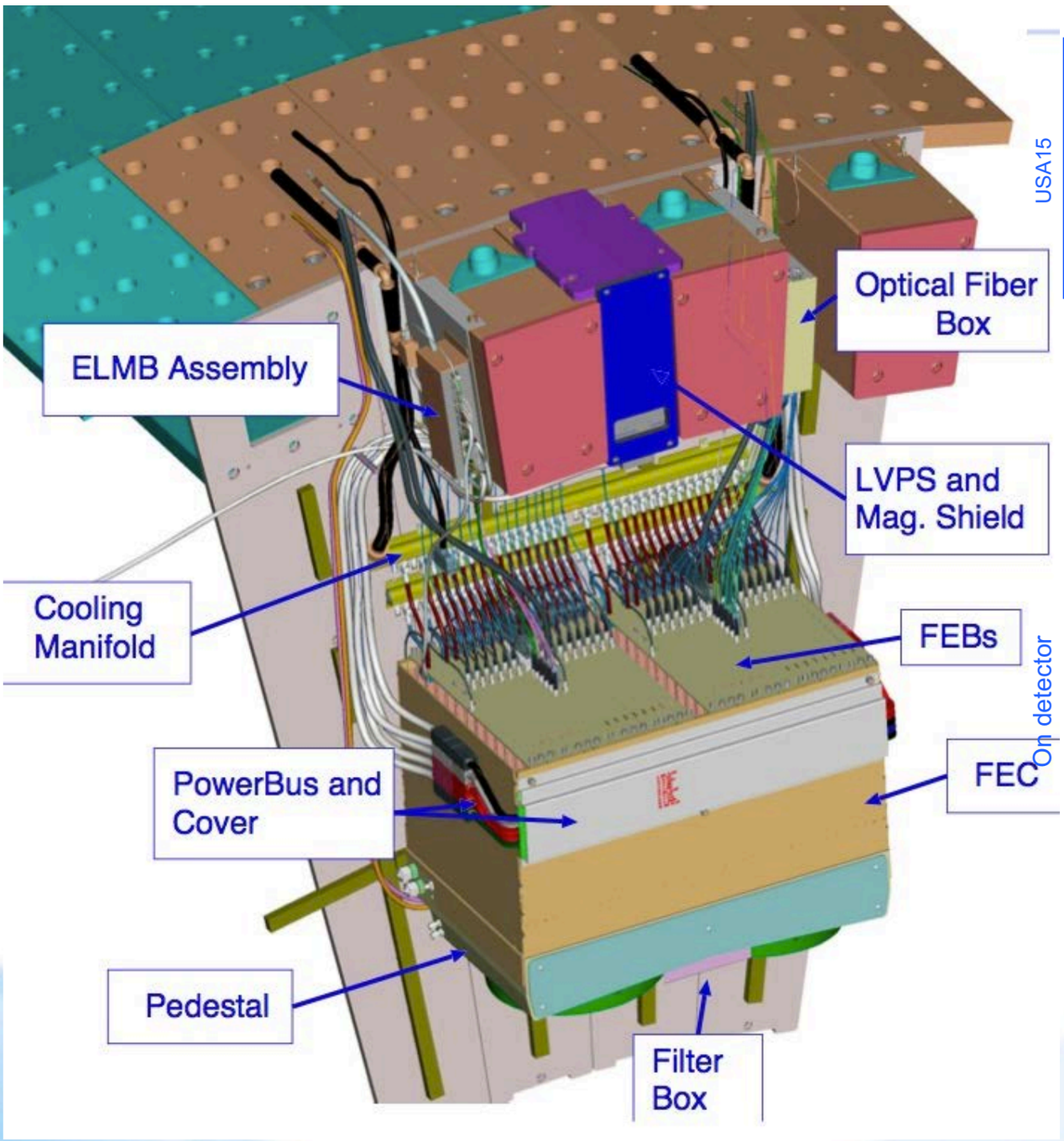
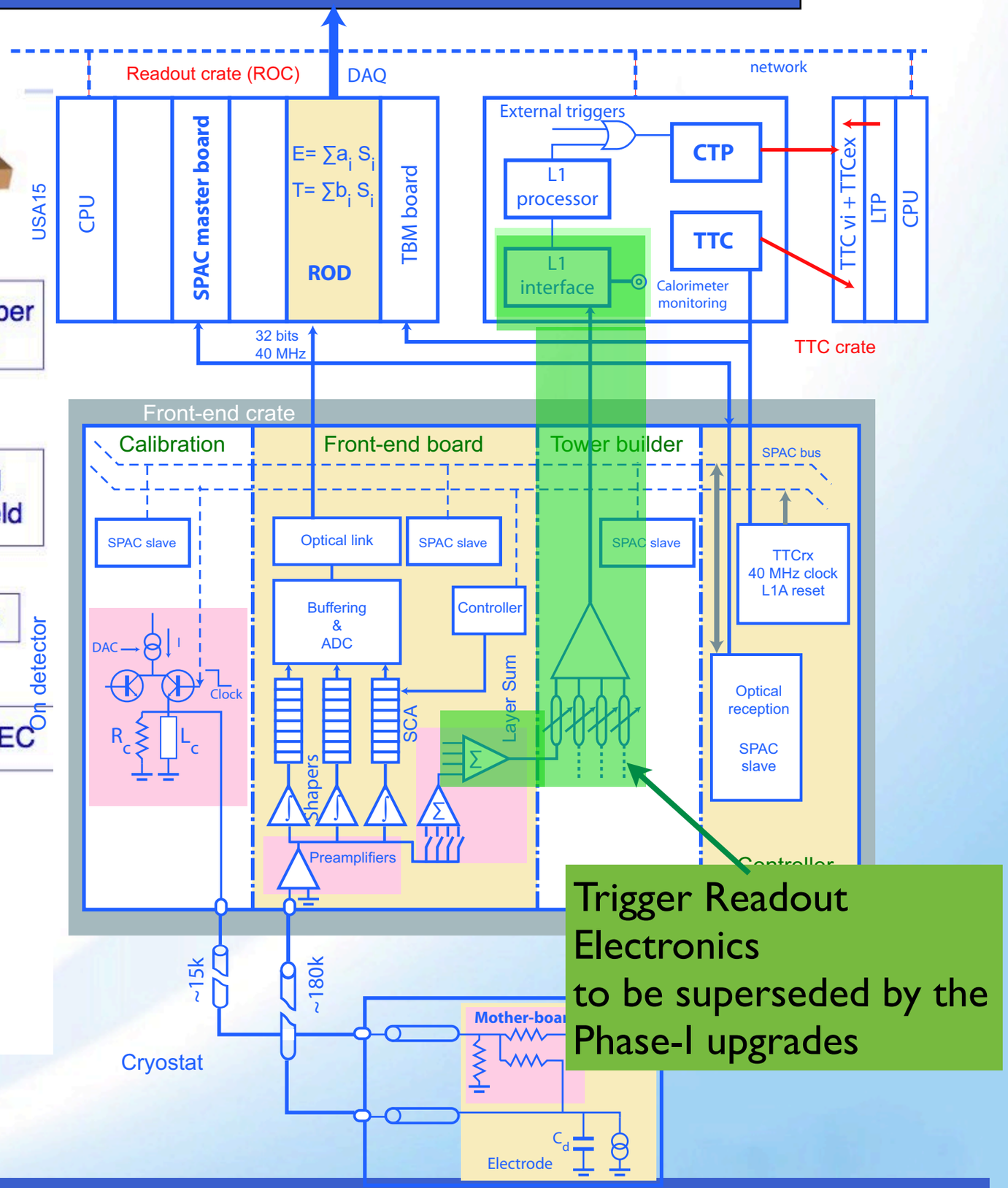
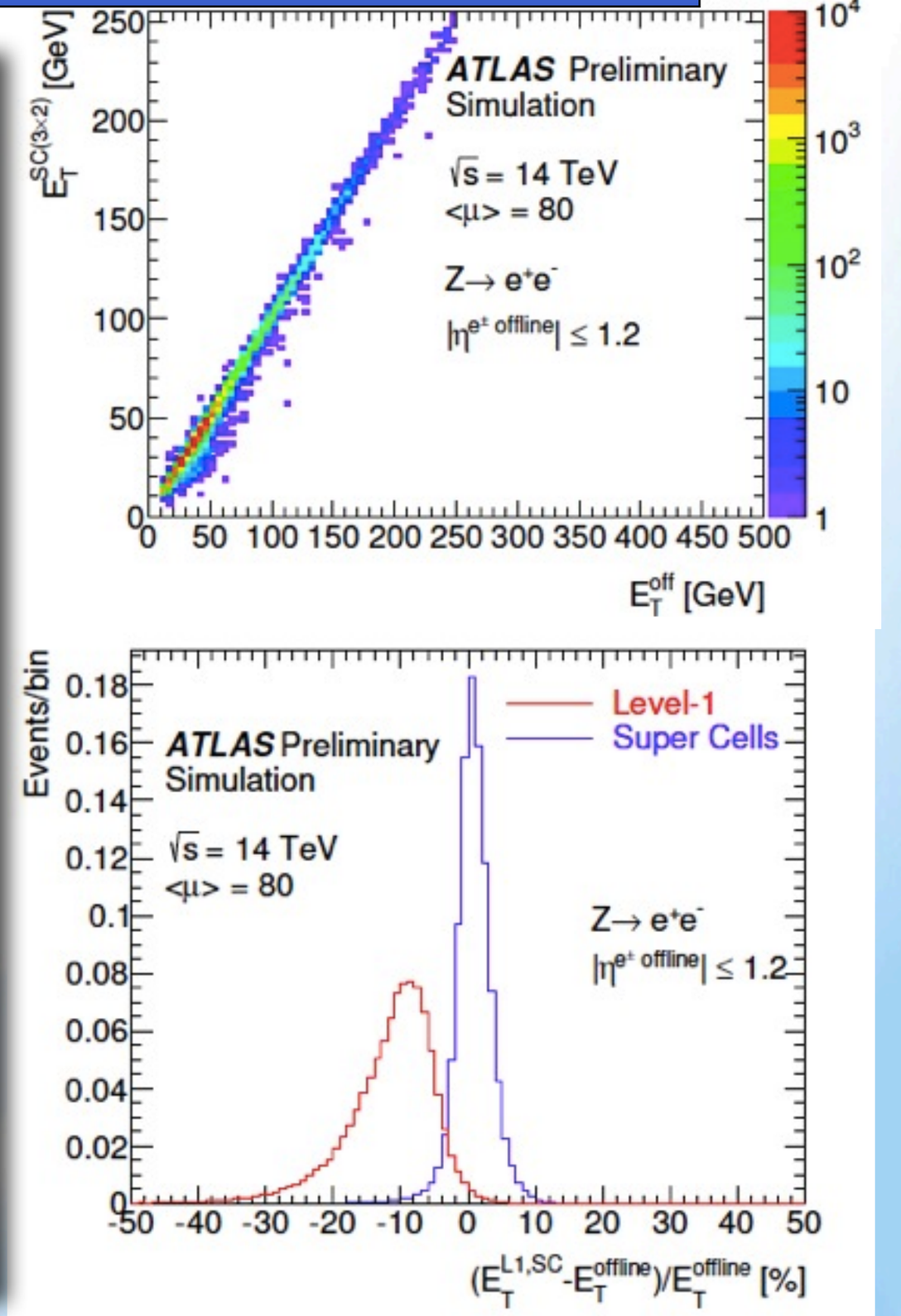




Trigger Readout Electronics to be superseded by the Phase-I upgrades

Expected Performance: EM Triggers

- Super-Cell energy reconstruction:
- 2 Algorithms being studied:
  - Optimal Filtering (OF)
  - Wiener Filters with forward corrections (WF)
- Cluster transverse energy resolution with 3x2 and 5x2 Super-Cells
  - SC energy from the sum of the single calorimeter cells: no second stage noise (small under-estimation)
  - Look-up table corrections with longitudinal weights to correct for leakage and up-front dead material (similar to Level-2 trigger strategies)



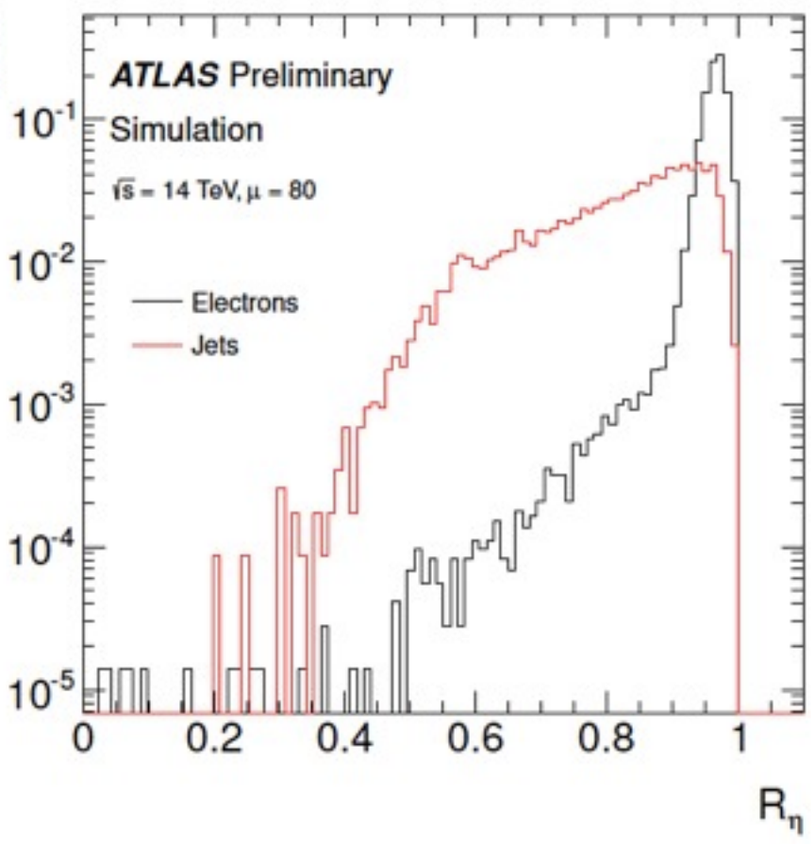
Expected Performance: EM Triggers

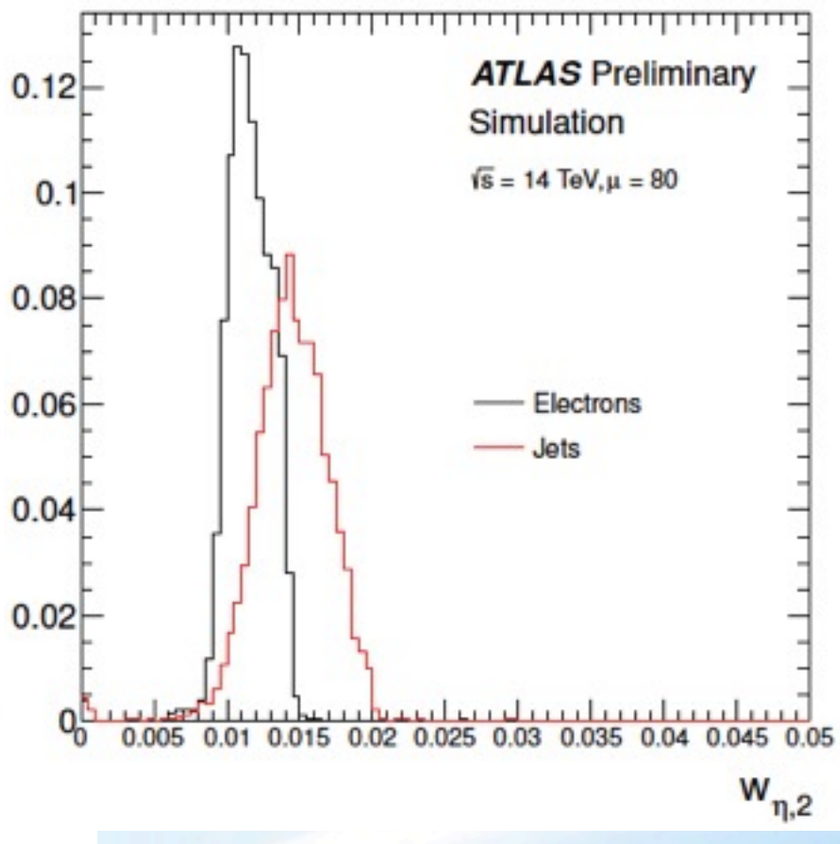
- Shower shape variables:

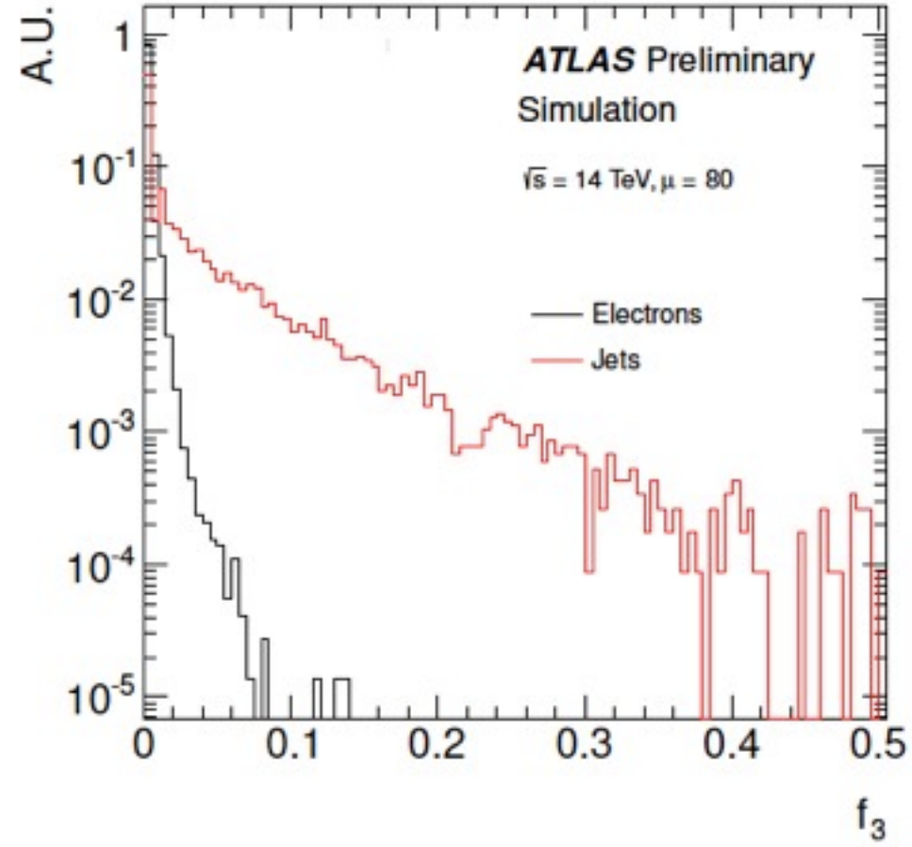
- $$R_\eta = \frac{E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2}}{E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.175\times0.2}}$$

- $$w_{\eta,2} = \sqrt{\frac{\Sigma\left(E^{(2)}_{\mathrm{T}}\times\eta^2\right)_{\Delta\eta\times\Delta\phi=0.075\times0.2}}{E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2}} - \left(\frac{\Sigma\left(E^{(2)}_{\mathrm{T}}\times\eta\right)_{\Delta\eta\times\Delta\phi=0.075\times0.2}}{E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2}}\right)^2}$$

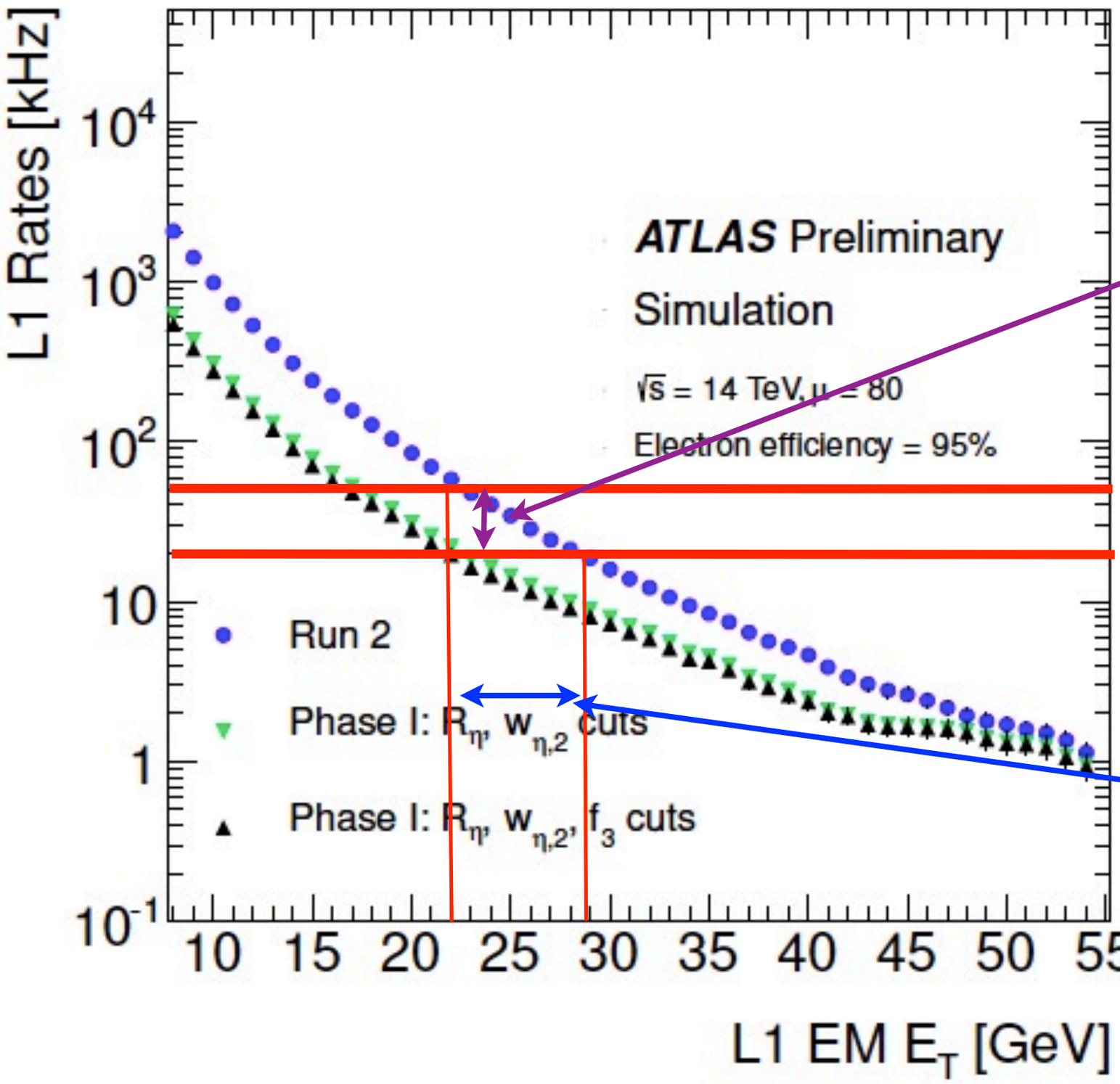
- $$f_3 = \frac{E^{(3)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.2\times0.2}}{E^{(1)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2} + E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2} + E^{(3)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.2\times0.2}}$$







Expected Performance: EM Triggers



Ratio ≃ 2.5

$\Delta E_T \simeq 7$ GeV

Expected Performance: τ-Triggers

- Shower shape variables:

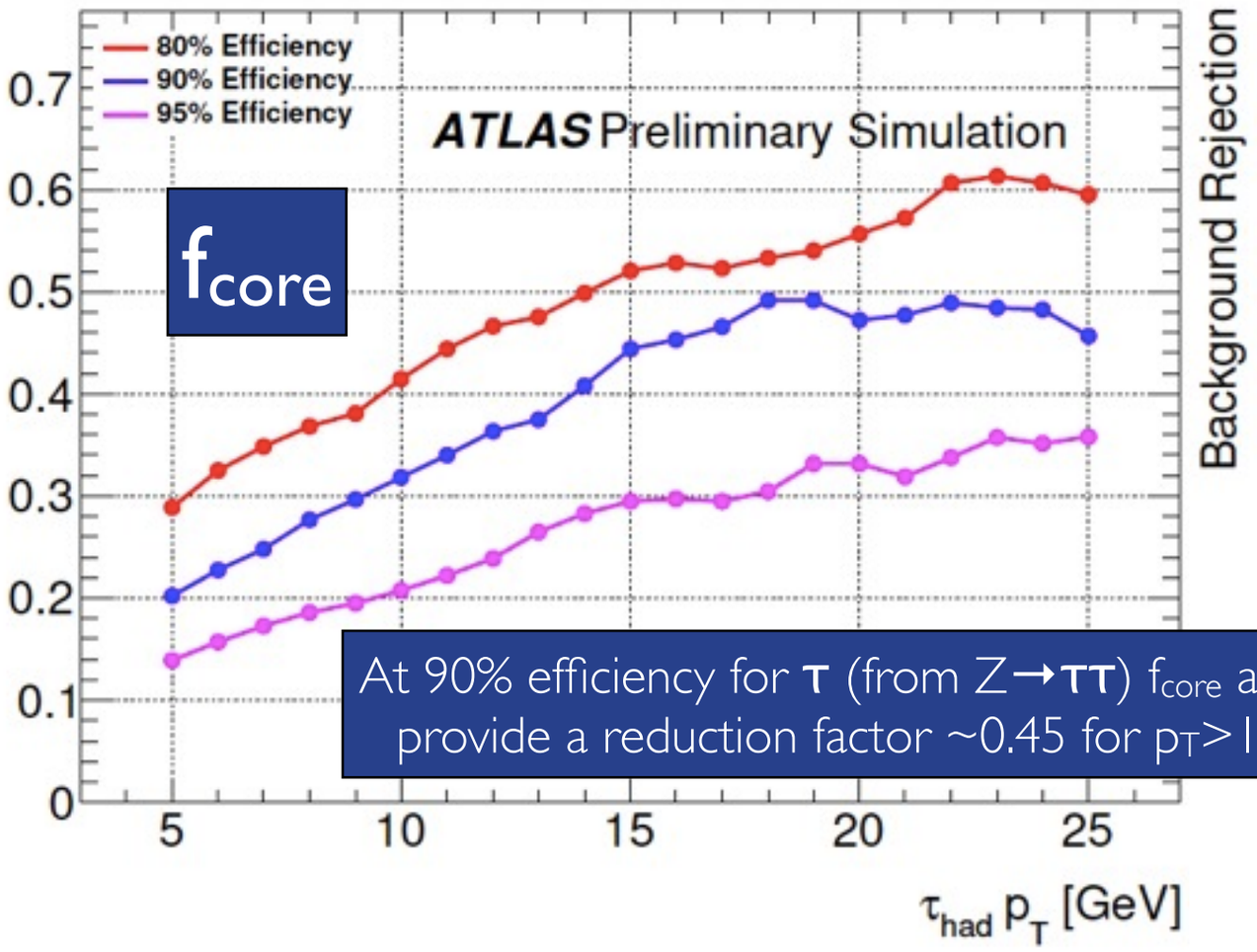
- $$f_{\text{core}} = \frac{E^{(2)}_{\text{T,small area}}}{E^{(2)}_{\text{T,large area}}}$$

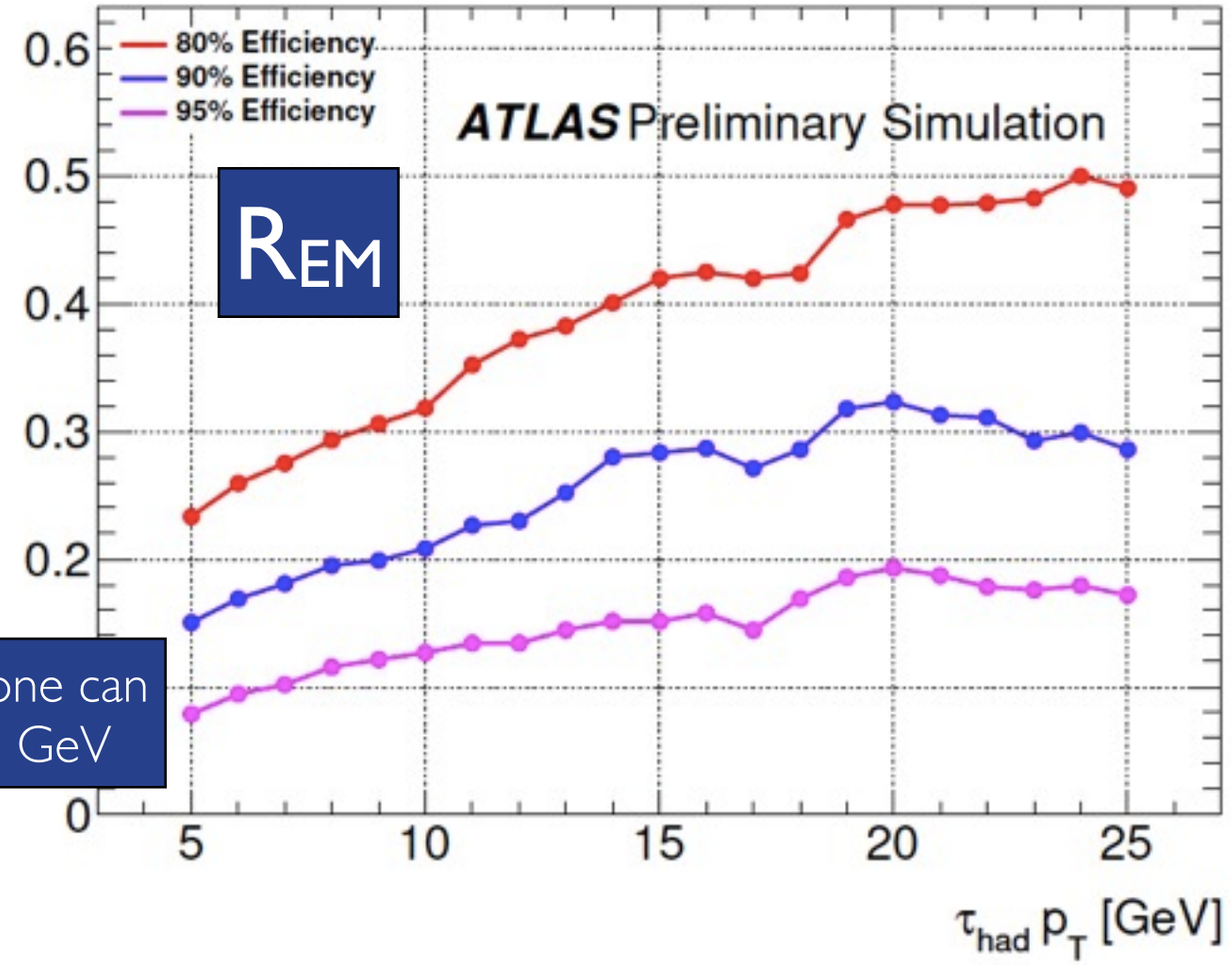
  Δη×Δφ=0.175×0.1

  Δη×Δφ=0.275×0.3

$$R_{\text{EM}} = \frac{\sum_{\text{area}} E_{\text{T}}^{(2)} \times \sqrt{(\eta_{\text{SuperCell}} - \eta_{\text{cluster}})^2 + (\phi_{\text{SuperCell}} - \phi_{\text{cluster}})^2}}{\sum_{\text{area}} E_{\text{T}}^{(2)}}$$

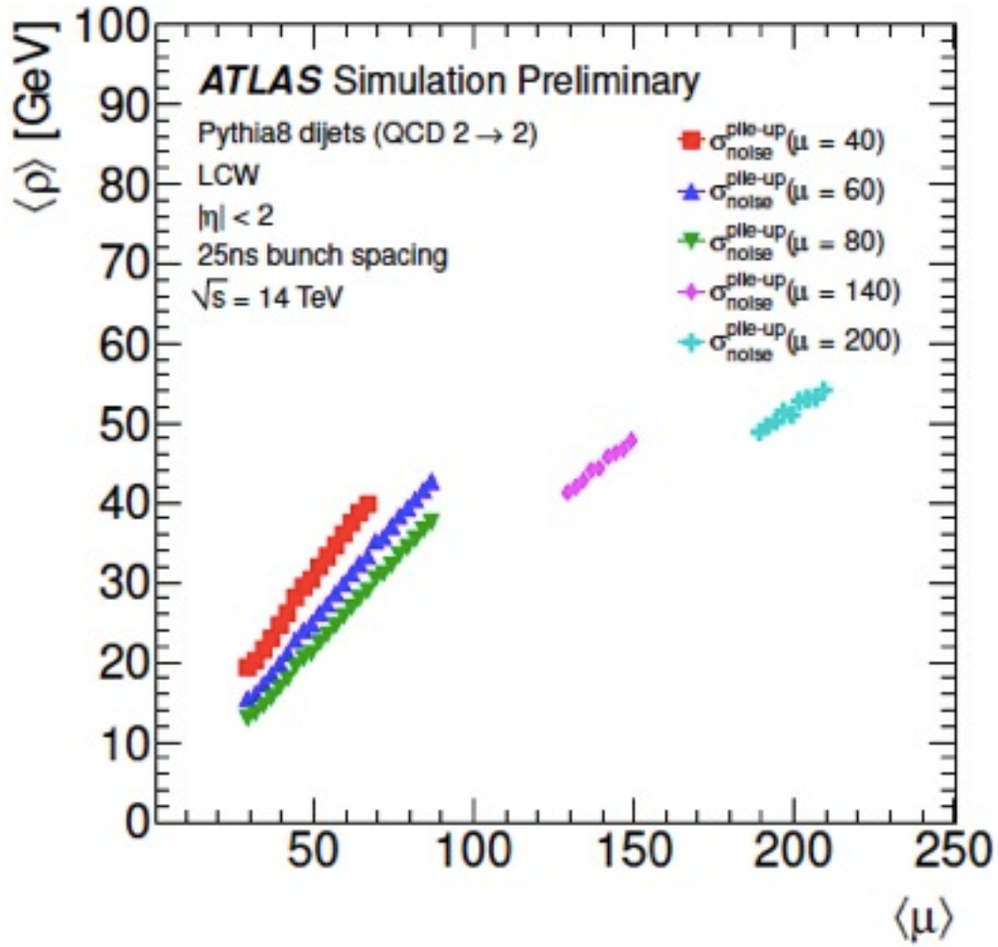
Δη×Δφ≃0.4×0.4

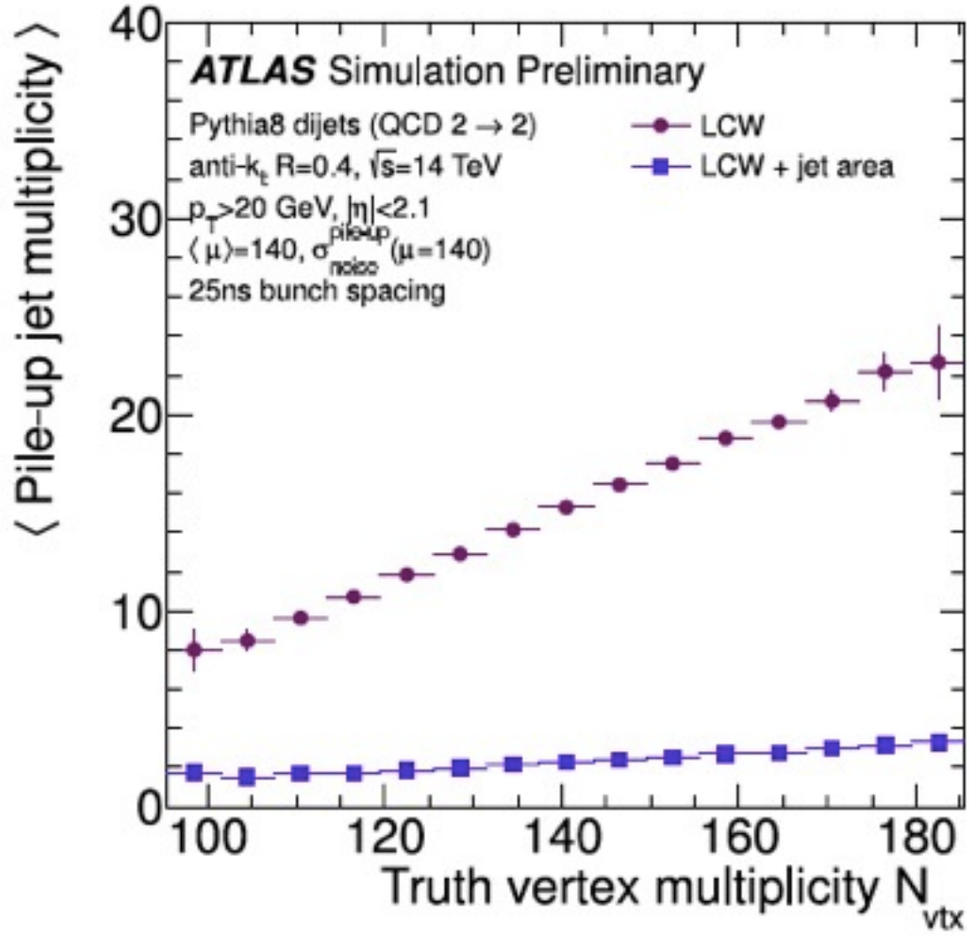




At 90% efficiency for τ (from Z→ττ) f_{core} alone can provide a reduction factor ~0.45 for p_T>15 GeV

Expected Performance: Jets

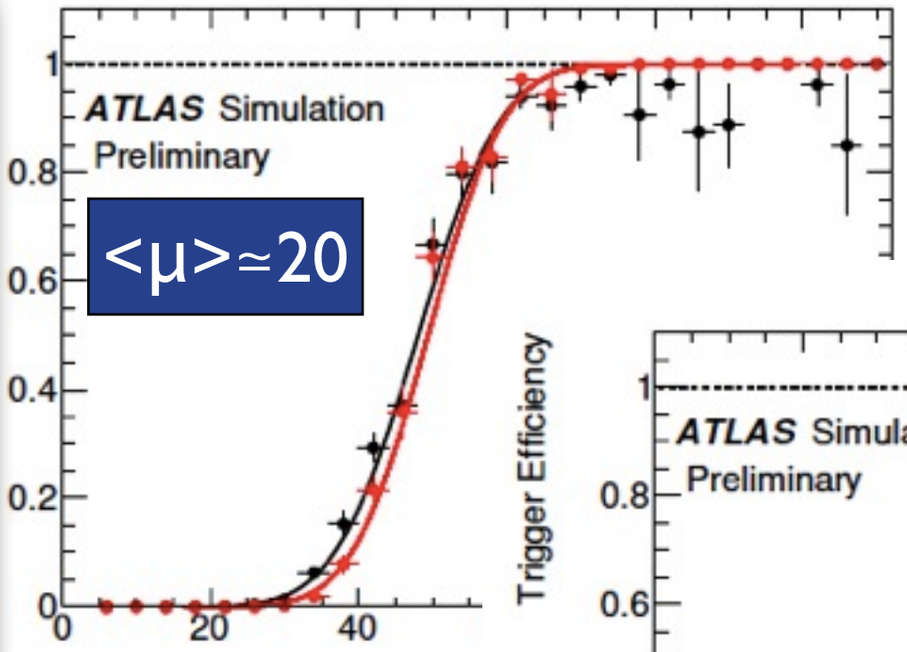




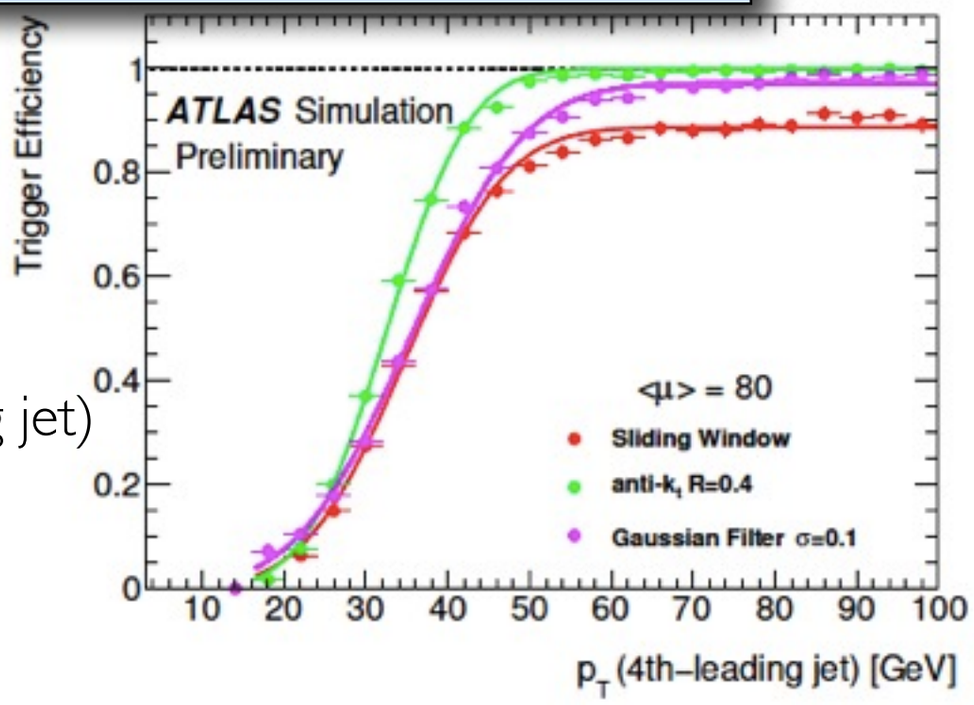
- In-time and out-of-time pileup will lead to significantly increased event activity
  - Jet multiplicity at $<\mu>\simeq 80$ and beyond will suffer dramatically
- Several approaches under investigation profiting from higher precision data (i.e. lower quantization scale), better reconstruction of the jet constituent energies (i.e. off-line energy reconstruction of the "Super Cells") and better jet algorithms

Expected Performance: Jets

- Out-of-time pileup impact energy reconstruction of the jets and bunch-crossing identification
  - ✦ Degradation of the turn-on efficiency curves
- Optimal filtering (or equivalent algorithms) and gaussian filtering [GF] techniques to seed and reconstruct jet energies eliminate dependency on out-of-time pileup (e.g. BC mis-identification)
  - ▸ Using layer information and finer quantization scale



Z'→tt̄
(4th leading jet)

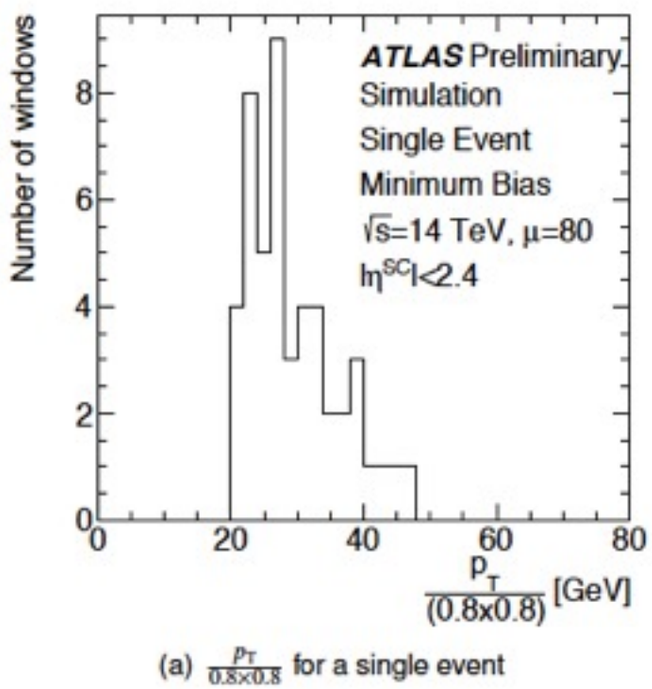


- GF also allows full efficiency recovery of multi-jet triggers which standard sliding window techniques would not provide

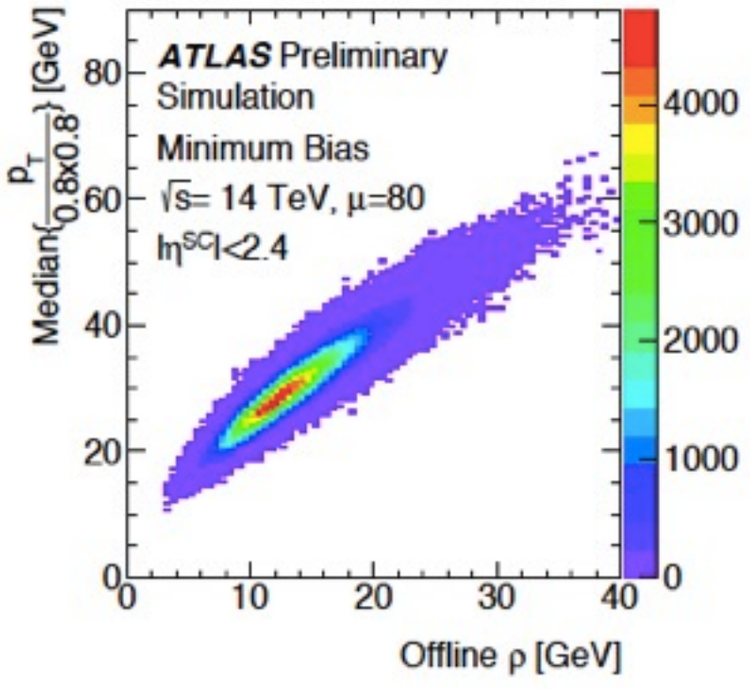
Expected Performance: Jets

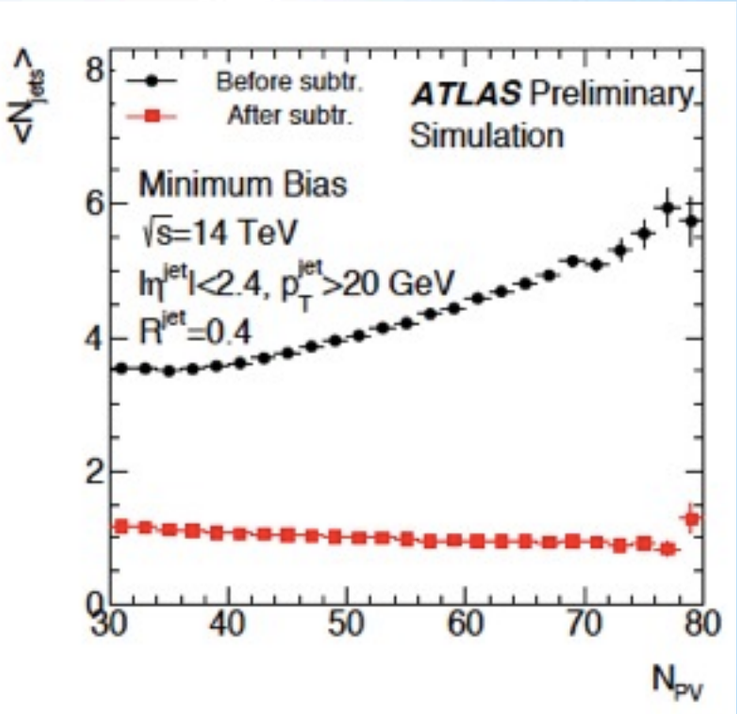
- Subtraction techniques on event-basis are used in offline reconstruction to mitigate the effects of in-time pile-up for both L1 jets and E_T^{miss}
- Two on-going investigations:

- Subtraction based on offline p_T density corrections:
  - $\Delta\eta\times\Delta\varphi$=0.8x0.8 grid
  - $\Rightarrow$ median $\mathcal{M}\{\Sigma p_{T,i}/\Delta\eta\times\Delta\varphi\}$ of the energy density distribution is highly correlated to the offline p_T density
  - Jet p_T corrected by $\mathcal{M}\{\Sigma p_{T,i}/\Delta\eta\times\Delta\varphi\}\times\pi R^2$ where R is the jet radius



(a) $\frac{p_T}{0.8\times0.8}$ for a single event

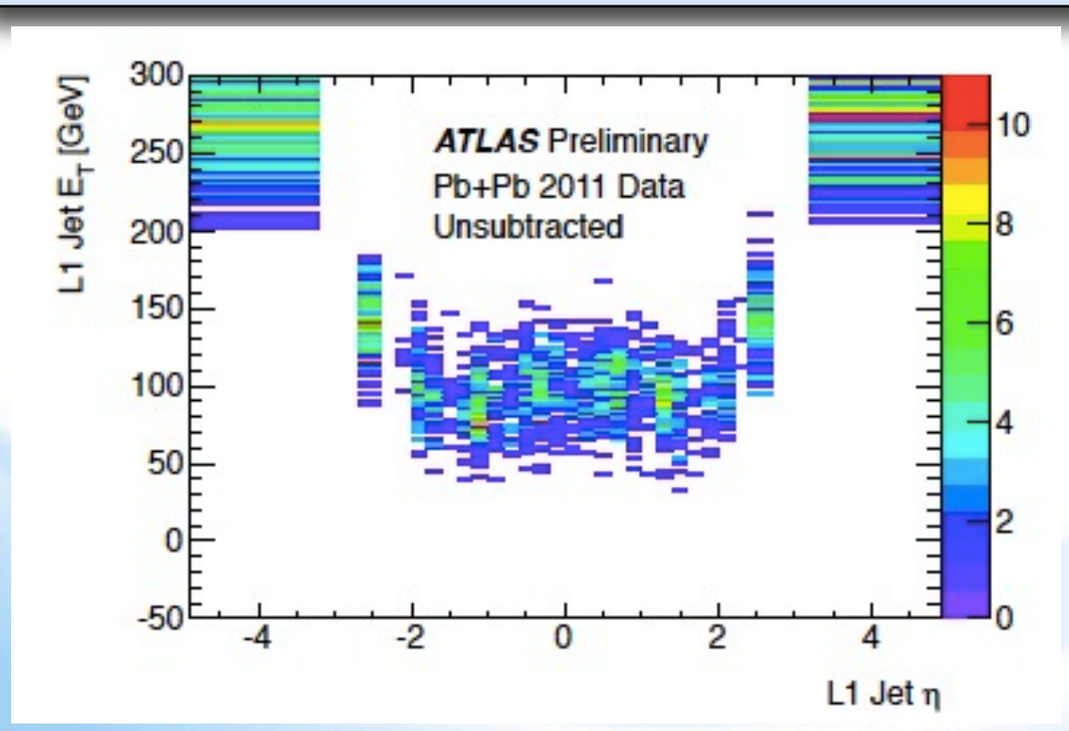


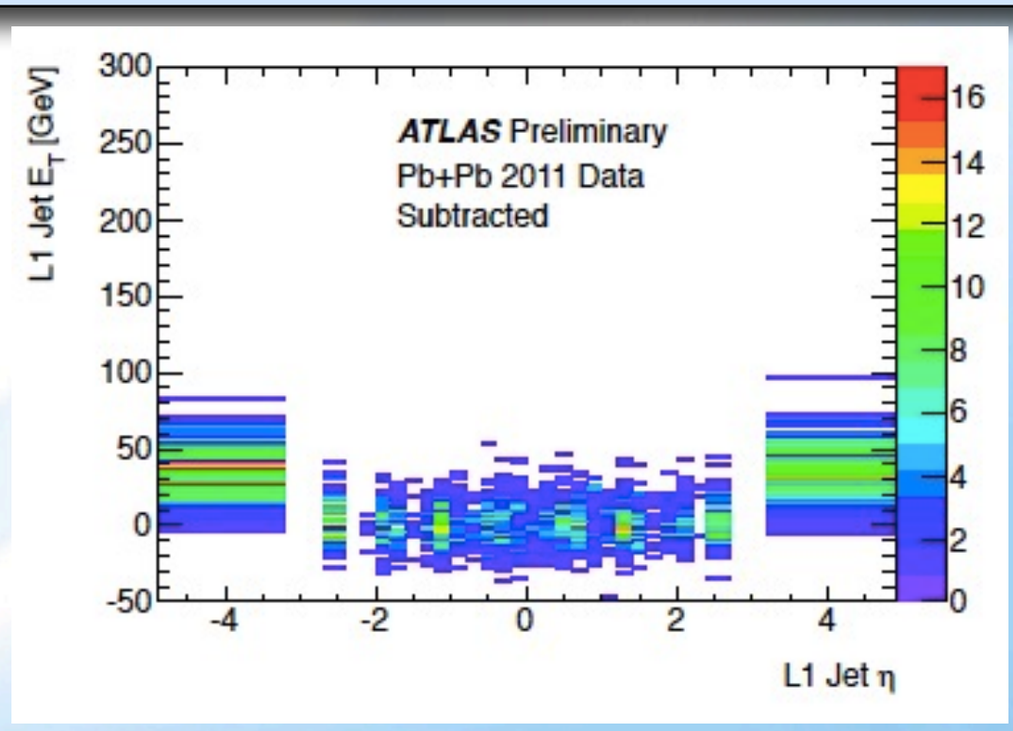


Expected Performance: Jets

- Subtraction techniques on event-basis are used in offline reconstruction to mitigate the effects of in-time pile-up for both L1 jets and E_T^{miss}
- Two on-going investigations:

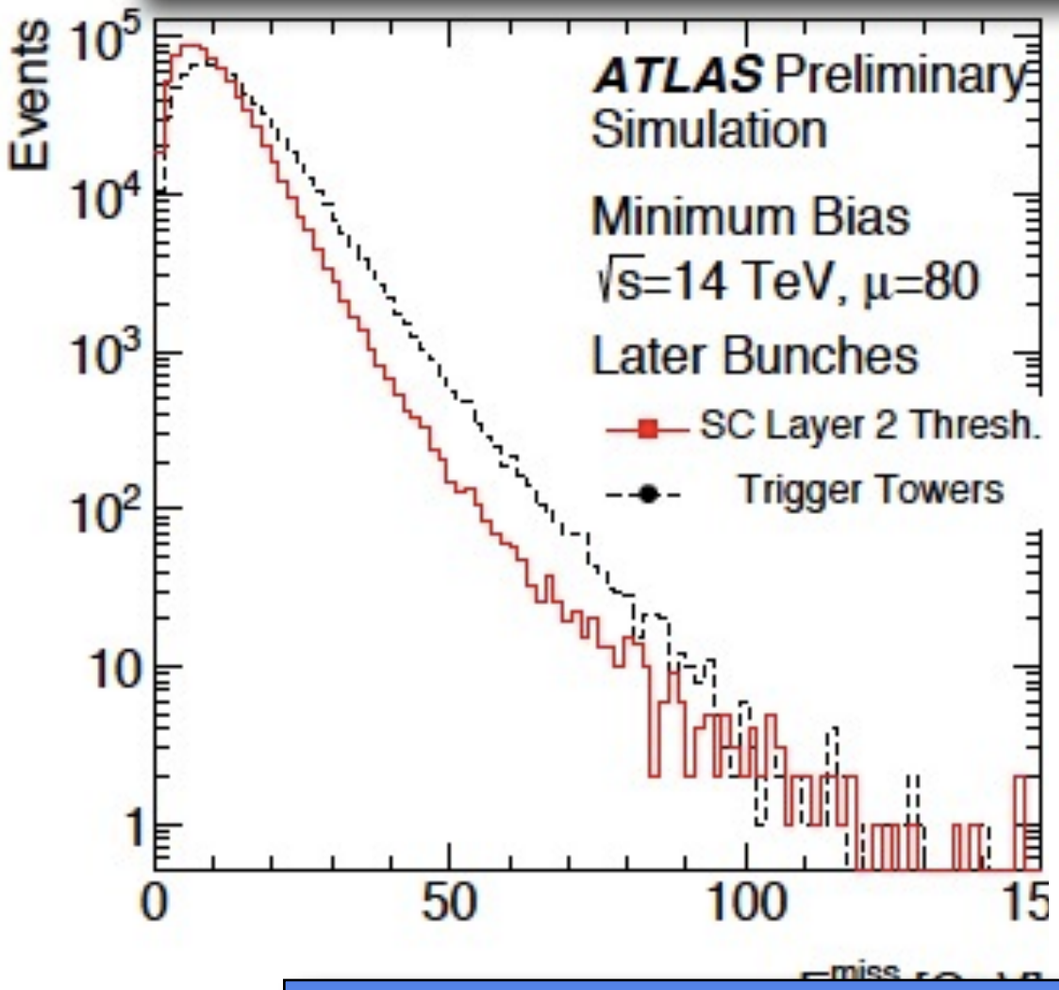
1. Subtraction based on calculation of $\Delta\eta$=0.2 slices ΣE_T:
   - studies underway to remove the spurious rate from underlying event fluctuations in Heavy Ion events without impacting real jets
   - Each of these energies are subtracted from the L1 jet p_T
   - In the central region the subtraction effectively reduce jet rates of ~1.7 for p_T >20 GeV, ~3.7 for p_T >30 GeV, ~60 for p_T >50 GeV

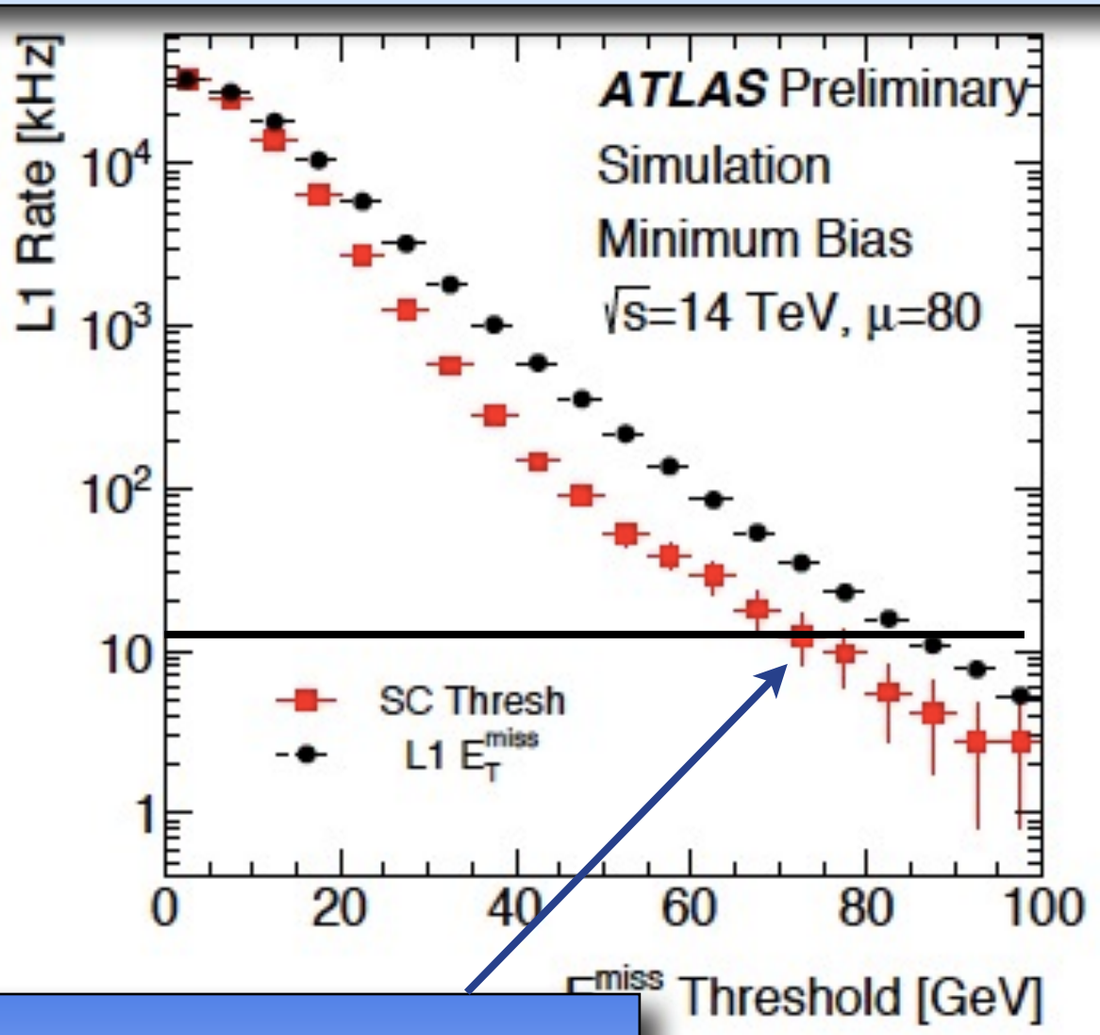




Expected Performance: E_T^{miss}

2. Only Trigger Towers with at least one 2nd layer Super-Cell having E_T above a given threshold ($3\sigma_{TOT}$ total noise) enter the calculation of E_T^{miss}





At 70 GeV reduction of approximately x2

OR

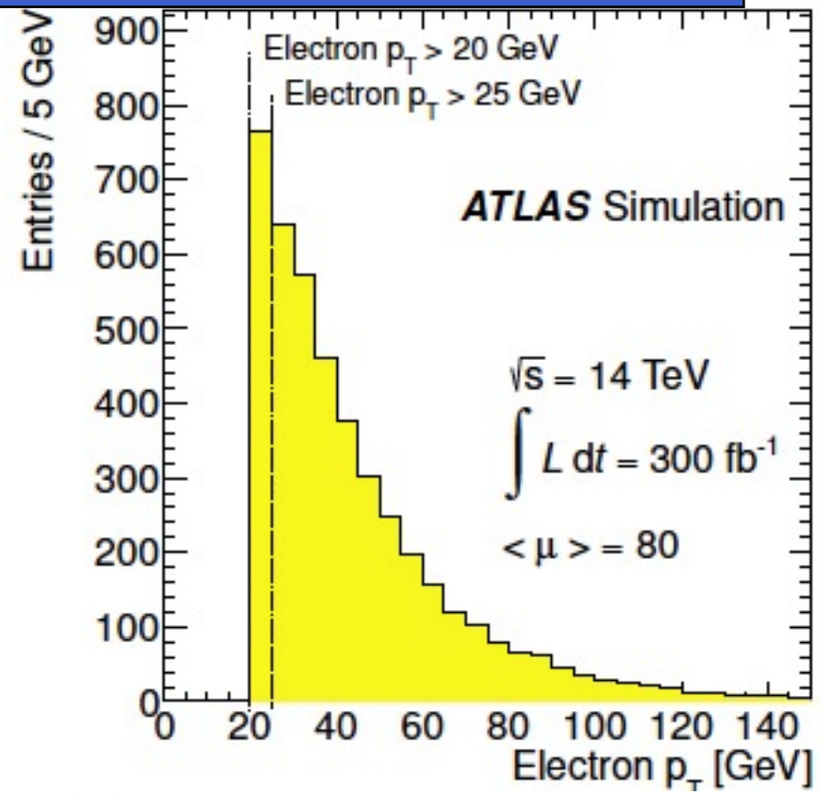
Rates comparable to the 90 GeV L1 E_T^{miss} in Run-2

Examples of impact on Physics: **Higgs Physics**

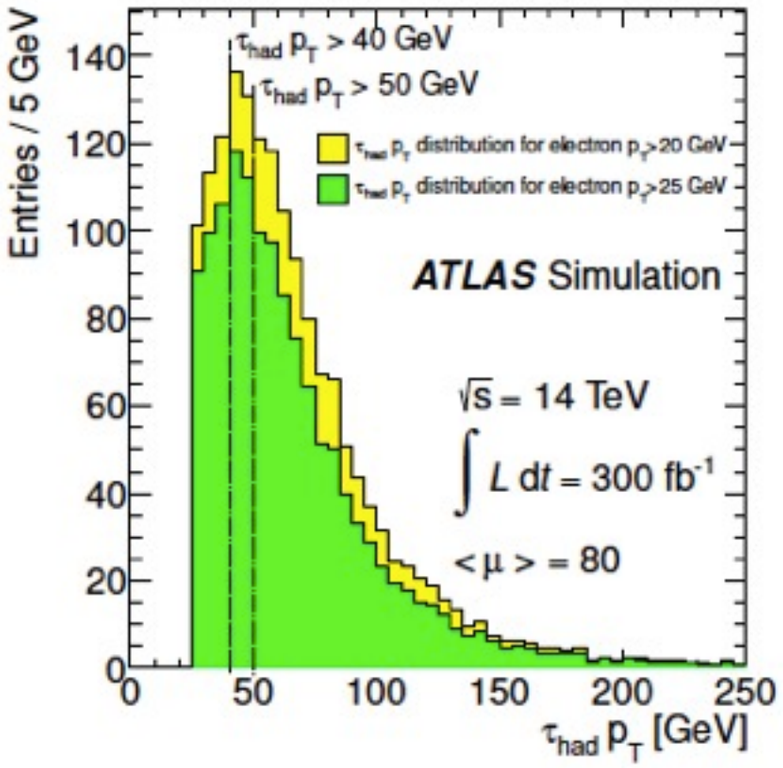
- The measurements of the properties and couplings of the Higgs boson will be an essential part of the LHC physics program during the Phase-I upgrades and beyond.
  - Decay to fermions to explain SM particle masses
  - Coupling to EW gauge bosons
- The Level-1 ATLAS trigger system has to be extremely robust to fulfill the physics program at luminosities up to $\mathcal{L}_{inst} \simeq 3 \times 10^{34} cm^{-2} s^{-1}$
- Maintaining low trigger thresholds on the physics objects into which it decays is mandatory to measure its properties with the highest precision
- (In addition the ability to trigger on low-p_T single lepton is important for a wide range of possible new physics signatures).

Examples of impact on Physics: $H \rightarrow \tau\tau$

- VBF production of the Higgs provides a distinct signature due to the presence of two forward jets
- $H \rightarrow \tau_{lep}\tau_{had}$
  - Single electron trigger
  - Electron + τ_{had}
  - Electron + τ_{had} + jet



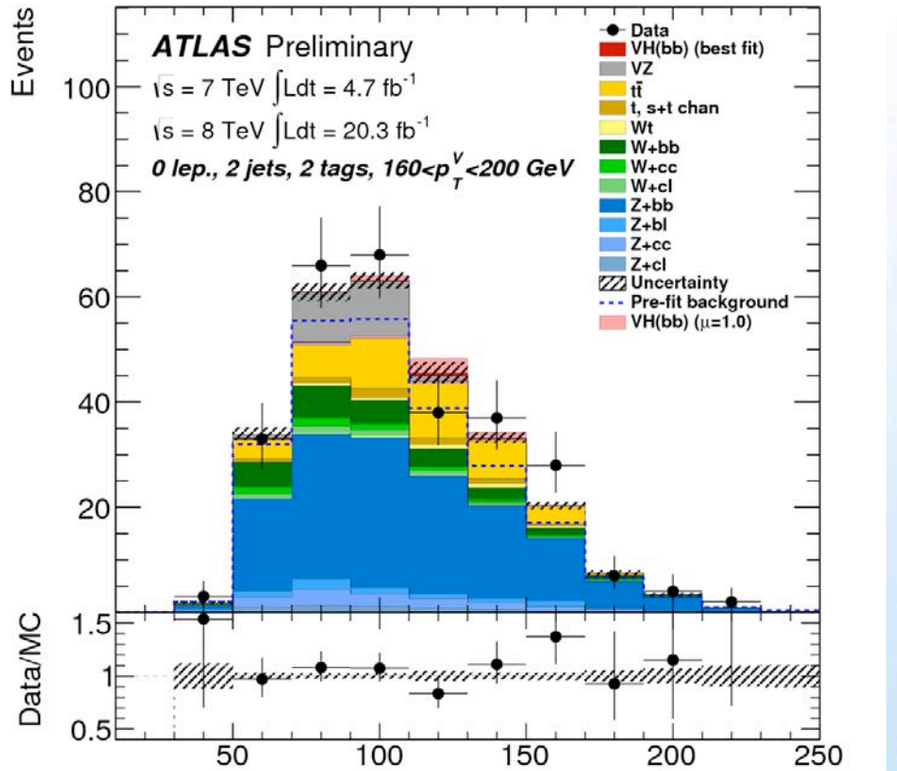
Trigger Requirement	with proposed upgrade $p_T(e) > 20$ GeV $p_T(\tau) > 40$ GeV	without upgrade $p_T(e) > 25$ GeV $p_T(\tau) > 50$ GeV
Electron selection efficiency	$(25.4 \pm 0.2)\%$	$(21.0 \pm 0.2)\%$
Electron and tau selection efficiency	$(7.5 \pm 0.1)\%$	$(4.7 \pm 0.1)\%$
Relative acceptance	1	0.631 ± 0.015

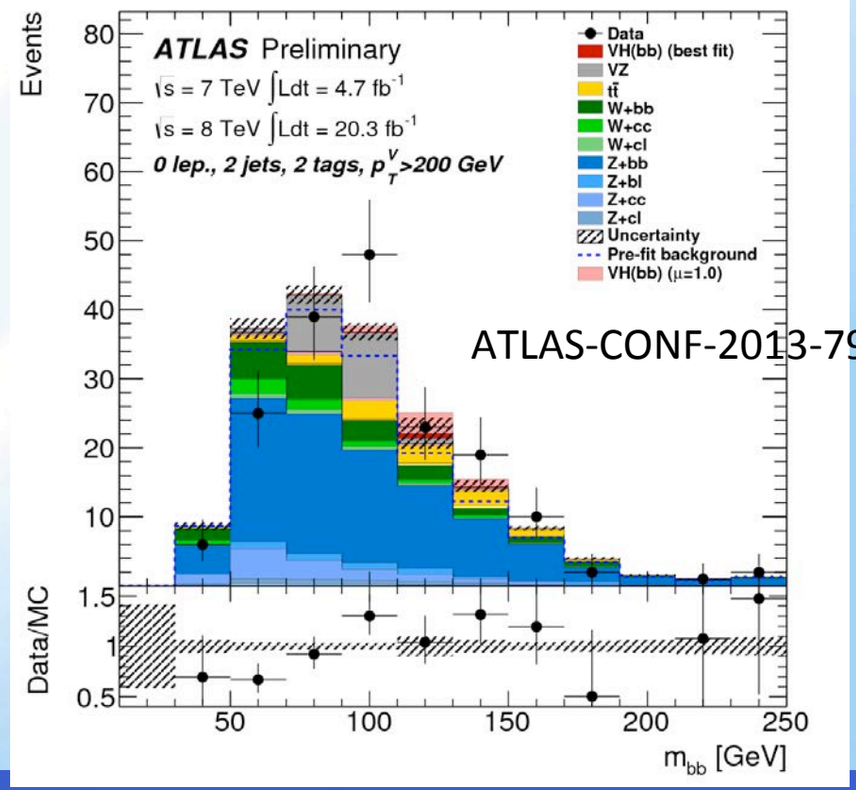


Significant impact on acceptance (~37% signal loss)

Examples of impact on Physics: $WH \to l\nu b\bar{b}$, $ZH \to \nu\nu b\bar{b}$

- Used MC samples for 2012 LHC data to estimate acceptance for different lepton and E_T^{miss} selection
- Current analysis with 3-bins in p_T^V (120-160, 160-200, >200 GeV) + categories for lepton/jet multiplicity to maximize significance
- *0-lepton category relies on E_T^{miss}*
  - 2012 offline selection $E_T^{miss} > 120$ GeV
  - without upgrades: $E_T^{miss} > 200$ GeV
    - ✦ Loss of 72% signal acceptance
  - with proposed upgrade: $E_T^{miss} > 160$ GeV
    - ✦ Reduced acceptance loss to 47%
- *1-lepton category relies on single electrons:*
  - 24% (12%) acceptance loss in the $e\nu e\nu$ ($e\nu\mu\nu$)
  - completely recovered with the proposed upgrade





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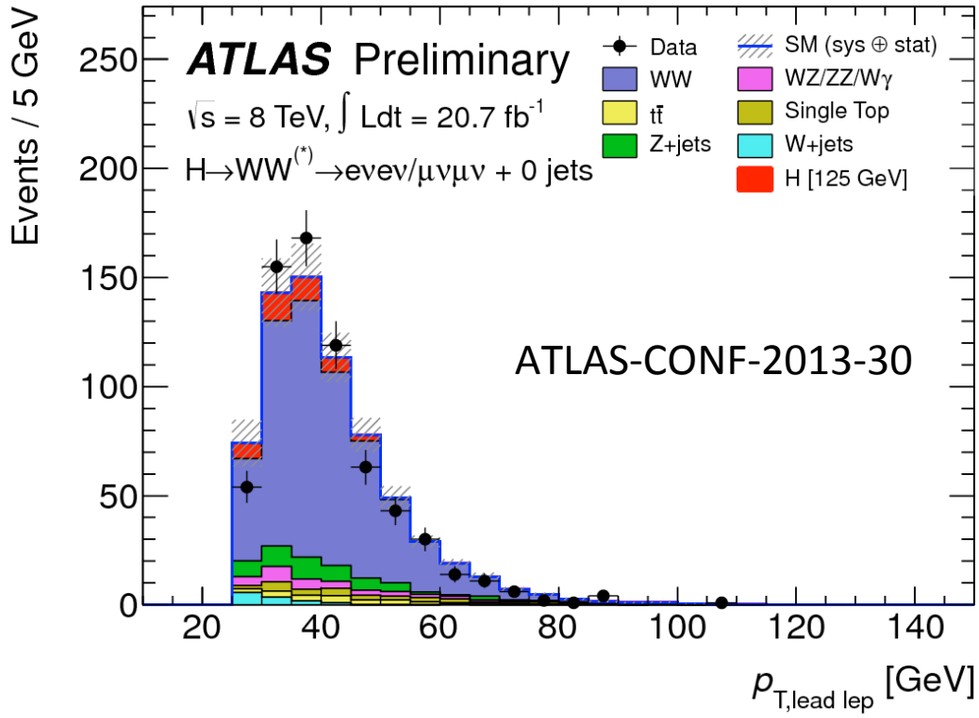
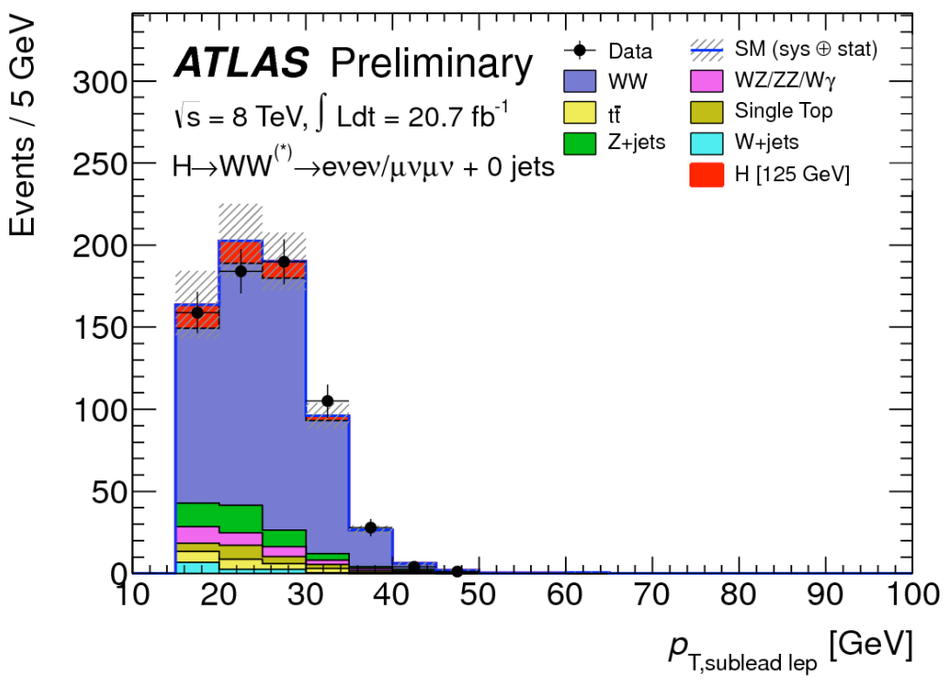
Examples of impact on Physics: H→WW*→eνeν

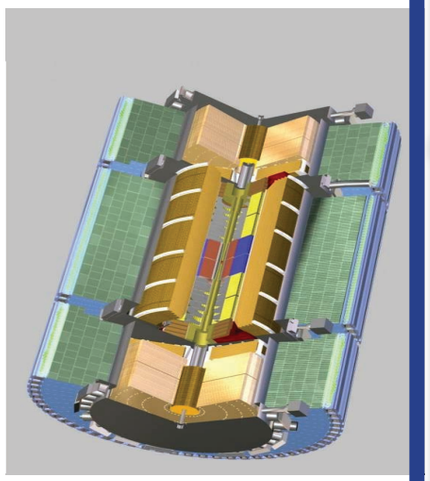
- Used MC samples for 2012 LHC data to estimate acceptance for different di-lepton
- 0-jet category eνeν: di-EM trigger
- 2012 offline selection p_T > 25,15 GeV for leading and sub-leading electrons
- without upgrades: p_T > 22,22 GeV
  - 24% signal acceptance loss
- with proposed upgrade: p_T > 26,16(*)
  - Acceptance recovered almost entirely (3% loss in **eνeν**, 7% in **eνμν**)



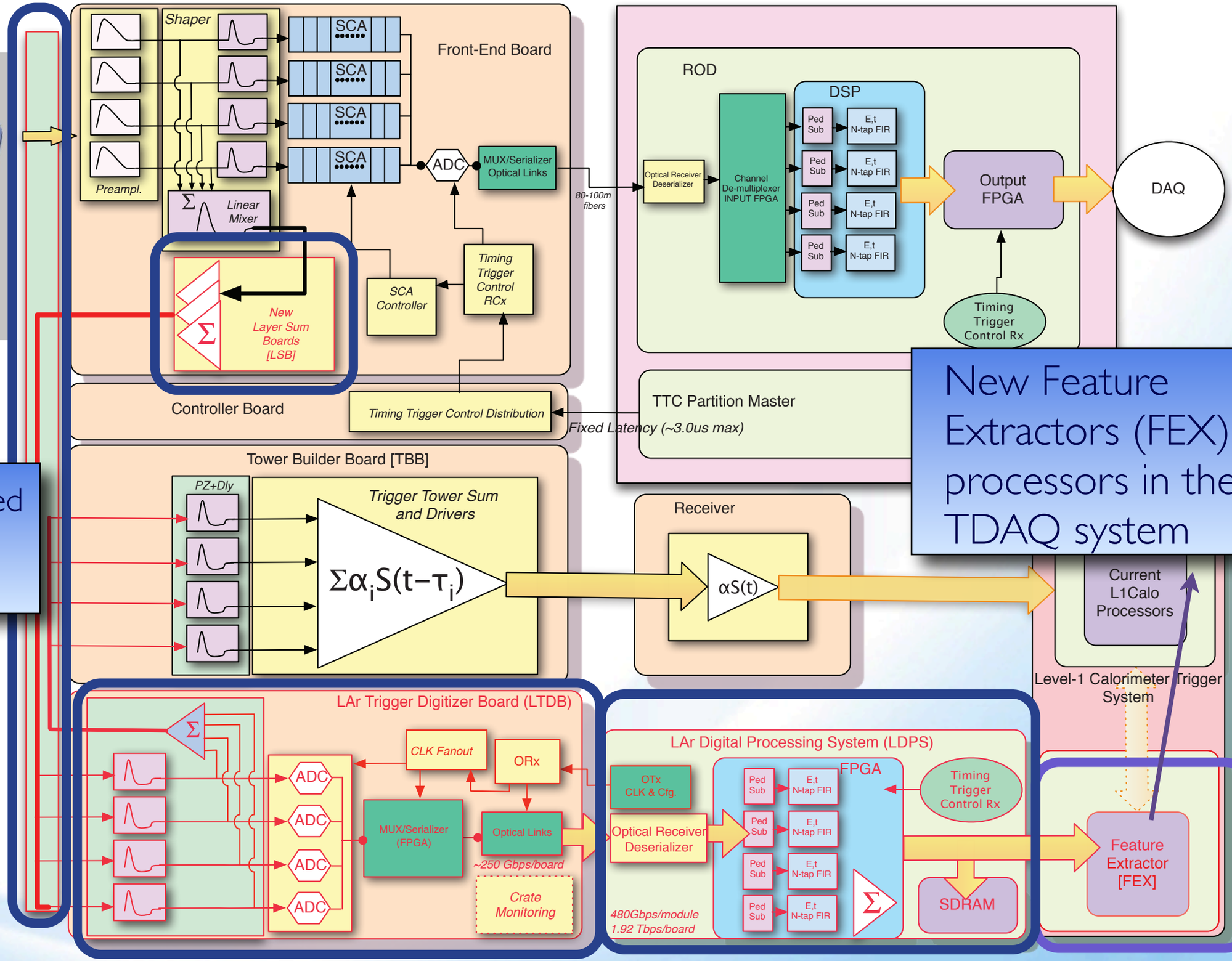


(*) similar rates to the 19,19 GeV in the TDAQ Trigger Menu Table example

Proposed LAr Phase-I Upgrade



New or modified components in blue (LAr TDR)

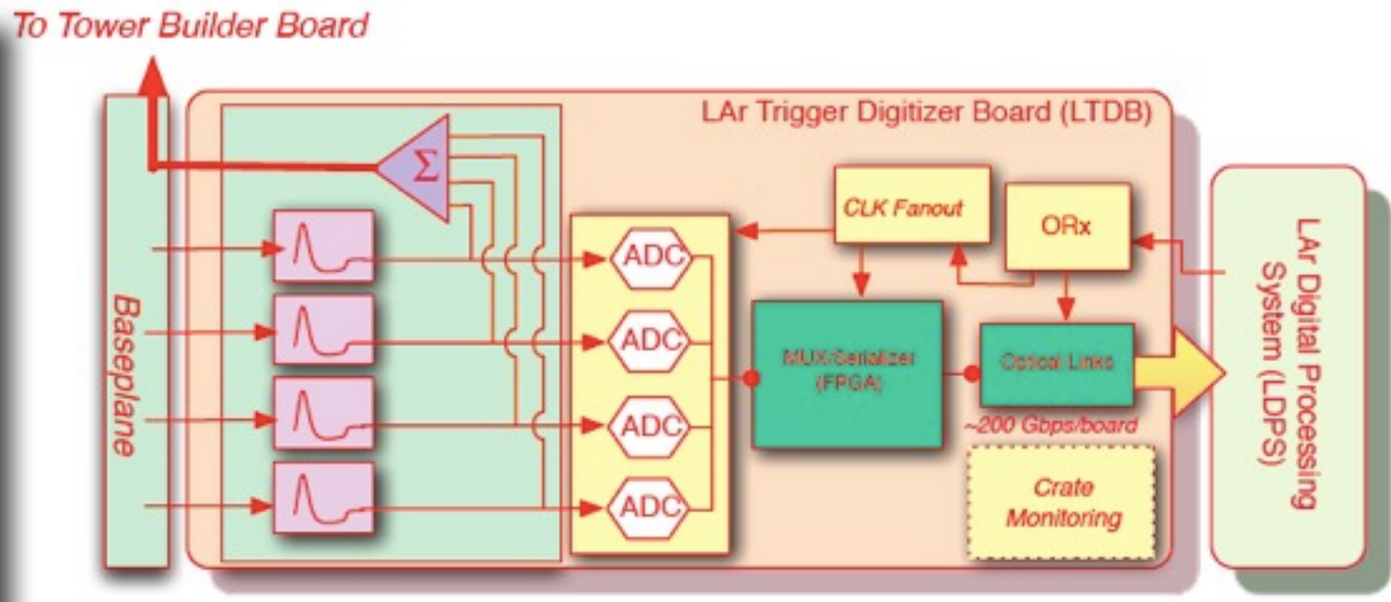


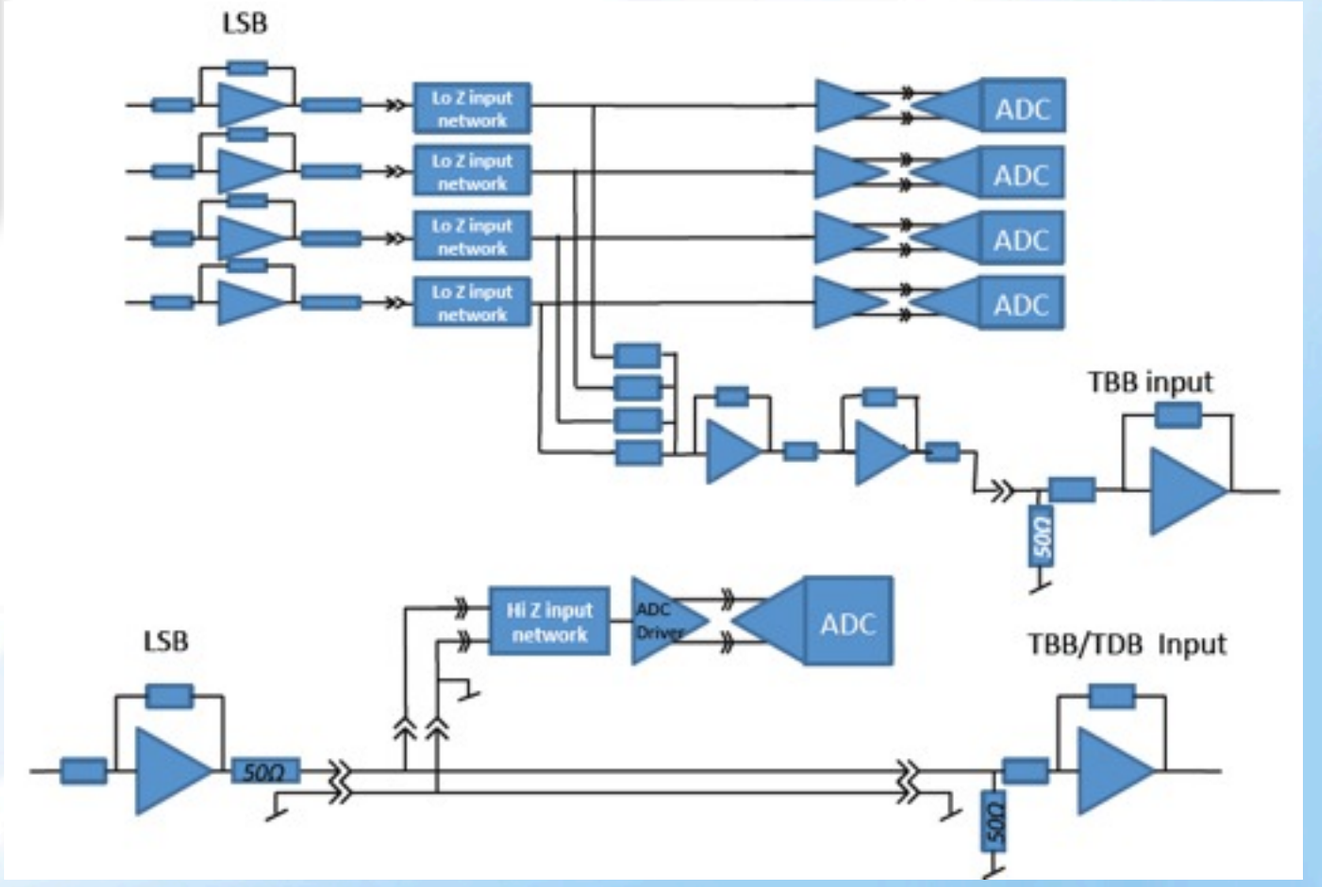
New Feature Extractors (FEX) processors in the TDAQ system

System Architecture: **Front-End**

- 124 **LAr Trigger Digitizer Boards (LTDB)**
- Receive Super-Cell signals from the Front-End Boards LSBs (=Layer Sum Boards), form layer sums to be sent back to the "legacy" Trigger Tower Board
- Each Super-Cell signal is at the same time digitized at 40 MHz and sent to the back-end processing modules on fast links.
- ***Challenge: integrity of the analog signals to preserve performance of the analog system.***

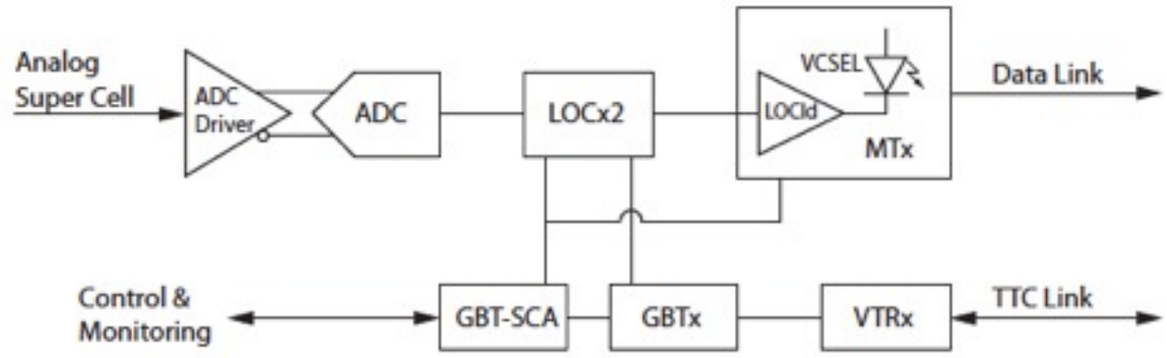
LTDB Type	Channels	LTDB per region
EMB	290	64
EMEC Std	312	32
EMEC Spc 0	240	8
EMEC Spc 1	160	8
HEC	192	8
FCAL 0	192	2
FCAL 1	192	2
Total		124





System Architecture: **Front-End**

- Digital circuitry of the LTDB:
- up to 320 channels ADCs/board
- Interface/serializer ASIC (LOCx2)
- Optical transceivers to transmit the signal off-detector
- GBT-based transceivers to distribute on board CLK/ TTC information



- Choice of components (ASIC development vs. COTS) is among the top priorities for 2014-2015:
  - ADC
  - Serializer ASIC (LOCx2 or GBT-based)
  - Optical transmitters (COTS vs. custom development)
- Challenges:
  - Moderate radiation environment
  - Power Budget
  - Tight Mechanical Integration on Board
- Full-scale prototypes being built for system integration studies

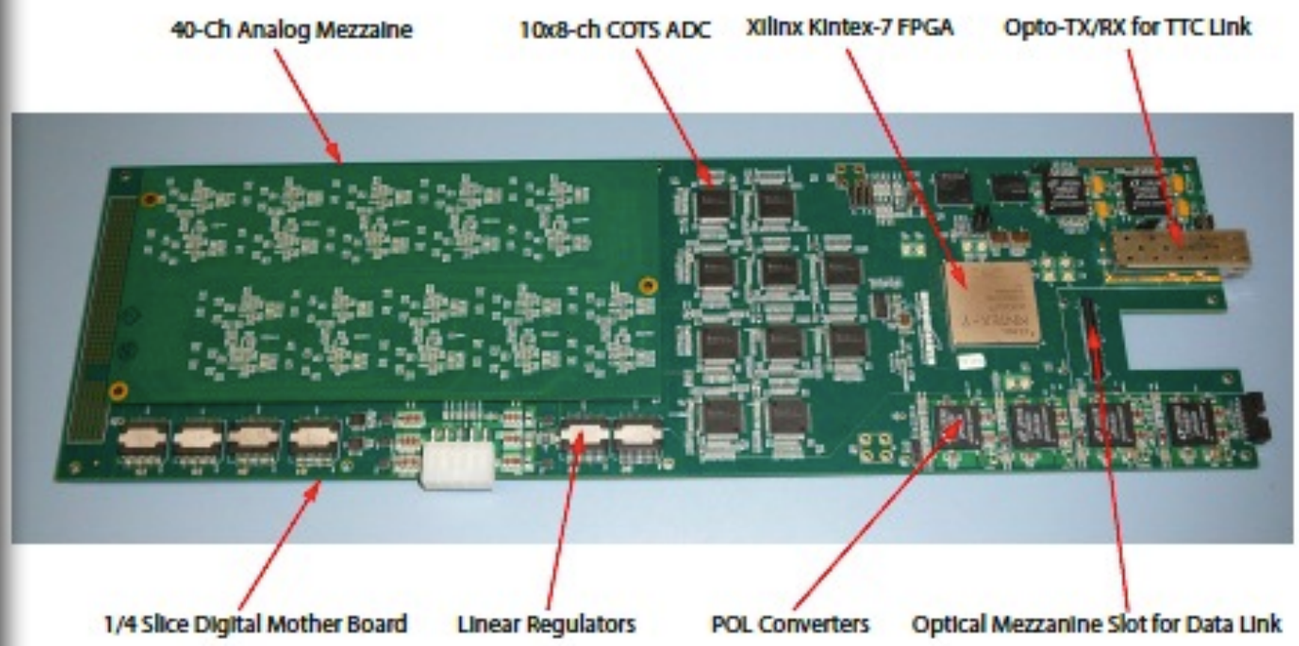
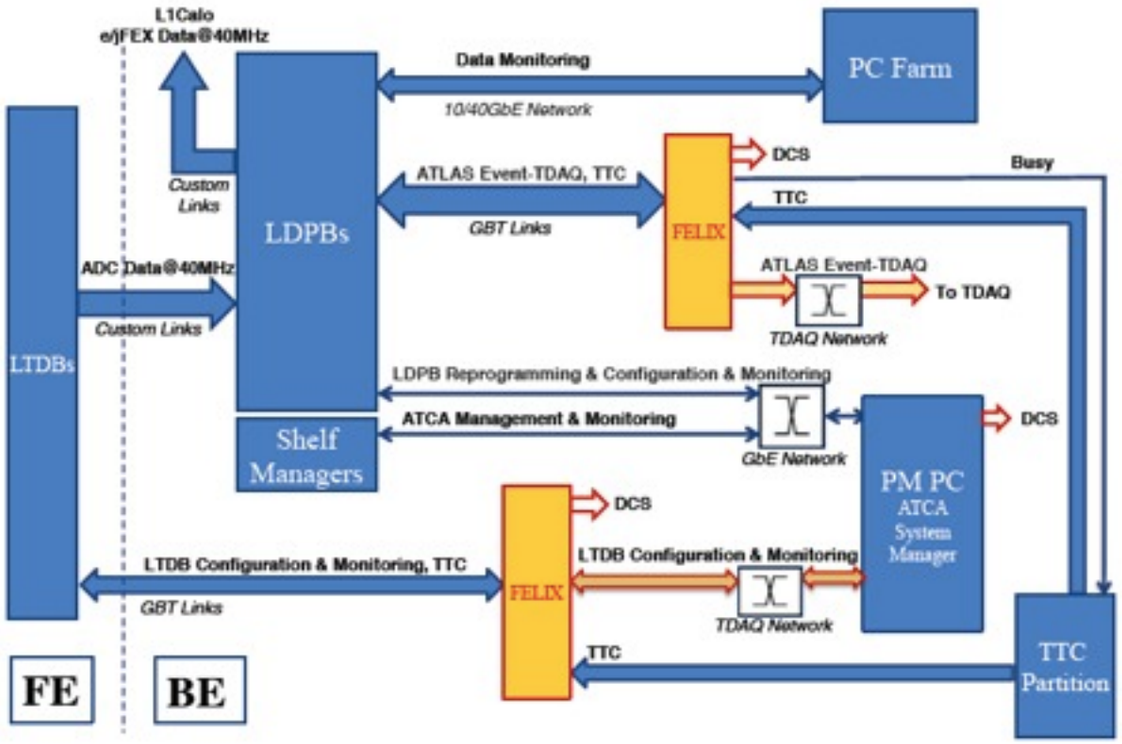
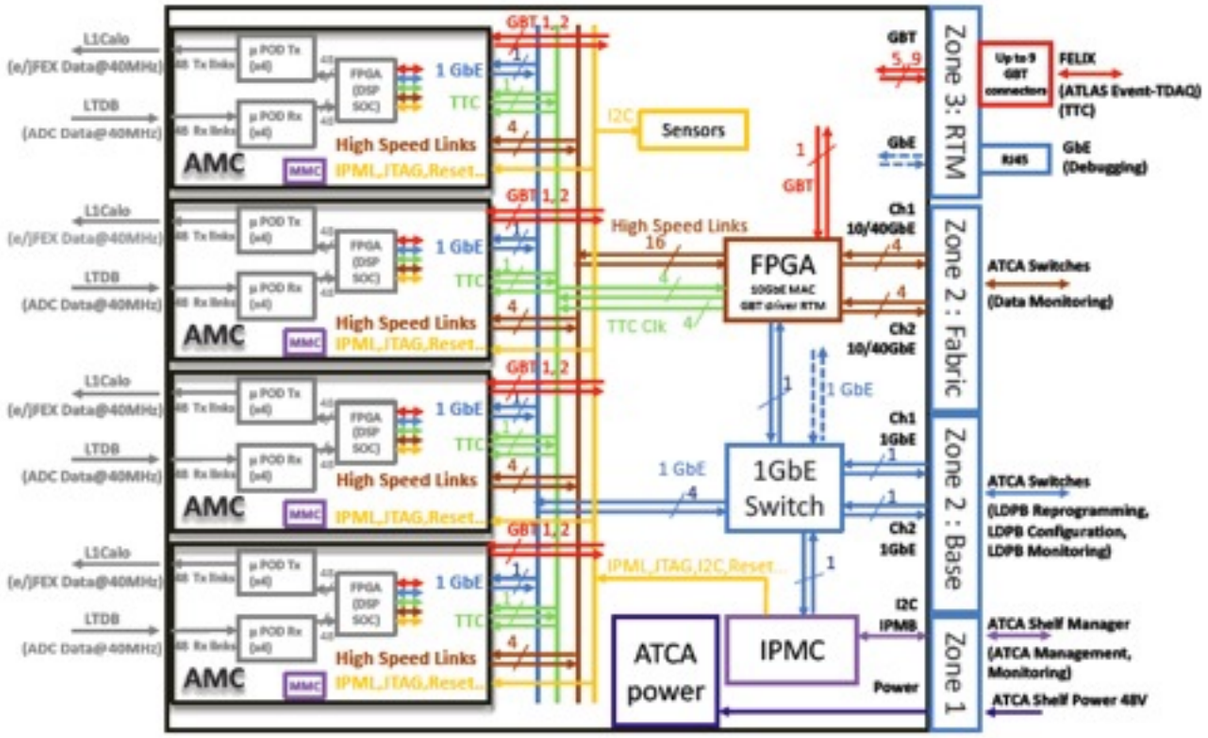
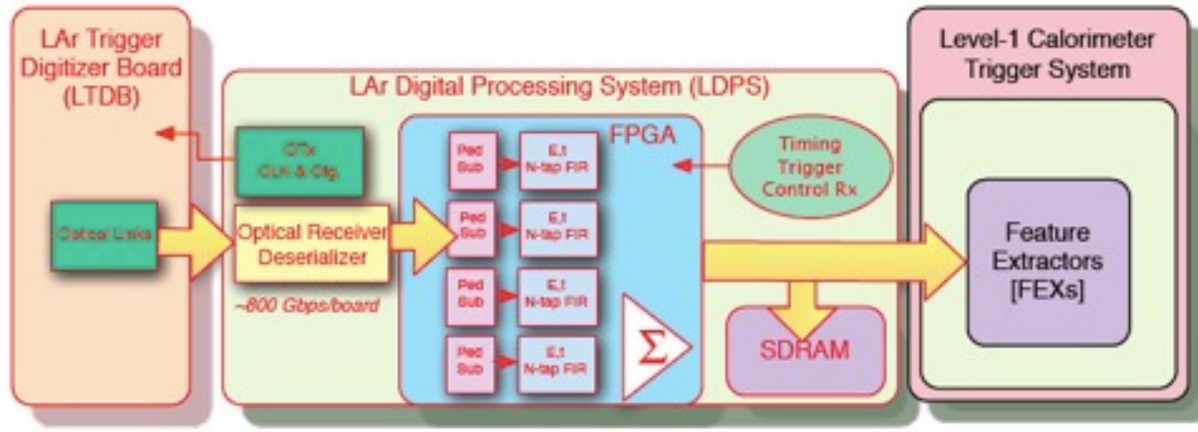


Figure 39. Photograph of the 1/4 slice LTDB prototype, which has one digital motherboard and two 40-channel analog mezzanines to process 80 Super Cell signals.

System Architecture: **Back-End**

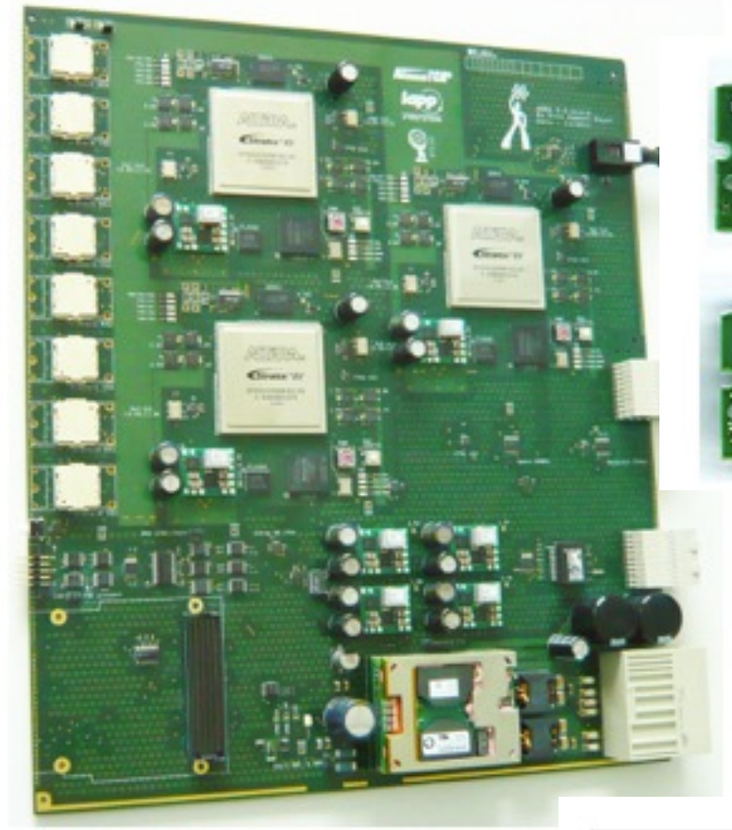


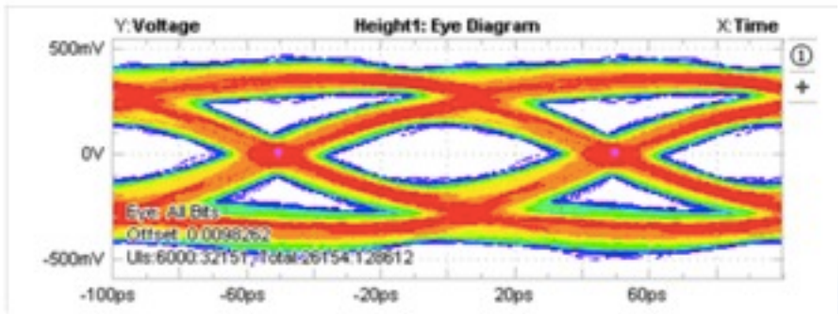


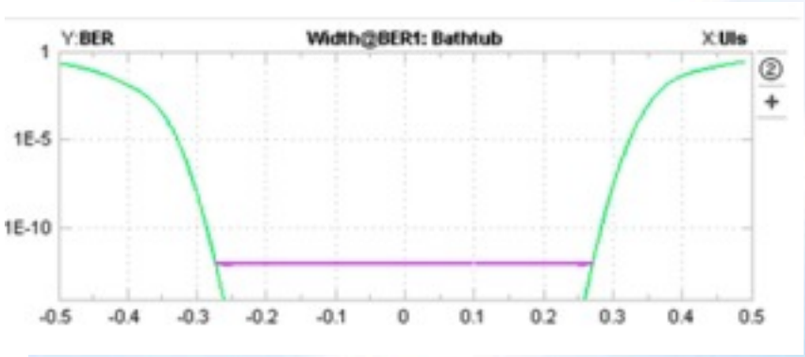


- Back-End system based on ATCA (Advanced Telecommunication Computing Architecture)
- 31 blades (**LAr Digital Processing Boards = LDPBs**) organized in 3 shelves
- Each blade housing 4 AMC (Advanced Mezzanine Cards) processing unit mezzanines
  - FPGA-based processing and E_T reconstruction at every bunch crossing
  - Each mezzanine receiving 4x12@5Gbps fibers and transmitting up to 4x12@10 Gbps to the Level-1 **Calorimeter Feature Extractors (FEXs)**

System Architecture: **Back-End**







- **ATCA Pre-prototype built** and tested successfully
  - Based on ALTERA Stratix IV and PPOD transceivers
  - Tested for communications up to 8Gbps and 70mt distance
- Configuration and management through IPMC (Intelligent Platform Management Controller) pluggable board. Prototype built and ready for production
- **Evaluation of MicroPOD transceivers tested successfully to >10 Gbps**
- Tests of signal transmission integrity on boards at 10Gbps+ speeds for different layouts and different PC board specifications

Conclusions

- The LAr Phase-I upgrade project has proposed the upgrade of the trigger readout providing higher granularity, layer information and higher precision information
- It has been shown that the proposed upgrade allows ATLAS to maintain the Level-1 trigger thresholds for single and di-EM objects at the necessary low level by improving the jet background rejection capability and the energy resolution of the EM object.
- It has also been shown that the upgrade improves the performance of the **τ**, jet and E_T^{miss} Level-1 trigger.
- The proposed LAr Phase-I upgrade is a pre-requisite for a successful ATLAS physics program for the LHC Run-3: 300 fb^{-1} p-p collisions at $\sqrt{s}$ = 14TeV ($\mathcal{L}$ up to $3x10^{34}cm^{-2}s^{-1}$, <μ>=80)

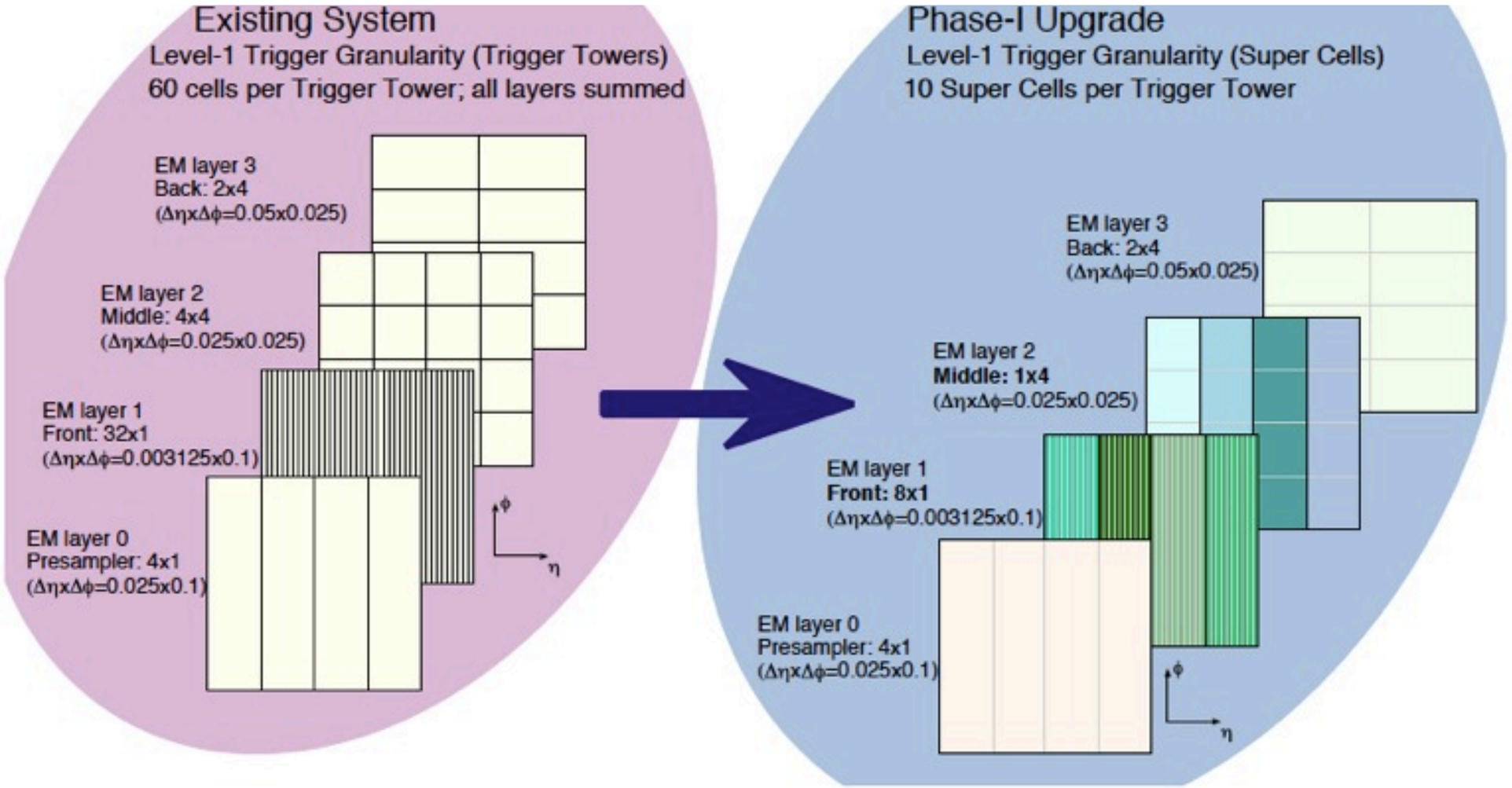
Conclusions

- The system architecture has been conceived to be compatible with the existing Level-1 calorimeter trigger:
  - It will operate in parallel and it allows for a "smooth" commissioning of the new fully digital trigger system
- The proposed architecture is also fully compatible with the ATLAS plans for the Phase-II upgrades and the possible ATLAS trigger system during the operations at the HL-LHC [see backup slide]
- Technical challenges for the on-detector electronics have started to be addressed and solutions are either already available or a plan is in place to identify them
- Project management, costs and resources are organized within the ATLAS LAr Calorimeter sub-system (with the addition of a few new institutions) to best match existing expertise, skills and because of the deep integration in the existing readout system and in its operations [see backup slides]

Backup

How to improve?

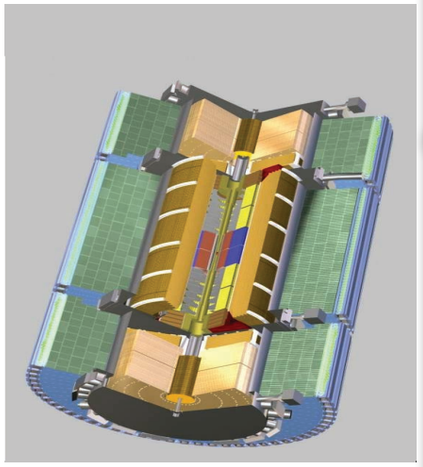
Layer		Elementary Cell	Trigger Tower		Super Cell	
		$\Delta\eta \times \Delta\phi$	$n_\eta \times n_\phi$	$\Delta\eta \times \Delta\phi$	$n_\eta \times n_\phi$	$\Delta\eta \times \Delta\phi$
0	Presampler	0.025×0.1	4×1	0.1×0.1	4×1	0.1×0.1
1	Front	0.003125×0.1	32×1		8×1	0.025×0.1
2	Middle	0.025×0.025	4×4		1×4	0.025×0.1
3	Back	0.05×0.025	2×4		2×4	0.1×0.1

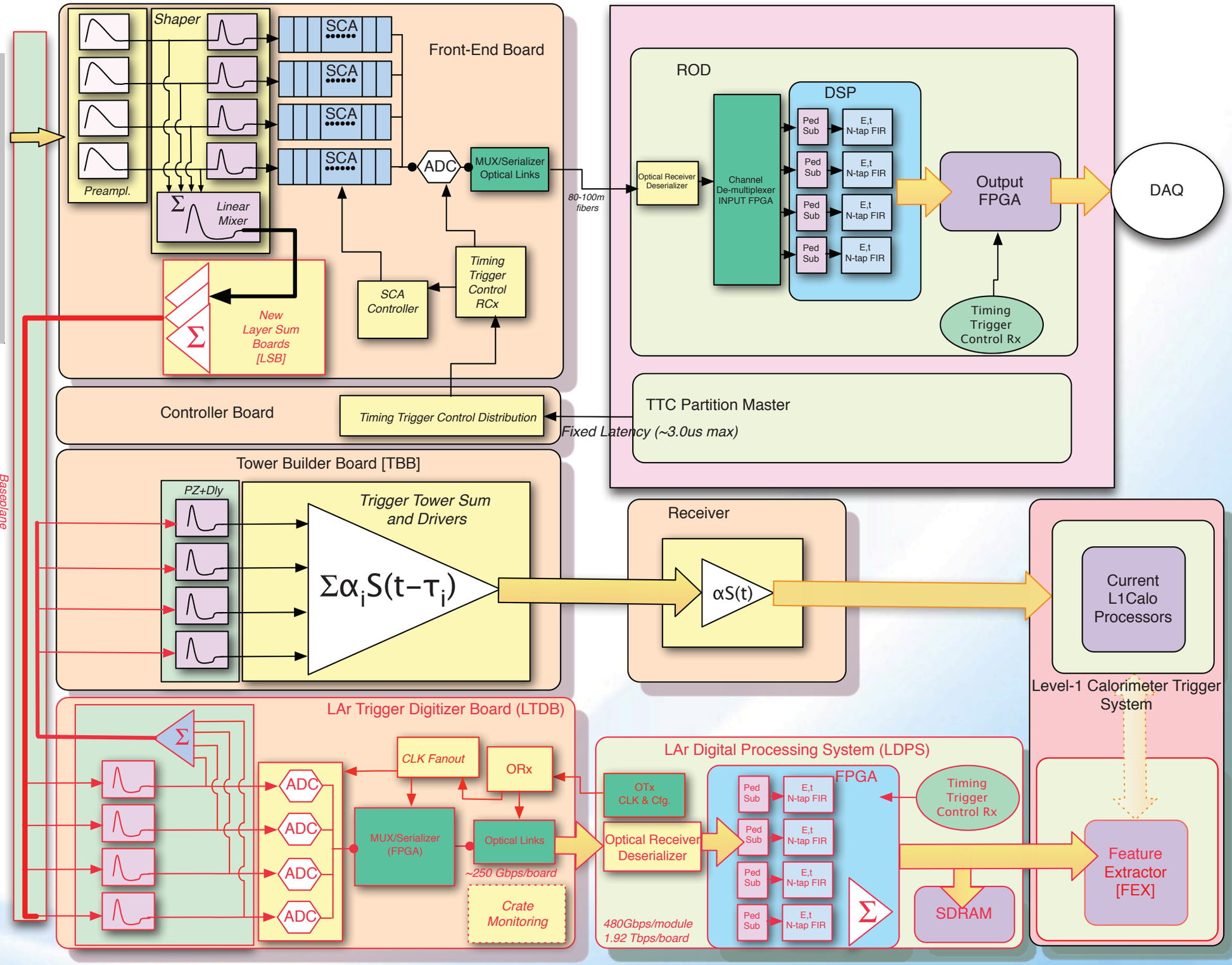


EM Barrel Calorimeter:

- 1 TT
- 10 SCells

System Architecture and Design Specifications



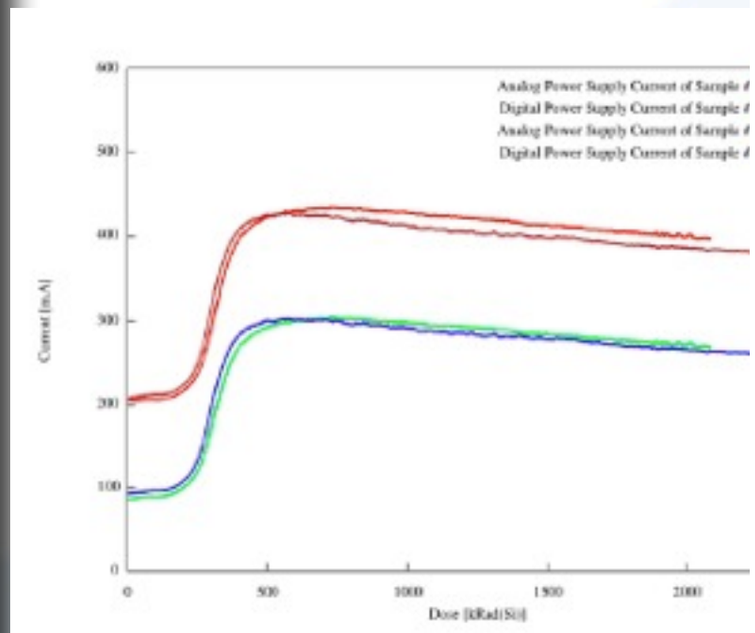


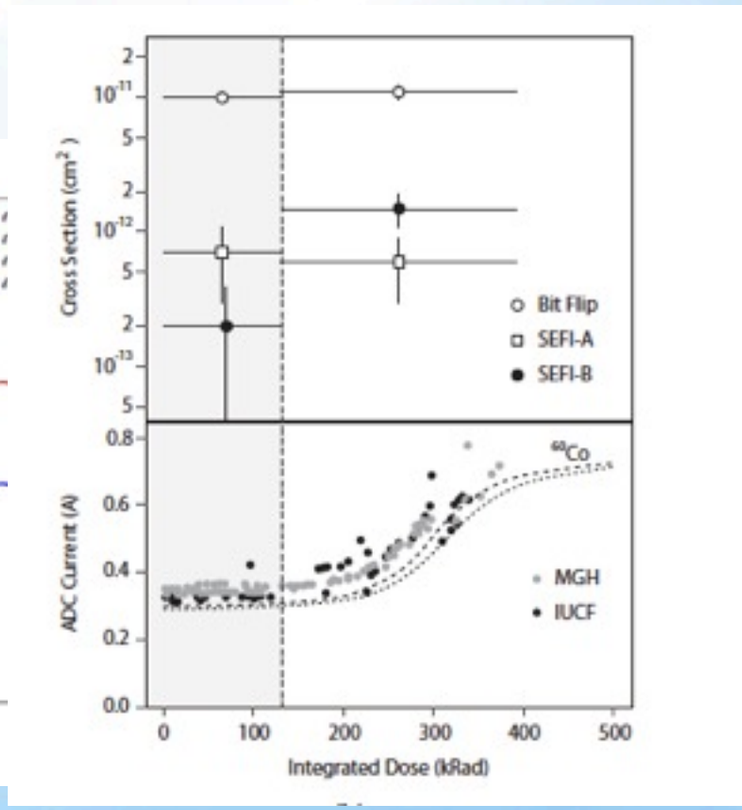
System Architecture: **Front-End**

- **ADC**
- 1 COTs identified as possible candidate (TI5272)
- surviving very high TID
- Annealing test successfully (not sensitive to enhanced low dose rates)
- Single Event Effects cross-section has been measured: two types of Single Event Fault Interrupt (SEFI) observed
  - SEFI-A mitigated through a periodical reset (200ns reset time)
  - SEFI-B cross-section should be sufficiently low for the ATLAS LAr applications

Table 10. Specifications for the ADC. The ADC must have a serial output using either standard LVDS or SLVS technology. The ADC word must be either 12-bit or 16-bit in one frame, with a frame clock at 40 MHz and a bit clock at 480 MHz (12-bit case) or 640 MHz (16-bit case). The latency is the time between the first sample and the last bit out. The power consumption is given per ADC channel at 40 MSPS. For comparison, values for the COTS TI ADS5275 ADC are given in the third column.

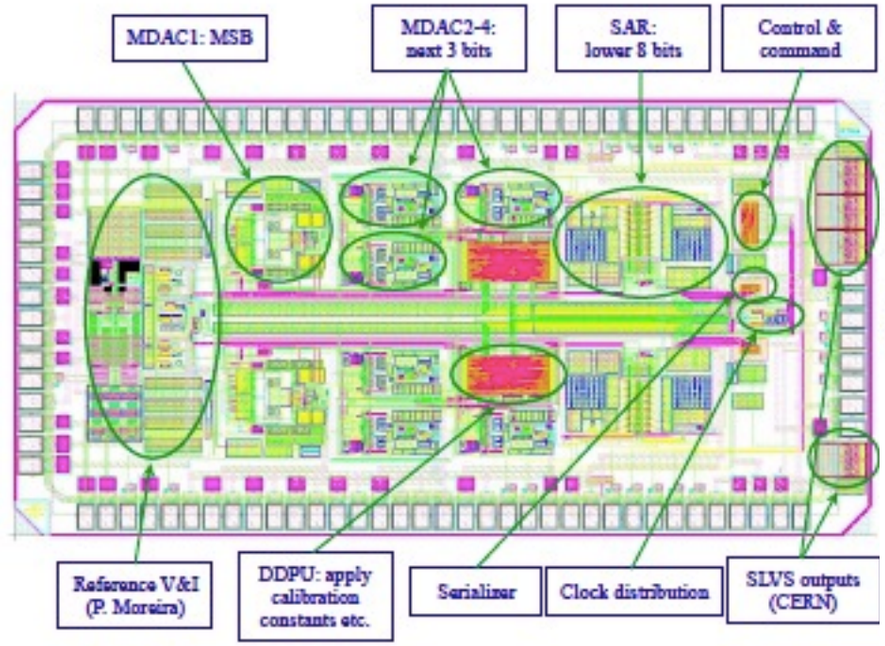
Parameters	Requirement	ADS5272
Sampling rate	≥ 40 MSPS	40 MSPS
Dynamic range	12 bits	12 bits
Resolution (ENOB)	≥ 11	11.5
Differential Nonlinearity	≤ 1 lsb	0.3 lsb
Integral Nonlinearity	≤ 1 lsb	0.4 lsb
Latency	≤ 200 ns	162.5 ns
Power consumption	≤ 145 mW	113 mW

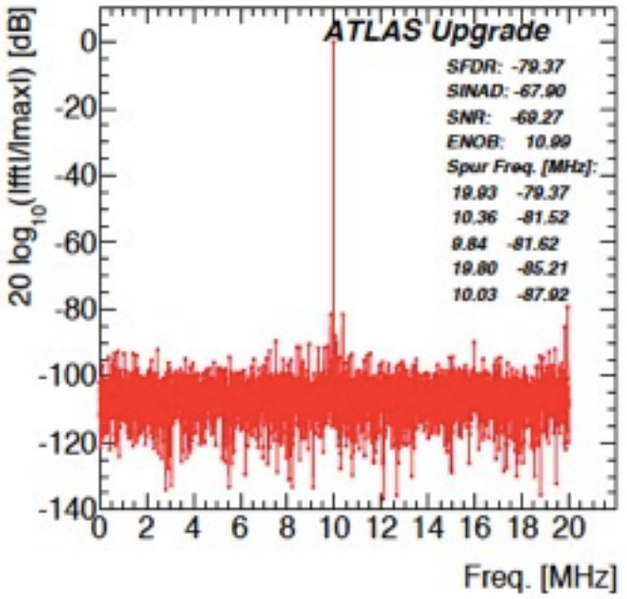


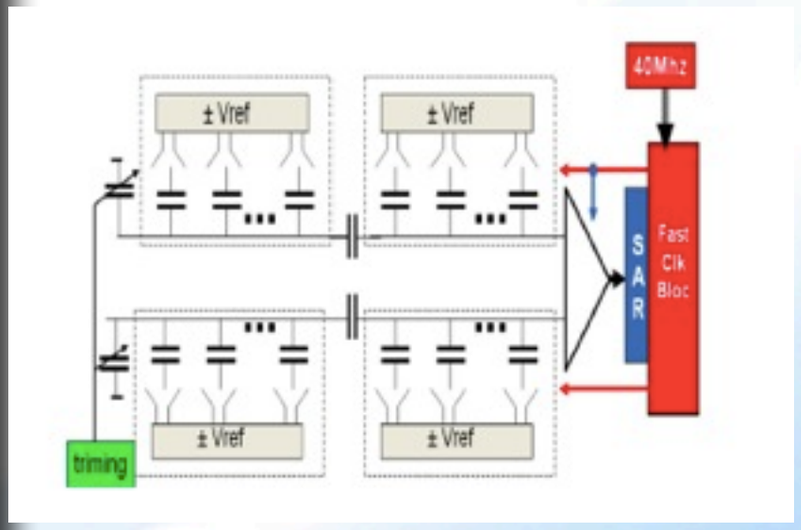


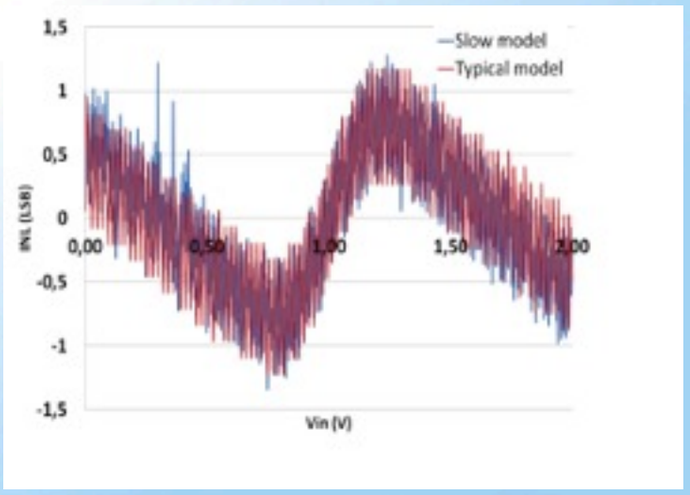
System Architecture: **Front-End**

- **ADC**
- Two ASIC options based on IBM 130nm CMS-8RF process.
- Prototypes manufactured and currently under test
  - 4-stage (SAR-based) pipelined ADC
    - ✦ Evaluation complete and radiation testing is next
  - Full SAR architecture ADC (very low power ~10mW/ channel)
    - ✦ 2nd iteration full prototype and 4 inputs being submitted.



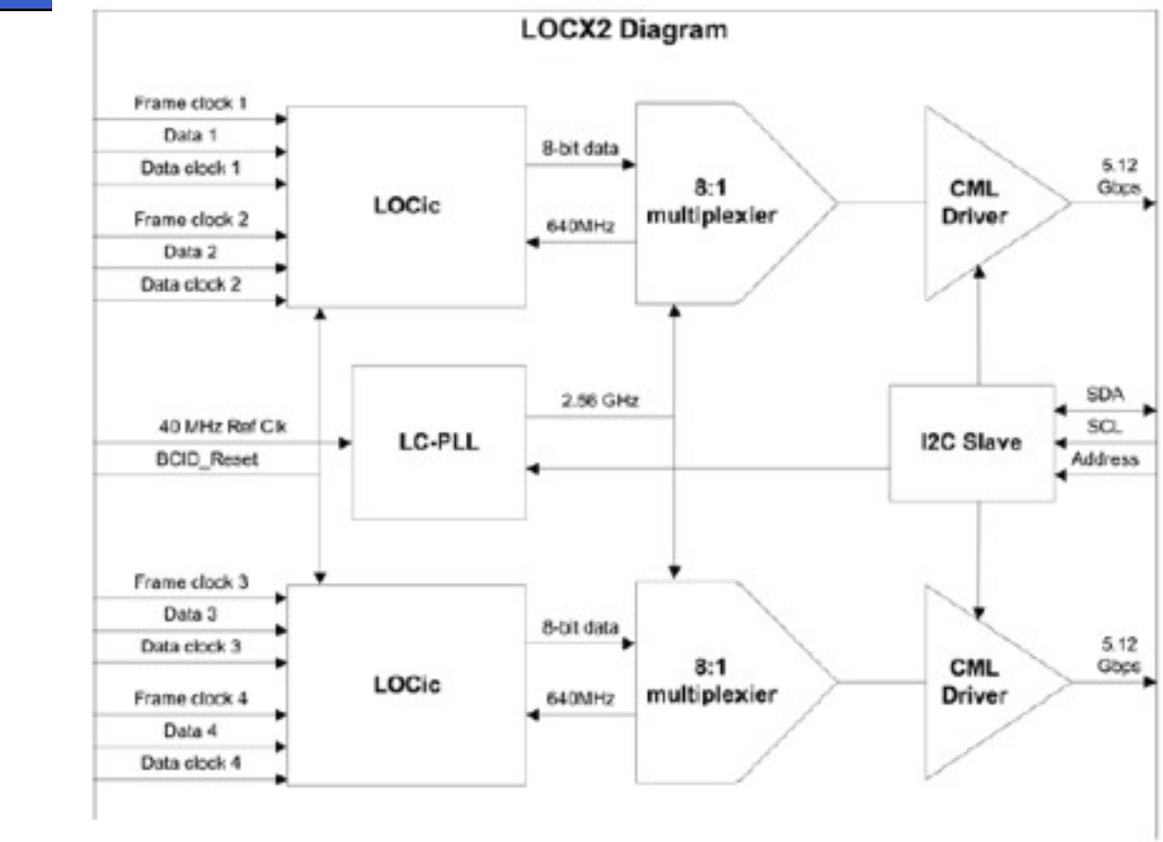


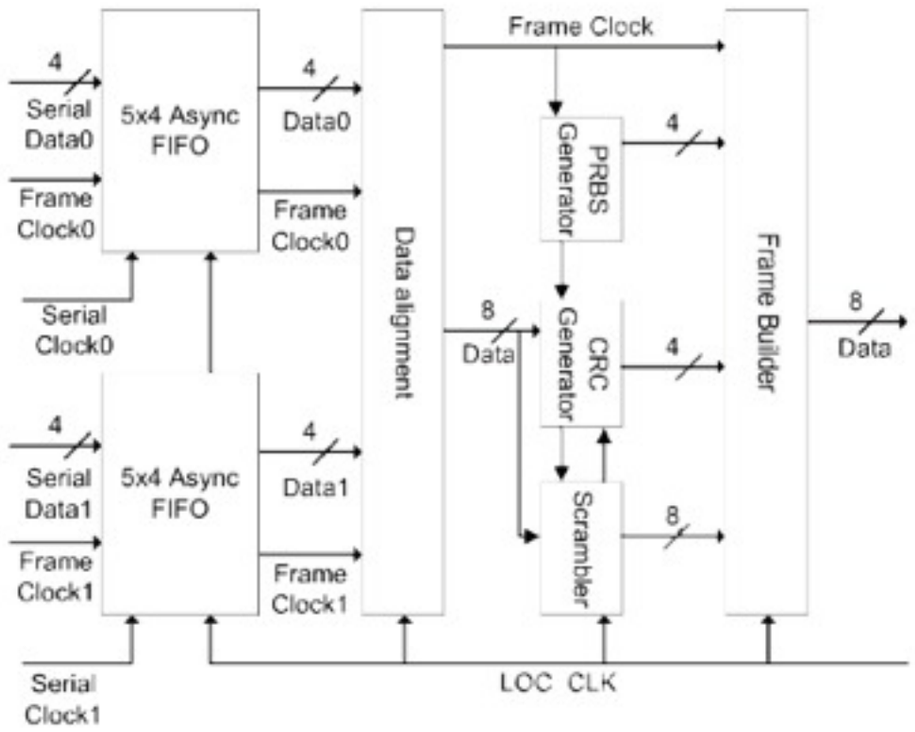




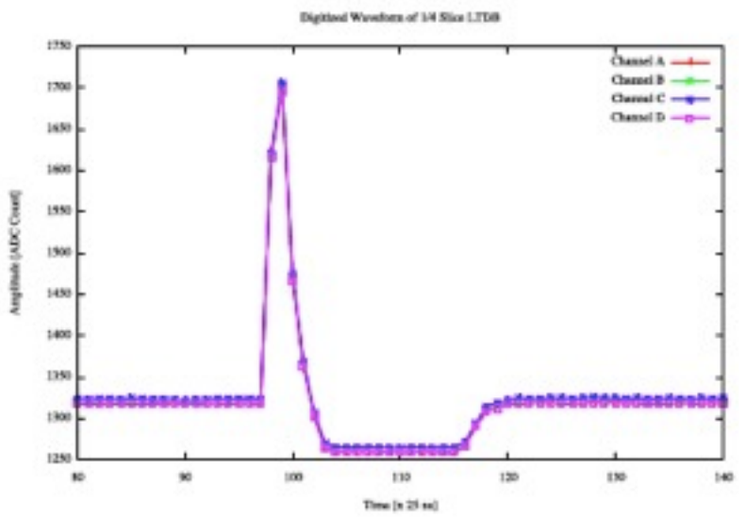
System Architecture: **Front-End**

- Development of serializer and interface ASIC in SoS 250nm technology quite advanced.
- System aspects being addressed pending decision on component choice (specifically for the ADC).



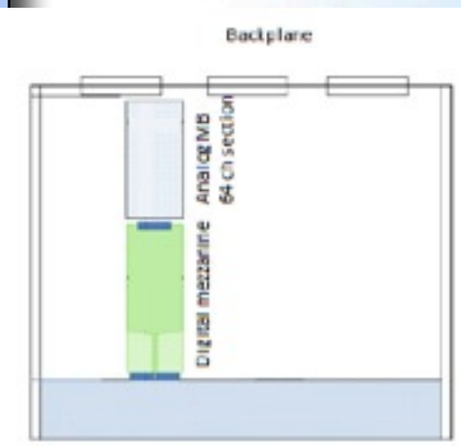


System Architecture: **Front-End**



Board Integration

- Two strategies being pursued:
  - Digital Motherboard with Analog mezzanines
  - Analog motherboard with digital mezzanines
- Options under studies and prototype being designed and built (based only on COTS).
- Full-size prototypes under design (end of this year) for system test use early 2014.



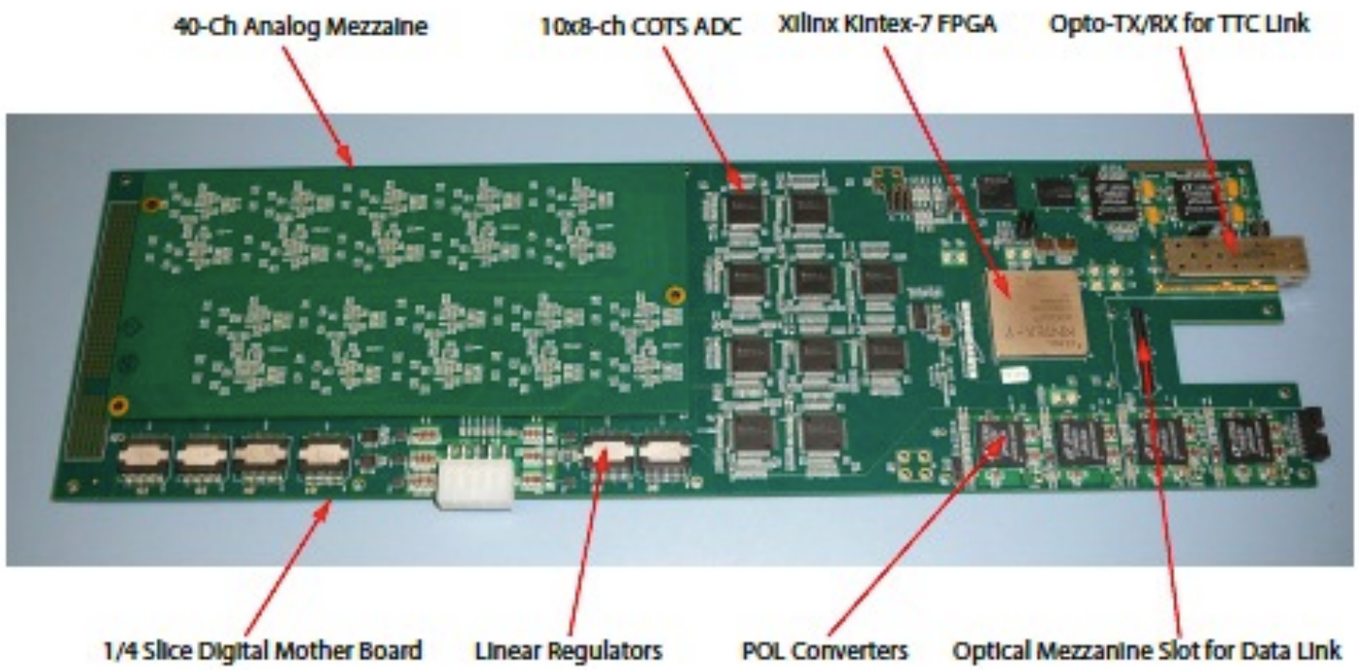


Figure 39. Photograph of the 1/4 slice LTDB prototype, which has one digital motherboard and two 40-channel analog mezzanines to process 80 Super Cell signals.

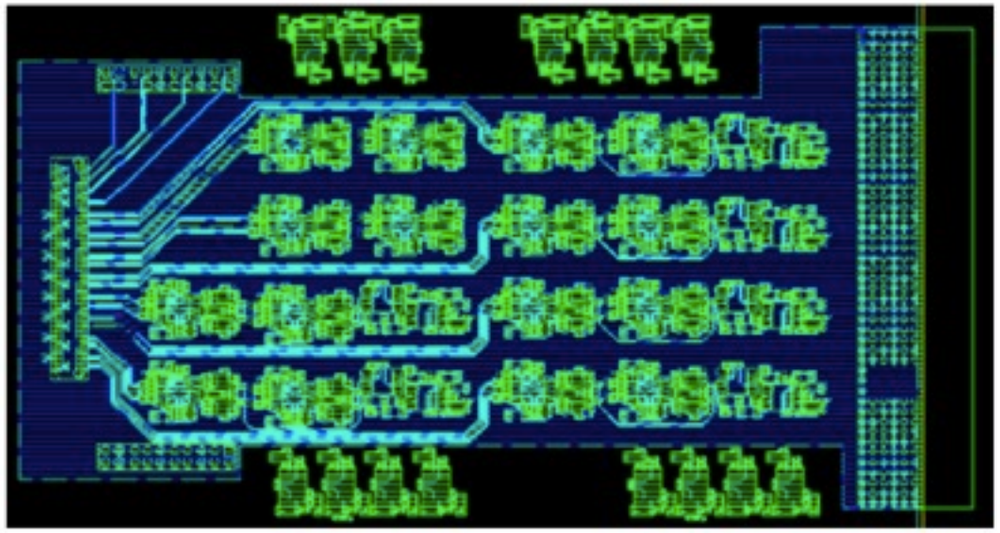
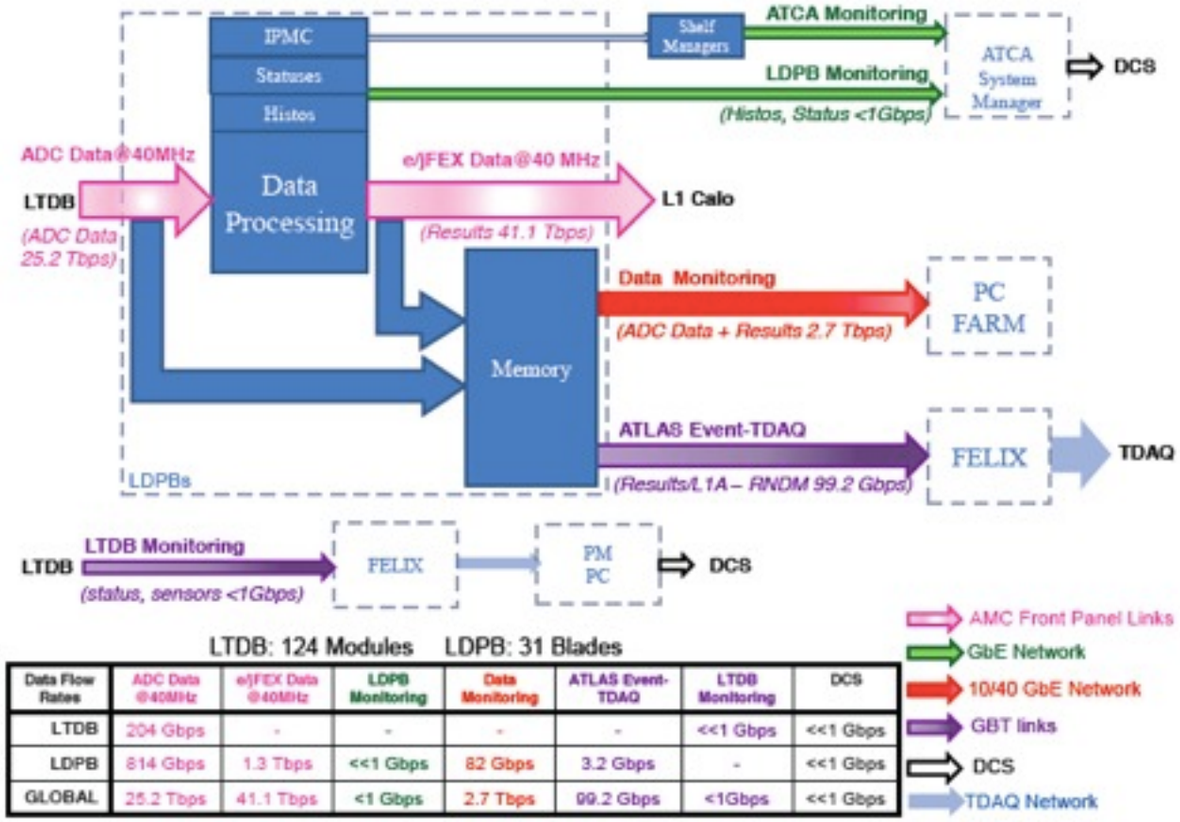
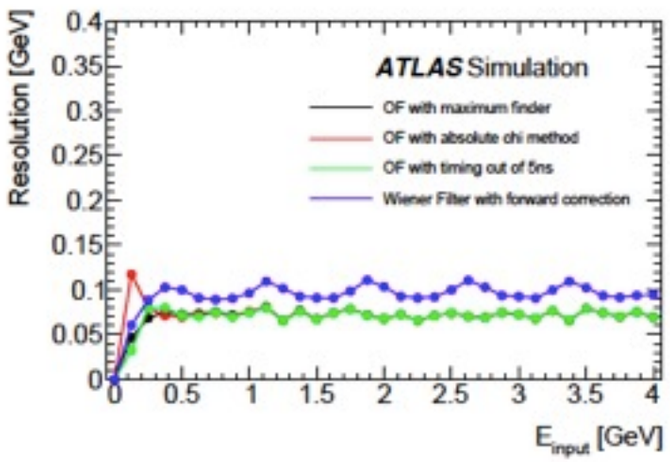


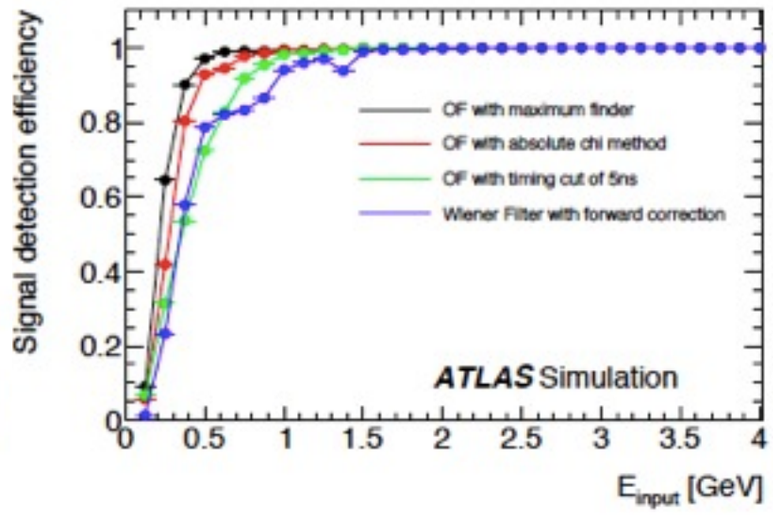
Figure 43. View of one face (representing 32 channels) of a 64 channel section motherboard prototype

System Architecture: **Back-End**



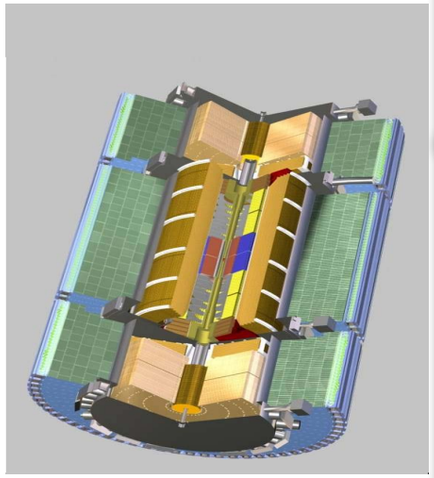
Data Flow Rates	ADC Data @40MHz	e/jFEX Data @40MHz	LDPB Monitoring	Data Monitoring	ATLAS Event-TDAQ	LTDB Monitoring	DCS
LTDB	204 Gbps	-	-	-	-	<<1 Gbps	<<1 Gbps
LDPB	814 Gbps	1.3 Tbps	<<1 Gbps	82 Gbps	3.2 Gbps	-	<<1 Gbps
GLOBAL	25.2 Tbps	41.1 Tbps	<1 Gbps	2.7 Tbps	99.2 Gbps	<1Gbps	<<1 Gbps





- **Open questions (post-TDR and toward Final Design Reviews):**
  - Specification of the protocols, mapping and data data bandwidth requirements from the LDPS to the e/j-FEX
  - Specification of the interfaces to the Trigger-DAQ datapath
  - Complete evaluation of the filtering algorithms to reconstruct energies (Optimal Filtering vs. Wiener Filter with forward corrections)

Planned LAr Phase-II Upgrade



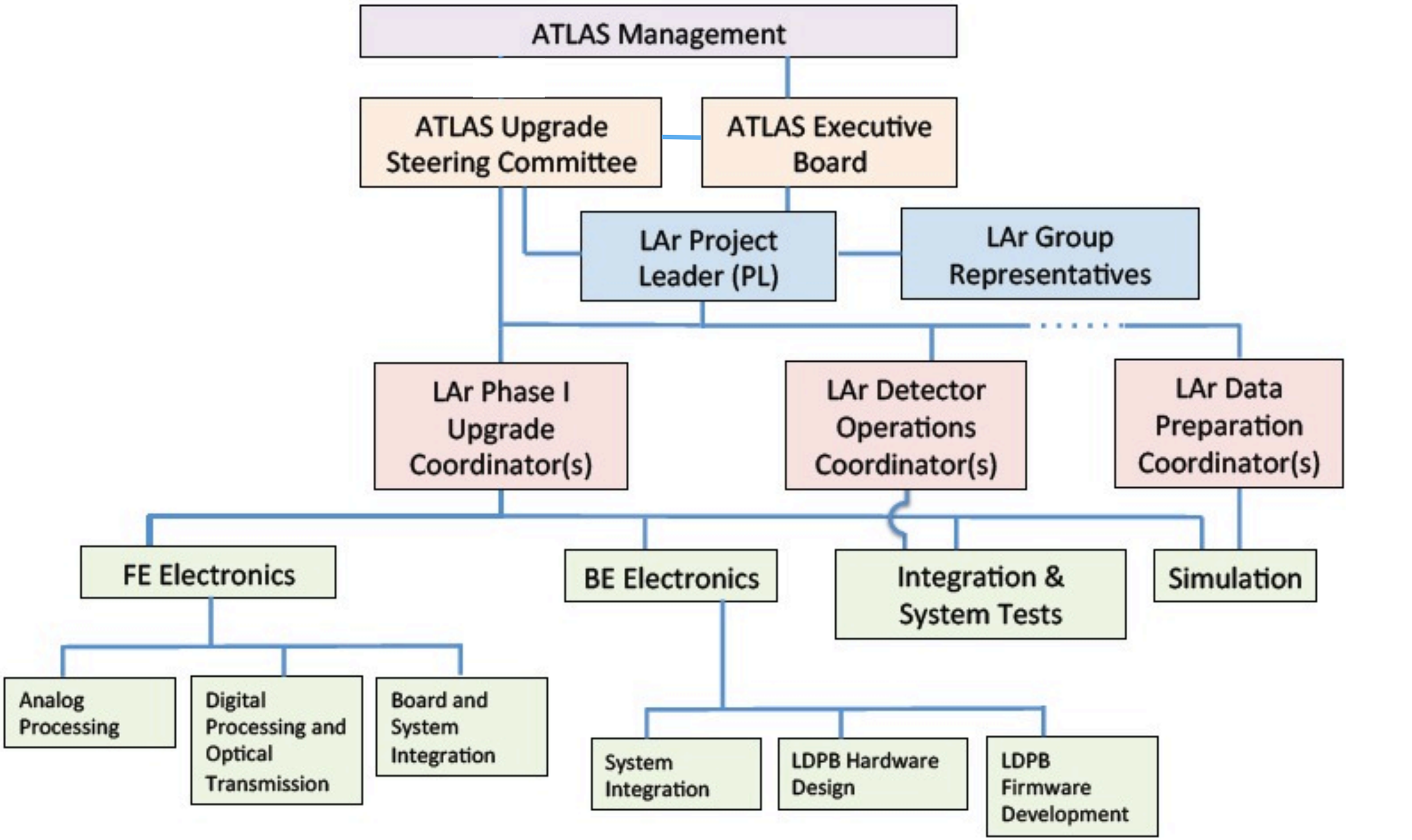
LTDB and LDPS feeding Level-0 trigger primitives

Analog trigger electronics de-commissioned

Fully compatible with Phase-II upgrade programs

Feature Extractors (FEX) processors could evolve into L0 trigger system

LAr Phase-I Upgrade Project Organization



Cost Estimates

- "CORE"-costing metric:

Component productions in 2014-2015 mainly
Sub-assemblies and board integrations in 2016-2017

Table 25. LAr Phase-1 Upgrade summary CORE cost table in units of kCHF

PBS	Item	Cost	2013	2014	2015	2016	2017	2018
1.1	**Front-End electronics**							
1.1.1	Baseplane	1076	-	100	438	538	-	-
1.1.2	Layer Sum Boards	225	-	12	100	112	-	-
1.1.3	LTDB	2958	-	400	1079	979	500	-
1.2	**Optical Cables**	592	-	-	-	296	296	-
1.3	**Back-End electronics**							
1.3.1	ATCA+shelves	40	-	-	10	10	20	-
1.3.2	LDPB	2573	-	100	986	1086	400	-
1.3.3	RTM	55	-	-	27	28	-	-
1.3.4	TTC Optical Couplers	8	-	-	-	4	4	
1.3.5	In-shelf switches	46	-	-	-	23	23	
1.3.6	Receiver PC	14	-	-	-	7	7	
1.3.7	Controlling PC	5	-	-	-	3	2	-
	Total	7590	-	612	2640	3086	1252	-

BE ~ 1 yr later wrt. the FE (very approximately)

Cost Estimates

- "CORE"-costing metric:

Component productions in 2014-2015 mainly
Sub-assemblies and board integrations in 2016-2017

Table 25. LAr Phase-1 Upgrade summary CORE cost table in units of kCHF

PBS	Item	Cost	2013	2014	2015	2016	2017	2018
1.1	**Front-End electronics**							
1.1.1	Baseplane	1076	-	100	438	538	-	-
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1.1.3	LTDB	2958	-	400	1079	979	500	-
1.2	**Optical Cables**	592	-	-	-	296	296	-
1.3	**Back-End electronics**							
1.3.1	ATCA+shelves	40	-	-	10	10	20	-
1.3.2	LDPB	2573	-	100	986	1086	400	-
1.3.3	RTM	55	-	-	27	28	-	-
1.3.4	TTC Optical Couplers	8	-	-	-	4	4	
1.3.5	In-shelf switches	46	-	-	-	23	23	
1.3.6	Receiver PC	14	-	-	-	7	7	
1.3.7	Controlling PC	5	-	-	-	3	2	-
	Total	7590	-	612	2640	3086	1252	-

BE ~ 1 yr later wrt. the FE (very approximately)

Milestones

- Construction Milestones and timelines for decision through formal ATLAS review, as managed by the Project Office in Technical Coordination (similarily to original construction)

Table 26. LAr Phase-1 Upgrade key dates for main deliverables. As explained in the text, these dates take into account constraints arising from shutdowns and periods of access to the detector and as such represent the latest dates for which these activities should be scheduled

Item	# units	Prod end	Prod start	PRR	FDR	PDR
Front-End						
Baseplane	124	5-2017	11-2016	9-2016	2-2016	
LSBs	2328	9-2017	9-2016	7-2016	12-2015	
Integrated LTDB	124	9-2017	3-2017	1-2017	6-2016	5-2014
Analog section	124*4	1-2017	10-2015	9-2015	4-2015	
Digital Components						
ADC	124*80	1-2017	10-2015	9-2015	4-2015	3-2014
ASIC Serializer	124*20	1-2017	10-2015	9-2015	4-2015	
ASIC Laser Driver	124*40	1-2017	10-2015	9-2015	4-2015	
VCSEL mezzanine (TOSA)	124*20	1-2017	10-2015	9-2015	4-2015	
DC Powering	124	1-2017	10-2015	9-2015	4-2015	
Optical pigtails	124*4	1-2017	7-2016	5-2016	10-2015	
Cooling plates	124*2	1-2017	7-2016	5-2016	10-2015	
Long Fibers	58	7-2017	1-2017	11-2016	4-2016	
Back-End						
LDPB	34	1-2017	10-2015	9-2015	4-2015	
AMC & FPGA	34*4	1-2017	10-2015	9-2015	4-2015	10-2014
IPMC	34*1	1-2017	10-2015	9-2015	4-2015	
MMC	34*4	1-2017	10-2015	9-2015	4-2015	
Optical pigtails	34*4	1-2017	10-2015	9-2015	4-2015	
MicroPod Cooling block	34*4*8	1-2017	10-2015	9-2015	4-2015	
Carrier Board & RTM	34	1-2017	10-2015	9-2015	4-2015	10-2014

PDR: Preliminary Design Review
Option evaluation and component selection.
Only for determined items

FDR: Final Design Review
Specification and design finalization

PRR: Production Readiness Review
To formally enable start of production

In addition a "Demonstrator" program in late 2013-2014 to validate the system aspects and possibly performance in ATLAS (see Appendix-D TDR):

- System Tests Dec 2013-Mar 2014 in a dedicated lab
- ATLAS review (Mar 2013)
- Installation in ATLAS (June/July 2013)
- Standalone Commissioning (remaining 2014)

Sharing and Institutional Responsibilities

Table 27. List of participating institutes and areas of interest for the construction of the project deliverables.

Institute	Country	Front-End Electronics							Back-End Electr.			
				LTDB						LDPB		
		Baseplanes	Layer Sum Boards	Analog Section	Digital Section	DC powering	Board Mechanics, Cooling and Integration	Optical Cable Plant & Pigtails	ATCA shelves & Computing Infrastructure	AMC	Carrier Board (& RTM)	Firmware
Sao Paulo[a]	Brazil				x							
TRIUMF	Canada	x		x	x							
Victoria		x		x	x							
Annecy	France/IN2P3								x	x	x	x
Grenoble					x							
Marseille									x	x	x	x
Orsay-LAL		x		x	x		x					
Saclay	France/CEA	x		x			x					
Dresden	Germany								x	x		x
Milano	Italy	x				x						
Tokyo[a]	Japan				x					x		x
Dubna-JINR	Russia	x		x								
Moscow-Lebedev								x				
Novosibirsk-BINP											x	x
CERN	Switzerland							x				
Arizona	United States	x								x	x	x
Brookhaven					x	x	x			x	x	x
Columbia					x							
Oregon[a]												x
Pennsylvania[b]				x								
Pittsburgh			x									
SMU					x							
Stony Brook										x	x	x

[a]New institution joining LAr for the upgrade project
[b]Institution contributing to LAr upgrade project, associated to LAr through Brookhaven

- Discussions among the LAr Calorimeter Group institutions for responsibilities and sharing (MoU in preparation)