A Large Ion Collider Experiment

Upgrade of the ALICE ITS

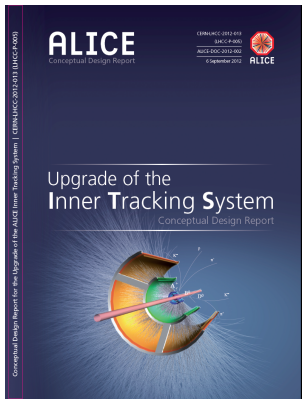
LHCC Detector Upgrade Review

CERN, 24 September 2013

L. Musa - CERN

New ITS Layout

25 G-pixel camera
(10.3 m^2)



CDR – LHCC-2012-013

7 layers of MAPS

Outer layers

Middle layers

Inner layers

Beam pipe

Radial coverage
22 – 406 mm

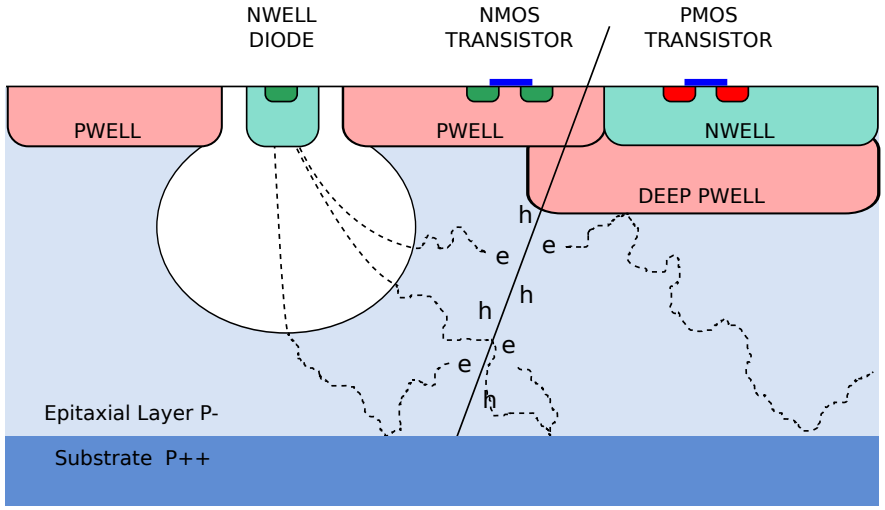
700 krad/ 1x10^{13} 1 MeV n_{eq}
Includes safety factor 10

PIXEL Chip - technology

Monolithic PIXEL chip using
Tower/Jazz 0.18 µm technology

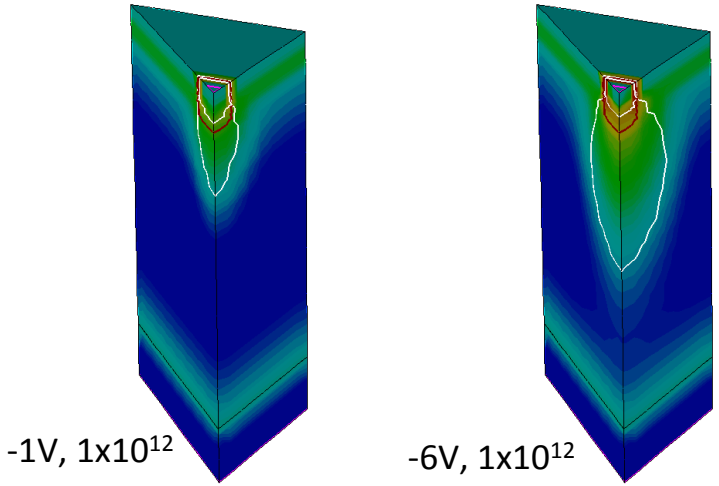
- feature size 180 nm
- gate oxide < 4nm
- metal layers 6

- high resistivity epi-layer
  - thickness 18-40 µm
  - resistivity 1-6 k Ω×cm
- "special" deep p-well layer to shield PMOS transistors (allows in-pixel truly CMOS circuitry)
- Possibility to build single-die circuit larger than reticle size



Schematic cross-section of CMOS pixel sensor
(*ALICE ITS Upgrade TDR*)

TCAD simulation of total diode reverse bias
(*ALICE ITS Upgrade TDR*)



diode 3µm x 3µm square n-well with 0.5µm spacing
to p-well white line: boundaries of depletion region

PIXEL Chip – General Requirements

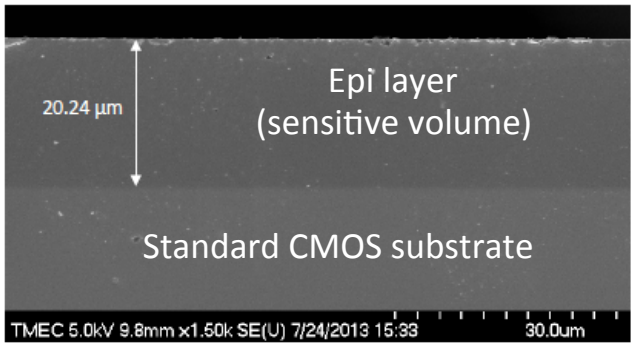
Parameter	Inner Barrel	Outer Barrel
max silicon thickness (μm)	50	
spatial resolution (μm)	5	30
chip dimensions (mm^2)	15 x 30	
max power density (mW)	300	100
max integration time (μs)	30	
TID radiation hardness	700 krad	10 krad
NIEL Radiation hardness	1.1 x 10^{13} 1 MeV neq/cm^2	3 x 10^{10} 1 MeV neq/cm^2

PIXEL Chip – Architectures under development

Architecture	Discriminator	Readout	Speed [μs]	Power (mW/ cm^2)
MISTRAL(IPHC/IRFU)	end-of-column	2-row rolling shutter	~30	~300
ASTRAL(IPHC-IRFU)	in-pixel	2/4-row rolling shutter	15 (10)	150 (200)
CHERWELL2(RAL)	Strixel (*)	rolling shutter	30	<100
ALPIDE (CERN,INFN,CCNU, YONSEI)	in-pixel	Sparse (priority encod)	4	<100

(*)Strixel: 128-pixel column over which the electronics is distributed

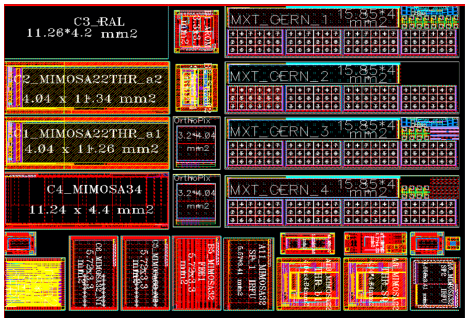
PIXEL Chip – R&D

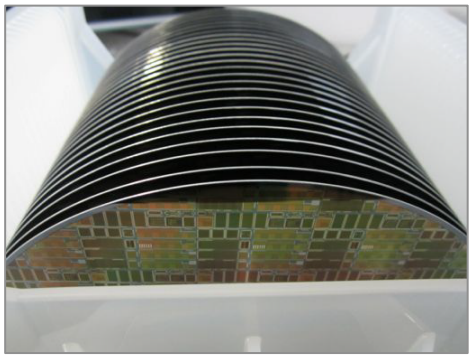


R&D started in 2011 continues till end 2014

- ✧ Improve signal/noise ratio
  - – Optimization of charge-collection diode
  - – Increase resistivity and thickness of epi-layer
  - – apply large reverse-bias voltage ➔ lower capacitance, smaller cluster size
- ✧ Study different front-end circuit and readout architectures
  - – Reduce power consumption
  - – Reduce integration/readout time
- ✧ Circuit/layout optimization for high yield and stiching

Engineering Run March 2013

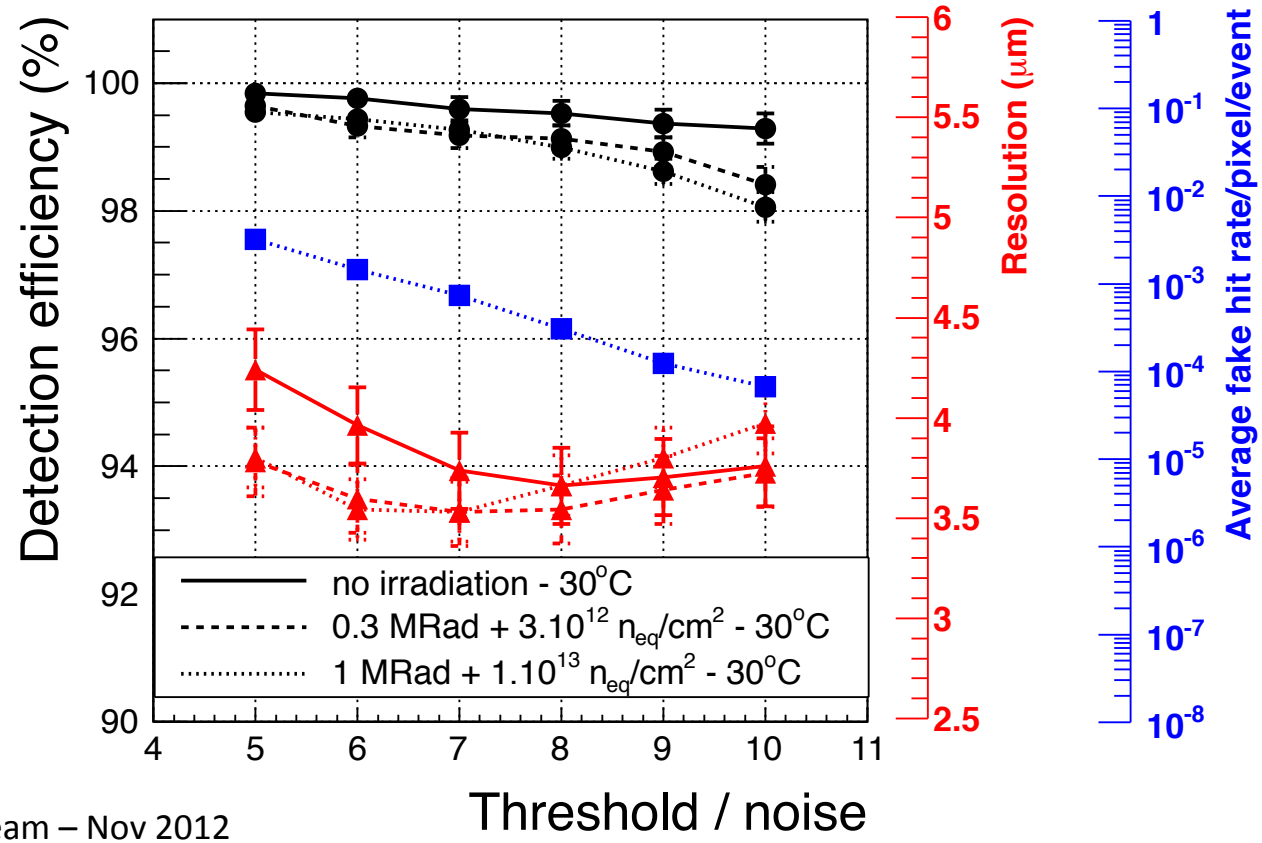




- What has been established so far
  - Adequate radiation hardness
  - Excellent charge collection efficiency for pixel 20-60 µm
  - Excellent detection efficiency
  - Prototypes of different readout architectures have being built and fully characterized

PIXEL Chip Prototypes – Experimental Results

MIMOSA-32 (IPHC-IRFU), performance from analogue output, pixel size: 20 x 20 μm^2

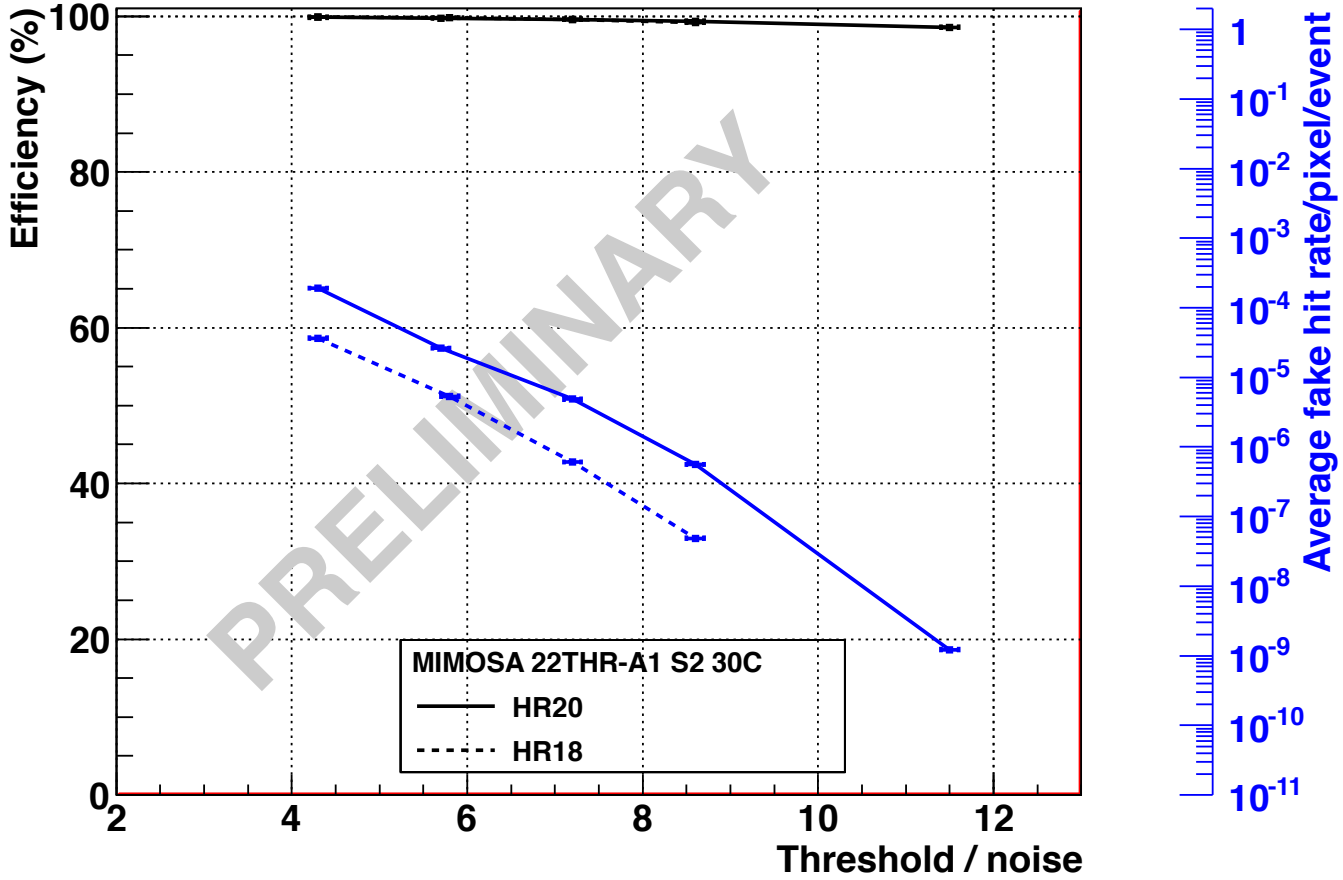


CERN SPS Test Beam – Nov 2012
80 Gev /120 Gev pion beam)

Excellent detection efficiency and spatial resolution, also after irradiation.
High fake hit rate due to RT Noise
=> increase size of input transistor in new prototypes to mitigate RTN

PIXEL Chip Prototypes – Experimental Results

MIMOSA-22-THR-A1 (IPHC/IRFU), performance from digital output
pixel size (22 x 33 μm^2) and in-pixel circuitry as proposed for final chip (**MISTRAL**)

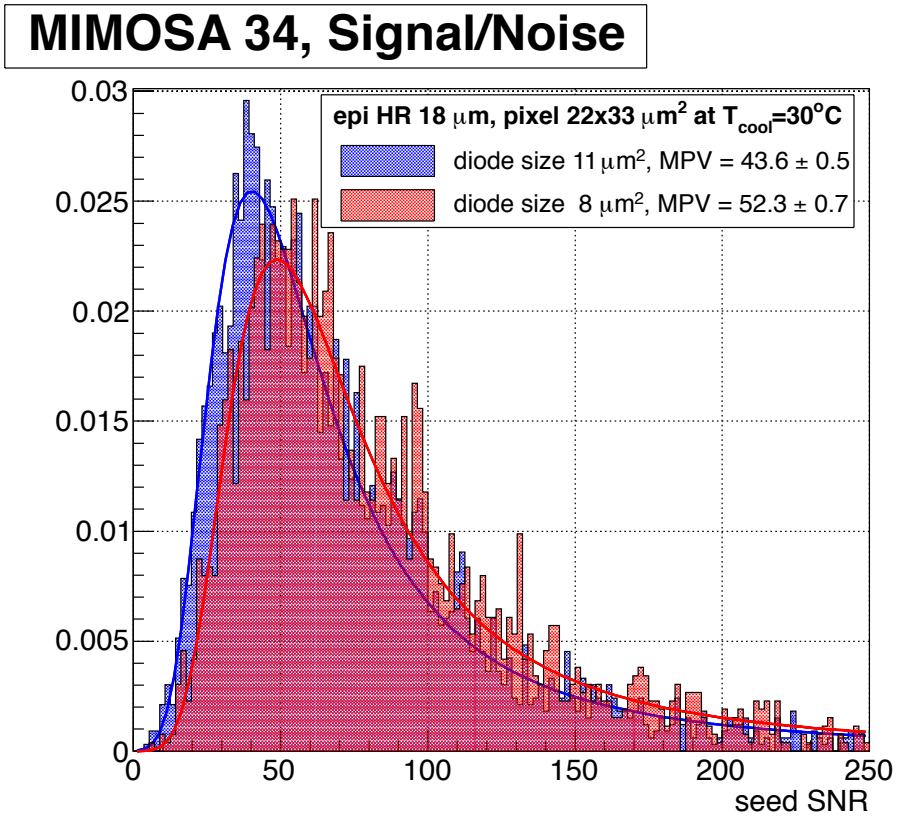


HR18 = standard Tower high-res epi-layer: (1kΩcm), 18μm thick
HR20 = epi-layer from different vendor: 6kΩcm, 20μm thick

=> Confirms that larger input transistor significantly decreases RTN

PIXEL Chip Prototypes – Experimental Results

MIMOSA-34 (IPHC), performance from analogue output, measurements at 30 C
pixel size: 22 x 33 μm^2 (as proposed for **MISTRAL)**



Further optimization
of layout of sensing diode

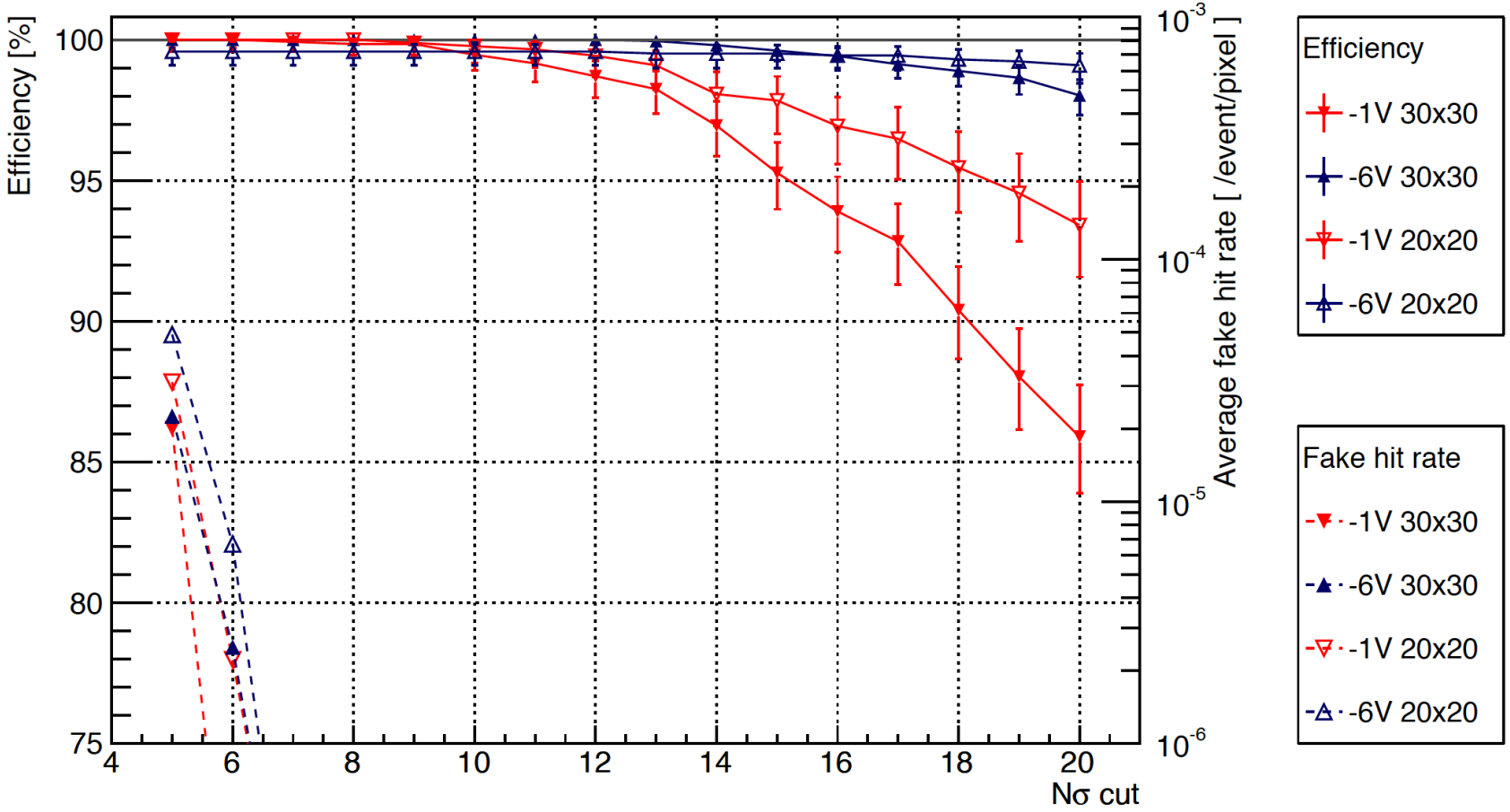
SNR 1.5 x MIMOSA32

Measurements at Desy Test Beam (4.4 Gev electron beam) – Aug 2013

Elongated staggered pixels (22 x 33 μm^2) show a spatial resolution of ~5μm

PIXEL Chip Prototypes – Experimental Results

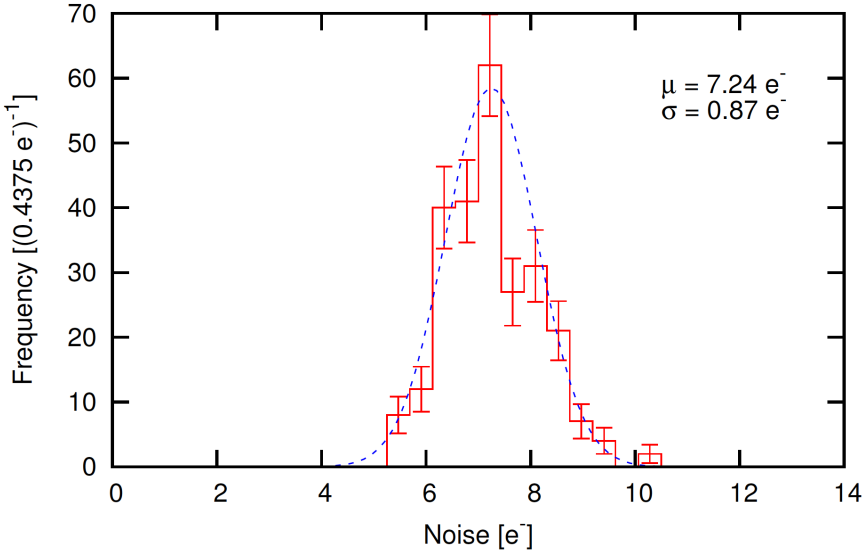
EXPLORER-1 (CERN), performance from analogue output
pixel size: 20 x 20 μm^2 and 30 x 30 μm^2

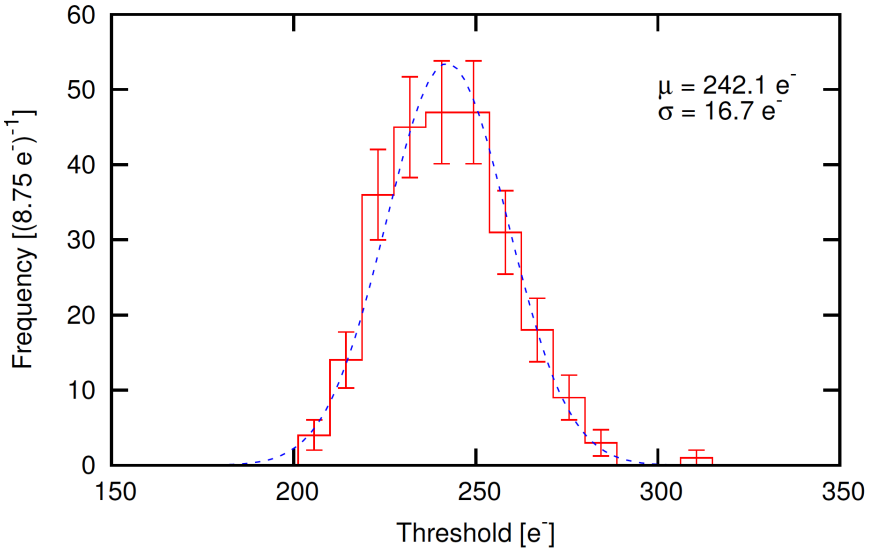


Measurements at Desy Test Beam (4.4 Gev electron beam) – July 2013

PIXEL Chip Prototypes – Experimental Results

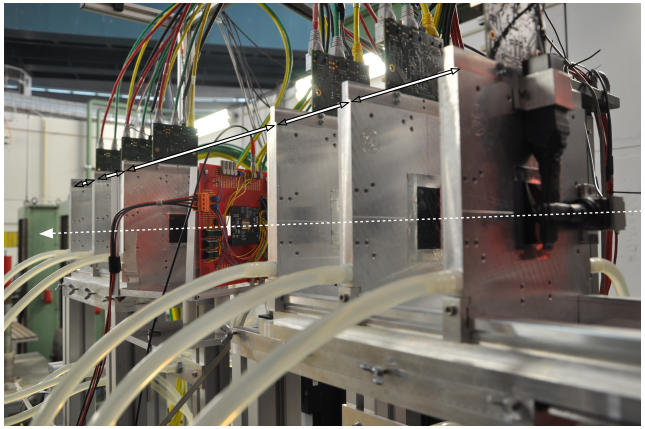
pALPIDE-1 (CERN), performance from digital output, pixel size: 22 x 22 μm^2

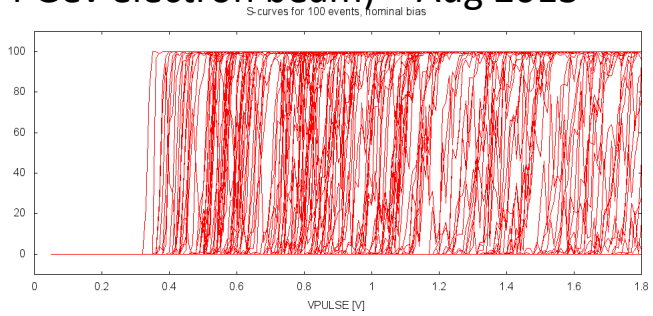




Parameters obtained from s-curve measurements at a back-bias of -2V using test pulse

Measurements at Desy Test Beam (4.4 Gev electron beam) – Aug 2013





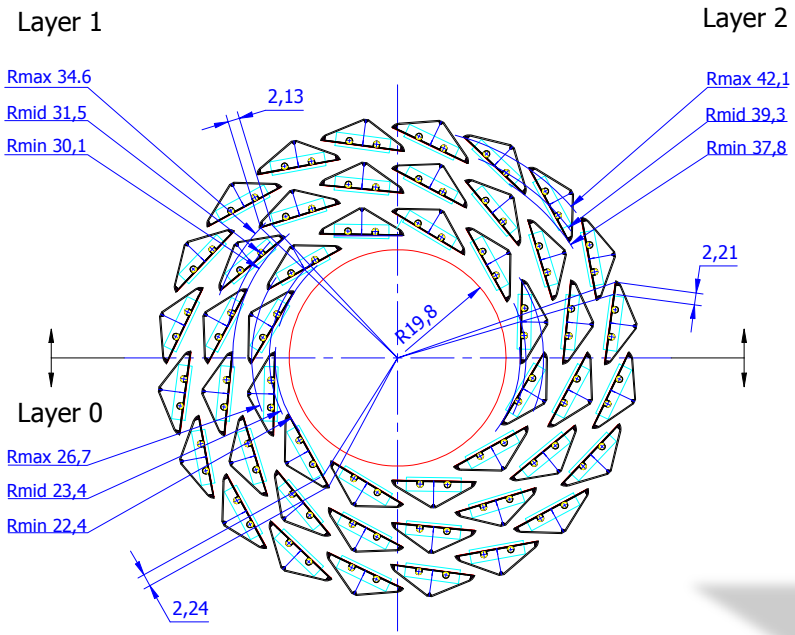
Measurement done with large spread of thresholds

Threshold spread
250 – 1000 e

Detection efficiency:
97% @ 0V back-bias

Fake hit rate < 10^{-8}

Inner Barrel



Inner Barrel (IB): 3 layers pixels

<Radius> (mm): 22,31,39

Length in z (mm): 270

Nr. of staves: 12, 16, 20

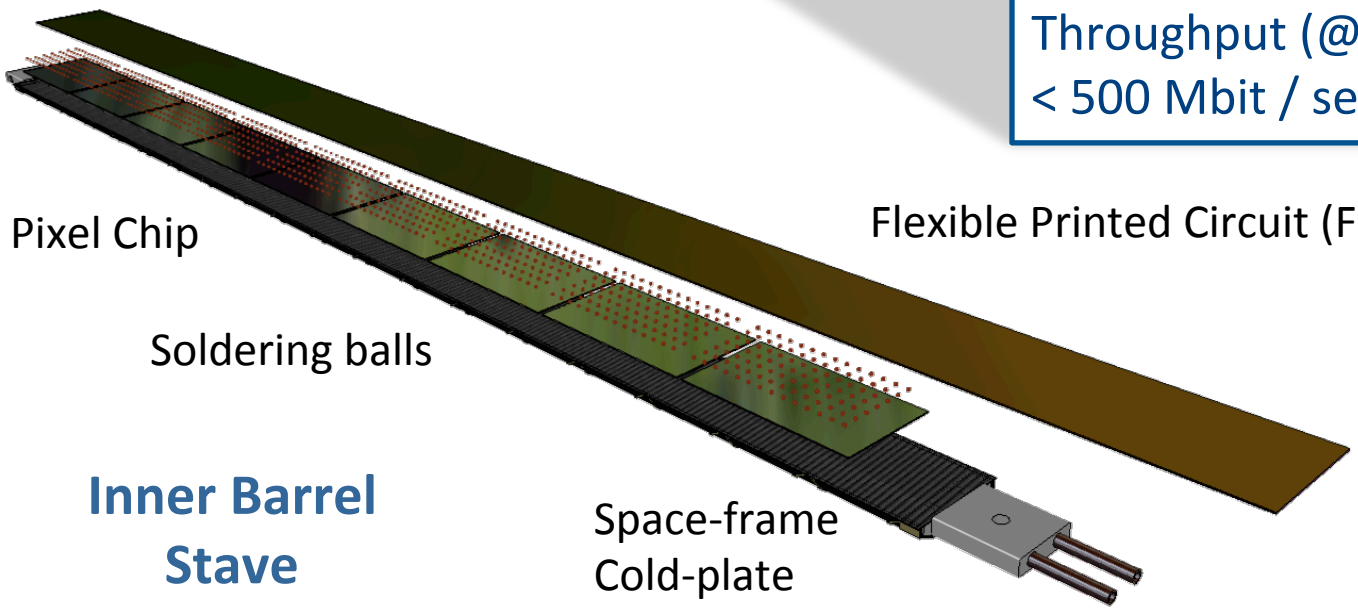
Nr. of chips/stave: 9

Nr. of chips/layer: 108, 144, 180

Material thickness: ~ 0.3% X_0

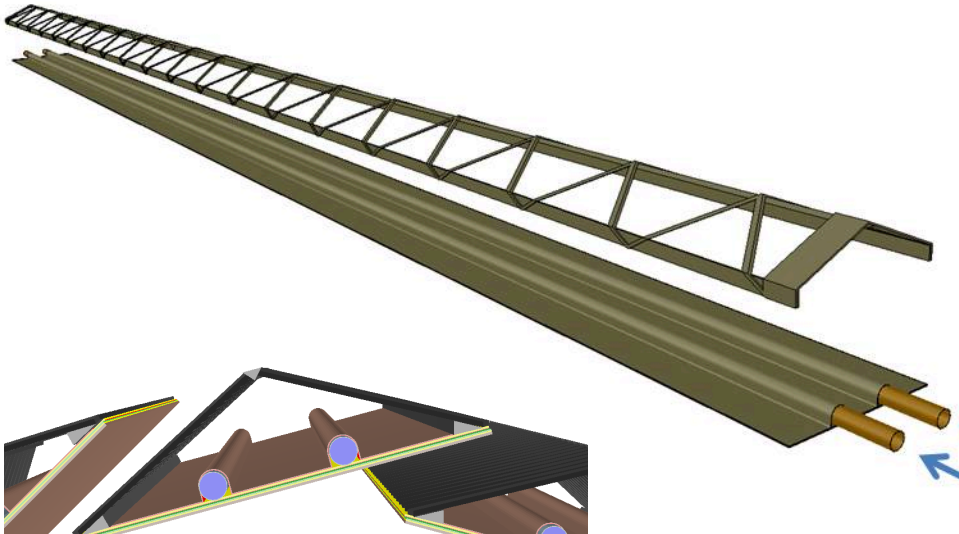
Power density: < 300 mW/cm^2

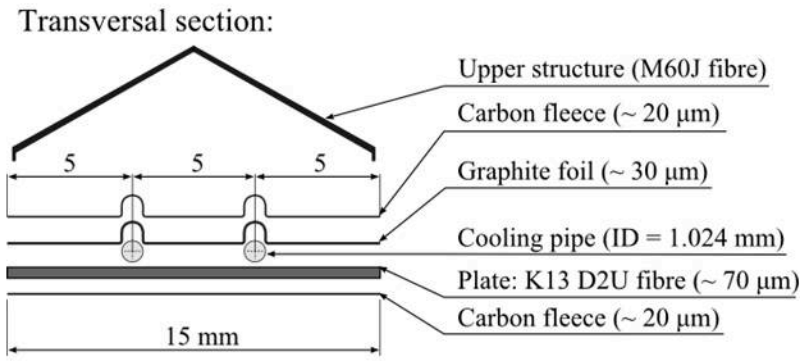
Throughput (@100kHz):
< 500 Mbit / sec x cm^2

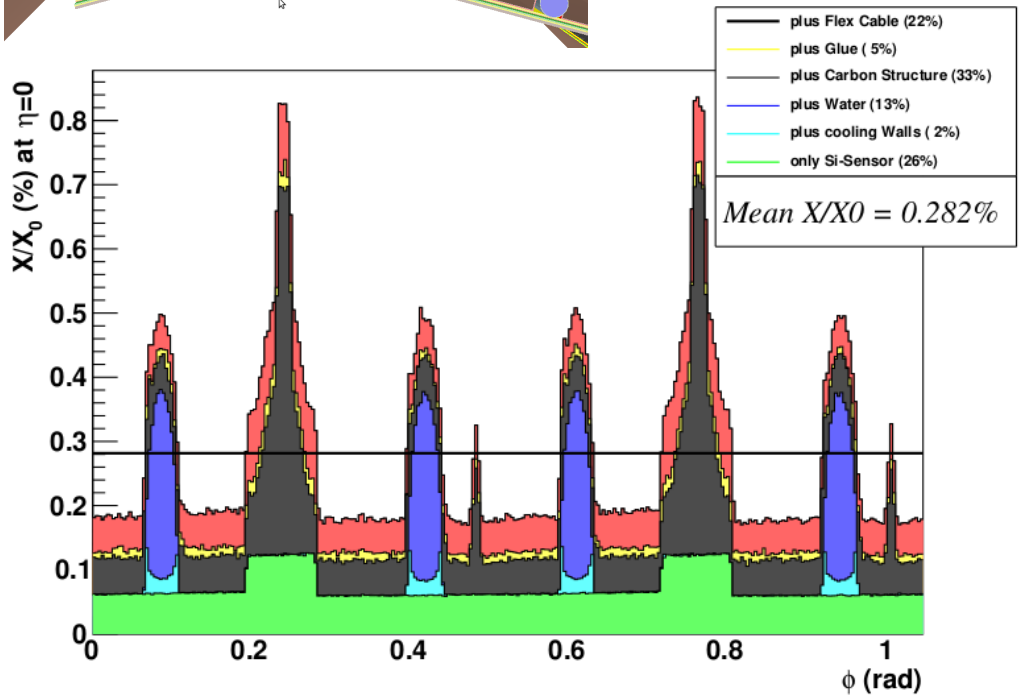


Inner Barrel Stave

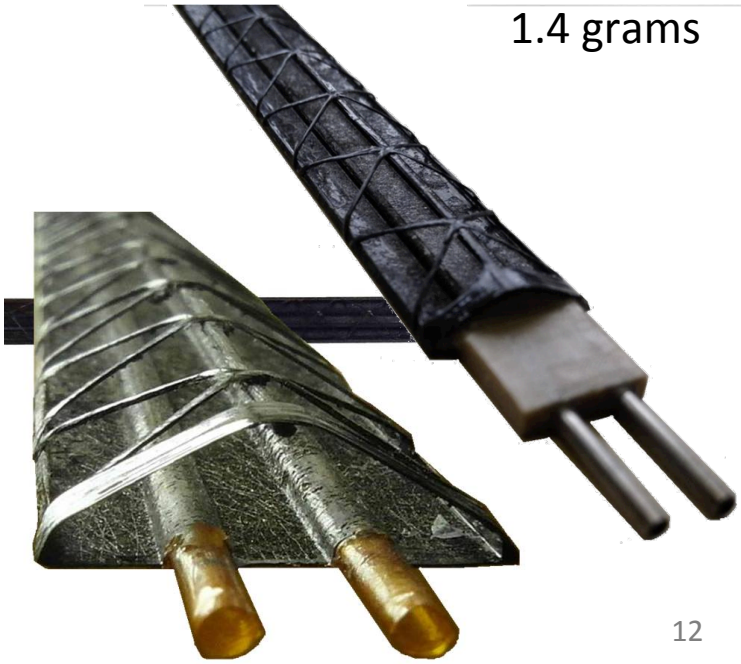
IB Stave – Design optimization and prototype







Total weight
1.4 grams



Outer Barrel

Outer Barrel (OB)

<radius> (mm): 194, 247, 353, 405

Length (mm): 843 (ML), 1475 (OL)

Nr. staves: 22, 28, 40, 46

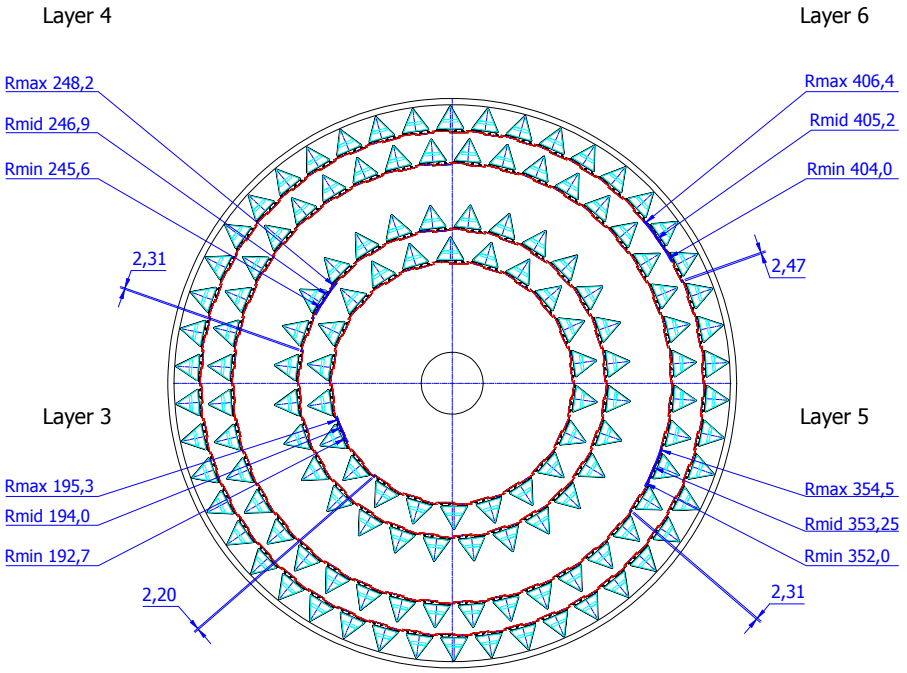
Nr. modules/stave: 4 (ML), 7 (OL)

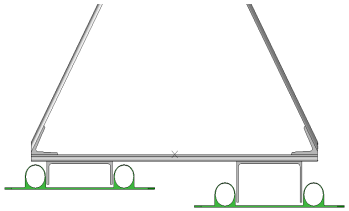
Nr. chips/module: 14

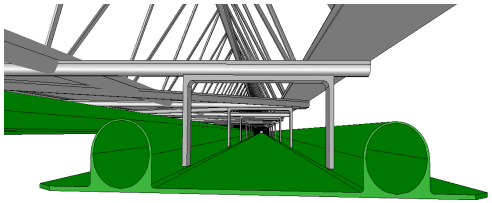
Material thickness: ~ 0.8% X_0

Throughput (@ 100 kHz):

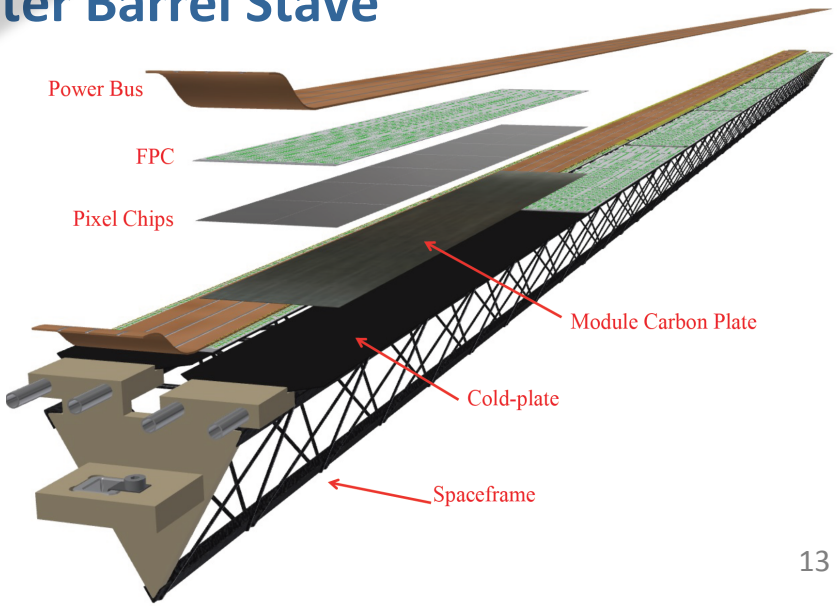
< 12 Mbit / sec x cm^2



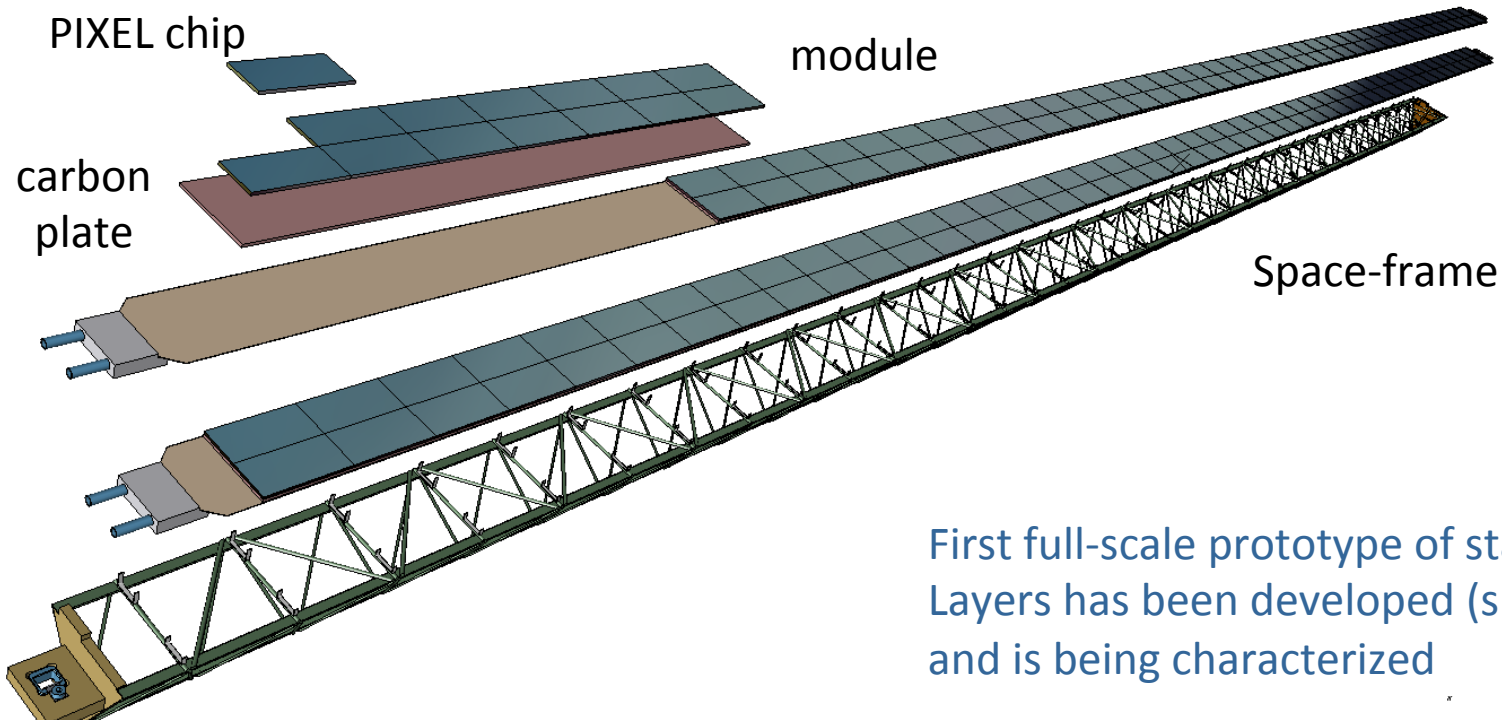




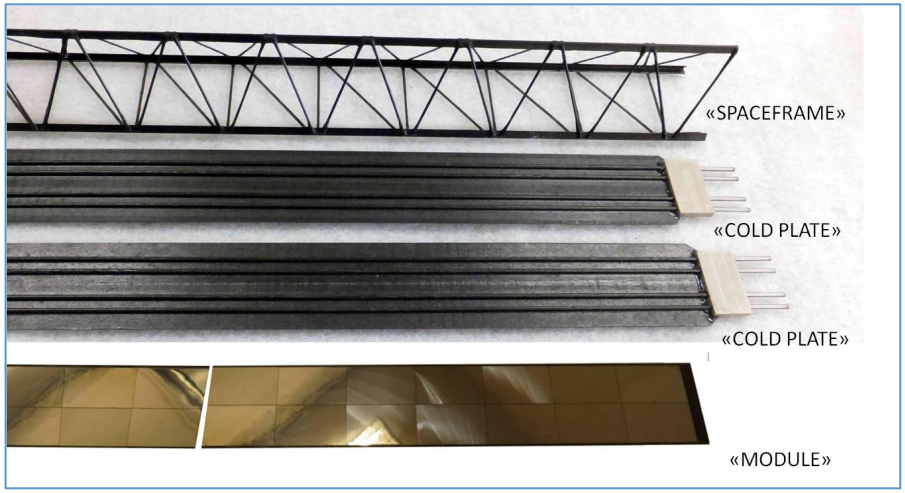
Outer Barrel Stave

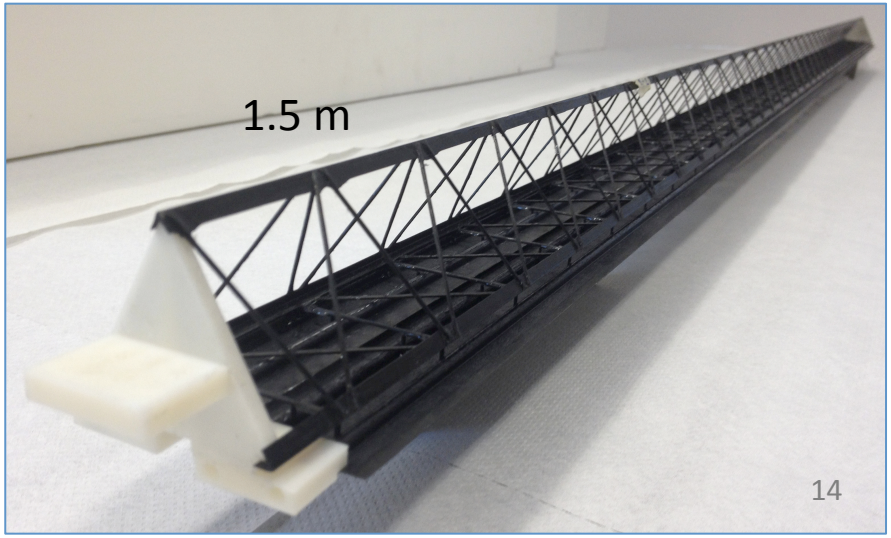


Outer Barrel – Stave prototype

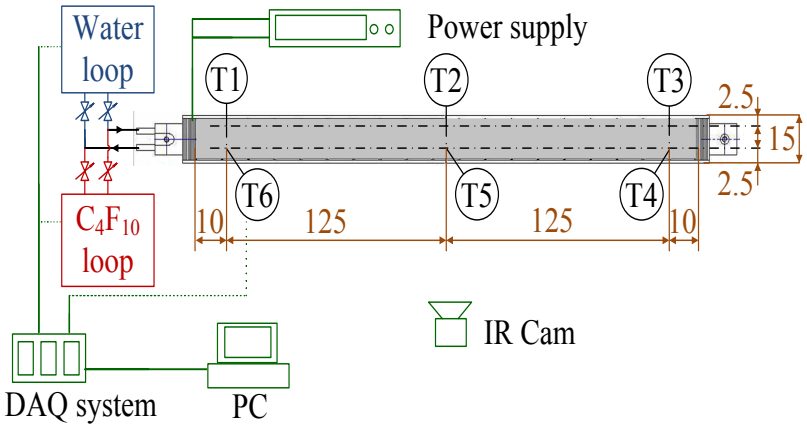


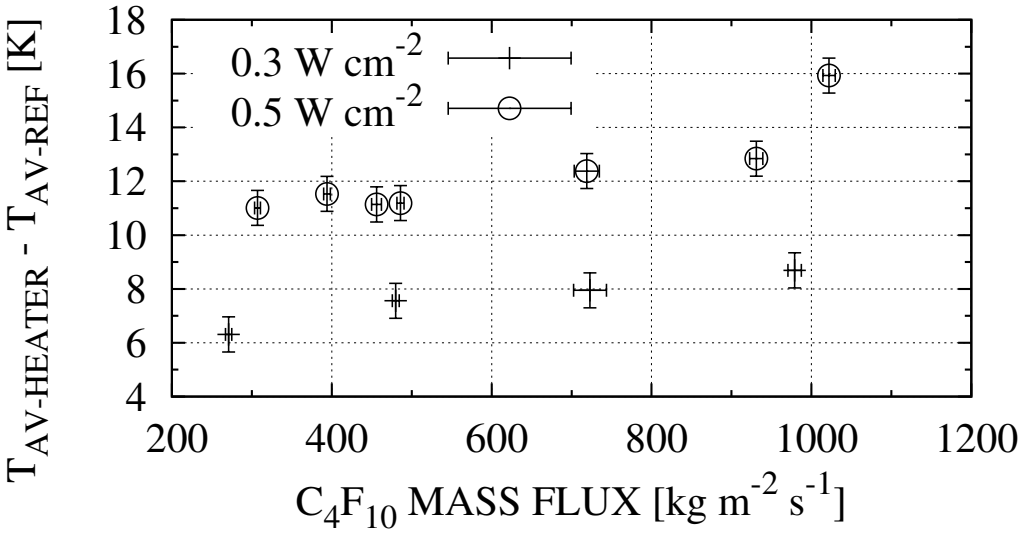
First full-scale prototype of stave for Outer Layers has been developed (summer 2013) and is being characterized





IB Stave – Thermal Characterization

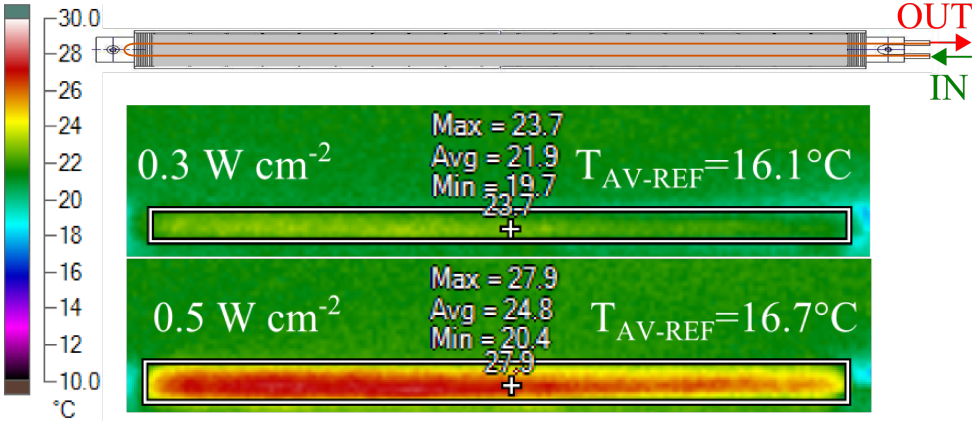




300 mW/cm^2 : <T^{chip}> - <T_{refrig}> = 6-9 °C

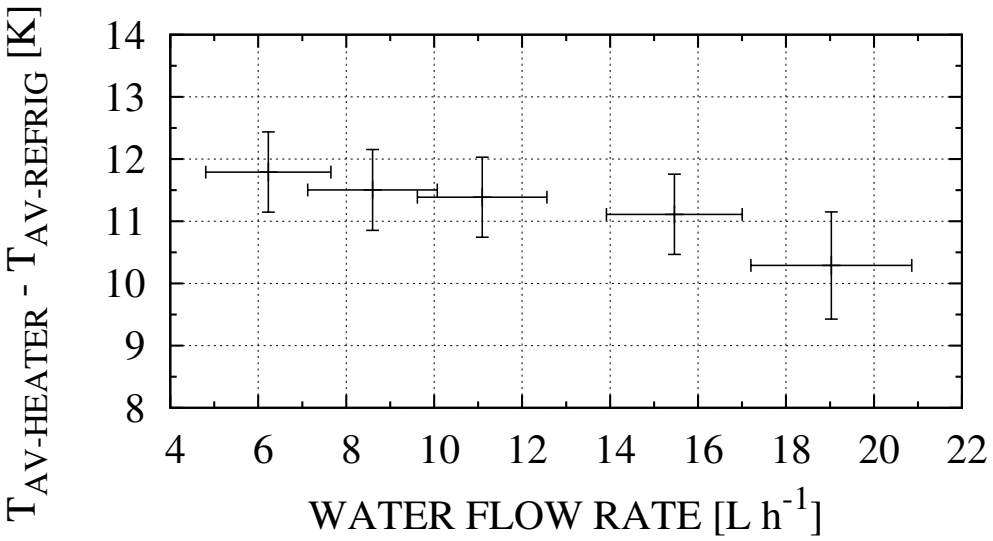
500 mW/cm^2 : <T^{chip}> - <T_{refrig}> = 11-16 °C

For T_{refrig} = 15 °C
<T_{chip}> < 30 °C up to 500mW/cm^2



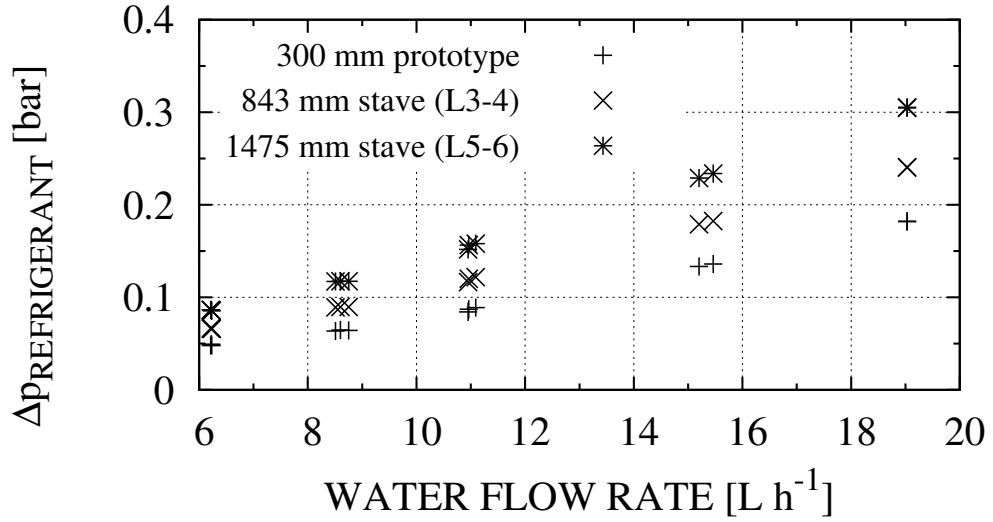
C4 F10 and water have similar performance:
=> conductive thermal resistance across stave >> convective thermal resistance between tube wall and refrigerant

OB Stave – Thermal Characterization



300 mW/cm^2 : <T^{chip}> - <T_{refrig}> = 13 °C
(max power density for OB: 100mW)

Possibility to further reduce the diameter of polyimide pipes and material budget



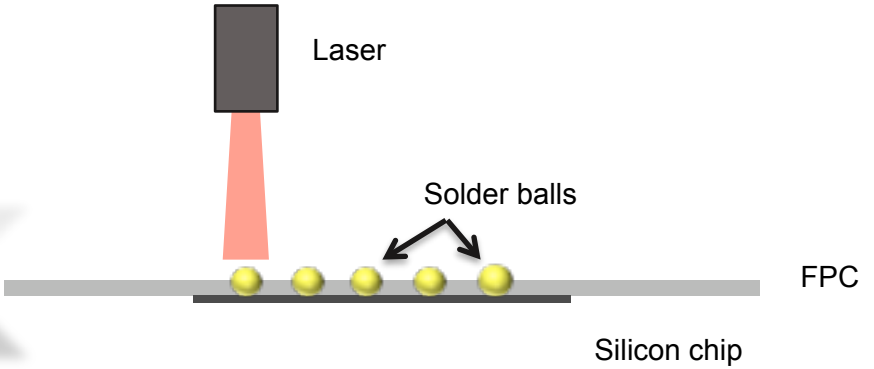
ΔP below 300 mbar in all cases

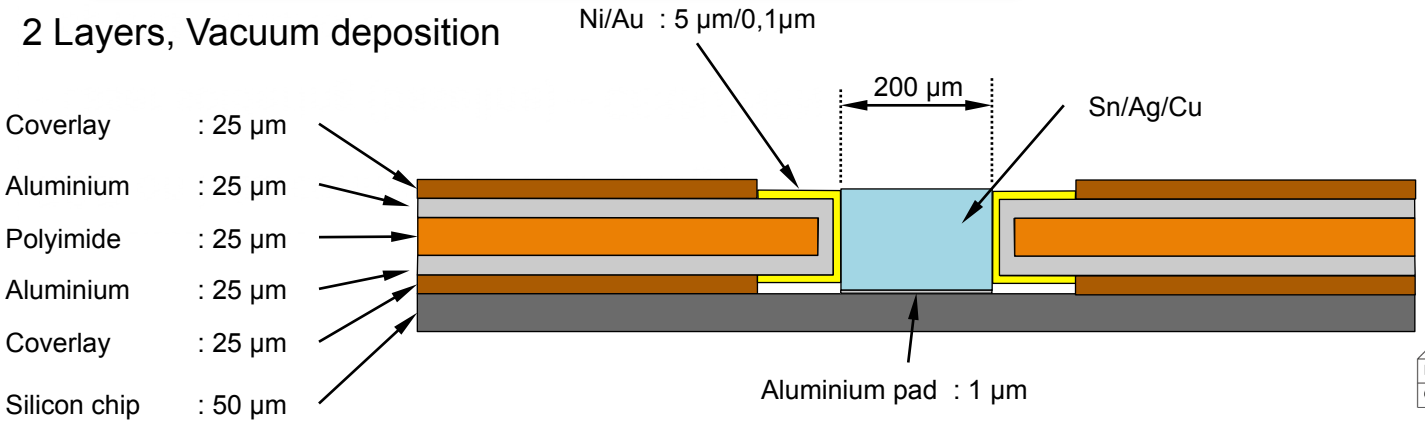
Leak-less water system can be adopted

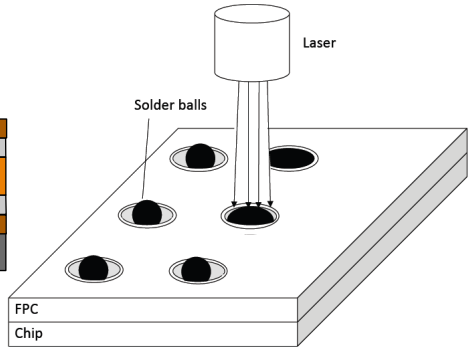
Chip Assembly – laser soldering

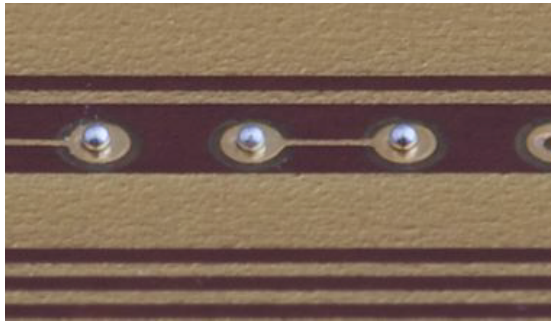
R&D on interconnection technology

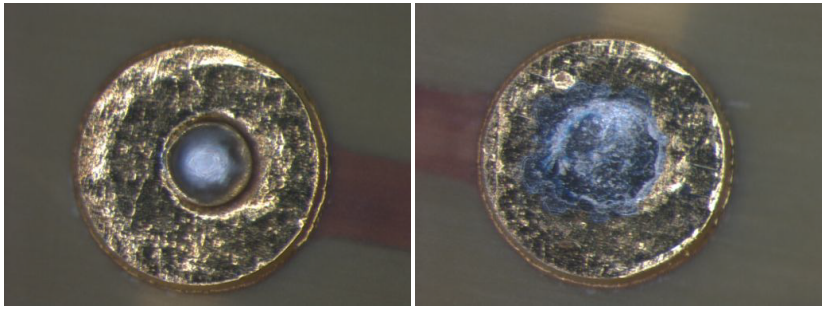
- Laser soldering (baseline) – CERN/INFN
- spTAB - Kharkov
- chip embedding – CERN

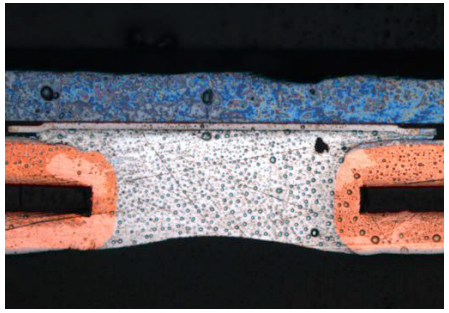








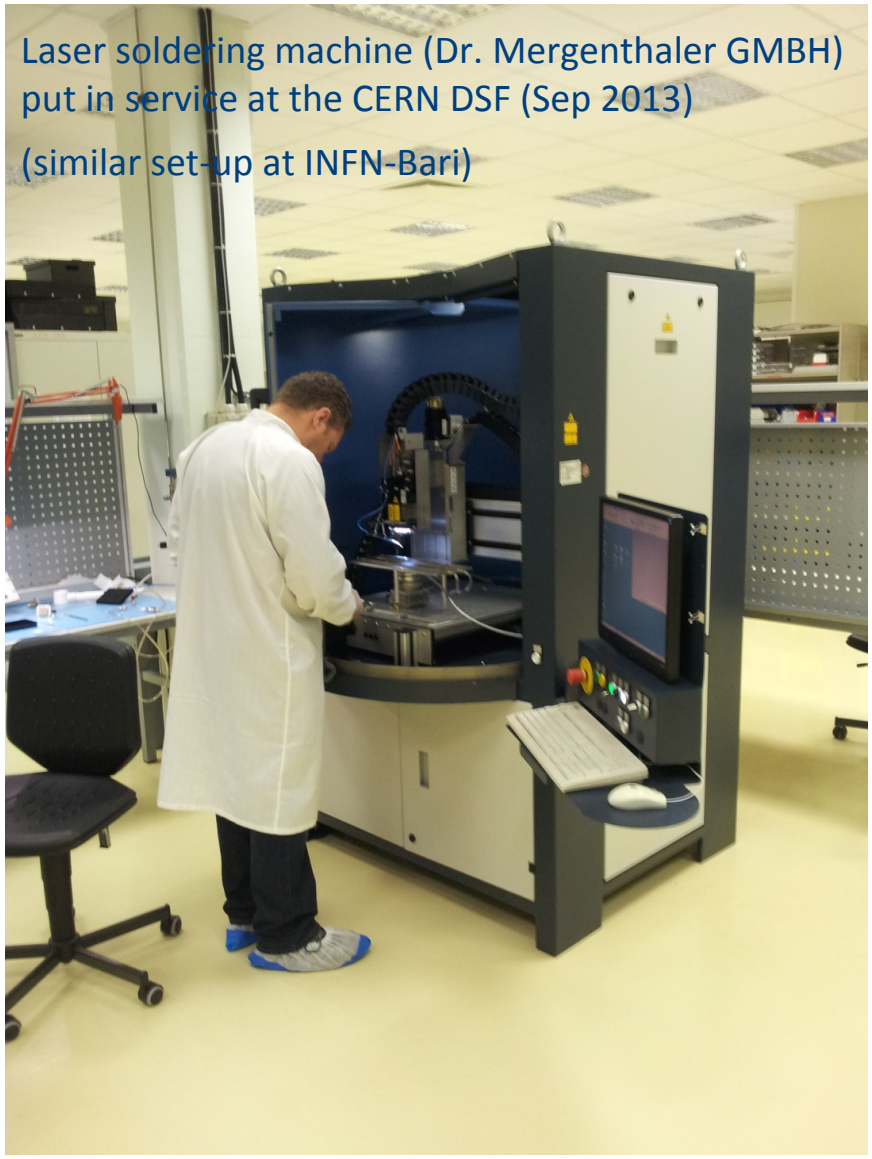


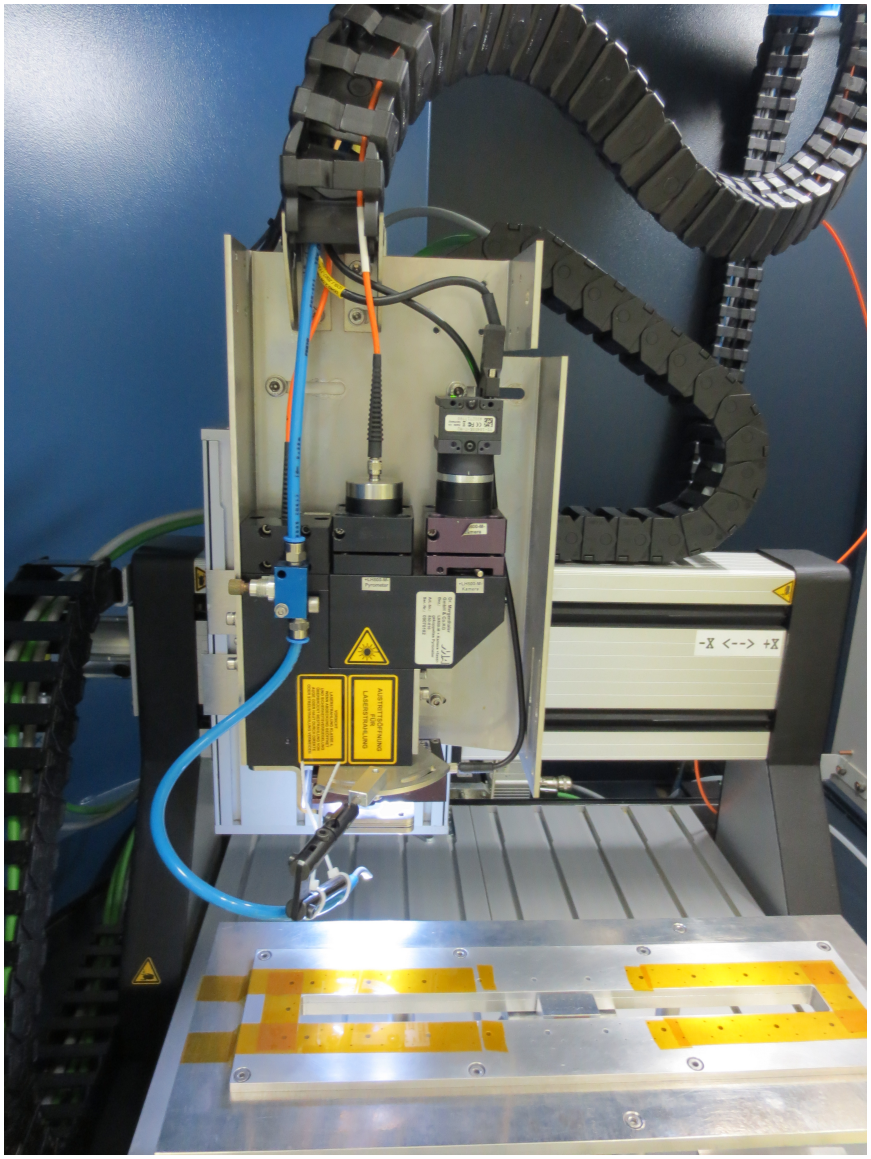


Chip Assembly – laser soldering

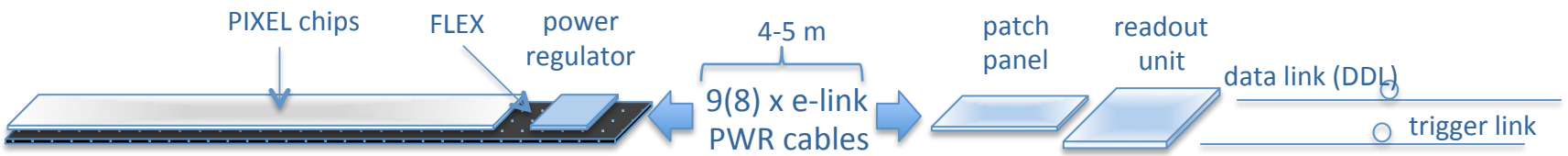
Laser soldering machine (Dr. Mergenthaler GMBH) put in service at the CERN DSF (Sep 2013)

(similar set-up at INFN-Bari)

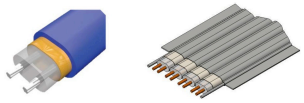




Readout – general scheme and data throughput



Schematic representation of the readout path



SAMTEC twinax "Firefly"

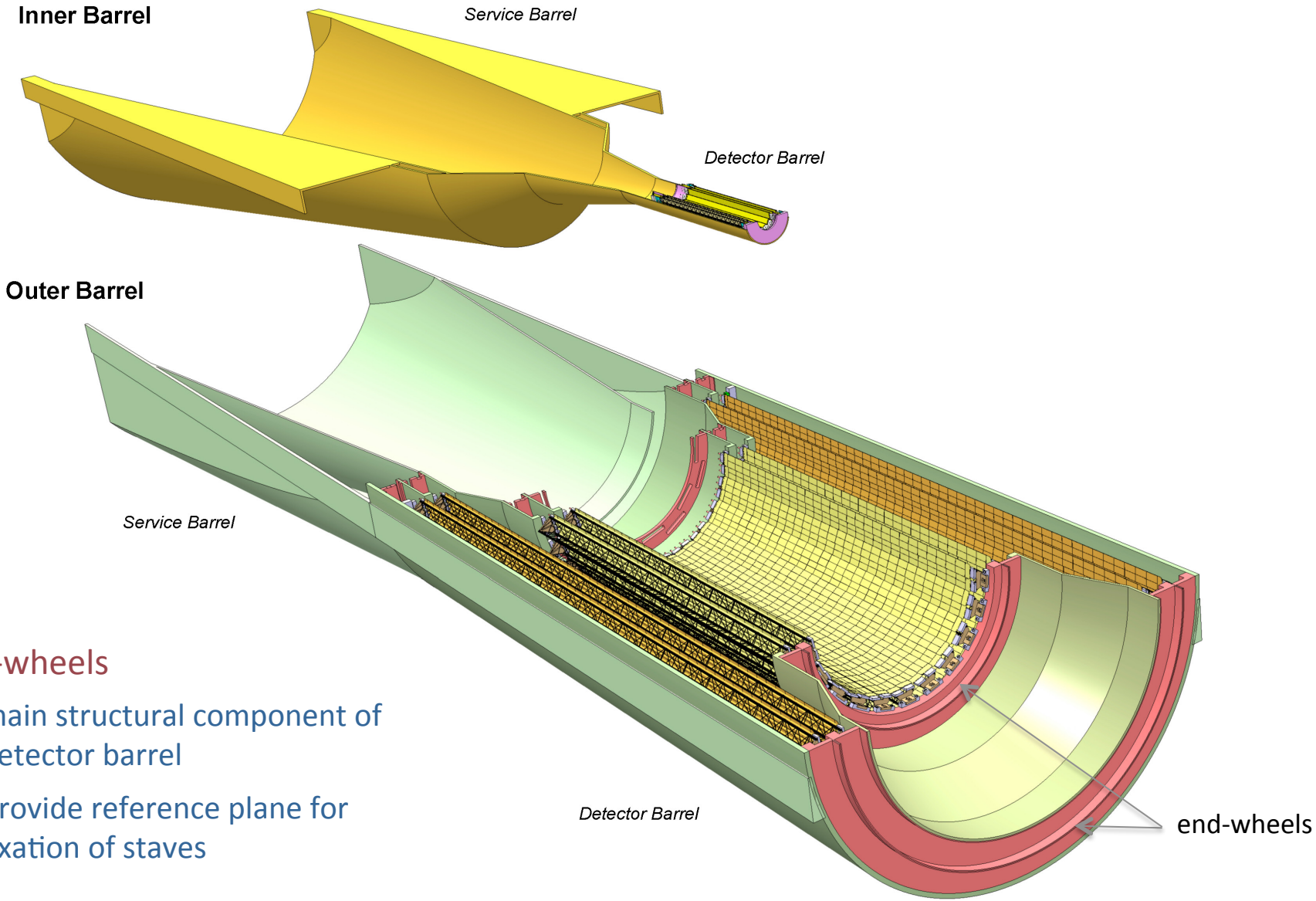
Data rates (*)

Layer	Chip (Mb/s)	Stave (Gbit/sec)	Layer (Gbit/sec)	Nr. DDL
O	351	3.1	38	12
1	225	2.0	32	16
2	157	1.4	28	20
3	12	1.3	29	22
4	10	1.1	31	28
5	6.9	1.3	50	40
6	6.6	1.3	60	46
Total	-	-		184

(*) Data rates estimated for:

a. 100 kHz interaction rate
b. QED electrons included assuming an integration time of 30μs
c. 80 bits to encode a hit
d. Fake hit rate 10^{-5}/pixel per readout frame

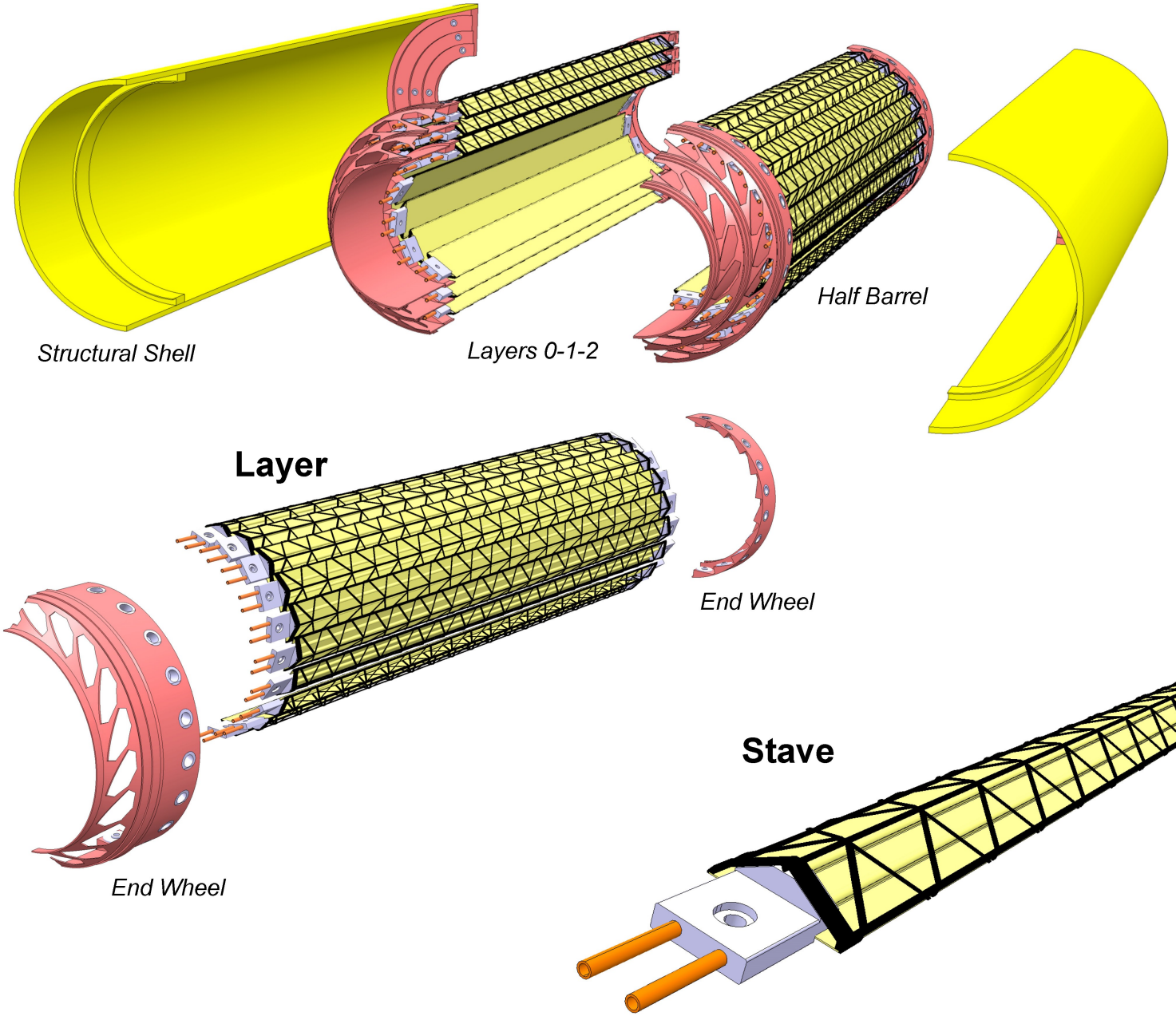
Detector Assembly



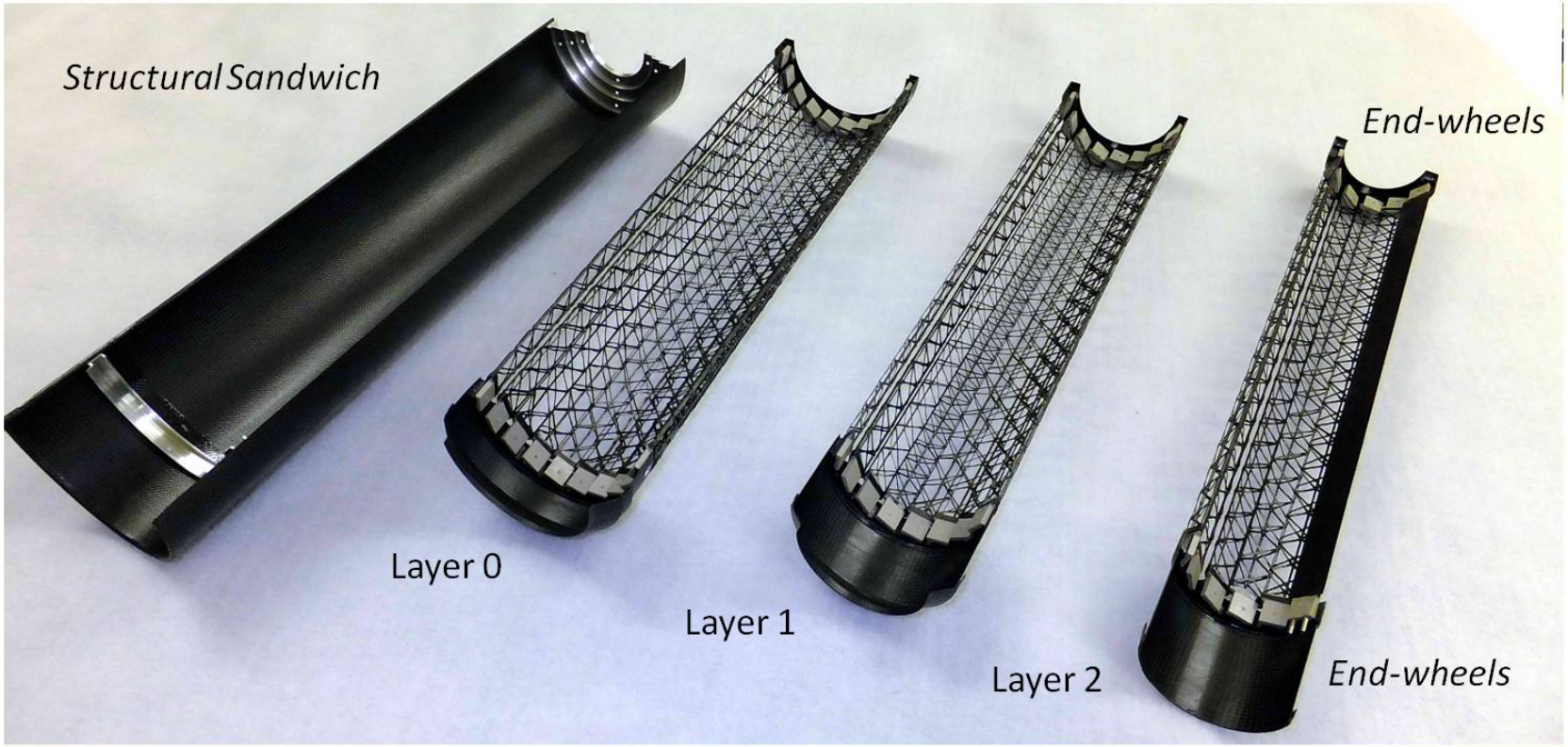
End-wheels

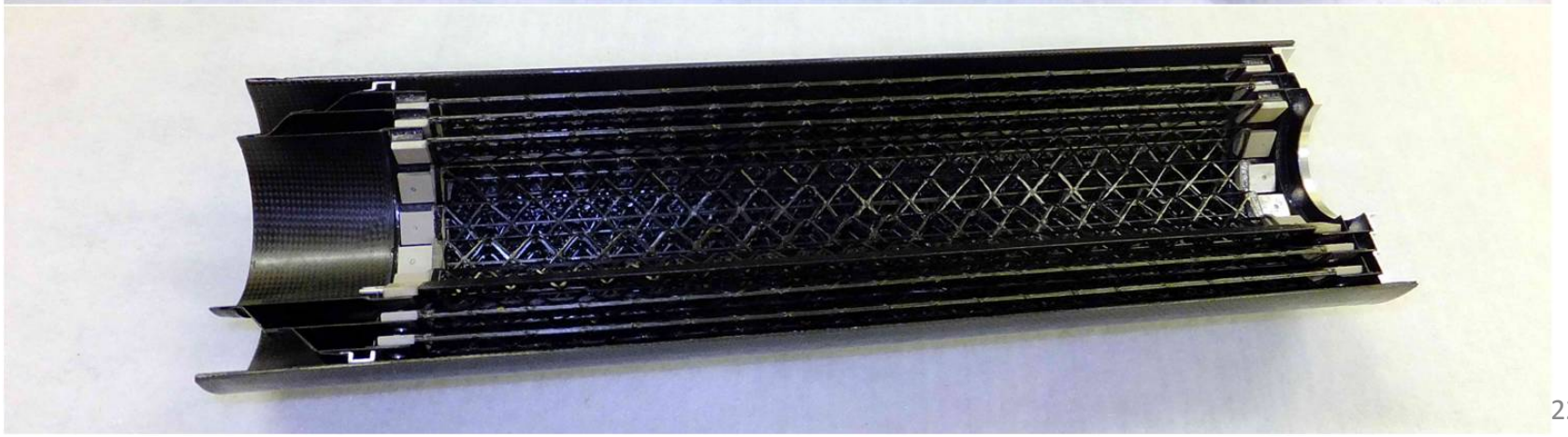
- main structural component of detector barrel
- provide reference plane for fixation of staves

Inner Barrel

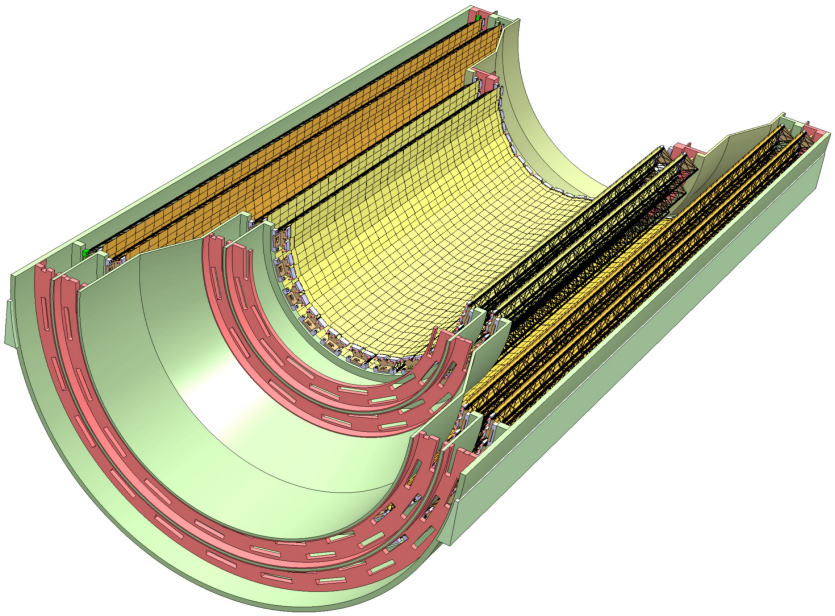


Inner Barrel – full-scale prototype (2012)

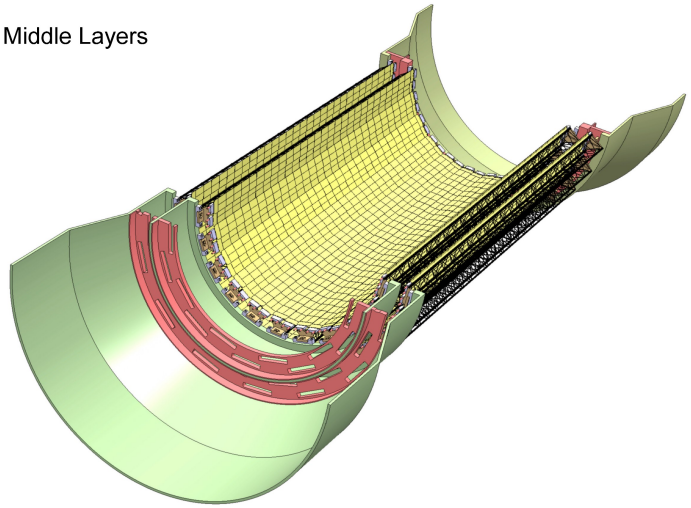




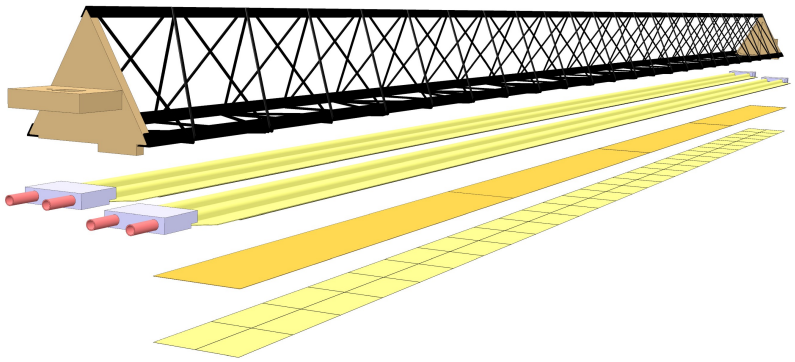
Outer Barrel



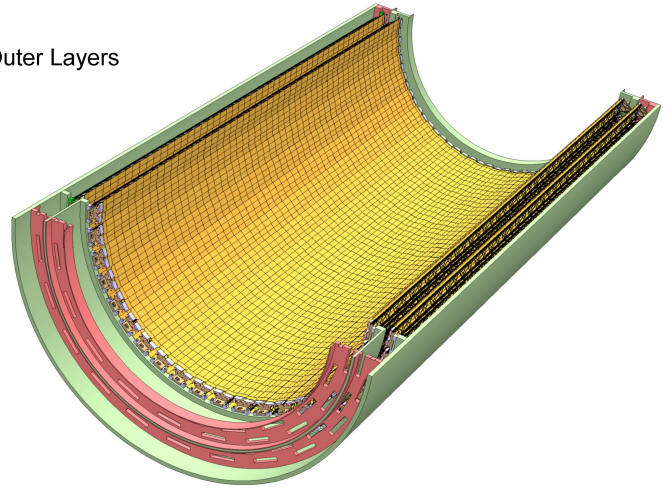
Middle Layers



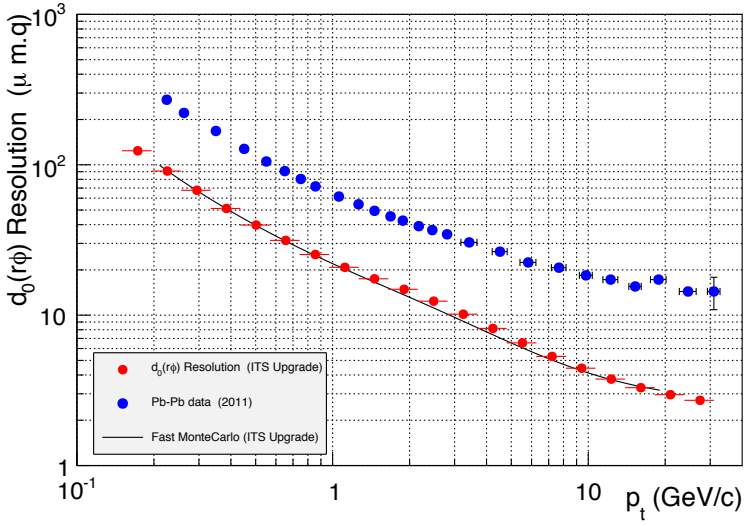
Stave

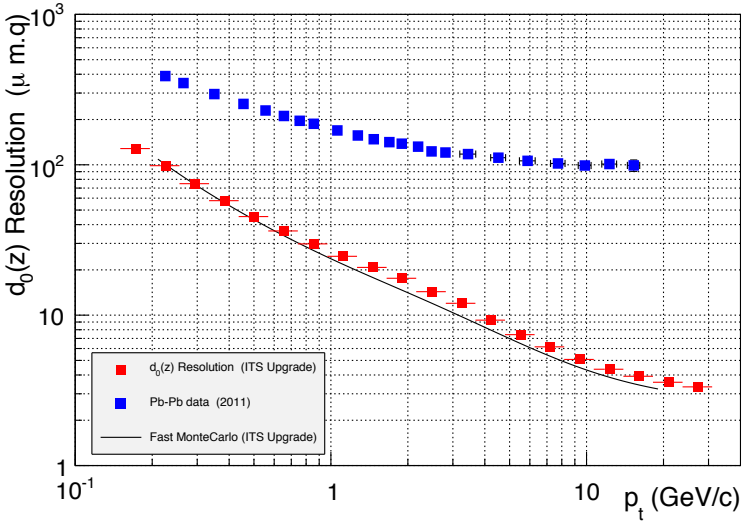


Outer Layers

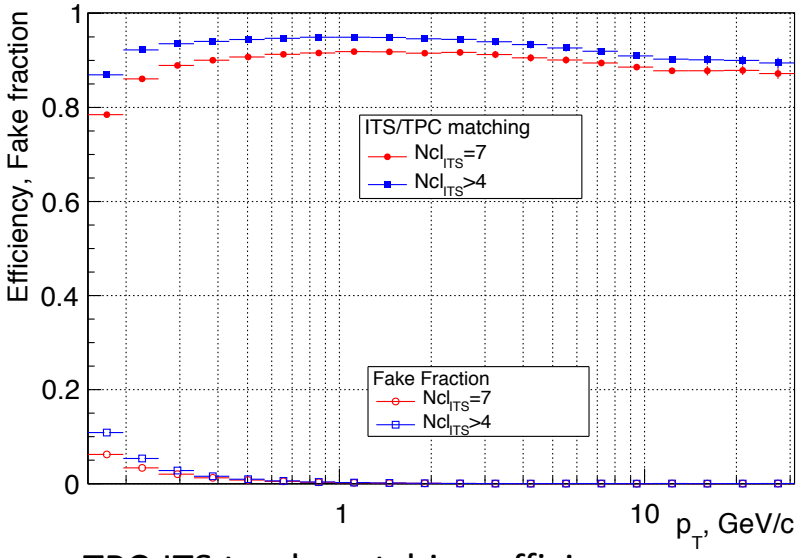


Full MC simulation

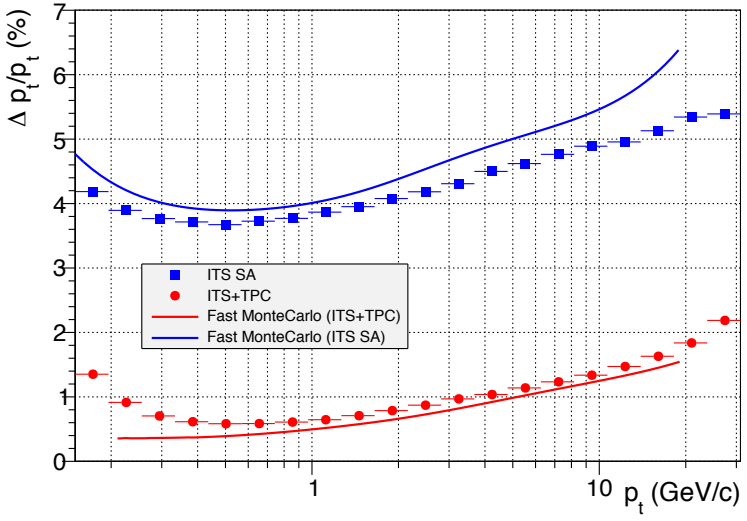




Impact parameter resolution in the bending plane (left) and longitudinal direction (right)



TPC-ITS track matching efficiency

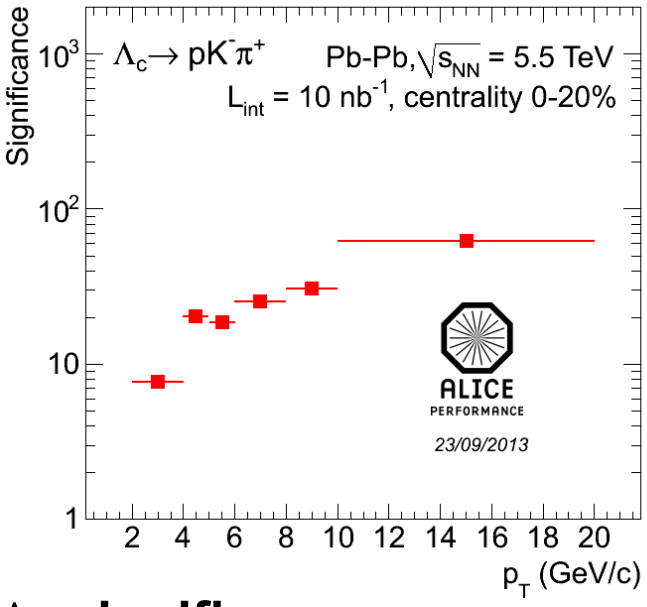


Transverse momentum resolution

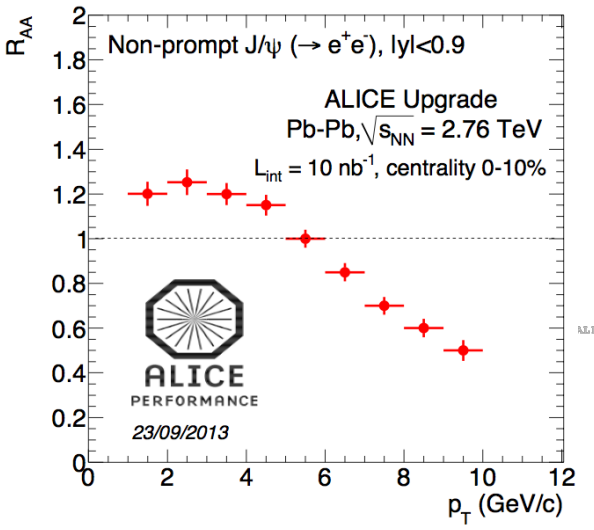
Performance for low-p_T heavy flavor

New studies for TDR: $\Lambda_c \rightarrow pK\pi$ with full upgraded ITS simulation, $D_s \rightarrow KK\pi$, $B \rightarrow J/\psi \rightarrow ee$, …

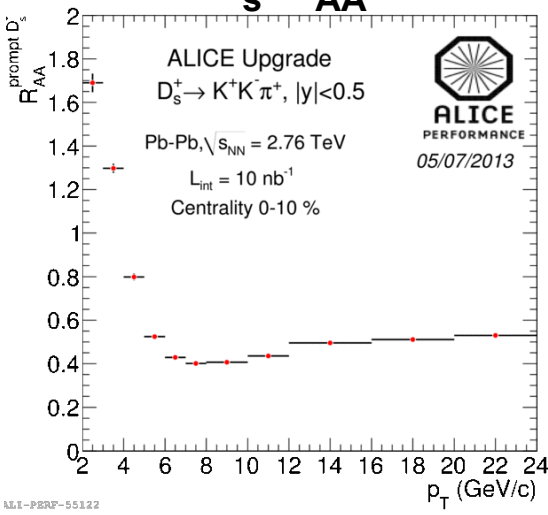
Λ_c significance



J/ψ from B R_{AA}



D_s R_{AA}



Λ_c significance:

	$2 < p_T < 4$ GeV/c	4–5	5–6	6–8	8–10	> 10
Full sim.	8	20	18	25	30	60
Hybrid sim.	8	13	11	12	12	50

Full simulation better than simplified Hybrid method

Conclusions

- ✧ Detector overall layout and technologies for main components defined
- ✧ Technical feasibility of main components demonstrated
- ✧ TDR being finalized and will be submitted to LHCC in about one month

Project timeline

- R&D continues till end 2014 (engineering of design, test, assembly and QA procedures)
- Production Q2 2015 – Q1 2017
- Layers assembly + global assembly (12 months) till Q1 2018
- Commissioning at surface (6 months) till Q3 2018
- Installation and commissioning in ALICE (4 months) Q4 2018

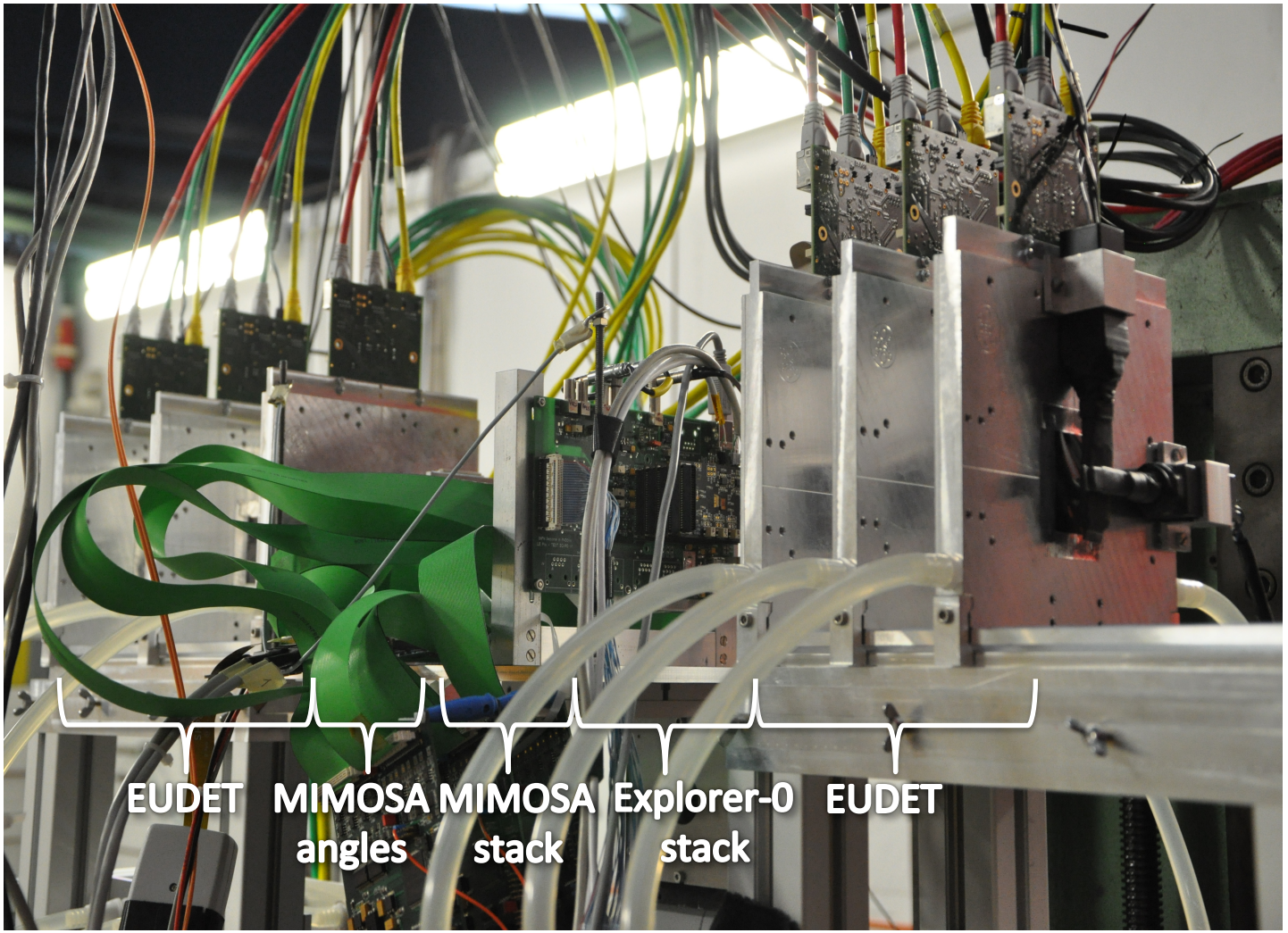
Cost: 10.8 MCHF (Construction) + 4 MCHF (R&D)

Collaboration: CERN, China (Wuhan), Czech Republic (Prague), France (Strasbourg, Grenoble) Italy (Bari, Cagliari, Catania, Frascati, Padova, Roma, Torino, Trieste), PAKISTAN (Islamabad) Netherlands (NIKHEF, Utrecht) , Rep. of Korea (Inha, Yonsey, Pusan), Russia (St. Petersburg) Slovakia (Kosice), Thailand (Nakhon), UK (Birmingham, Daresbury, RAL) Ukraine (Kharkov, Kiev), US (Berkeley)

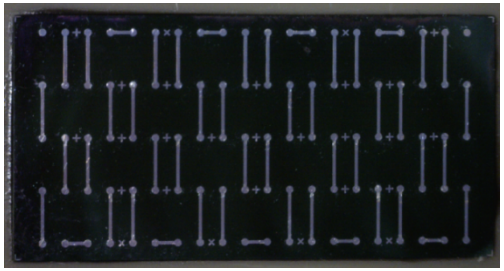
SPARE SLIDES

PIXEL Chip Prototypes – Characterization at CERN and Desy

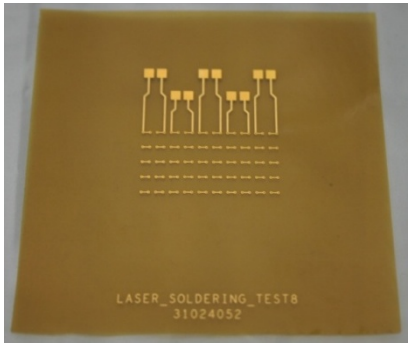
Desy setup @ “Strahl 21”, 4-5 Gev electron beam



Chip Assembly – laser soldering

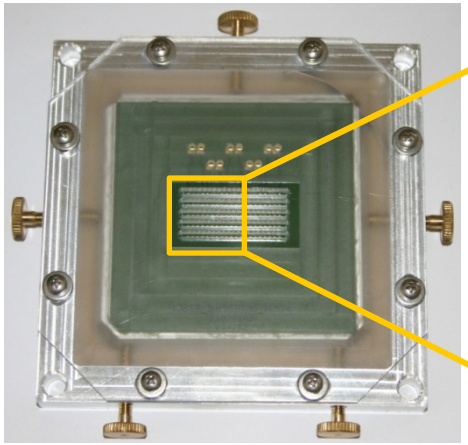


- size 15 mm × 30 mm
- 50 µm thick
- 100 pads per chip
- pad size: 400 µm diameter

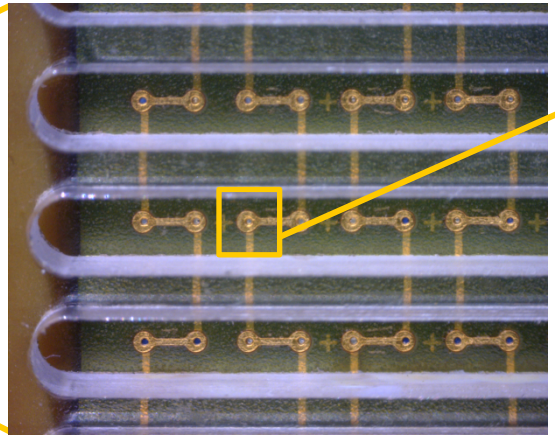


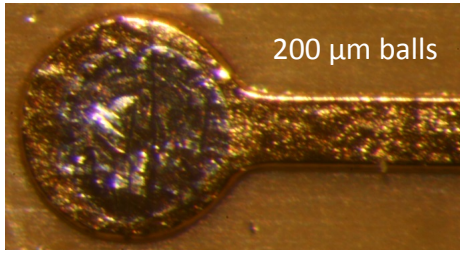
- size 70 mm × 70 mm
- ~ 70 µm thick
- hole diameter: 200 µm

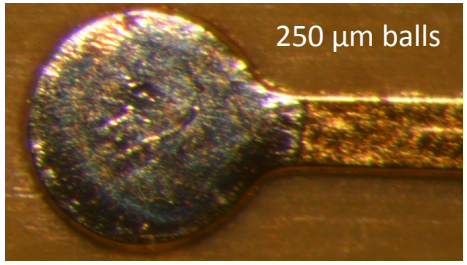
Mechanical tool

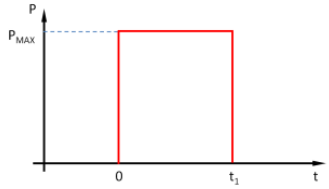


Plexiglass grid







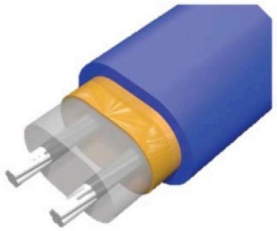


Power (6 ÷ 8) W, t_1: (60 ÷ 80) ms

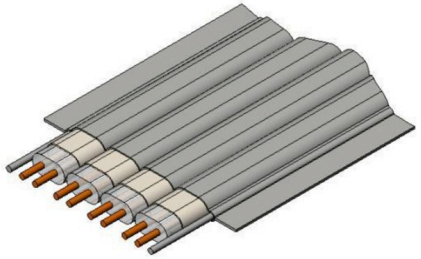
Readout – electrical link

Communication between Pixel Chip and Readout Unit via electrical links:
data rate <500Mbit/s cable length ~4m

Investigation of COTS cables ➡ SAMTEC AWG30 twinax "Firefly" (100Ω impedance)

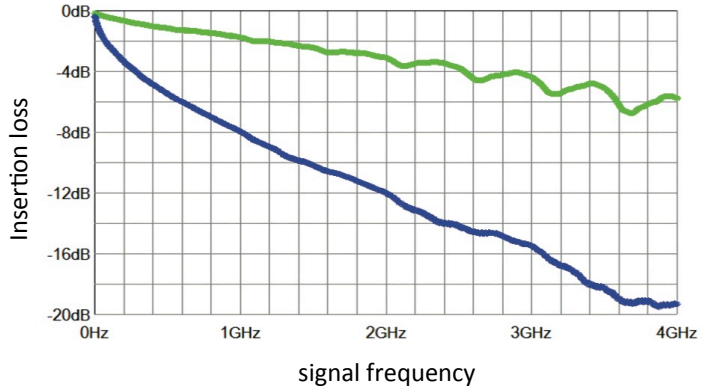


Twinax pair

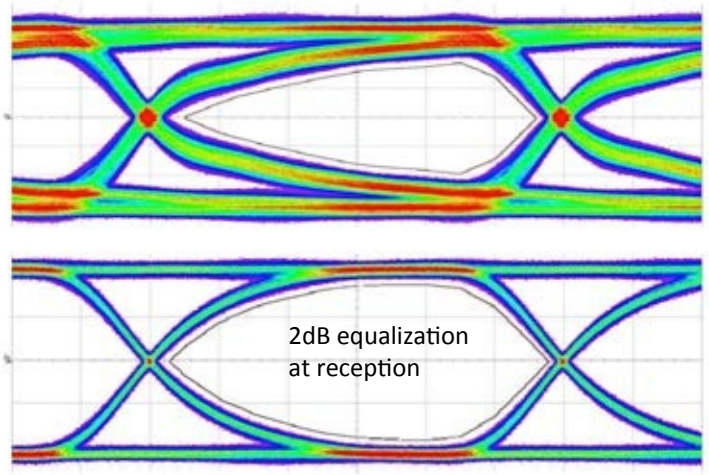


Laminated assembly

Measurement of insertion loss (left) and eye diagram (right) for a 4-m long SAMTEC twinax cable

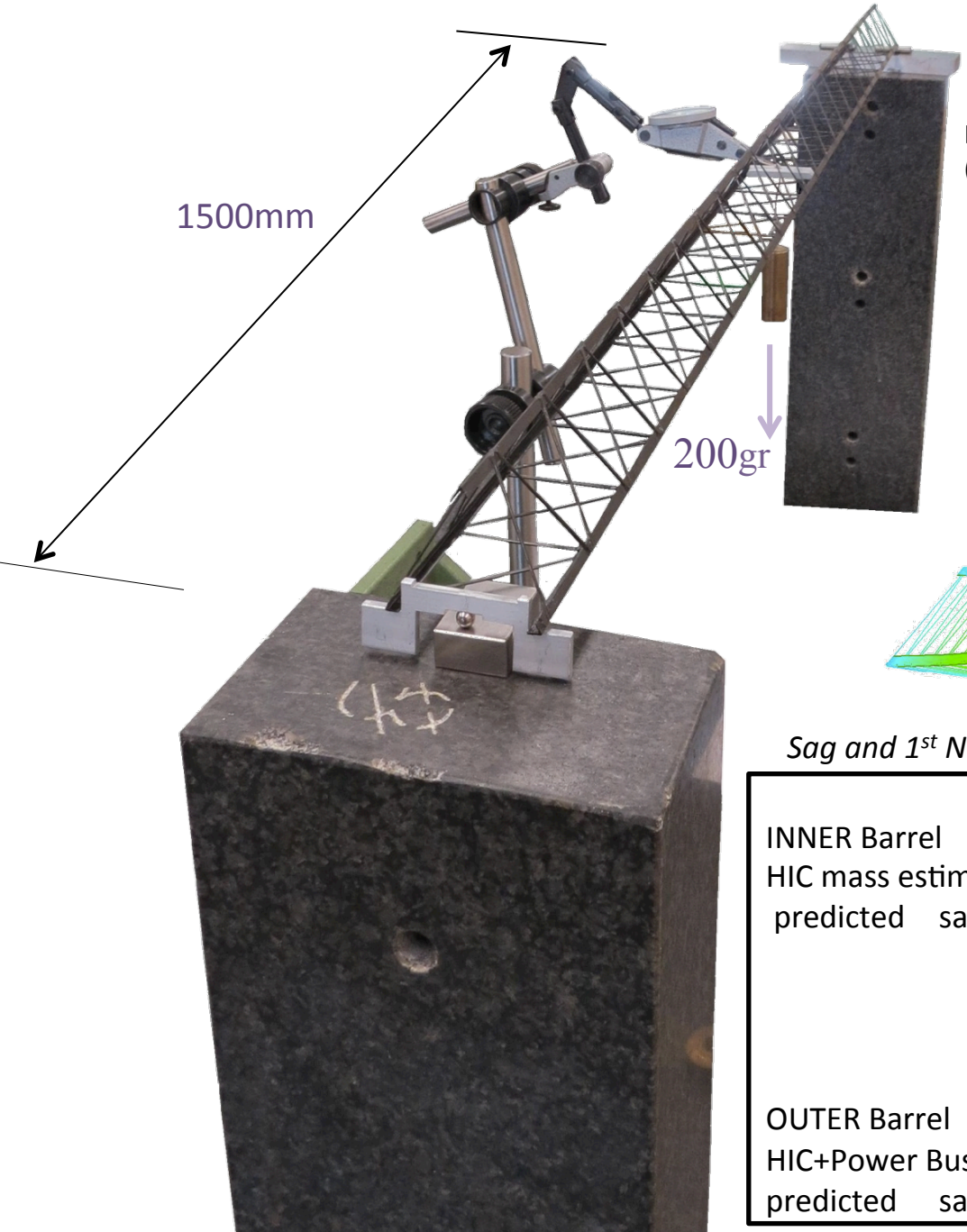


@1Gbit/s

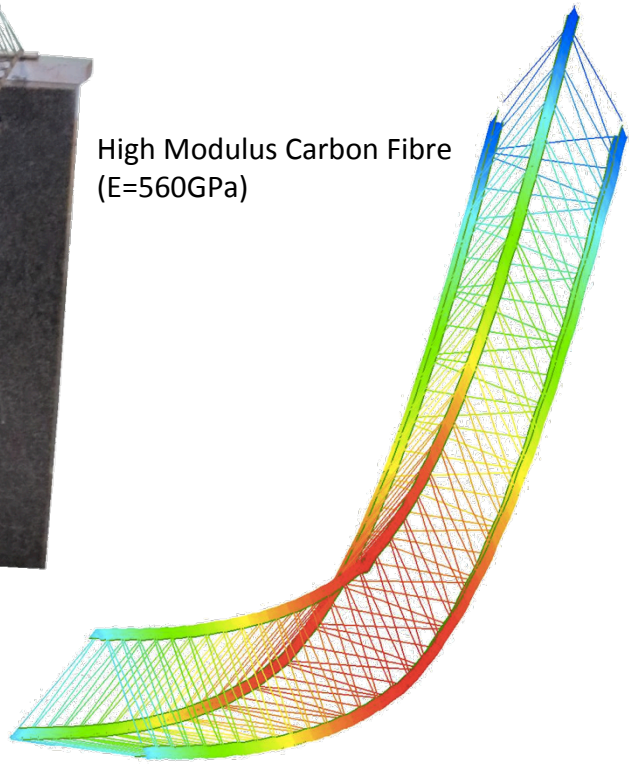


TEST

Finite Element SIMULATION

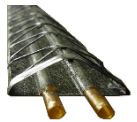


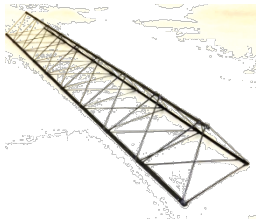
High Modulus Carbon Fibre
(E=560GPa)



Sag and 1st Natural Frequency prediction under working condition

INNER Barrel
HIC mass estimate =2 gr
predicted sag 4-9 µm 1° Natural Frequency>100Hz



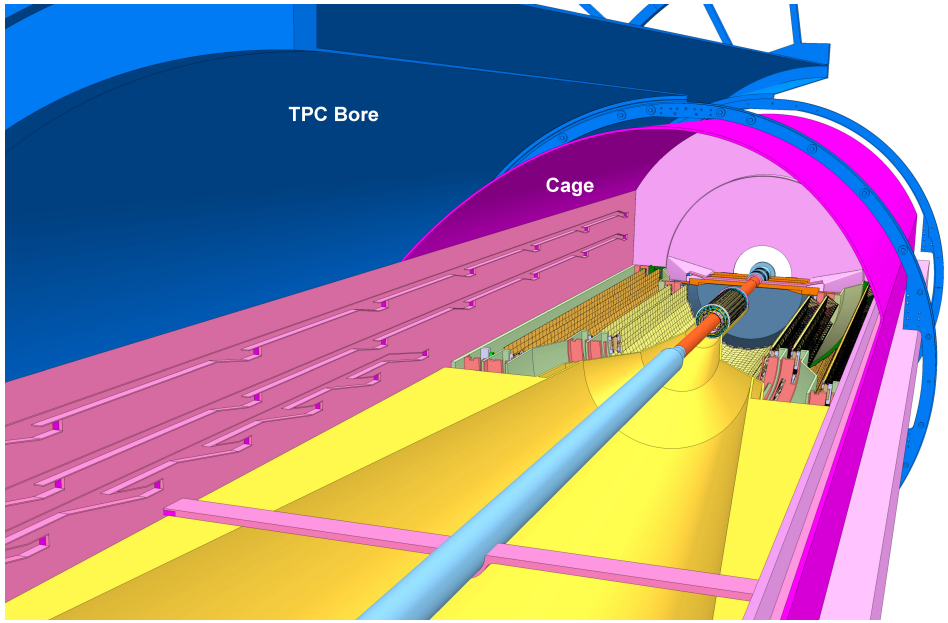


OUTER Barrel
HIC+Power Bus+Coldplate mass estimate = 200 gr
predicted sag 40-110 µm 1° Natural Frequency>50Hz

Mechanics for insertion and removal

Detector Cage : stiff shell (light composite material) fixed inside the TPC bore

Provides common support for the barrels and the beampipe



Cage contains precise guiding rails for the insertion of the detector-service barrels

Installation Sequence