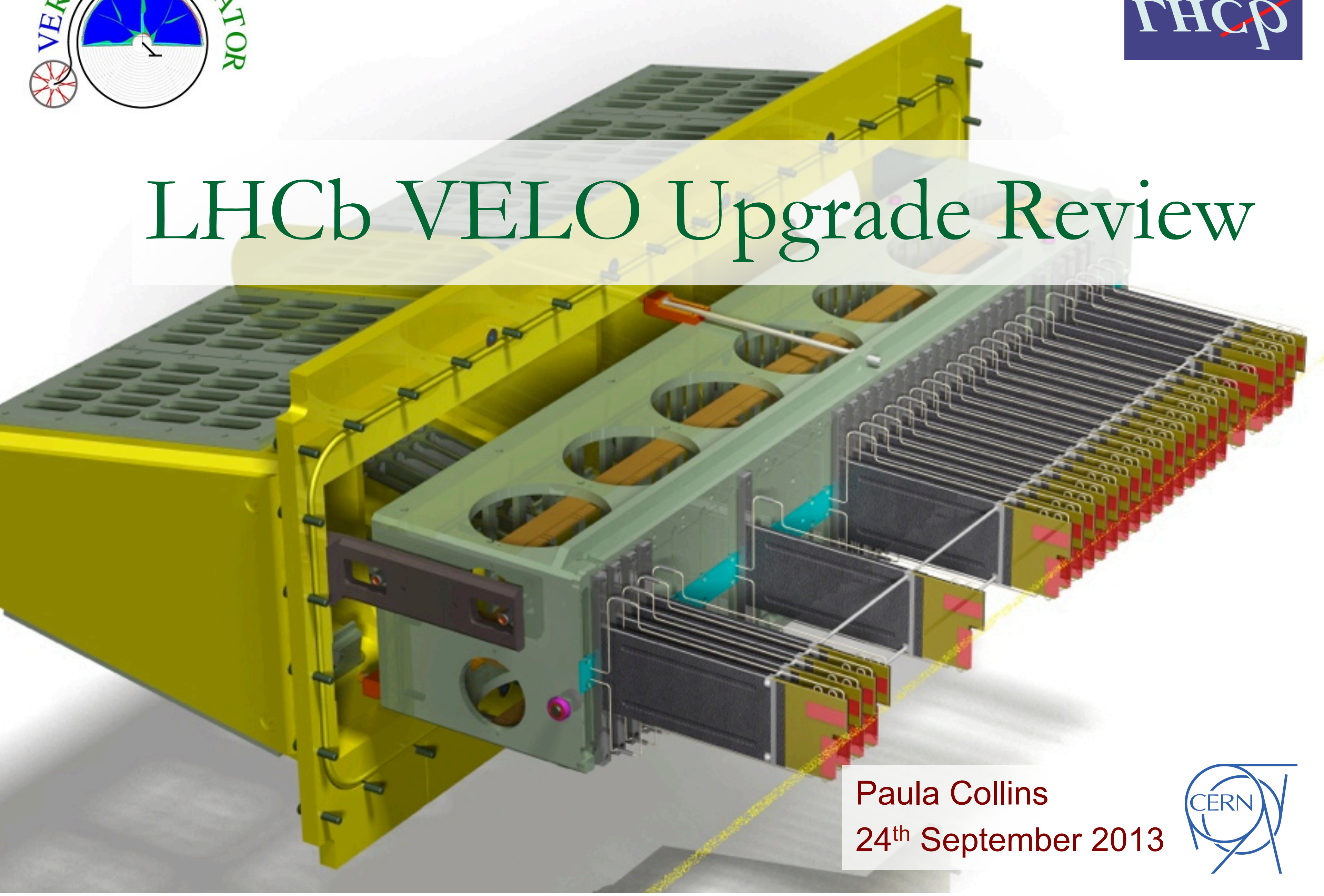
LHCb VELO Upgrade Review



Paula Collins

24th September 2013

Introduction & Contents

Since last LHCC collaboration has made major technology choice at the VELO Upgrade Technology Review (VUTR)

➔ Decision made for microchannel cooled pixel technology
➔ Conclusions of meeting will be described in this talk

Two major upgrade bids related to LHCb VELO have been submitted:

➔ UK: Covers RICH, VELO, physics+computing (+SciFi)
➔ Netherlands: Covers VELO, SciFi, HLT

VELO TDR planned for end of year, supported by important system electronics review on November 7th

A few highlights from developments since the VUTR will be described in this talk

➔ Microchannel cooling developments
➔ News from the Pixel ASIC
➔ Sensor Development

VELO Review Process

22-23 May Velo Upgrade Technology Review Nikhef, Amsterdam → Velo Upgrade meeting 14th June → Technical Board 20th June → Collaboration Approval 17th July

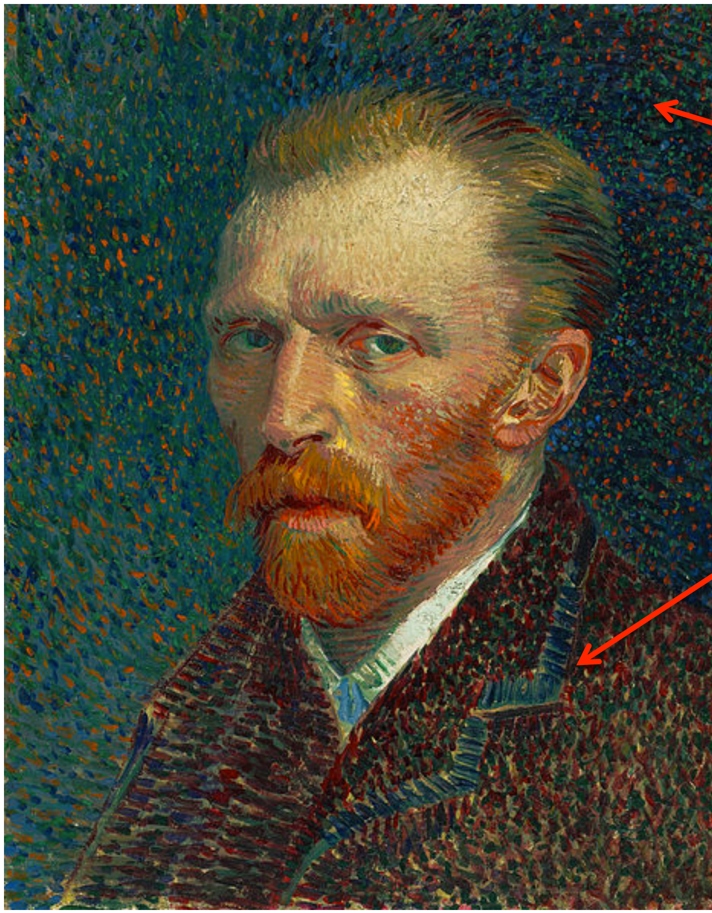
Supporting Documentation (Internal LHCb documents)

VELO Upgrade Technology Review Support Document
UPT (Upgrade, Physics and Trigger) Document
Referee Report
Group statements and Group Leader Statements

Many thanks to referees:

Richard Brenner, Hans-Juergen Hilke, Petra Riedler, Thomas Ruf and Andrea Venturi.

VELO Upgrade Technology Review
Amsterdam 22-23 May 2013



Segmentation:

Pixels

or

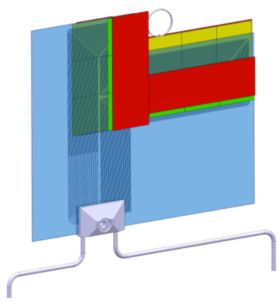
Short Strips

Which gives the better definition?

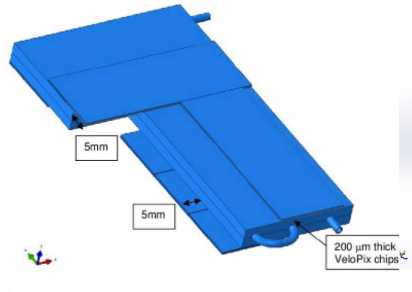
Scope of Review

Consider viability of four specific scenarios

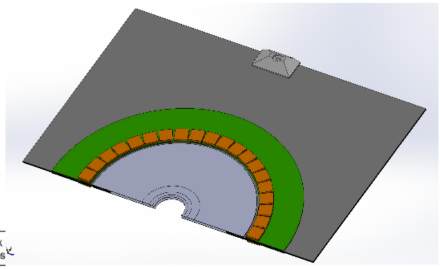
Pixel sensors, microchannel cooling



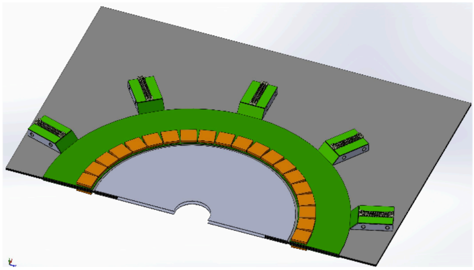
Pixel sensors, pocofoam cooling



Strip sensors, microchannel cooling



Strip sensors, TPG block cooling



All options have equivalent foil thickness and clearance, same minimum radius, full geometric efficiency etc.

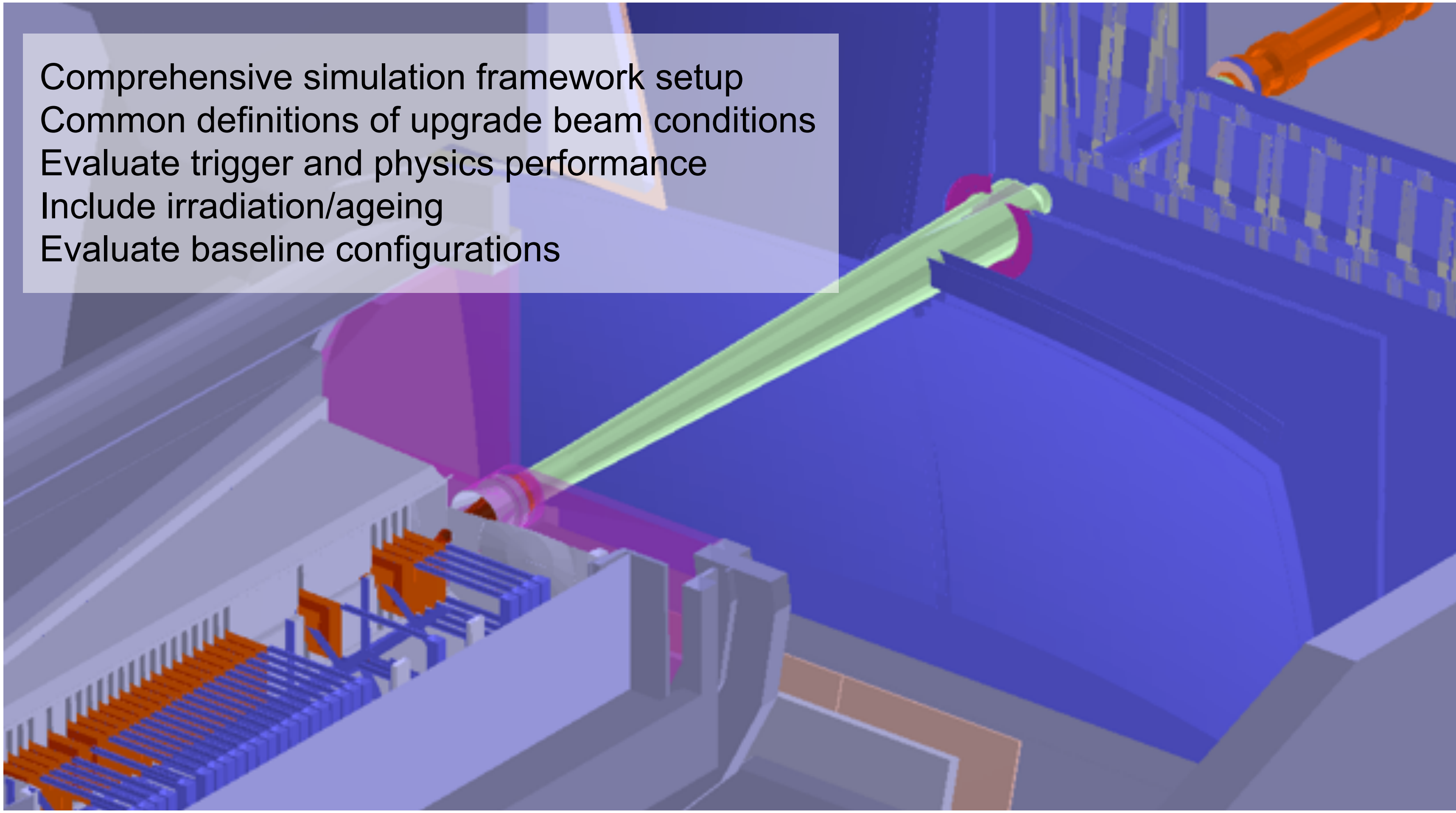
All options have integrated cooling (departure from current VELO)

Focus on system aspects which are affected by technology choice

Reviewer mandate: Review “fairness” of comparisons, identify missing items, identify risks, highlight pros and cons of sensor technology and cooling technology

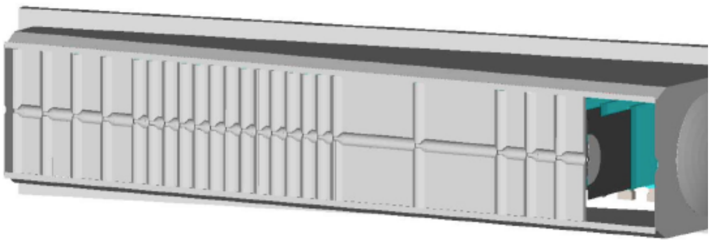
Upgrade Simulation

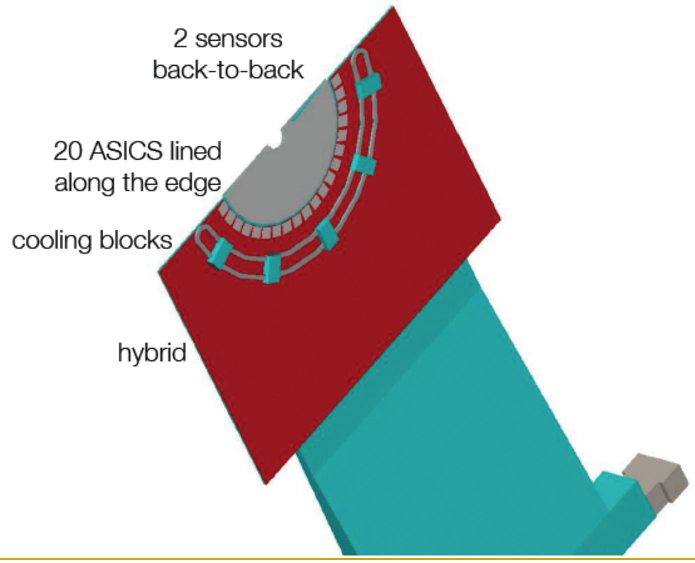
Comprehensive simulation framework setup
Common definitions of upgrade beam conditions
Evaluate trigger and physics performance
Include irradiation/ageing
Evaluate baseline configurations



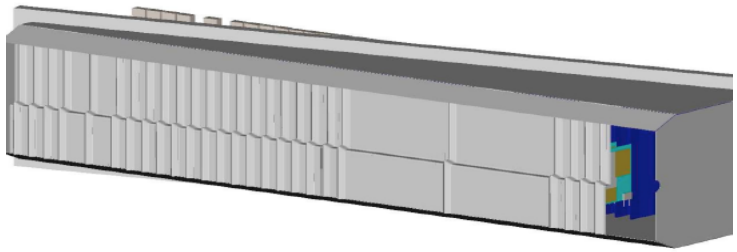
Pixel/Strip module concepts

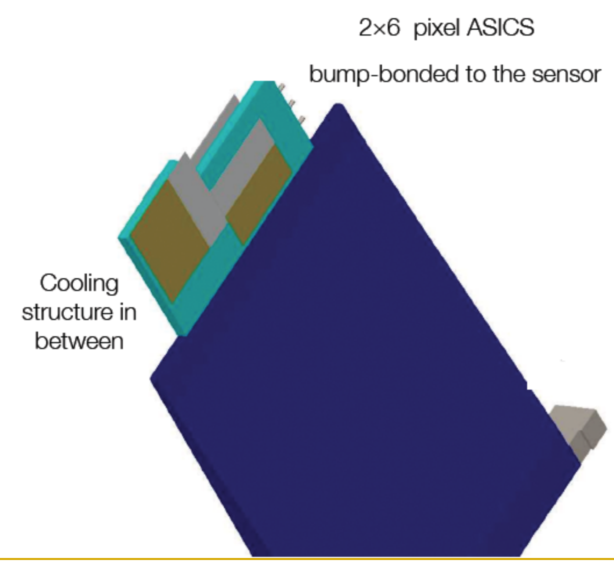
Strip modules, U shape foil



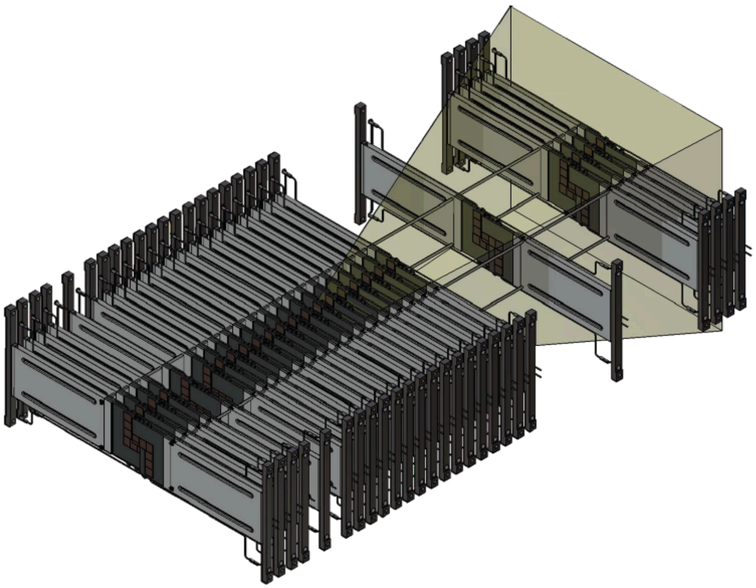


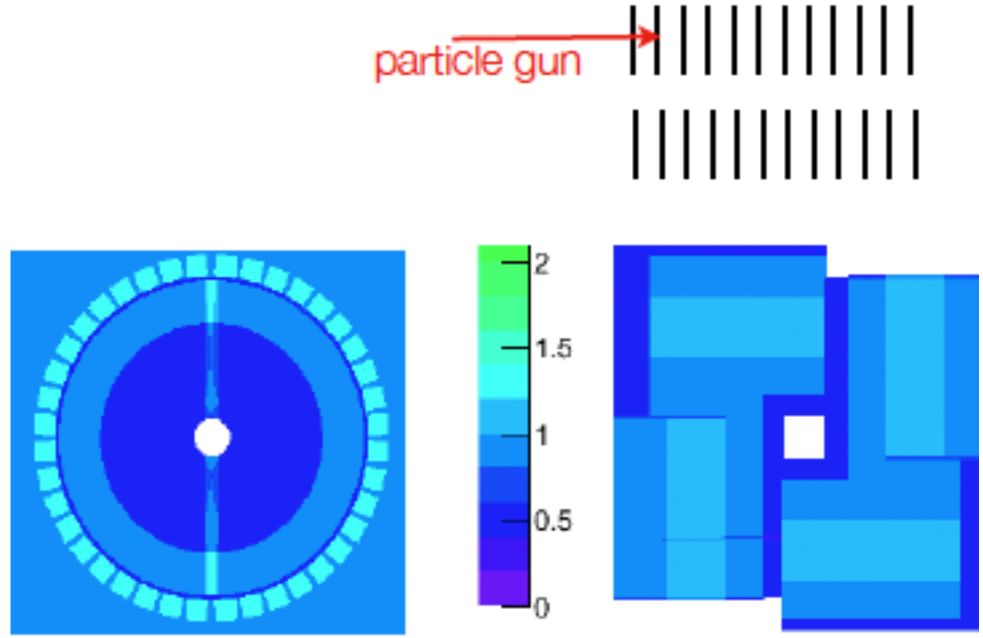
Pixel modules, L shape foil





Material budget

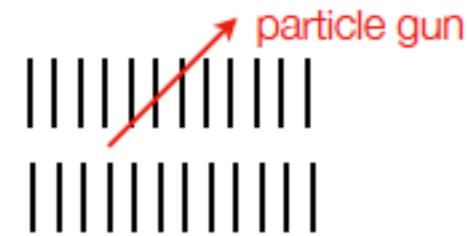




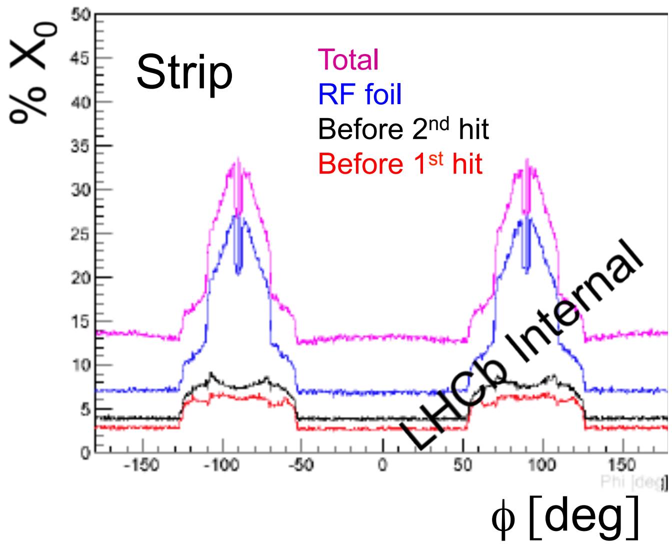
Innermost module material, particle gun

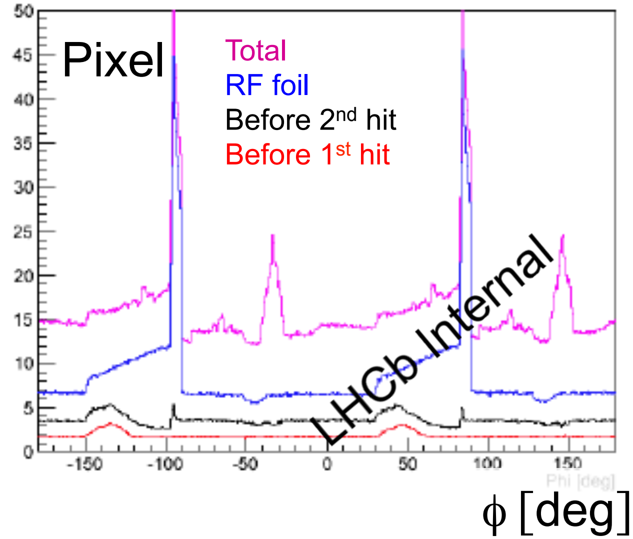
All VELO module material is in the acceptance
Strong dependence on angle and z origin
Strip modules have slightly lower material budget

Material Budget



Material budget seen by particles produced in proton proton collisions in LHCb

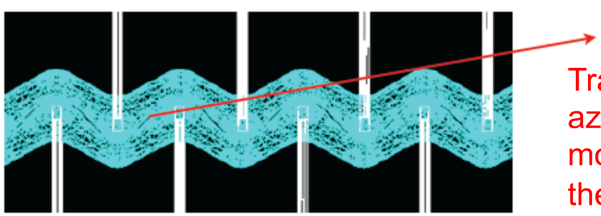




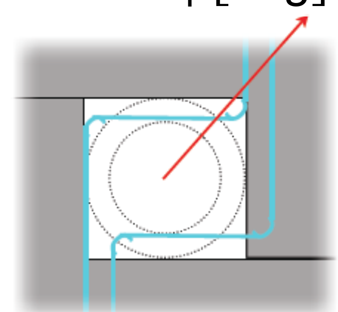
Total amount of material similar between strip/pixel

Pixels have less material before 1st measured point

1st measured point in the pixels is slightly further away

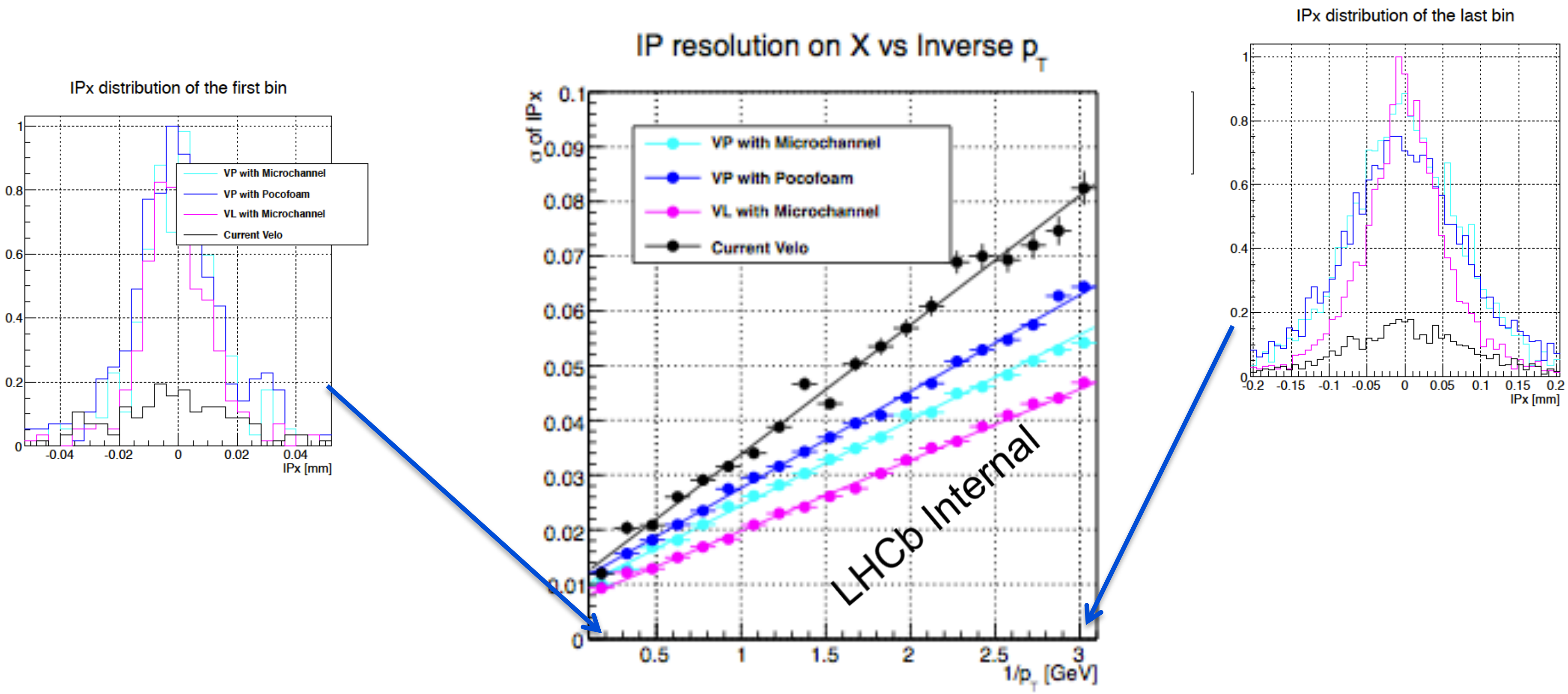


Tracks with large azimuthal angle see more material from the overlapping foils



L shaped foil breaks the radial symmetry. Tracks traverse high X_0 region more acutely

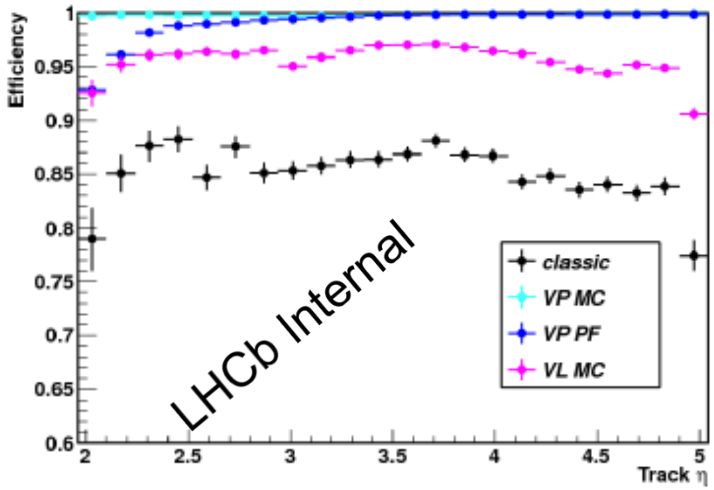
Simulation: Impact Parameter

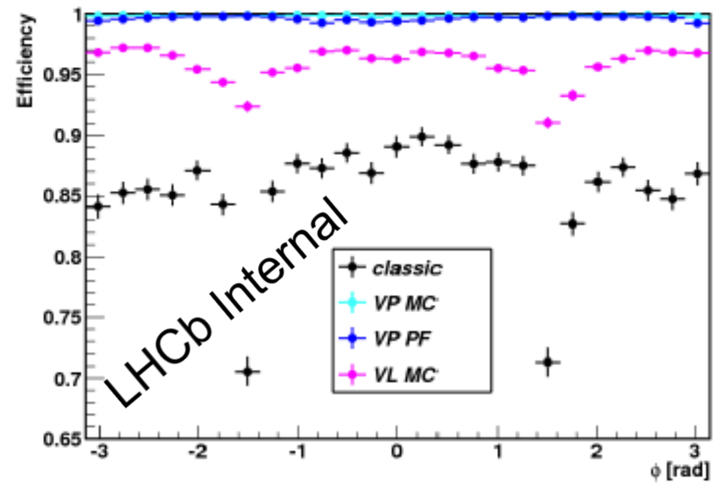


All options better than current VELO, in upgrade conditions
Excellent pixel performance reflects in part advantages of L shape design
phi dependence for both strips and pixels

Tracking Efficiency and Timing

VELO reconstruction efficiency: Upgrade conditions





All options superior to current VELO, in upgrade conditions

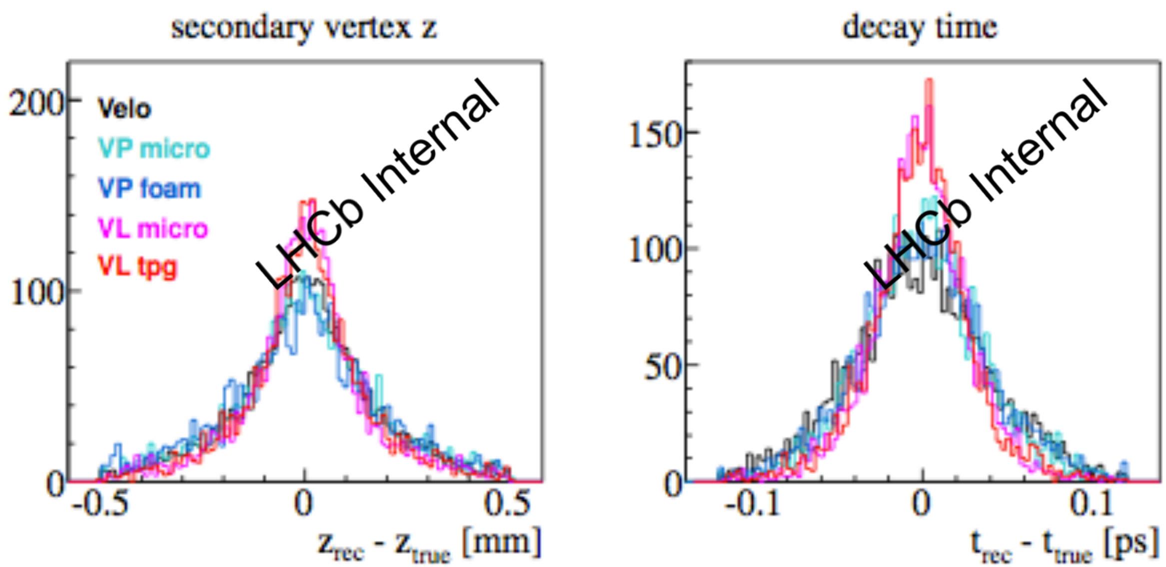
Pixel option uniformly close to 100%

Strip option ~ 96%

VELO pixel timing faster (with caveat that clustering must be added at <2 ms)

Setup	Time [ms/evt]
Velo classic $\nu = 3.8$	< 2
Velo classic $\nu = 7.6$	4.8
VL TPG $\nu = 7.6$	8.7
VL μCh $\nu = 7.6$	7.5
VP pocofoam $\nu = 7.6$	3.6
VP μCh $\nu = 7.6$	2.8

Decay Time Resolution



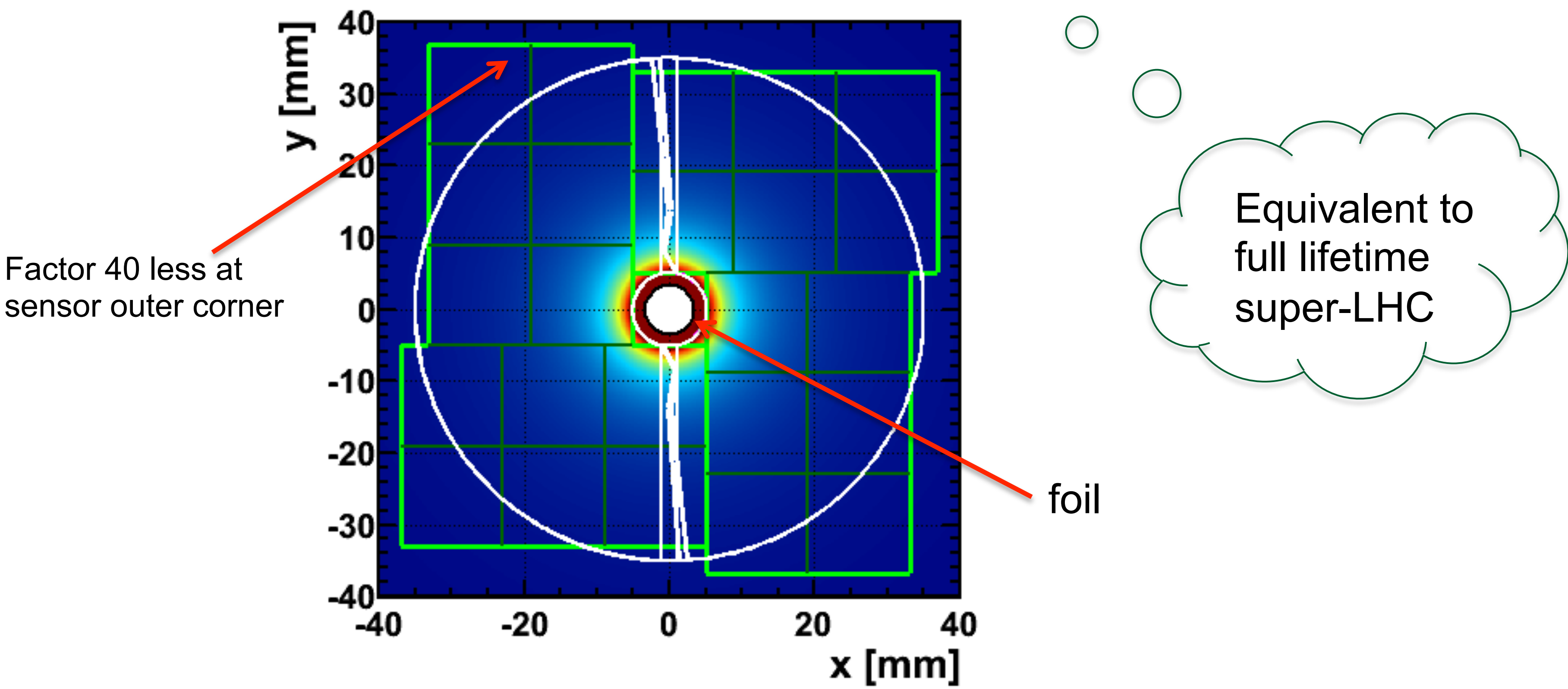
20-30% advantage for strips – for time dependent analyses
Translates (via dilution) to a ~15% statistical advantage
This must be weighed against the tracking efficiency

We note that other resolution dependent effects remain unquantified
Hence we cannot relax the pressure on material reduction in modules and foil

Radiation Damage

Common problem to either solution

Highly non-uniform radiation damage of up to 8 x 10^{15} n_{eq}/cm^2 for 50 fb^{-1}



Strip (white) and pixel (green) layouts superposed above anticipated flux (arbitary scale)

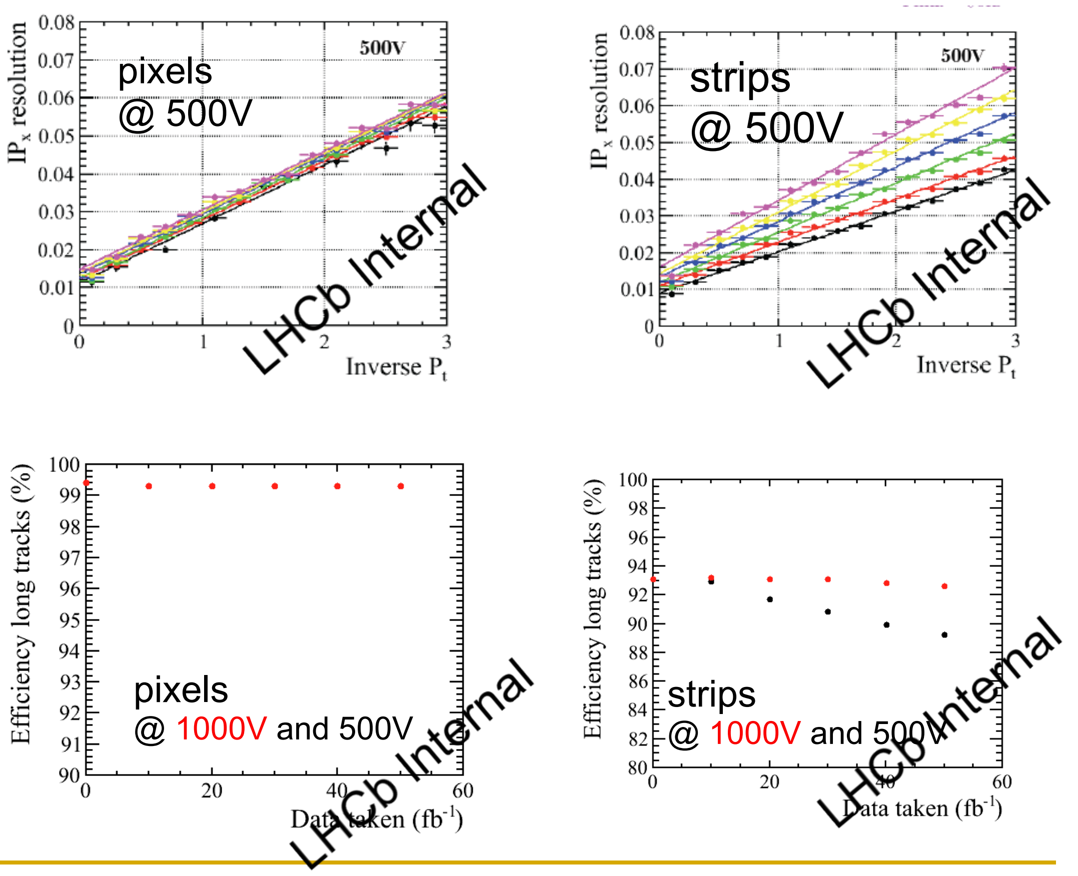
Radiation Damage

Assessed with a simple module of depth dependent charge collection
Model is pessimistic in some aspects, optimistic in others

At 1000V both solutions stable over full lifetime

At 500V changes seen for strip case

Difference driven by the S/N of each option



Referee Report – Key Points

- No real show stopper identified for any solution!
- Physics performance perceived to be rather equivalent -> Don't focus on it now, but optimise, optimise, optimise, once the choice is taken
- Sensor prototoyping and radiation hardness programme encouraged
- RF foil is critical in either option and further efforts to optimise and thin the design are encouraged with high priority
- Risk assessment for microchannel necessary
- ASIC development schedule highlighted as critical (incorporating possible second submission and serialiser MPW), detailed suggestions for design.
- Schedule is tight

VELO Group Leader meeting

Collaboration Endorsement

VELO Upgrade group recommendation:

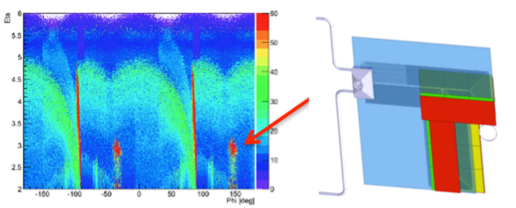
The collaboration adopts the pixel module with microchannel cooling as the baseline solution. This recommendation endorsed by all institutes.

Collaboration endorsement July 17th 2013.

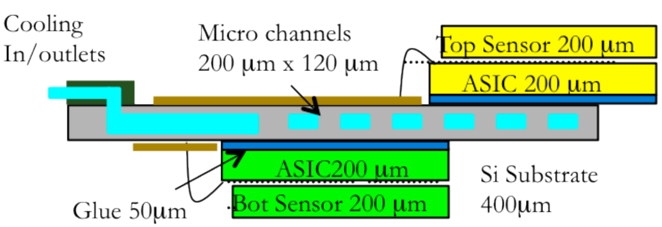
Recommendations of referees highlighted in following slides.

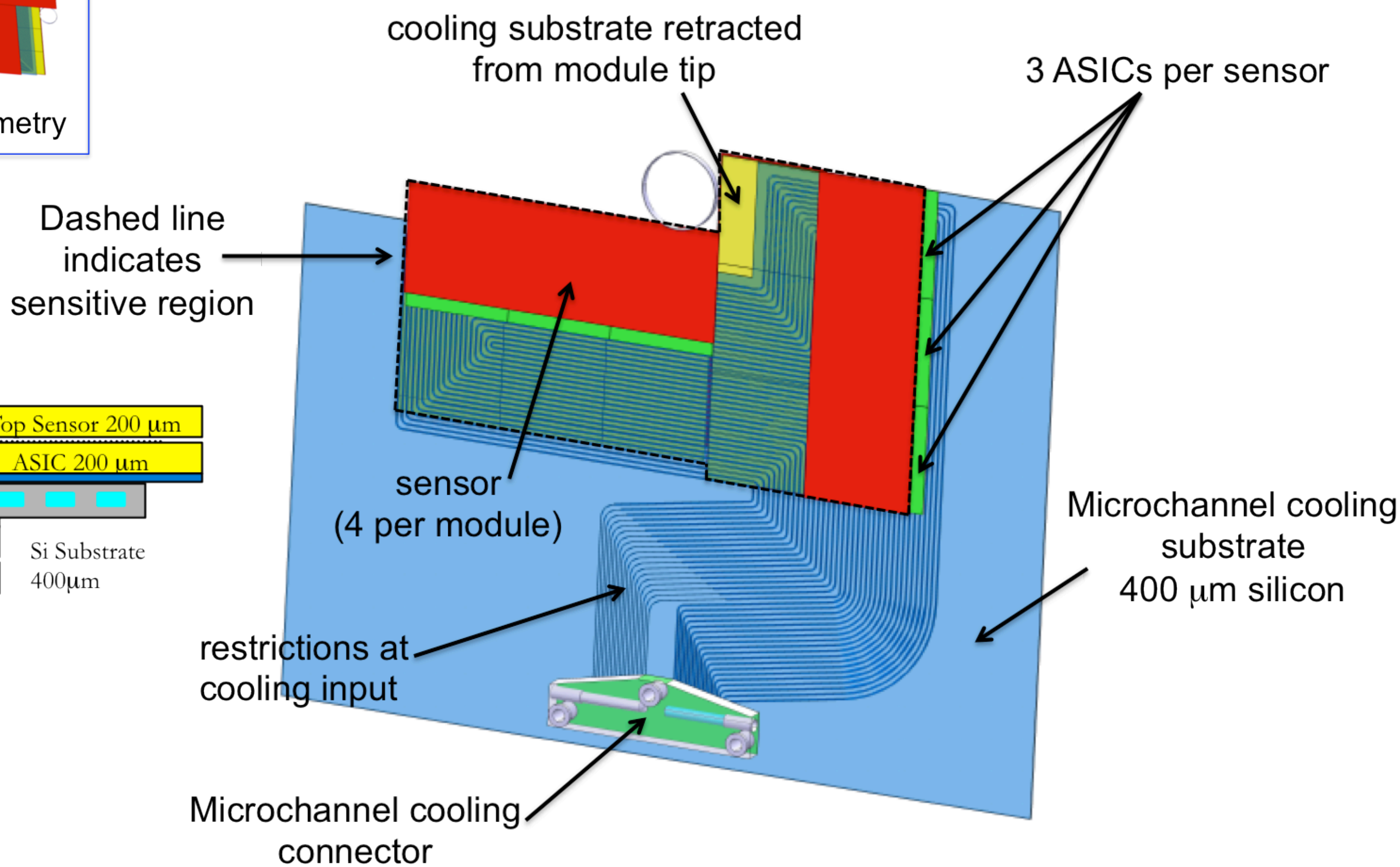
Highlights since VUTR

Pixel module layout and modifications



VUTR design: up down asymmetry

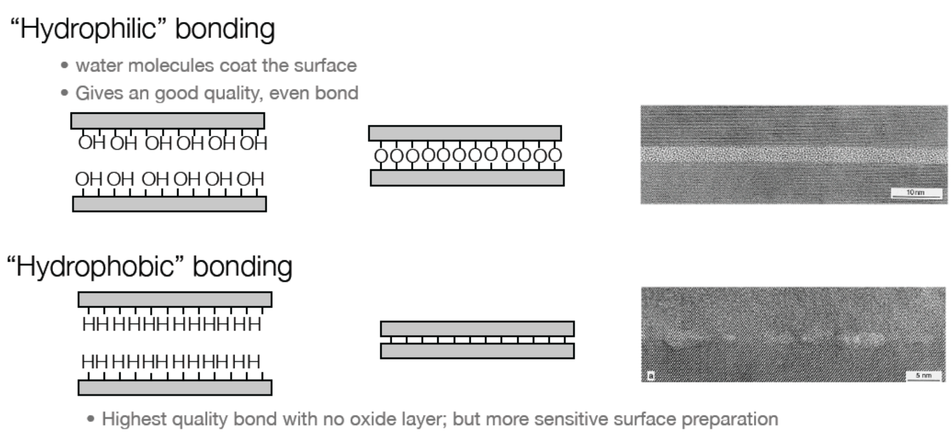




Microchannel cooling: Endurance

Expect operational pressures of ~15 Bar, and ~60 Bar at room temperature
Including safety limits, must withstand > 150 bar

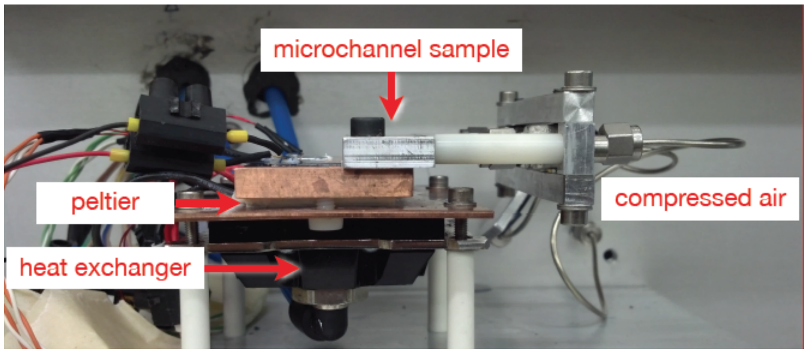
Possible to provoke breakage in early prototypes with large outlet manifolds
Hydrophillic and Hydrophobic bonded samples broke in different ways, with hydrophobic samples being much stronger



Hydrophillic breakage:
laterally across bond layer

Hydrophobic breakage:
within silicon crystal

Microchannel cooling: Endurance



Automated cyling of temperature and pressure to most extreme values and with numerous repetitions

Measurement complicated by moisture in dry air blocking channels

Measurement history

High Pressure (100-200 bars) and temperature cycles	• Partially/completely blocked at low temperatures (ice making)
Only high pressure cycles (room temperature)	• No problems!
Temperature and high pressure cycles with dry air	• occasional blockages at low temperatures (< 0˚C)
Temperature cycles at constant low pressure (3,12 bars)	• Sample got blocked while raising pressure at low temperature
Temperature and pressure cycles only when T>0˚C	• No problems so far (12 bars, next step: 70 bars)

Measurement summary

Hydrophobic samples do not break up to 700 bar

Most temperature cycles: 1184 @ 12 bar
-38˚C up to 42˚C (ΔT ~80˚C)

Most pressure cycles: 1000 @ 21˚C
ΔP ~ 143 bar

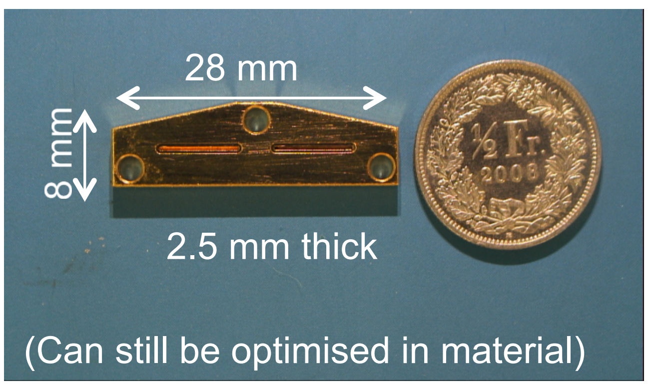
Next step: temperature cycles at high pressure

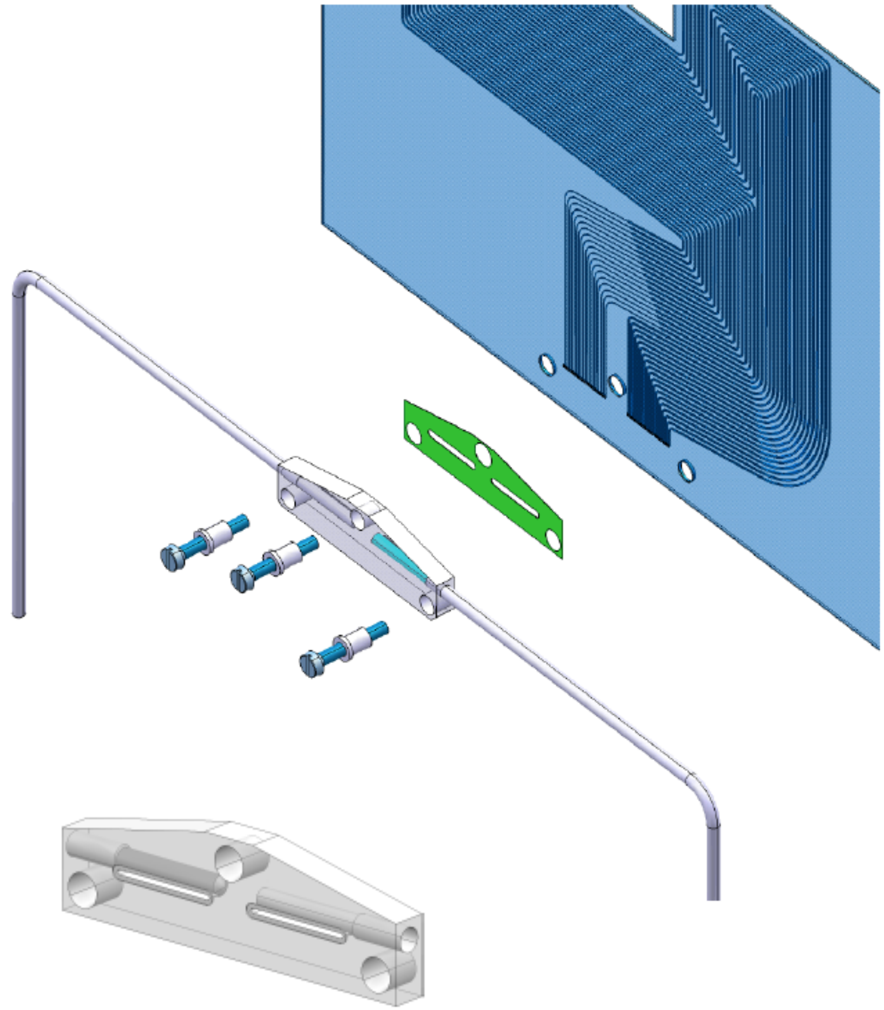
Microchannel cooling: Connectors

New fluidic connector design

500 um diameter inlet hole replaced by 7000 x 200 um long slid

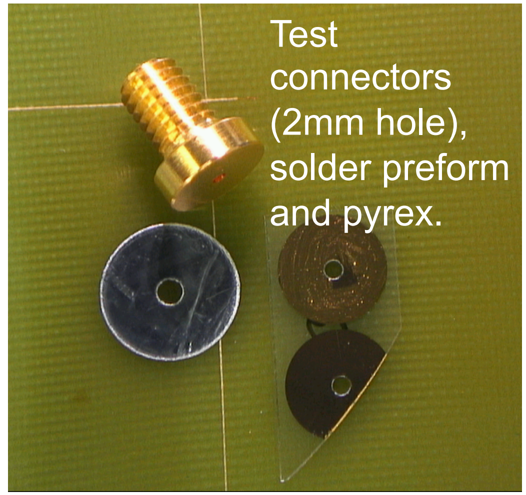
Less pressure drop
More pressure safety (smaller critical dimension)

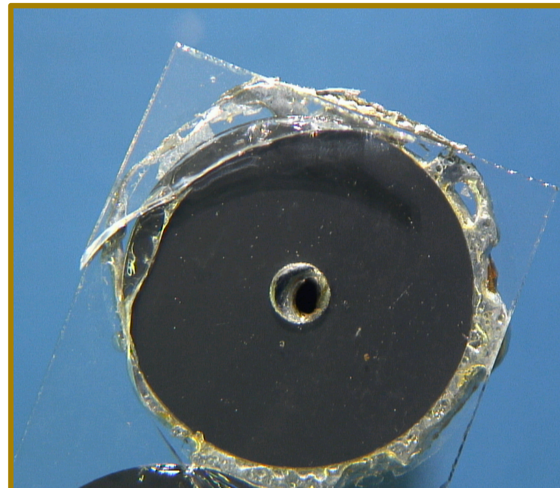




Microchannel cooling: Connector attachment

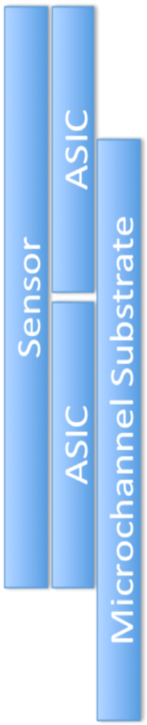
- Soldering trials done with test connectors and pyrex (500um).
- Solder test on new iron connector and Pyrex will be done this week.
- Later, Covar connectors will be soldered on Si samples.
- Then extensive stress testing (temperature & pressure cycling).
- Production of a full size microchannel layout in Si-Pyrex has started at EPFL.

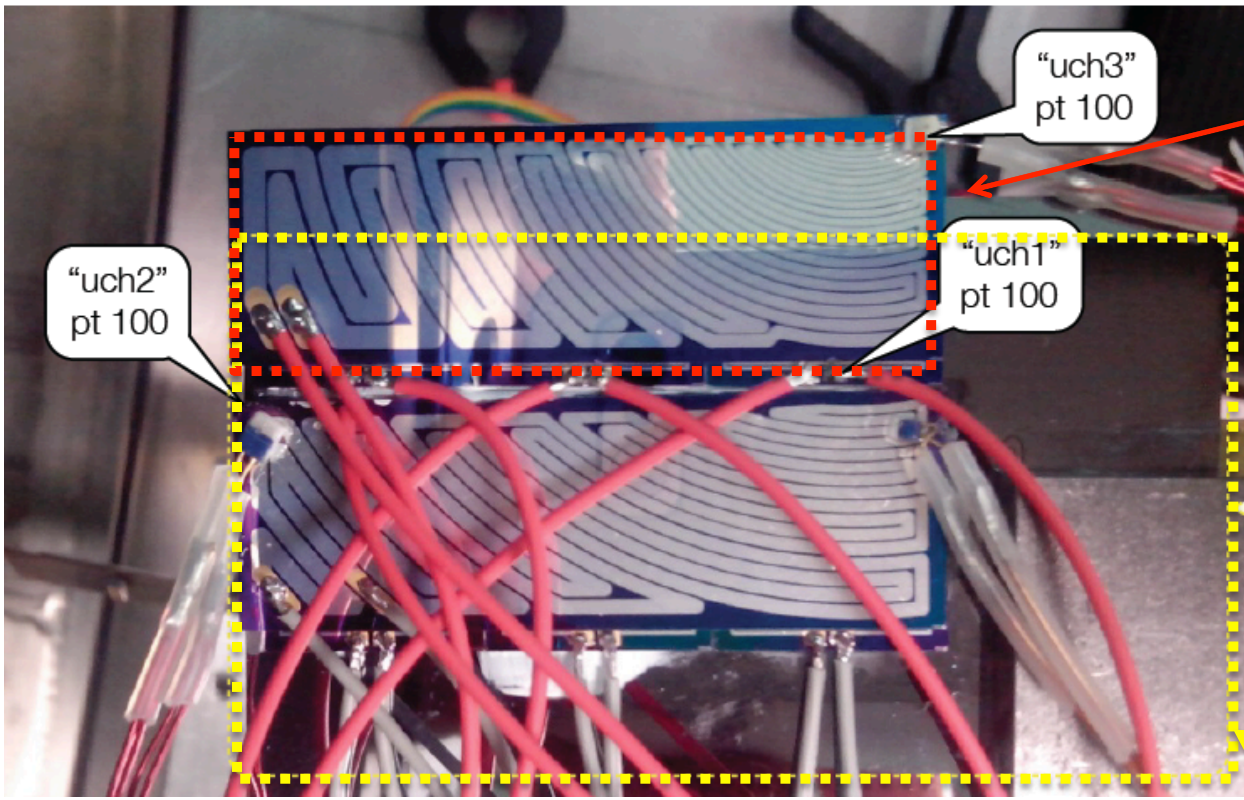


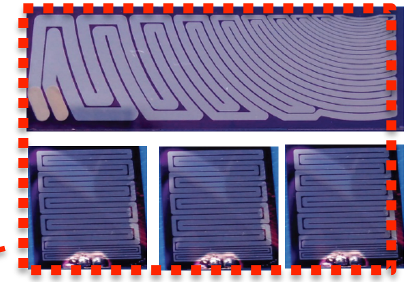


Test connectors soldered on pyrex. Allows to view how the solder has flowed.
(Pyrex has cracked along the periphery due to CTE mismatch. No delamination on solder joint!)

Microchannel cooling: Performance







Sensor +
3xASIC mockup

microchannel
substrate

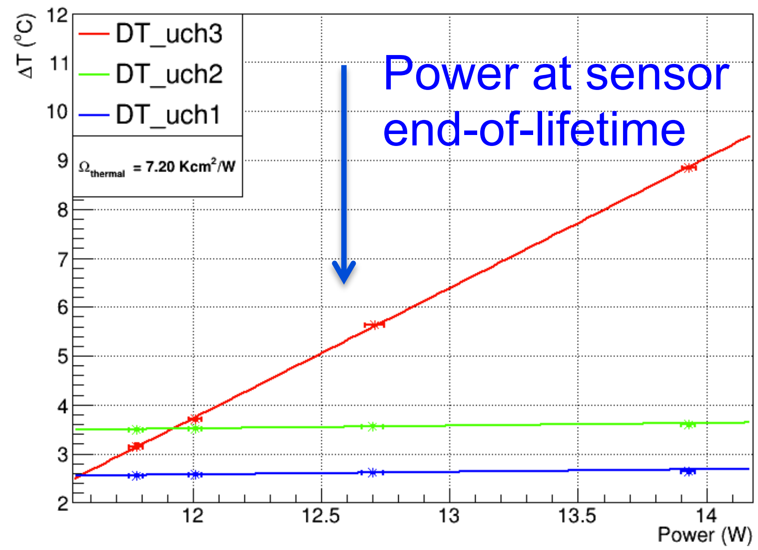
Microchannel cooling: Performance

Results of tests on ½ scale mockup

ASICS operated at full power

Sensor power gradually increased

Red curve: ΔT at sensor tip
(allowed $\Delta T < 15^{o}C$)

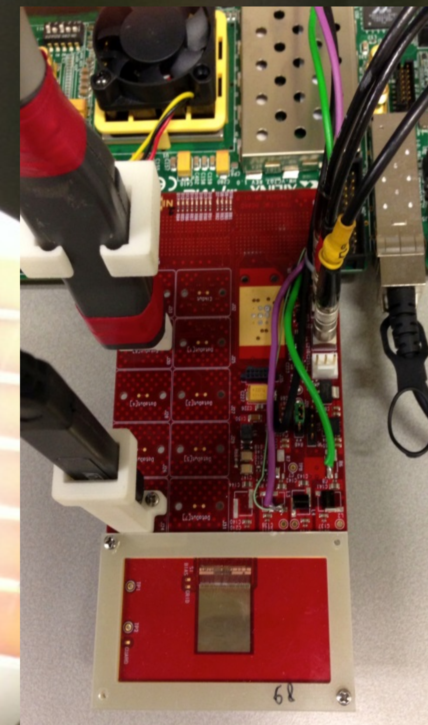


Based on this experience, the following changes made to the design:

- 200x120μm^2 channels (was 200x70μm^2) – reduce flow resistance
- 60x60μm^2 restrictions (was 30x70μm^2) – reduced risk of clogging
- 500 μm channel spacing (was 200μm) – reduced number of channels

Timepix3*

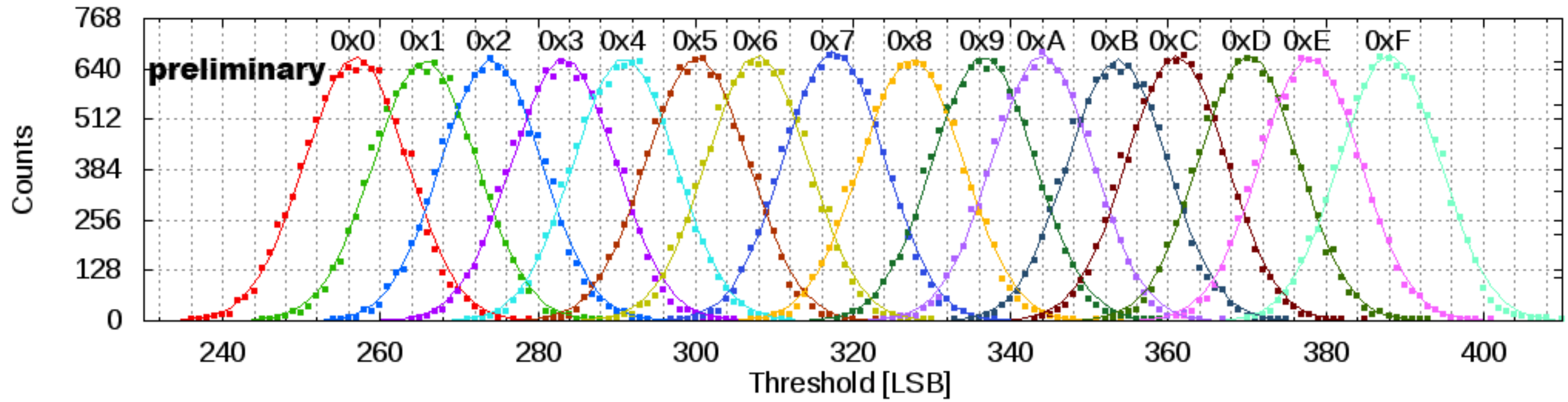
- 6 wafers received in August.
- 1 wafer diced.
- 2 ASICS under test at CERN and NIKHEF.
- Periphery and pixel matrix are fully functional. No problems detected so far.
- Serial output links running at 640 MHz
- Pixel noise is very low: ~65 e- (preliminary).
- Threshold mismatch after equalization is excellent: ~30e- (preliminary).
- Power consumption as expected 450mA (analog), 370mA (digital, 'no hits')

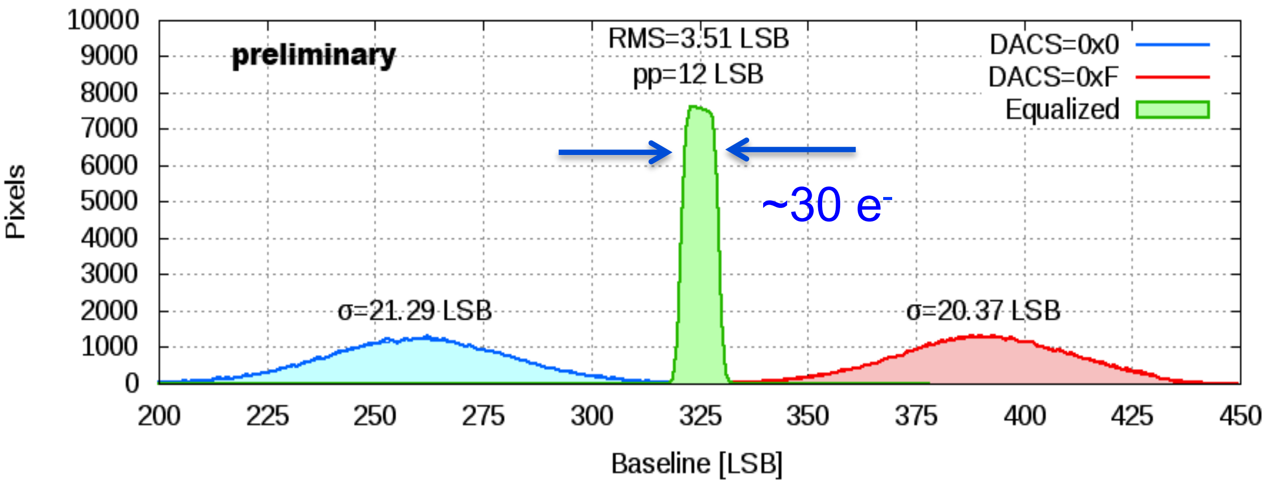


Timepix3 is a 'precursor' of Velopix.
Same design & test team and environment
VERY ENCOURAGING step towards VELOPIX

* Designed in the context of the Medipix3 Collaboration by CERN, NIKHEF, Univ. Bonn

Timepix3 - Highlights



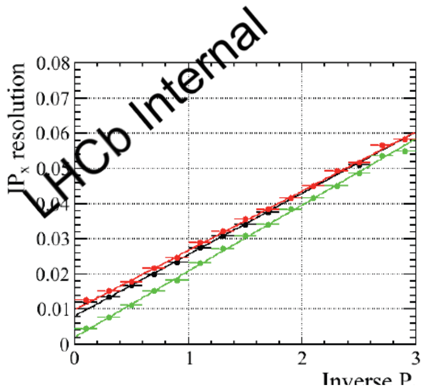


- Equalisation fully functional
- gain to be confirmed
- Calibration DAC: excellent linearity
- More results to come!
  - TWEPP, IEEE-NSS

S. Kulis, CERN-LCD

Binary versus ToT read-out

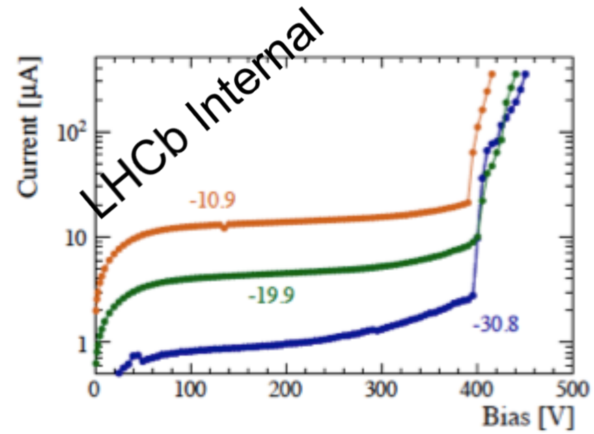
- Binary read-out has advantages over ToT for the chip design
  - 2x4 super-pixels are preferred
    - ToT very tight fit
  - Binary simplifies logic in ASIC (and TELL40)
    - fixed packet length format
    - Also reduced data size
    - Allows faster discharge of front-end, reducing dead-time
- ToT advantages
    - Better resolution (marginally)
    - Front-end characterisation
    - Avoids threshold scans
    - In particular during beam time
    - Extra physics information; converted γ, dE/dx…
- Decision end of this week



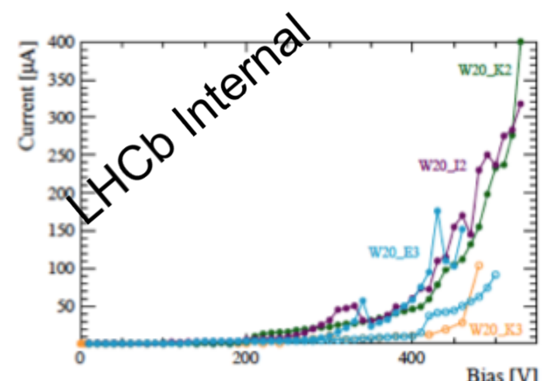
Black: 4bit ToT
Red: Binary
Green: "Perfect resolution

Sensor & bump-bonding prototyping

- August Workshop to plan the prototyping & testing
  - TimePix(3), sensors, bump-bonding
- Main issues concerning the sensors
  - HV tolerance (guard ring design)
  - Thickness (bump-bonding yield)
- Reduce phase-space in prototyping
  - 200 µm thickness (both for sensor & ASIC)
  - 450 µm guard ring + conservative option
  - n or p type: discuss with vendors
- Test programme
  - Irradiations (3 fluences)
  - Lab tests (I/V, source, …)
  - Beam test (DESY Feb. 2014, TimePix3)



Post irradiation IV curves of 100 um n-in-p VTT edgeless Medipix assemblies



pre-irradiation IV curves Micron assemblies with and without paralyne coating

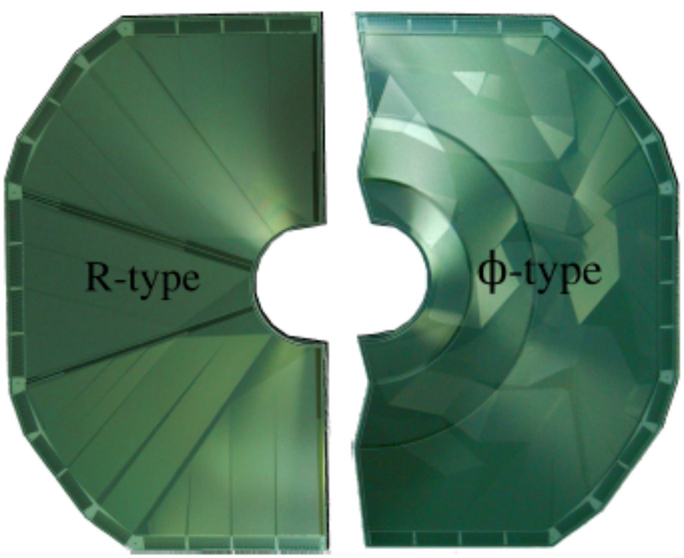
Swan song from strip sensor R&D

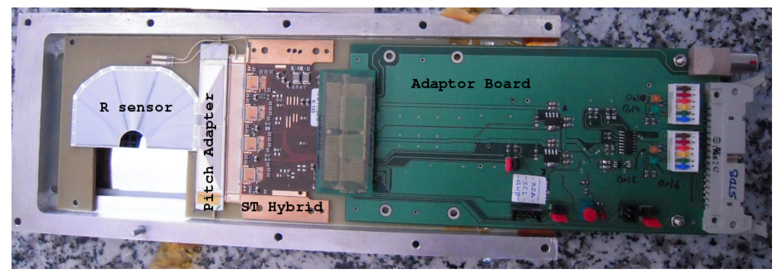
Full scale (non-compact) HPK prototypes produced **and assembled into module**

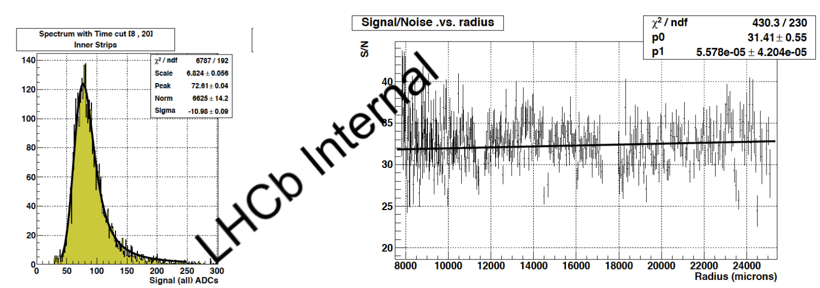
- Full metrology and electrical characterisation satisfactory
- Excellent S/N at all radii
- Referees encouraged completion and documentation

of a large body of work

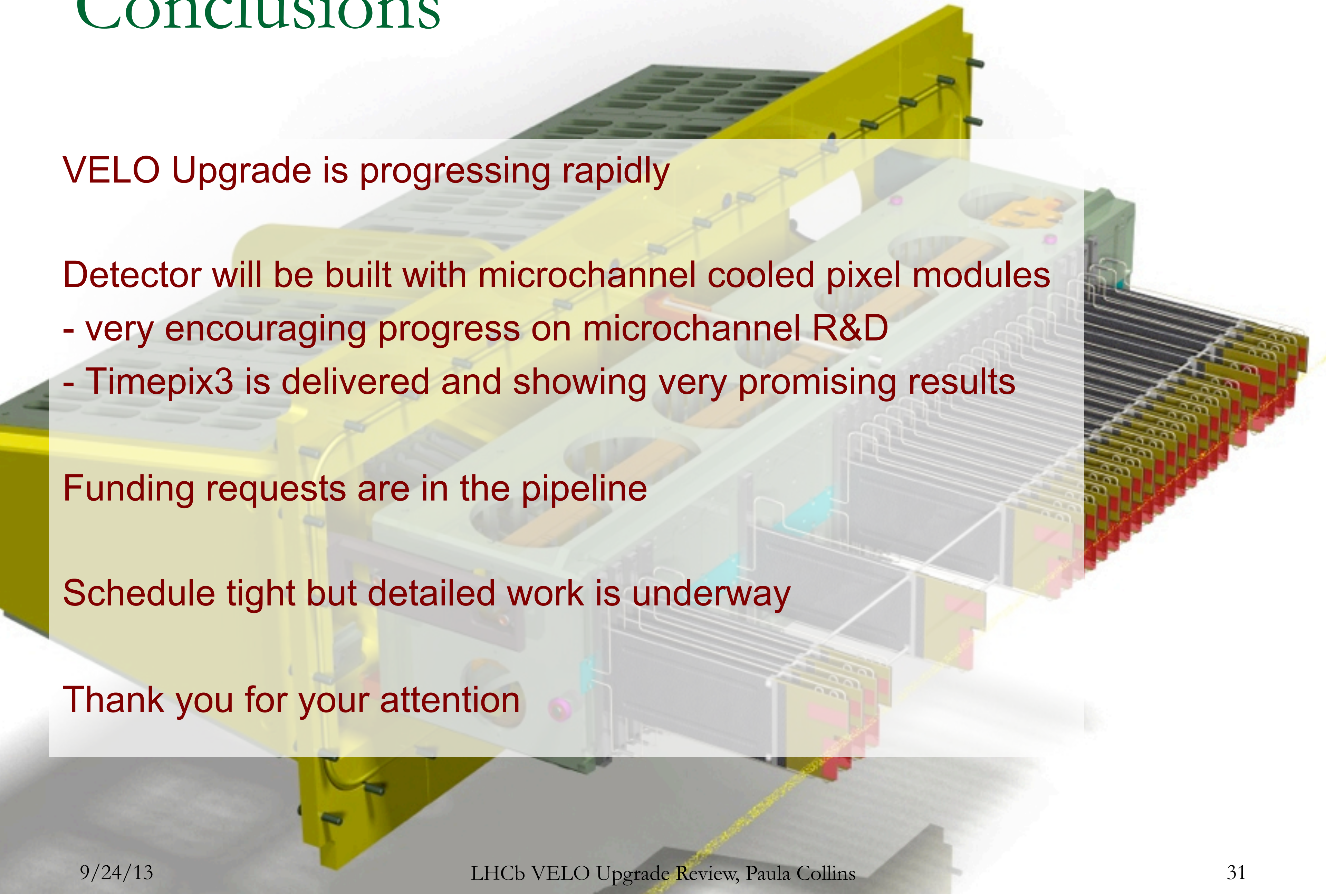
Some caveats on HV, but 800V achieved







Conclusions



VELO Upgrade is progressing rapidly

Detector will be built with microchannel cooled pixel modules
- very encouraging progress on microchannel R&D
- Timepix3 is delivered and showing very promising results

Funding requests are in the pipeline

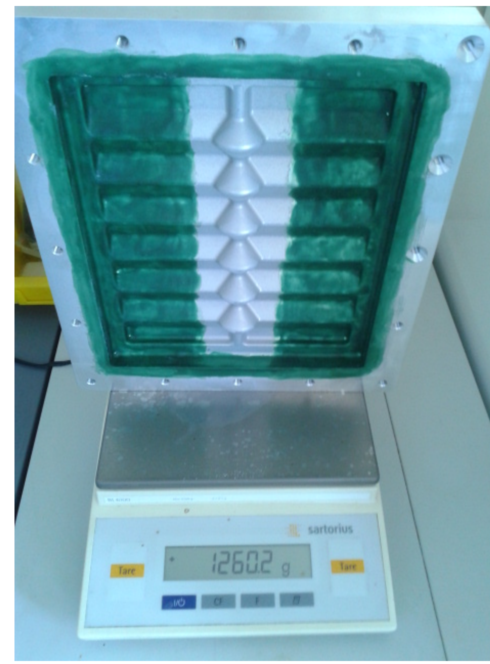
Schedule tight but detailed work is underway

Thank you for your attention

Backup slides

Thinning of the RF foil

- Aim: develop a method to thin down RF foil
    - machining unlikely to reach 100 um
- Use chemical etching (NaOH)
- Four prototype foil samples produced
- Procedure:
    - metrology (thickness map)
    - vacuum leak test
    - etch
    - vacuum leak test
    - metrology (confirm thickness control)
- First tests promising
    - first results before end Sep



thanks to: EN-MME and TS VSC colleagues for support in this R&D

VL vs VP (microchannel) – common understanding

Tracking efficiency – Advantage pixels! (by 4-5%)

IP resolution – Advantage strips! (slender advantage)

Ghosts – not an important factor from HLT viewpoint

Timing – Advantage pixels! (but not so dramatic)

Radiation Damage – Advantage pixels!

Systematic uncertainties - let

RF box - let

Risk (sensors) – Advantage pixels!

Risk (modules) – level (experience is with strips)

Risk (ASICs) – No showstopper! (not assessed for strips)

Game, Set and Match…?