EUDRB activities and plans

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The EUDET Data Reduction Board (EUDRB)

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Abstract

The EUDET Data Reduction board was developed at INFN-Ferrara in collaboration with University of Insubria-Como and INFN-Roma 3 to read out Monolithic Active Pixel Sensors (MAPS). The motherboard ("EUDRB_MoBo") is a VME64x slave in 6U Eurocard format. The motherboard supports one "analog" ("EUDRB_DCA") and one "digital" ("EUDRB_DCD") daughter cards with PCI Mezzanine Card (PMC) format. The EUDRB_DCD provides detector timing signals and it is also provides the EUDRB with a USB2.0 port for diagnostic and stand-alone data acquisition. The EUDRB-DCA has 4 single-ended/differential analog inputs and it is based on the design developed by IPHC (Institut Pluridisciplinaire Hubert-Curien) and the SUCIMA collaboration. The EUDRB has been so far employed with the IPHC MIMOSA-5, MIMOSTAR 2 and MIMOTel devices.

Progress on the VME side

- Writing thresholds/pedestal in SRAM with VME Single Cycle Transfers (SCT) was definitely slow (minutes for MimoTel)
  - problem traced down to the VME library which still included more system calls than strictly necessary, to provide the flexibility and diagnostics needed in the development phase
  - Lorenzo prepared a new library which allows to go down a couple of orders of magnitudes in the execution time of a SCT
  - We feel it is no longer mandatory to modify the EUDRB's VME interface to support MBLT write cycles, as it was proposed to speed up the thresold/pedestal upgrading

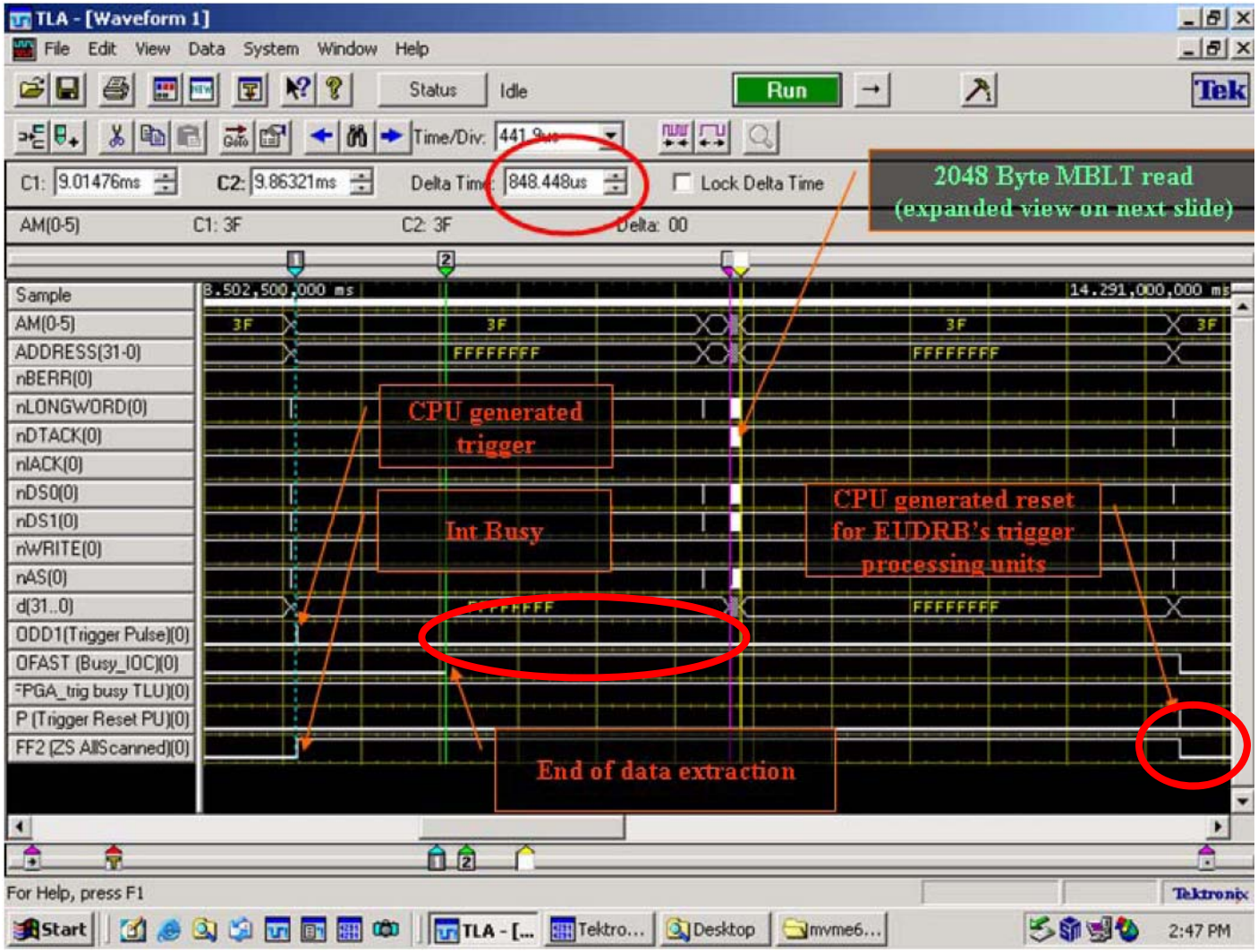
- Managing slave-terminated blocks is now possible, due to a modification in the driver
  - Lorenzo has modified the driver and tested slave-terminated transfers in 2eVME and 2eSST successfully on a commercial board (CAEN V1290A): a slave-terminated block read does not cause anymore the flushing of all data buffered in the VME-PCIx bridge. To be tested on the EUDRB as soon as the 2eSST transfer mode is implemented

VME: future plans

1) MBLT→2eSST (from present ~42MB/s peak to at least 160MB/s peak)
   - It needs only modification of the VHDL code of VME interface
2) Multi-event mode
   - Implement at least one buffering level:
     - this would allow to clear the “busy” signal (which blocks the TLU) as soon as an event is written in the output FIFO.
     - readout of one event can go in parallel with processing the next one
   - It implies rewriting the VHDL code of VME interface and any modules involved in trigger processing

- Of course, one step at a time (likely: 1 before 2)

The previous steps should minimize deadtimes…



Interfacing Mimosa 18

- No major redesign implied
- Daughter cards are OK
- Update software/firmware only
- Should be done by April 1st (no kidding)

What next?

- Readout the binary sensors!
- The issue is understanding whether upgrading the EUDRB (hw and sw) to comply with the M22 will bring any advantage towards the M22+
- We believe the design baseline should be driven by the final chip and regard compliance with M22 as an (interesting) option
- A technical discussion on the specifications of M22+ / SuZe01 is needed, including milestones
- Shall we read also anything analog from M22+ ?
- The following slides show the current EUDRB layout and might be useful for the discussion

DIGITAL DAUGHTER CARD connector pinout
DIMENSIONS 75 x 130 mm

ALTERNATE PINOUT OF CONNECTOR D_J1 (RJ-45)
FOR MIMOSTAR / MIMOSA 5

RJ-45 conductor no.	Signal Name	Type	Standard
1	MSTAR_TCK / MKOFF1	O/O	3.3V TTL
2	GND		
3	MSTAR_TMS / MKOFF2	O/O	3.3V TTL
4	MSTAR_TDI / OFAST	O/O	3.3V TTL
5	GND		
6	MSTAR_TDO / OSHUT	I/O	3.3V TTL
7	GND		
8	MSTART_Ntrst / CDS_TP	O/O	3.3V TTL

ALTERNATE PINOUT OF CONNECTOR D_J2 (RJ-45)
FOR MIMOSTAR / MIMOSA 5

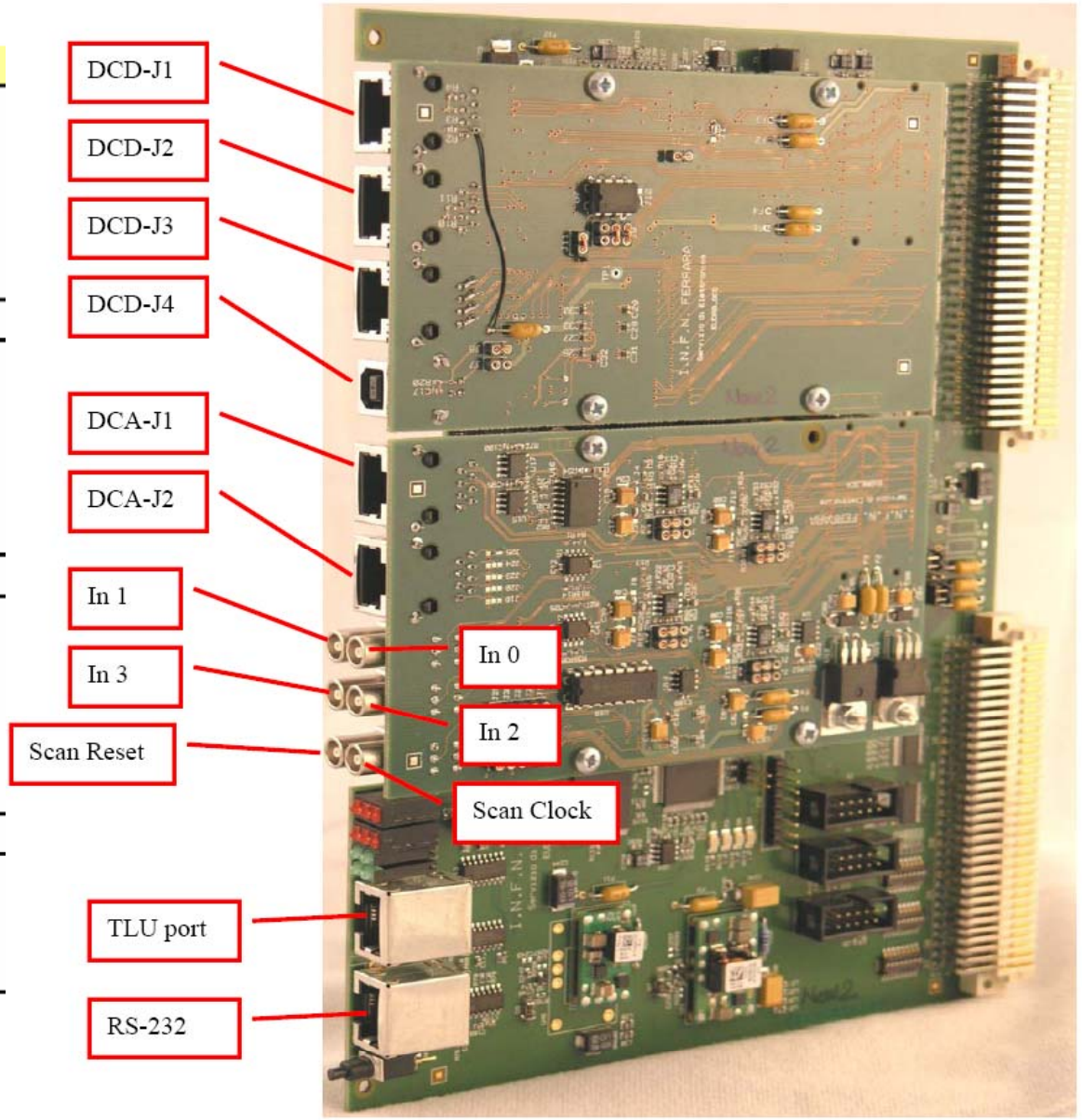
RJ-45 conductor no.	Signal Name	Type	Standard
1	MSTAR_CLKRDn / M5_CLKRDn	O/O	LVDS
2	MSTAR_CLKRDp / M5_CLKRDp	O/O	LVDS
3	GND		
4	GND		
5	MSTAR_CLK10Xp / ----------	O/O	LVDS
6	MSTAR_CLK10Xn / ----------	O/O	LVDS
7	MSTAR_SYNCp / M5_nRSTp	O/O	LVDS
8	MSTAR_SYNCn / M5_nRSTn	O/O	LVDS

ALTERNATE PINOUT OF CONNECTOR D_J3 (RJ-45)
FOR MIMOSTAR / MIMOSA 5 / MIMO-ROMA

RJ-45 conductor no.	Signal Name	Type	Standard
1	LVDSOUT4n / LVDSOUT4n / MR_CLKOUTn	I / I	LVDS
2	LVDSOUT4p / LVDSOUT4p / MR_CLKOUTp	I / I	LVDS
3	LVDSOUT3n / LVDSOUT3n / ----------	I / I	LVDS
4	LVDSOUT3p / LVDSOUT3p / ----------	I / I	LVDS
5	LVDSOUT2n / LVDSOUT2n / ----------	I / I	LVDS
6	LVDSOUT2p / LVDSOUT2p / ----------	I / I	LVDS
7	LVDSOUT1n / LVDSOUT1n / MR_SOF_OUTn	I / I	LVDS
8	LVDSOUT1p / LVDSOUT1p / MR_SOF_OUTp	I / I	LVDS

PINOUT OF CONNECTOR D_J4 (USB-B)
FOR MIMOSTAR / MIMOSA 5 / MIMO-ROMA

USB-B conductor no.	Signal Name	Type	Standard
1	+ 5V		power
2	- DATA		USB
3	+ DATA		USB
4	GND		power



ANALOG DAUGHTER CARD connector pinout
DIMENSIONS 75 x 130 mm

PINOUT OF CONNECTOR A_J1 (RJ-45)

RJ-45 con	Signal Name	Type	Standard
1	ASG3p	In	analog
2	ASGL3n	In	analog
3	ASGL1p	In	analog
4	ASGL1n	In	analog
5	ASGL2p	In	analog
6	ASGL2n	In	analog
7	ASGL0p	In	analog
8	ASGL0n	In	analog

PINOUT OF CONNECTOR A_J2 (RJ-45)

RJ-45 con	Signal Name (normal/alternate) (*)	Type	Standard
	(*) Alternate pin functions to drive the MIMOSA V with analog board alone		
1	DAC_OUT1 / MKOFF1	Out /Out	analog/LVTTL
2	GND		
3	DAC_OUT2 / MKOFF2	Out /Out	analog/LVTTL
4	GND / OFAST	Pwr /Out	power/LVTTL
5	DAC_OUT3 / OSHUT	Out /Out	analog/LVTTL
6	GND		
7	DAC_OUT4 / CDS_TP	Out /Out	analog/LVTTL
8	GND		

PINOUT OF CONNECTOR A_J3 (LEMO)

LEMOcon	Signal Name	Type	Standard
1	ASGL0p	In	analog
2	GND		

PINOUT OF CONNECTOR A_J4 (LEMO)

LEMOcon	Signal Name	Type	Standard
1	ASGL1p	In	analog
2	GND		

PINOUT OF CONNECTOR A_J5 (LEMO)

LEMOcon	Signal Name	Type	Standard
1	ASGL2p	In	analog
2	GND		

PINOUT OF CONNECTOR A_J6 (LEMO)

LEMOcon	Signal Name	Type	Standard
1	ASGL3p	In	analog
2	GND		

PINOUT OF CONNECTOR A_J7 (LEMO)

LEMOcon	Signal Name	Type	Standard
1	External Pixel Scan Clock (MIMO-ROMA)	In	analog
2	GND		

PINOUT OF CONNECTOR A_J8 (LEMO)

LEMOcon	Signal Name	Type	Standard
1	External "Start Of Frame" (MIMO-ROMA)	In	analog
2	GND