

Plans for TLU v0.2

Summary:

- TLU v0.1 used (more or less) “for real” in test beams during summer 2007
- Extremely useful feedback received (many thanks)
- Design work under-way for TLU v0.2
 - Suggestions and/or comments welcome.

Existing (Hardware) Interface

- TLU v0.1 interfaces:
 - Six “RJ45” connectors with LVDS trig/busy/reset/clock signals
 - Two sets of LVTTTL trig/busy/reset signals on LEMO.
 - Lemo/RJ45 selected by soldering links on motherboard.

TLU v0.2 DUT Interfaces

- TLU v0.2
 - RJ45 connectors unchanged.
 - Add four “HDMI” connectors (to allow connection to Calice clock-and-control unit)
 - Four sets of LEMO trigger/busy/reset signals. Two sets with LVTTTL output levels. Two sets with NIM output levels. Inputs can be switched between 50-ohm and high-impedance. Threshold software controllable (10-bit bipolar DAC).
 - Total number of DUT interfaces remains unchanged at six, but can be switched between LVDS, HDMI and LEMO under s/ware control

TLU v0.2 “user interface”

- TLU v0.1 has six LEDs. Not adequate for “stand-alone” operation.
- TLU v0.2 will use I2C “bus extender” to allow:
 - two LEDs per socket to indicate status.
 - Input switches
- Probably a 40x2 LCD display.
- FPGA unit will need upgrade to allow stand-alone operation.