irfu

saclay

Status of Mimosa 22

Eudet JRA-1 meeting

30 January 2008

Fabrice Guilloux

on behalf of ***IRFU – Saclay*** *(ex DAPNIA - Saclay) and* ***IPHC - Strasbourg***

OUTLINE

- From Mimosa-16 to Mimosa-22
- Mimosa 22 design sum up
- Planning toward the final sensor
- Summary

From Mimosa-16 to Mimosa-22

irfu

cea

saclay

Mimosa-16.1 & 16.2 : design features

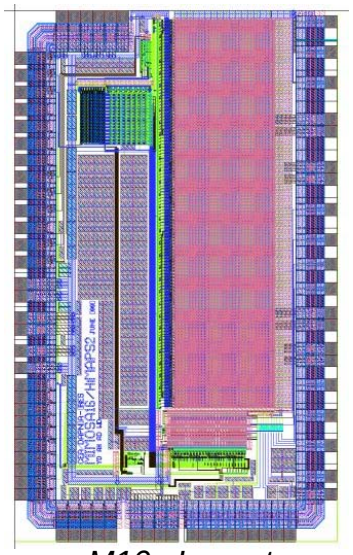
- AMS-OPTO 0.35*µm*
  - M16.1 : Epitaxial layer 14*µm* (~ 11*µm*)
  - M16.2 : Epitaxial layer 20*µm* (~ 16*µm*)
- Pixel pitch (25µm)² 32 col. x 128 lines
- 4 sub-arrays
  - S1 : Diode 1.7x1.7 *µm²*
  - S2 : Diode 2.4x2.4 *µm²*
  - S3 : S2 with ionizing radiation tolerant pixels
  - S4 : Diode 4.5x4.5 *µm²* (Selfbias, Gain enhanced) [1]

  } Mimosa-8 ref.
- 8 Analog Outputs + 24 end-column discri.
- Characterization tests (same setup than M8)
  - Analog outputs : performed at Saclay in Nov. 06 for M16.2 and in March 07 for M16.1

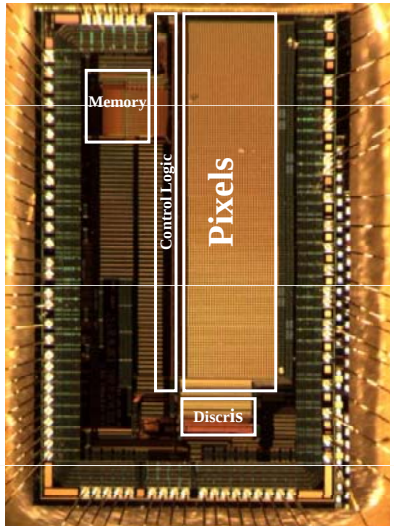
➔ Pixel noise is independent of r.o. *Freq* up to 150MHz

➔ From CCE : Optimum diode size should be around 4x4 *µm² (S4 : CCE ~ 66 %)*

[1] A. Dorokhov *et al.*, "NMOS-based high gain amplifier for MAPS", Talk given at *5th Int. Meeting on Front-End Electronics (FEE)*, 17-20 May 2006, Perugia, Italy.



M16 : Layout



M16 : Photography

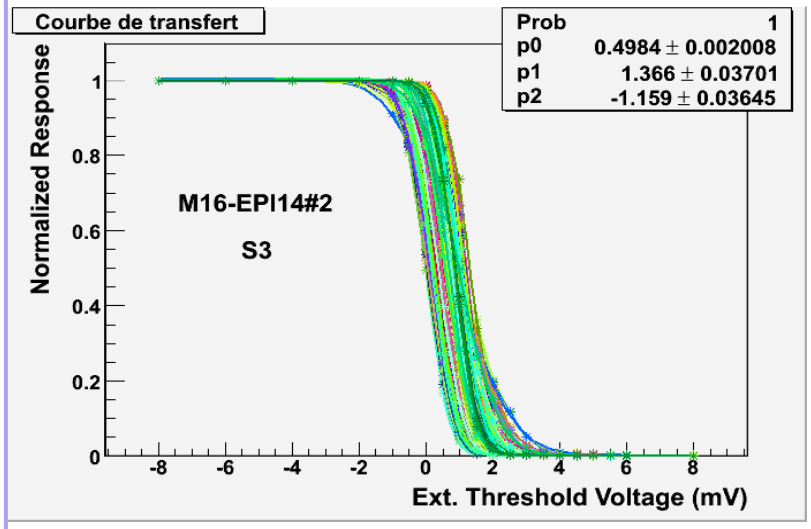
irfu

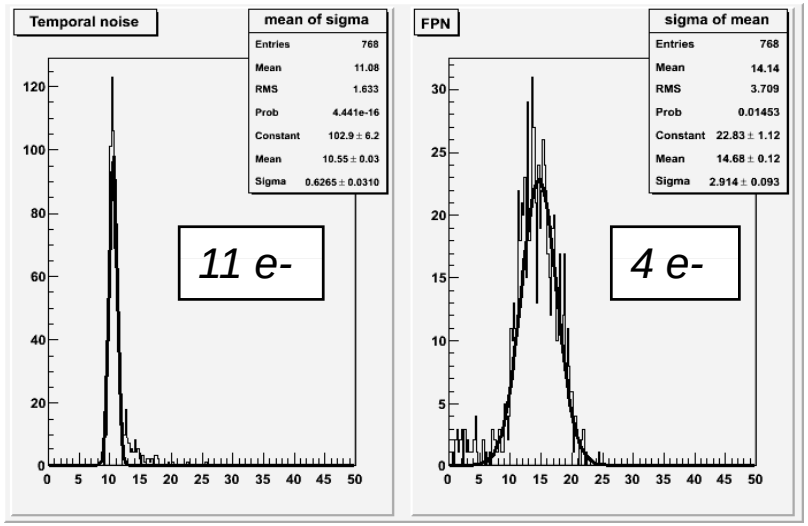
cea

saclay

Mimosa-16.1 & 16.2 : Test Results

- Digital Outputs : performed at Strasbourg in July 07
  - *Extraction of FPN and Temporal noise @ Fck = 40 MHz for the complete readout chain*





S3, Fck = 40MHz	**Analogue (e-)**	**Digital (e-)**
Fixed Pattern Noise	*3*	*4*
Temporal Noise	*12*	*11*

➔ FPN noise and Temporal noise are closed to those found from analog outputs

➔ Temporal noise is dominated by pixel noise (as expected)

From Mimosa-16 to Mimosa-22

irfu
cea
saclay

Mimosa-16.1 & 16.2 : Test Results

- Beam Tests
  - Analog & Digital Outputs : performed at CERN in Sept. 07
    - *Preliminary results were available before M22 submission !*

  Cf. ***A. Besson****, Testbeam Results Mimosa16 and Mimosa18, JRA-1 Hamburg*

➔ Higher in-pixel amplifier gain, better performances

Conclusions of M16 test campaign: All parameters are almost « green »
noise performances , digital conversion , fake hits rate, detection efficiency, Hits multiplicity …excepted for CCE parameter which must be improved for next design (but at least one sub-array matches requirements)

Mimosa 16.3 : Mimosa 16 pixel optimization

New submission

- Same parameters than M16.1 (➔ Epi. 14µm)
- Sub-arrays :
  - S1 : Diode 3.5x3.5 μm^2
  - S2 : Diode 2.4x2.4 μm^2
  - S3 : Diode 3.0x3.0 μm^2
  - S4 : Diode 4.5x4.5 μm^2 (Selfbias, Gain enhanced amplifier + internal buffer)

Ref. pixels ← S2

S1, S2, S3 → Increase of diodes sizes

From Mimosa-16 to Mimosa-22

irfu
cea
saclay

Mimosa-16.3 vs 16.1 (Saclay August 07)

CHIP Nb and type	Subarray	CVF (µV/e-)	Temporal Noise (e-)	FPN (e-)	CCE (%) (for 9 pixels)
M16.1-EPI14 chip#3	**S1** (1.7µm)²	64.0	10	3	**7 %**
	S2 (2.4µm)²	59.2	11	2	**34 %**
	S3 (2.4µm)² rad-tol	54.0	12	3	**35 %**
	S4 (4.5µm)²	58.0	14	3	**66 %**
M16.3-EPI14 chip#15	**S1** (3.0µm)²	44.8	14	2	**24.8%**
	S2 (2.4µm)²	57.0	11	2	**12.7%**
	S3 (3.5µm)²	39.0	16	2	**29.1%**
	S4 (4.5 µm)²	39.6	22	3	No cluster pic (biasing pb ?)

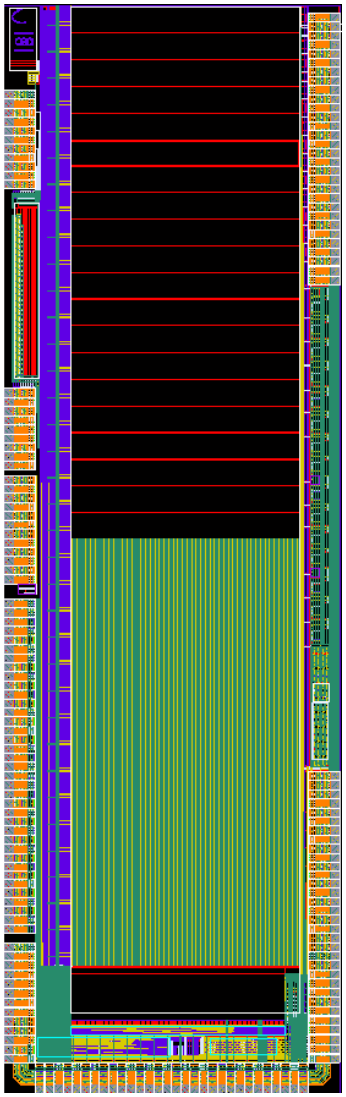
- Sub-array S2 are identical ➔ about third of the charges collected by M16.3vsM16.1 !?
  Explanation : the chips delivered come from an Hi-Res wafer (no Epi !!!)
  - *CMP apologized for the mistake ➔ Good chips were send at the beginning of January*
  - *Tests of M16.3 EPI should start at the beginning of February*

Mimosa - 22

irfu
cea
saclay

Main parameters & Functionalities

	Mach final ?
AMS-OPTO 0.35*µm*	☑
Pixel Size 18.4 x 18.4 µm²	☑
136 x 576 pixels [Final : ~ 1088x576]	☒
8 Analog Outputs	//
128 end-column discriminators	//
Slow Control Interface : JTAG	☑
Internal Bias (DAC)	☑
New r.o. protocol *Cf. **M. Goffe,** Mimosa 22 testing preparation*	☑
Not in the Chip : Zeros Suppress *Cf **W. Dulinski**, First Results on SUZE01*	☒



M22 : Layout

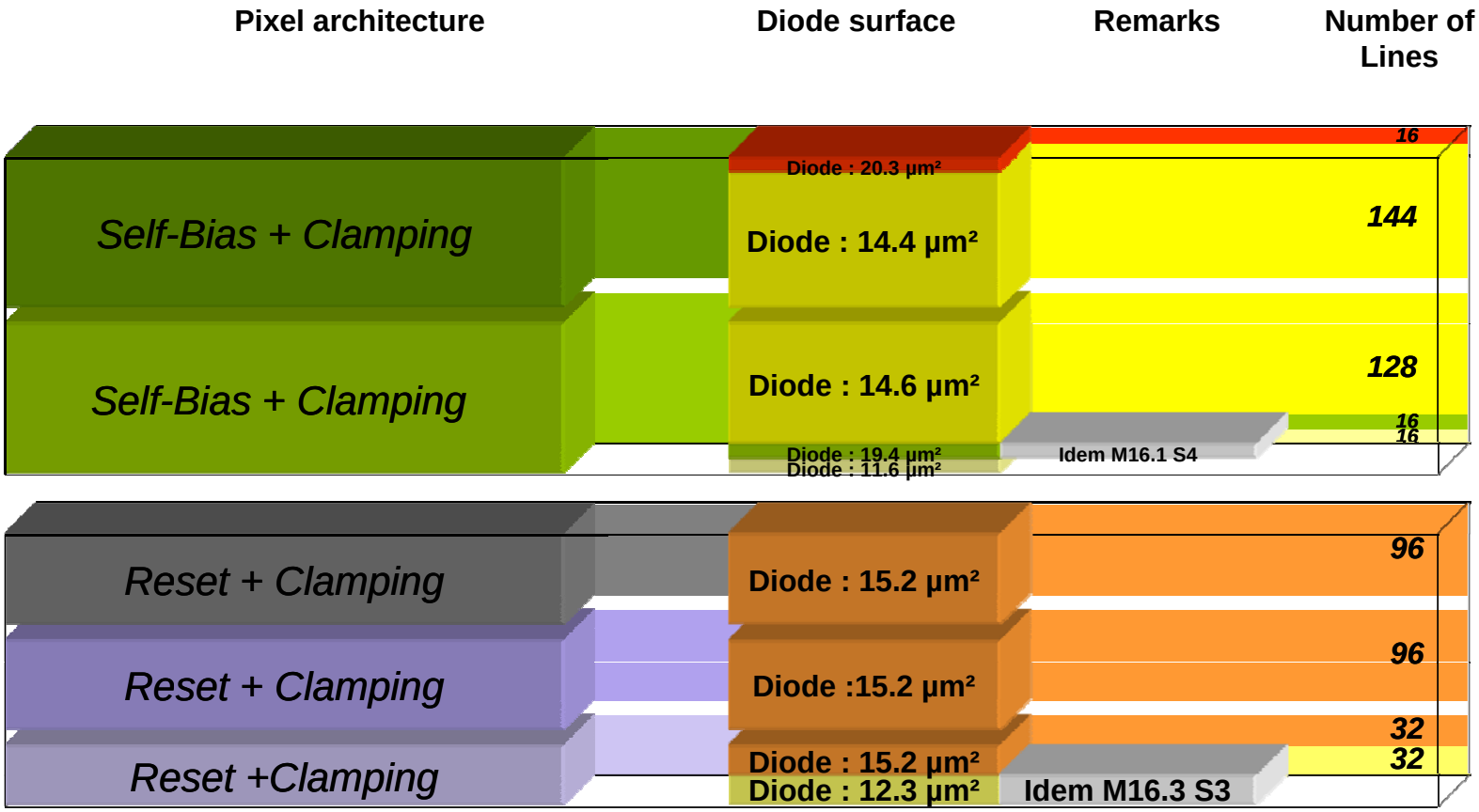
- Submission done the 26th October 2007
- Back from foundry since 9th January 2008

irfu

cea

saclay

Matrix : 9 Sub-arrays with different diode surfaces



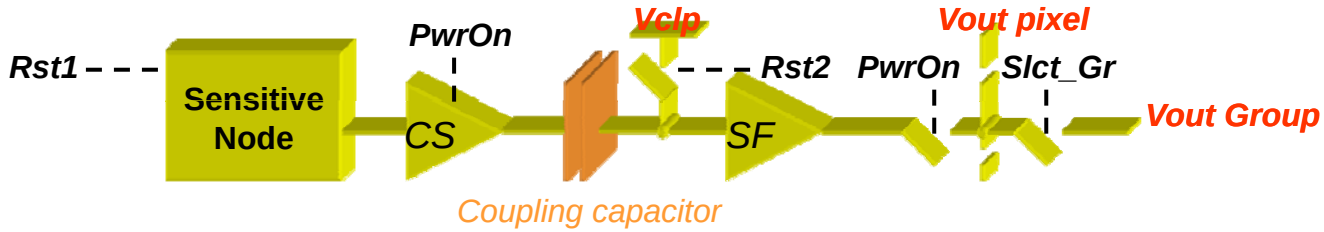
irfu
cea
saclay

Pixels characteristics

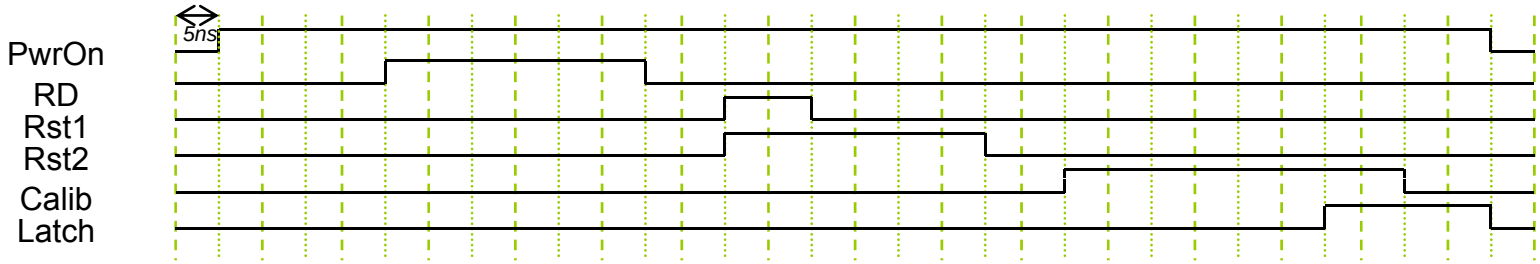
- **Finding the optimum :**
  - Amplifier Gain
  - Sensitive Diode biasing schemes and size: Reset or Selfbias

  } The best S/N ratio

- **In a M16-like pixel structure :**
  - In-pixel Amplifier (CS or HG), Correlated Double Sampling and Source Follower



  - Common digital commands chronogram ➔ 16 clock cycles / line for signal conversion



- **M22 optimization :**
  - Double selection switches (lines and group of 16 lines) to reduce line capa.
  - Double metals strategy to reduce line res.
  - "Stronger" Digital Buffers

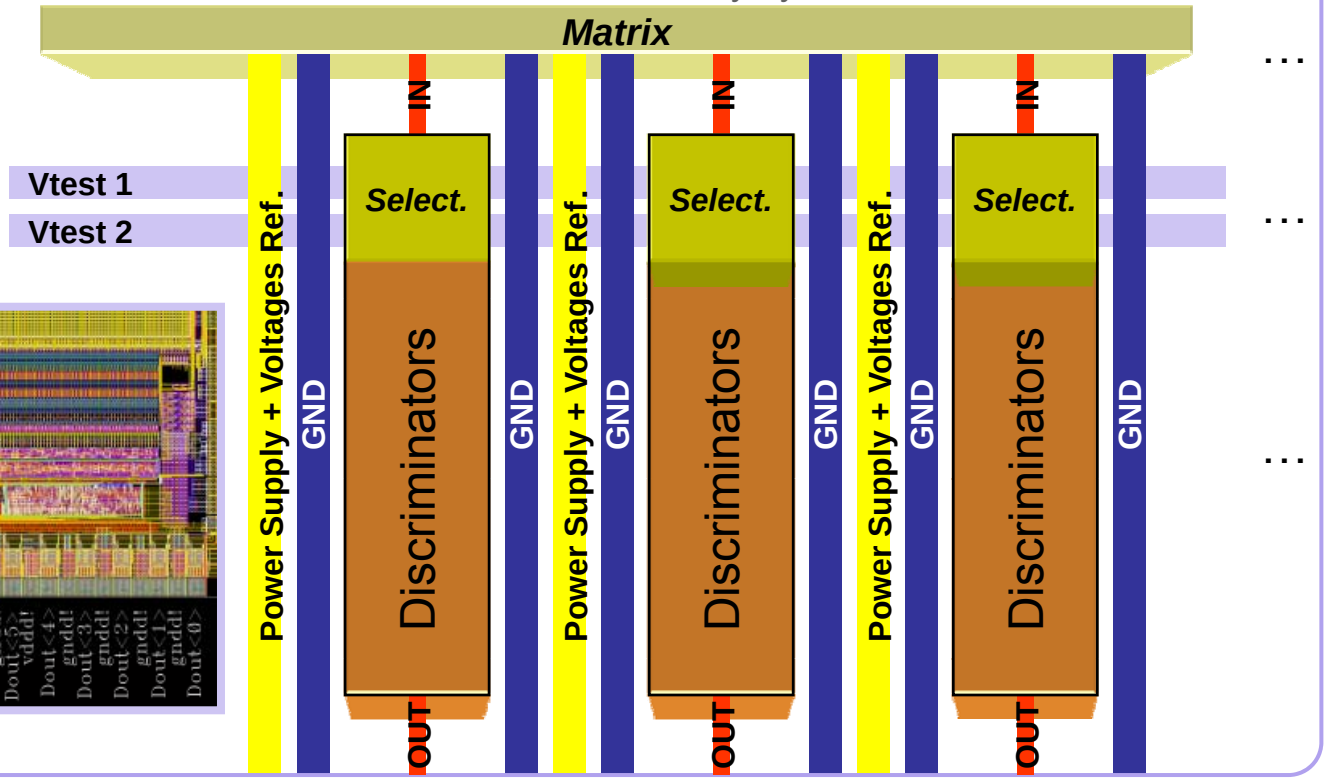
irfu

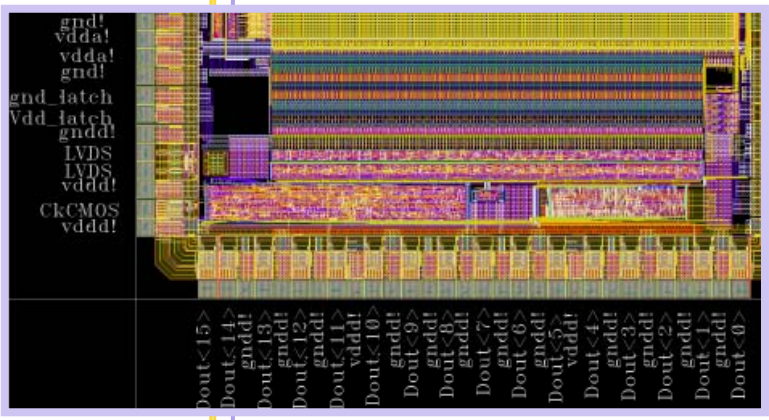
cea

saclay

Discriminators

- M16 : *25 x 300 µm²* ➔ M22 *14.6 x 435 µm²* : adaptation to pitch size (18.4 µm) + symmetrical layout to feed the matrix
- Tests features :
  - 2 lines simulate pixels levels
  - Discriminator latch could be disabled individually by slow control





irfu

cea

saclay

Digital functions : Nominal F_{ck} = 100MHz

- JTAG Controller + Registers
- Matrix Sequencer and multiplexer
- Digital outputs multiplexer
  128 ➔ 16 bits @ 50MHz
- Read out Controller

+

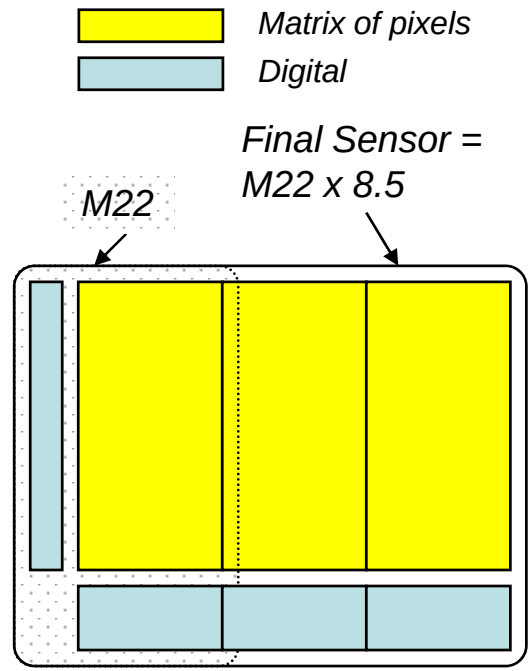
- Discriminators

=

➔ Digital (& matrix of pixels) layout is optimized for repetitions along the horizontal axis

Digital Bottom : 2 500 x 1 065 µm²
Total Area :2 500 x10 600 µm²

Digital Left : 335 x10 600 µm²
➔ Digital ~ 20 % of total area



Voltage References & Internal DAC

- 15 DACs programmable through Slow Control
- Critical voltage references could be supply by external circuits
- Specific analog buffers

Planning & Summary

irfu

cea

saclay

Tests schedule :

- First data taking in lab. : At the beginning of march
- Beam Tests : Q3 2008

Summary

- M22 fulfils is objectives in term of :
  - Architecture : The couple “Pixel” + “Discriminator” has already proven its reliability in AMS 0.35µm technology to reach the Eudet requirements.
  - Functions included : all the analog parts and the ¾ of the digital parts are embedded, with careful “scalable” design technique.
  - Layout : The chip is ready for an “horizontal stretch”
- M22 should answer to the questions :
  - Do all the functions work correctly together ?
  - Does the “scalable” design affect performances ?
- Next step to the final sensor
  - Full size analog & digital optimizations ➔ mainly due to long (~ 2cm) wires
  - Implementation of Zeros Supress