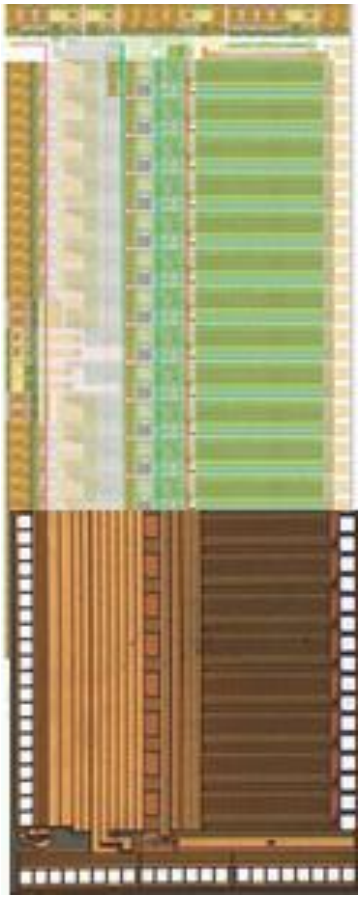
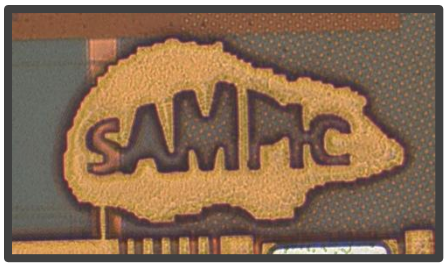
Last updates about the SAMPIC0 chip



H. Grabas

E. Delagnes



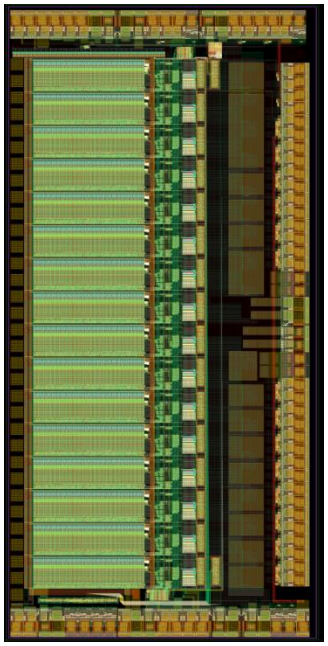
1 CEA/IRFU/SEDI Saclay
Collaboration with D. Breton + J Maalmi
CNRS/IN2P3/LAL Orsay

This work has been funded by the P2IO LabEx (ANR-10-LABX-0038) in the framework « Investissements d'Avenir » (ANR-11-IDEX-0003-01) managed by the French National Research Agency (ANR).

SAMPIC0: a Waveform based TDC chip

SAMPIC0 : a 16 channel WTDC

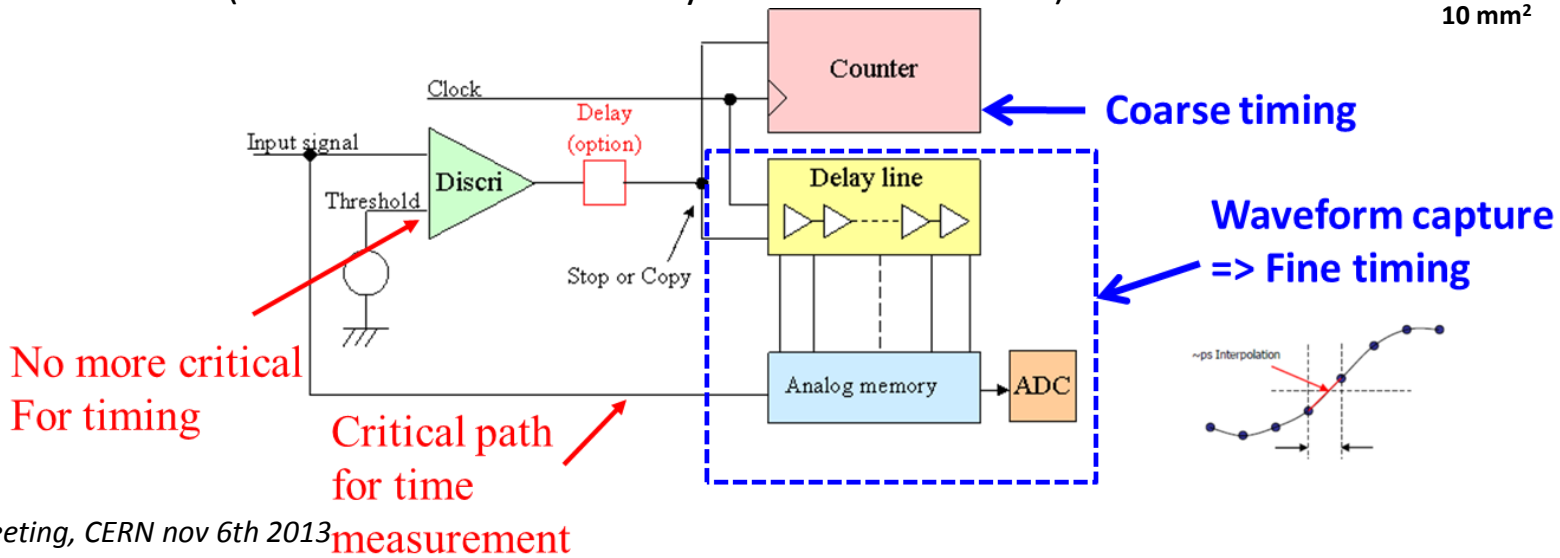
- proof of concept chip **already usable with detectors**
- Test of CMOS **AMS0.18µm** (**low cost**, low leakage, 1.8V technology)
- Compatible with buffered architecture (deatime free) => future chips



AMS CMOS 0.18µm
10 mm²

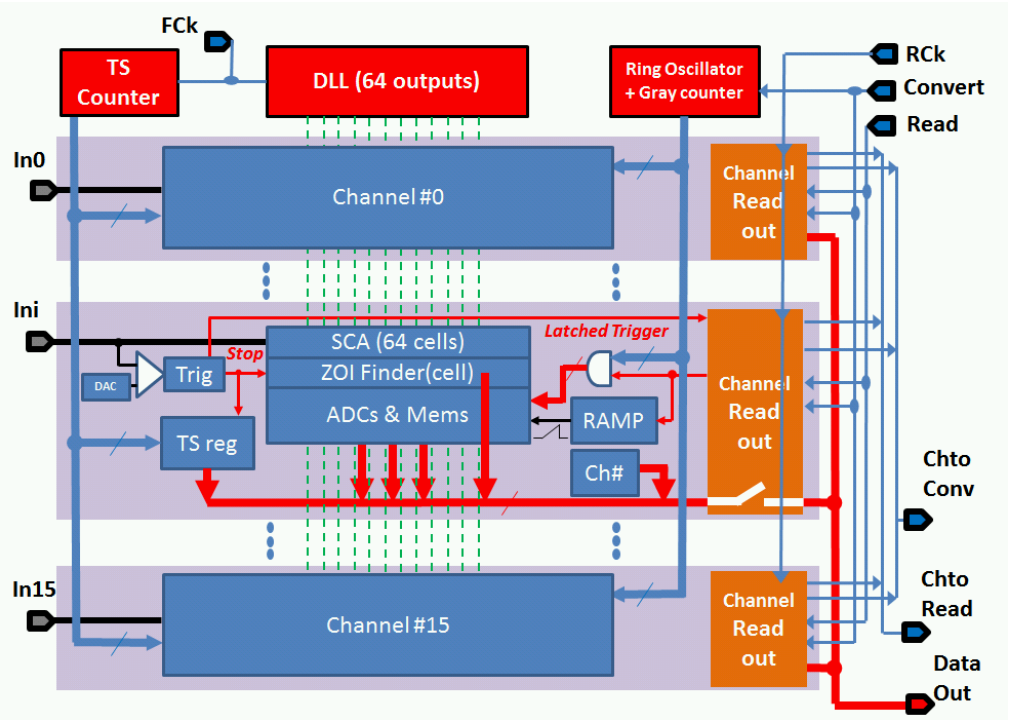
Each channel Self-Triggerable to catch parameters of fast pulses:

- **Timing :**
  - Coarse = timestamp counter
  - Middle = DLL based TDC *also defining a Zone of Interest for sampling*
  - Fine = few samples in the ZOI of the sampled waveform
- **Waveform Shape, Charge, Amplitude** available through samples
- **No need for high-end discriminator** => low power, versatility
- **Short SCA** (to accommodate the delay of the discriminator)



SAMPIC0: a 16-channel WTDC

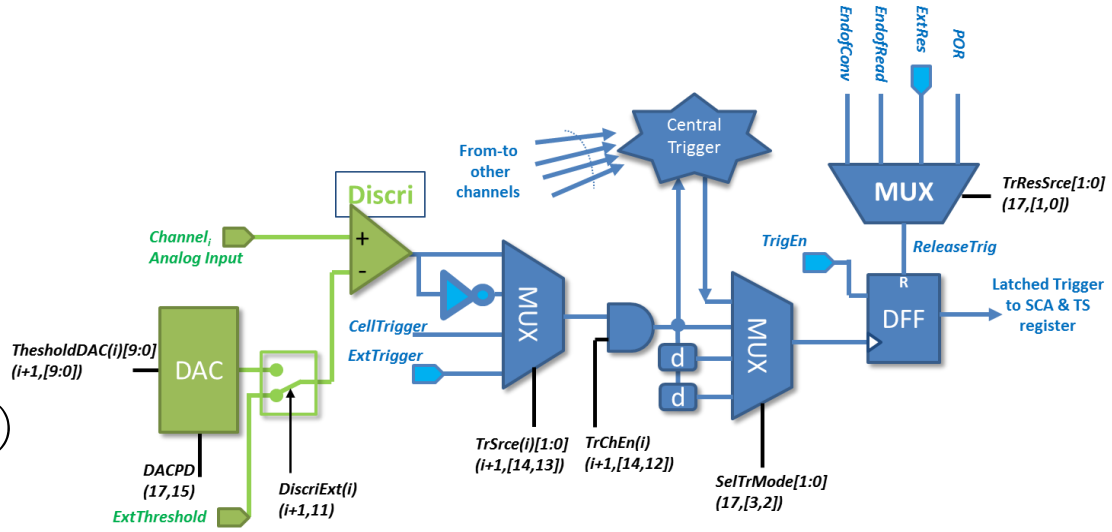
- Common “Slow” (160MHz) 12-bit Gray Counter = **Coarse Timestamping/ch**
- **Common Timing generator**: servo-controlled DLL: (1-10 GHz) used for **middle precision timing** & analog sampling commands
- 16 (short) SCA self-triggerable channels:
  - No analog input buffer
  - 64 cells, ~ 50fF capacitor
  - 1.5 GHz Bandwidth
- Several modes of triggering: discri on threshold (+/-), External, Or…
- On-chip fast Wilkinson digitization :
  - 1.3 GHz common gray counter.
  - tunable ramp slope=> trade-off conversion time/precision 1.6µs/11bit to 200ns/8bit
  - Simultaneous conversion of all the SCA cells of the triggered channels



- **Deadtime** = only for triggered channels waiting or in conversion ***=> independent DEADTIME*** (can be common if required)
- Region of Interest Readout
- Read-Out through a 12 bit/160 MHz (up to 400) LVDS bus: negligible readout deadtime
- SPI for configuration (Trigger modes, discriminator thresholds (1/ch),…)

Chip Triggering

- 1 discriminator/ channel
- 10 bit DAC/ch for trigger
- A lot of trigger modes programmable for each channel:
  - External
  - Edge selection
  - Enable/disable
  - Internal/external threshold
  - Postrig
  - "CENTRAL" trigger (= OR)

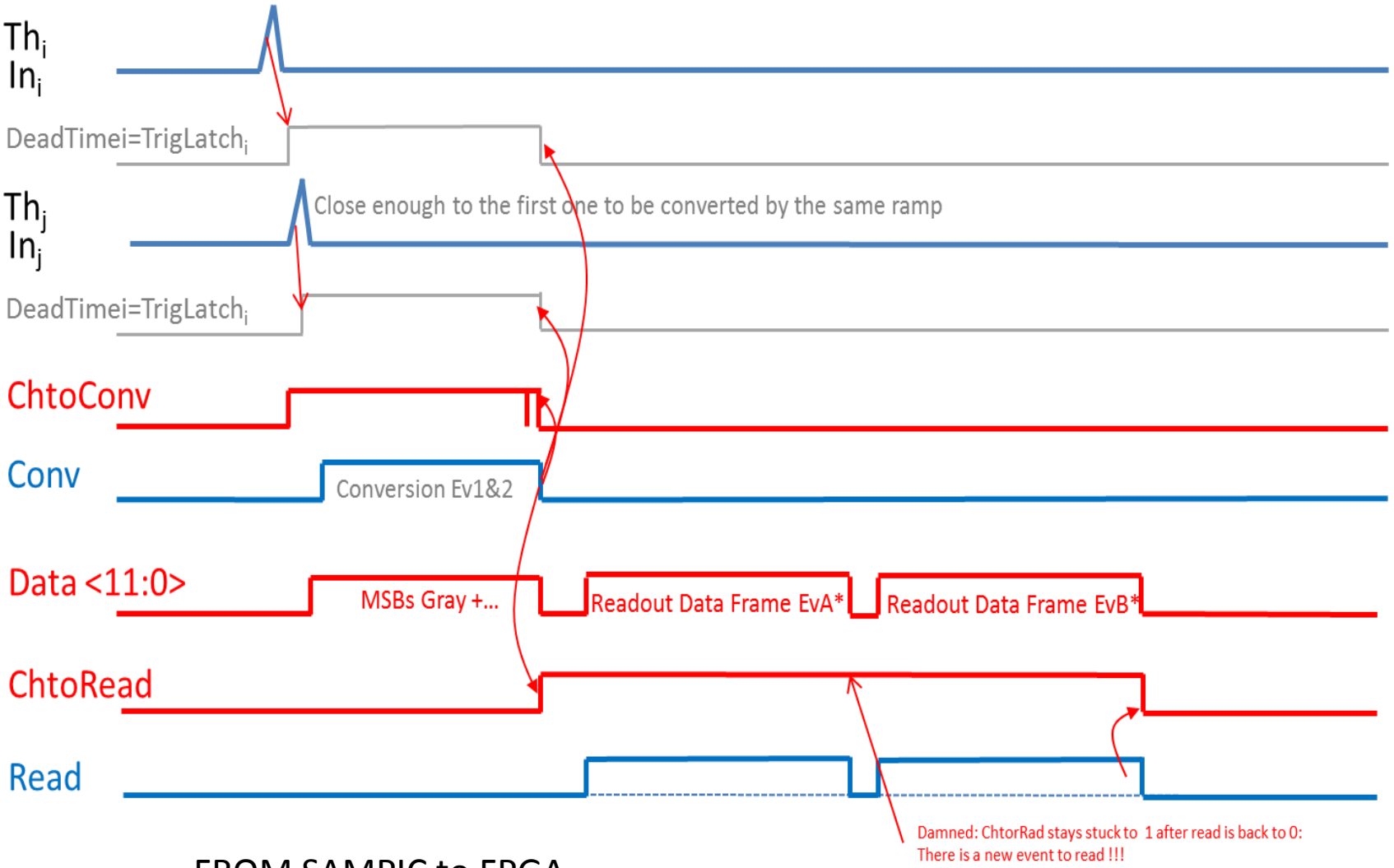


- Stops the sampling in the SCA and catch the Timestamp
- Rise the "ChtoConv" signal for the user

Readout

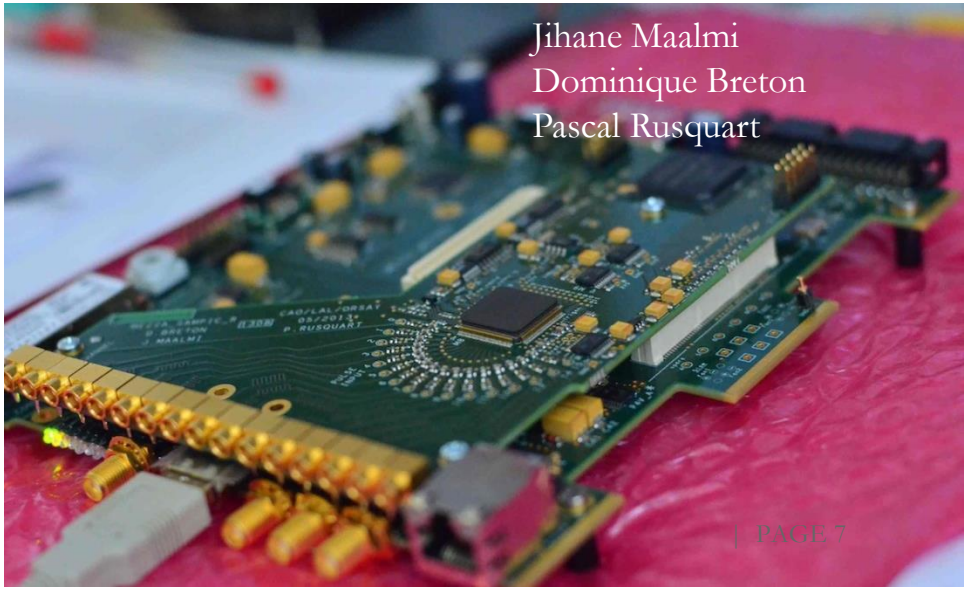
- End of conversion rise "ChtoRead" flag.
- Stays high until all available data read.
- Readout driven by the user (Read and RCk signals)
- Data read channel by channel
- Region of interest readout to reduce the deadtime
- Rotating priority mechanism to avoid reading always the same channel.
- Readout of the converted data through a 12 bit LVDS bus:
  - Timestamps
  - Trigger Cell Index
  - Channel Identifier
  - The cells (all or a selected set) of a given channel are read sequentially
- **Channel is not in deadtime during Readout (the data register is already a buffer)**

RO exemple: Hits on 2 Channels, 1 conversion



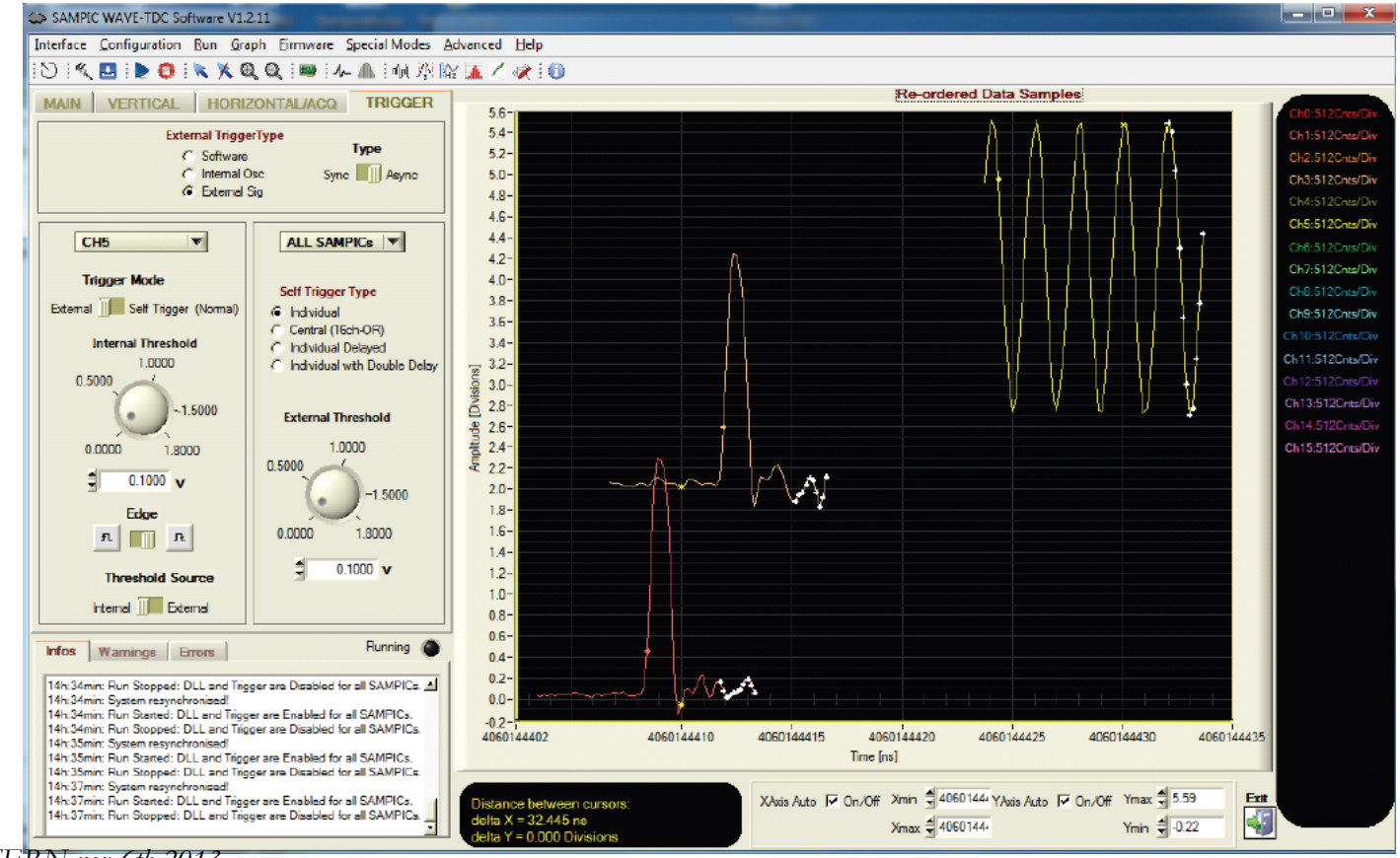
THE ACQUISITION BOARD (LAL)

- Mezzanine board for 16 channels.
- SMC connectors
- Mother board can hold 2 mezzanines: 32 channels
- **USB** – Ethernet – Fiber Optic readout
- 5V voltage supply – 1Amp
- Windows software
- 2 boards are currently available



THE ACQUISITION SOFTWARE (LAL)

- Usable for test
- Already usable for small size experiment.
- Special visualization for WTDC mode



TEST STATUS

- **Everything is working well excepted**:
  - ROI readout: fail in zone case. Bug found, easy to fix
  - Central trigger : bug found, easy to fix
- The 2 last features are not absolutely necessary. The chip is usable as it is
- Sampling is ok :
  - from 3 to 8.2 GSPS on all the channels.
  - up to 10 GSPS on 8 channels.
  - Not tested under 3 GSPS
- Readout ok @ 80MHz. To be tested at higher frequency
- Leakage ok. Data not damaged for storage times of few tens µs

POWER CONSUMPTION: 0.15W @ 6.4 GSPS

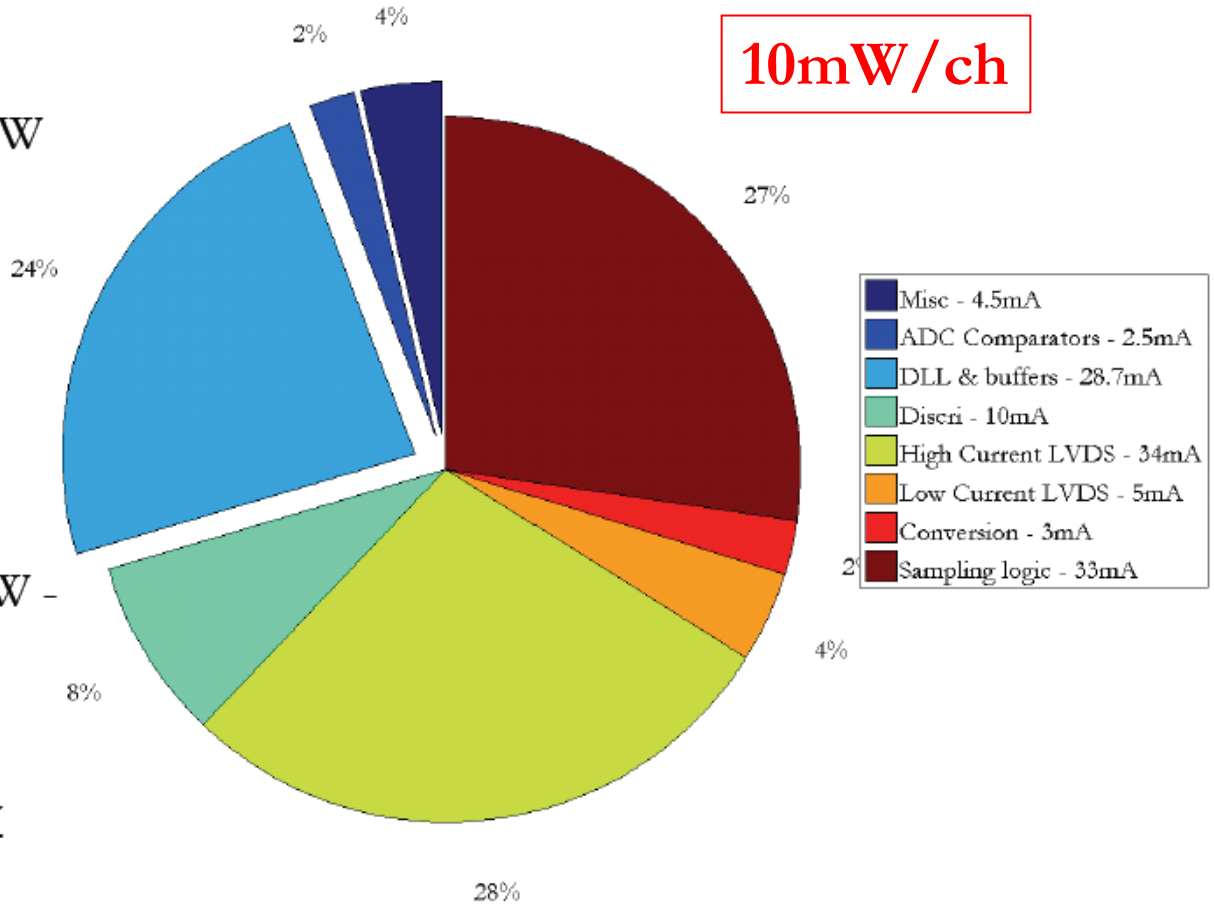
Analog

- DLL & buffer: 51mW - 1/3rd of the chip.
- ADC: 2µW/cell.

Digital

- LVDS output: 70mW - ~ half power.
- Sampling logic (for trigger & ZOI): 60mW.
- Discri: 1.1mW/ch.

10mW/ch

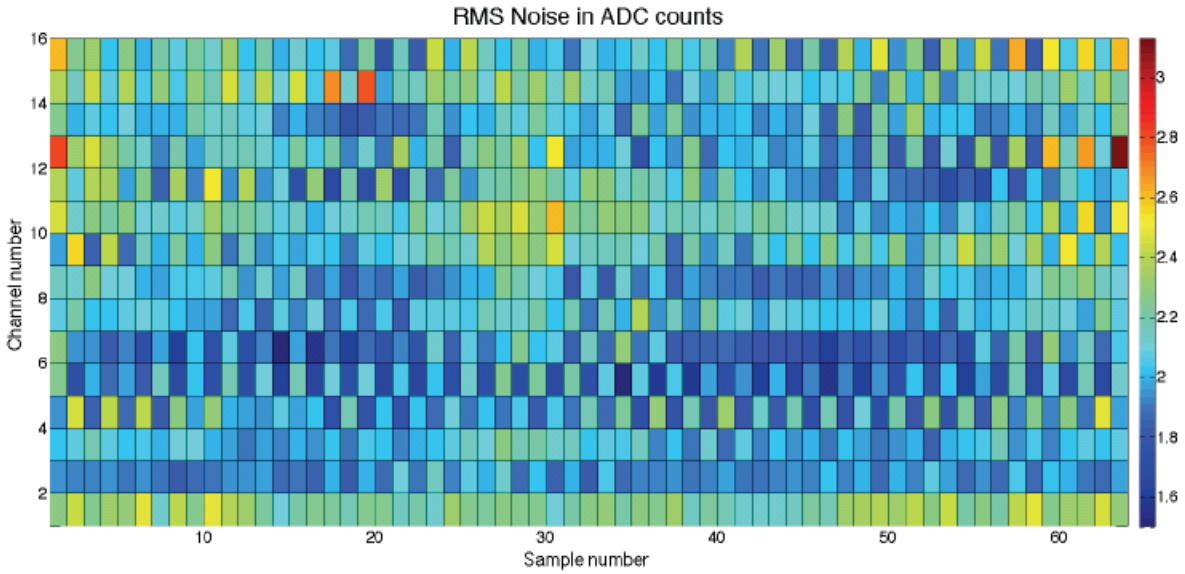


SamPic power consumption - 120mA High Current LVDS - 84mA Low Current

SAMPIC NOISE

- Wilkinson conversion works perfectly @ 1.3 GHz
- After cell/cell pedestal calibration
- No change with sampling frequency
- Noise floor at 1mV RMS
- 1 V total dynamic
- **~10 bit rms range**
- Noisiest cells are at 1.3mV RMS

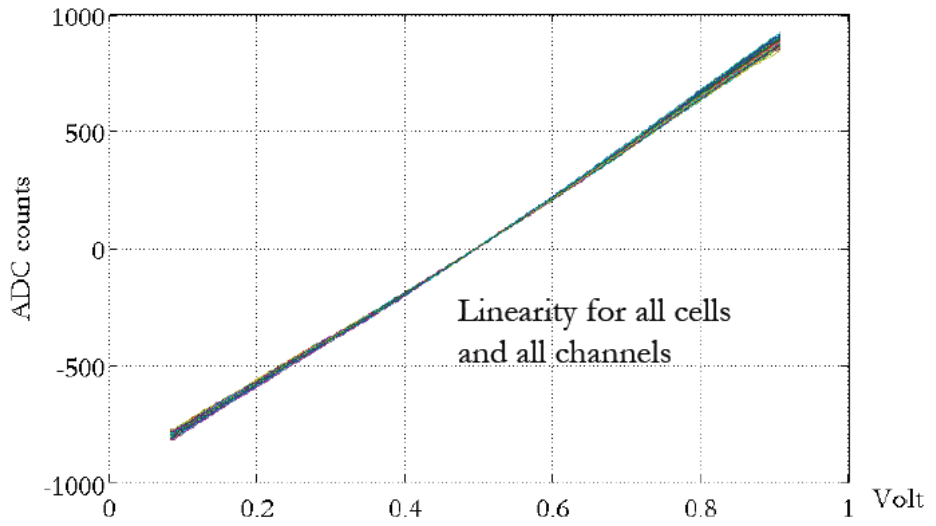
Noise MAP



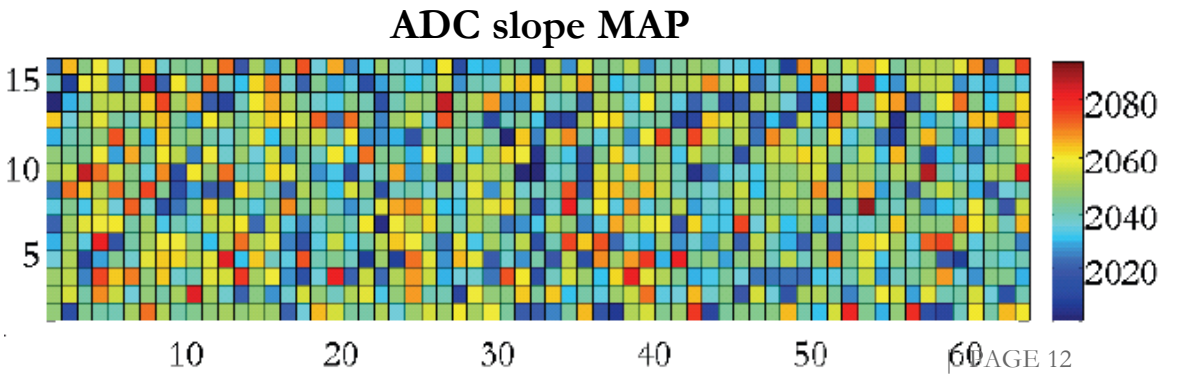
1mV = 1.95ADC count

LINEARITY

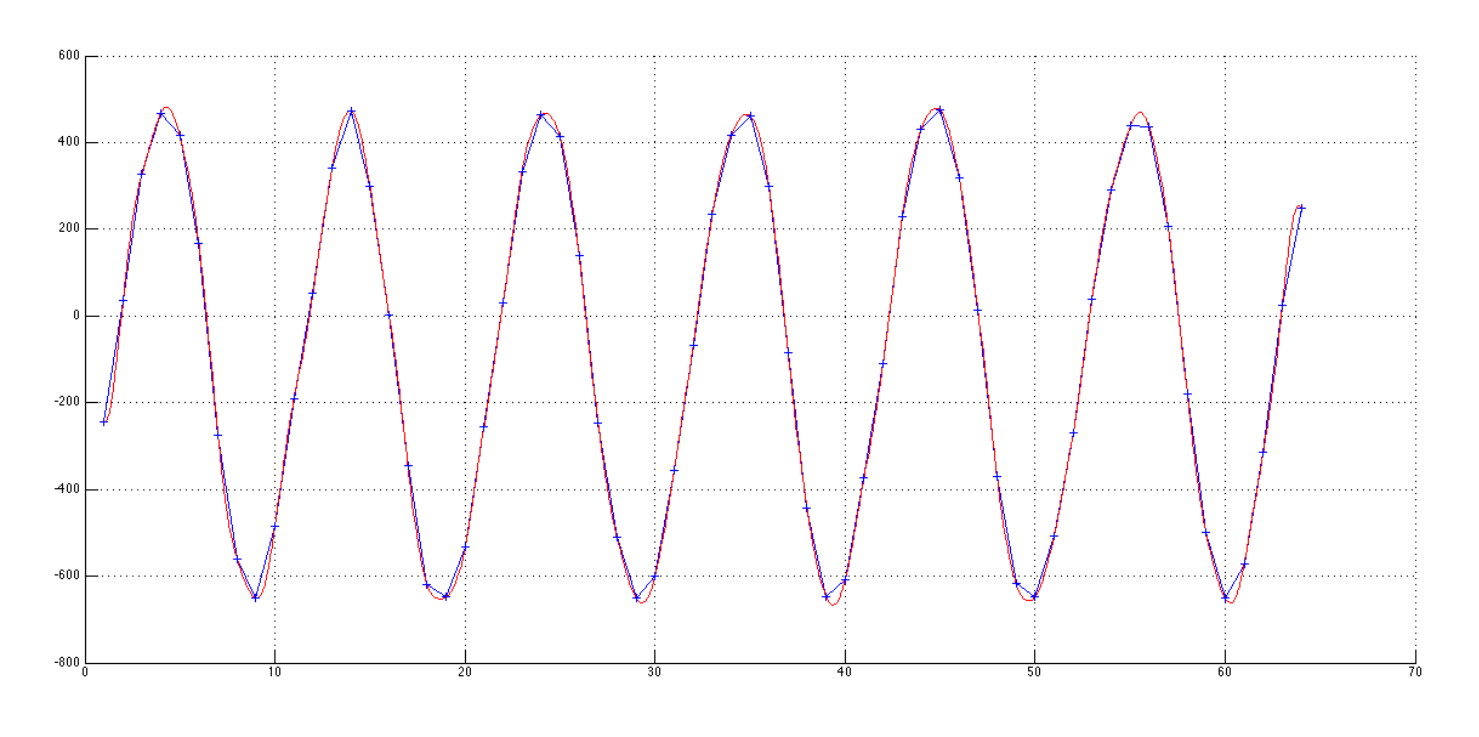
- 3% of non-linearity
- Due to non-linearity of :
  - * Charge injections
  - * ADC comparator time response
- Cell-to-cell spread of slopes = 3% pp



- Both effects are systematic and can be corrected after calibration
- **None of these 2 effects are corrected in the following measurements**



QUALITY OF SAMPLING



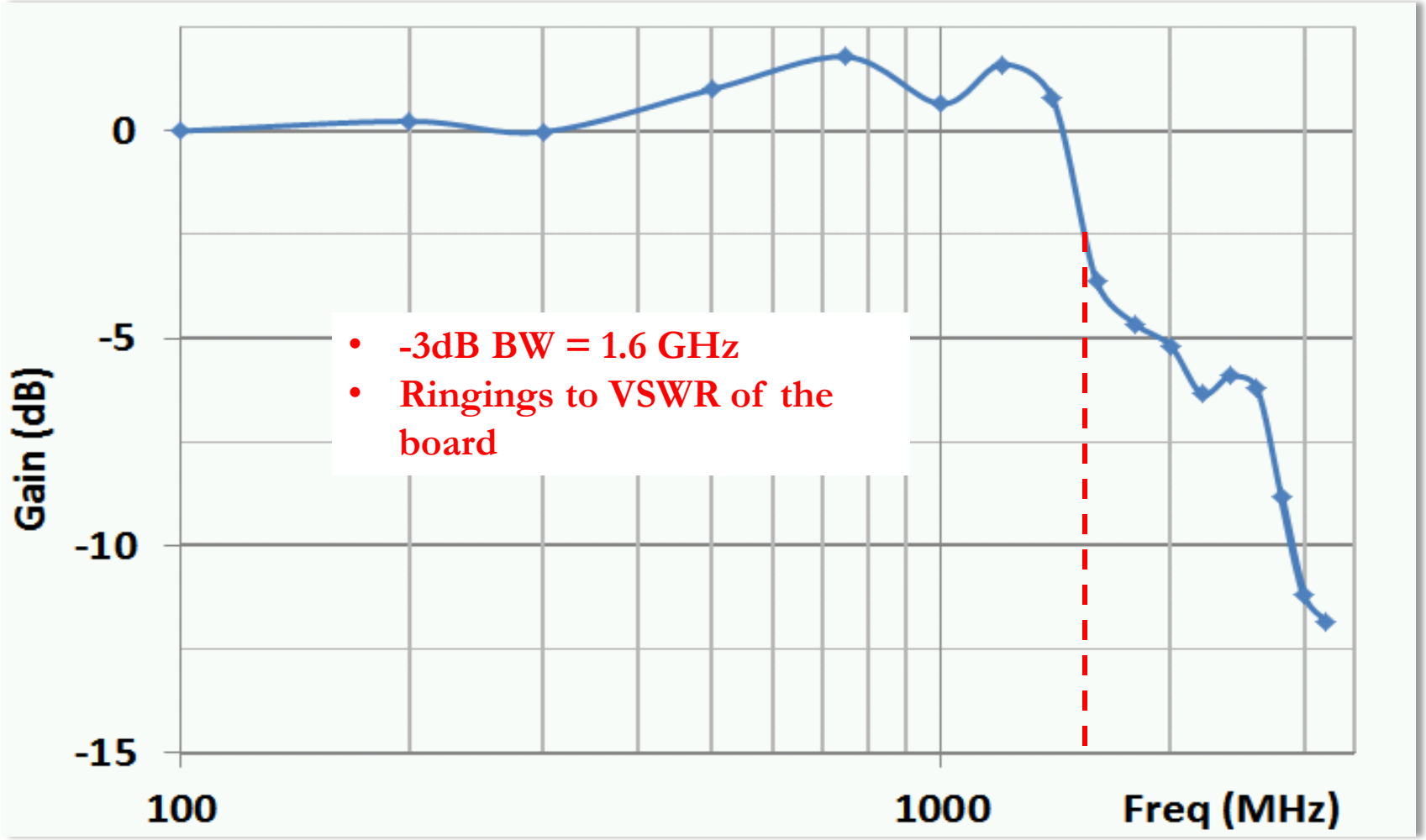
1 GHz sinewave (0.5V peak-paek) 64 samples 'out of the box' (pedestal cal. only) @ 10.2 GSPS

64 usable data points

Already looks good

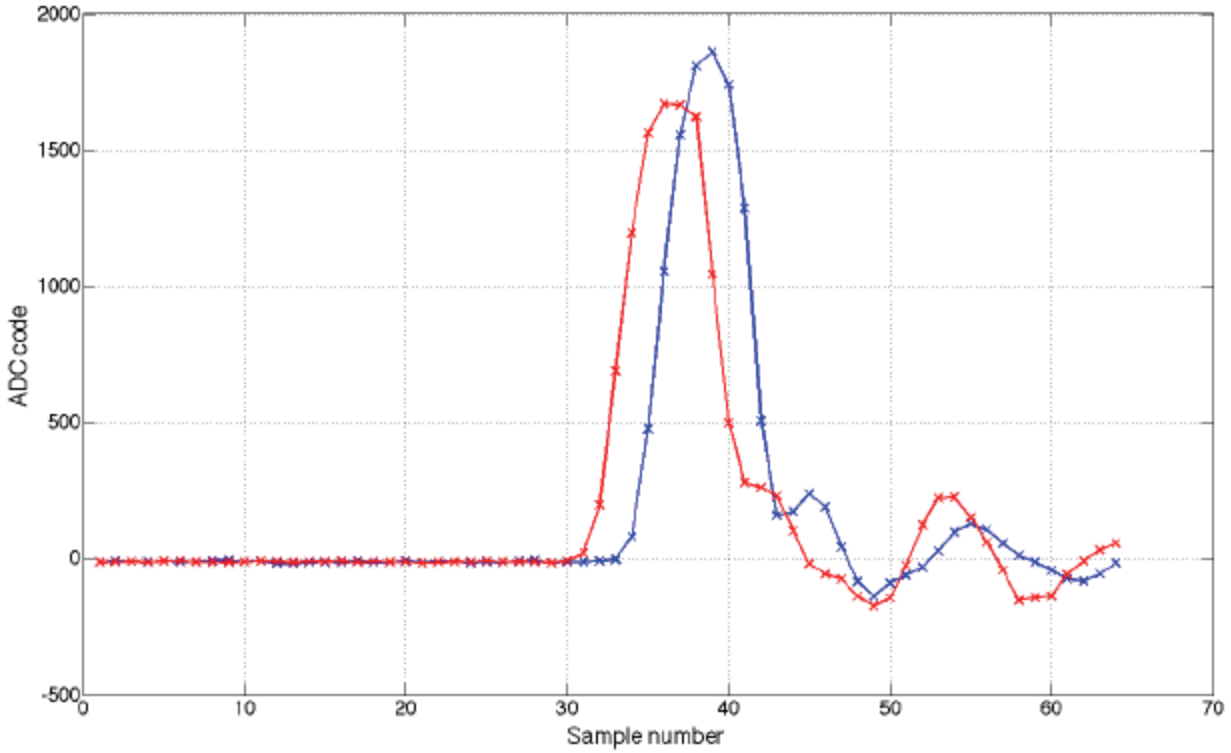
Will be improve with timing and ADC linearity calibrations

BANDWIDTH


0
-5
-10
-15
Gain (dB)
100
1000
Freq (MHz)
• -3dB BW = 1.6 GHz
• Ringings to VSWR of the board

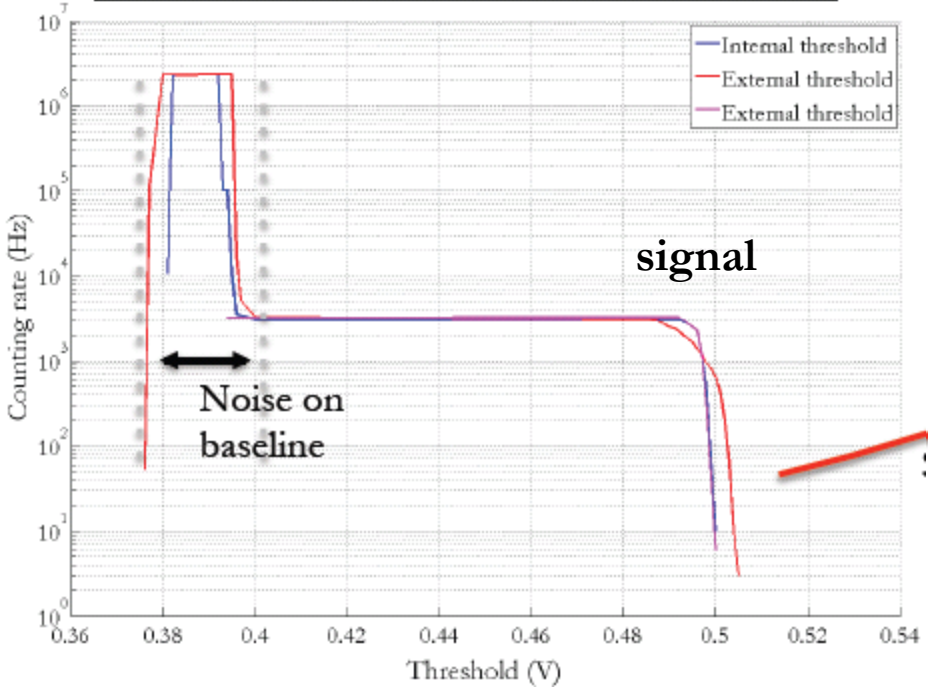
PULSES RESPONSE

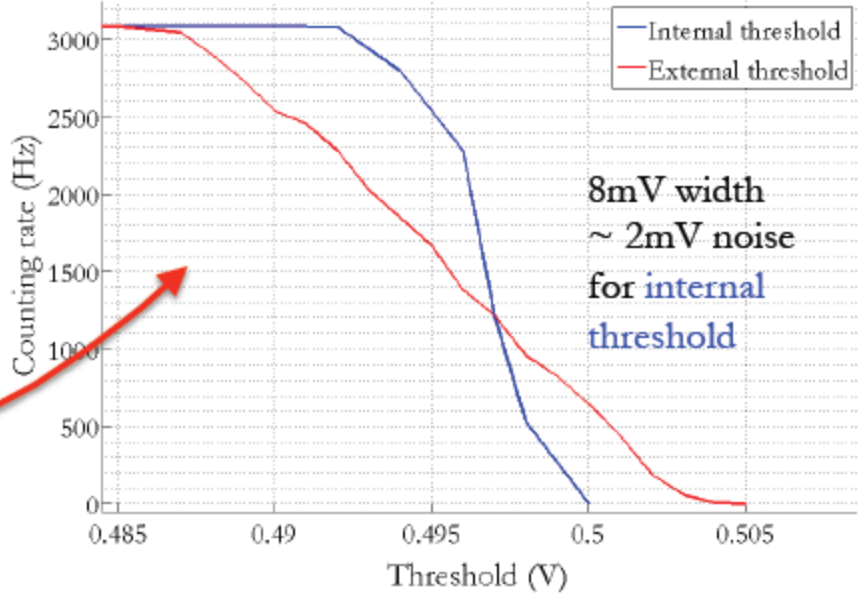
- Further tests made with **0.85ns-FWHM** pulse split in 2. 1 output delayed by cable => 0.9V amplitude
- 6.4 GSPS sampling
- Self triggered



SELF-TRIGGER EFFICIENCY AND NOISE

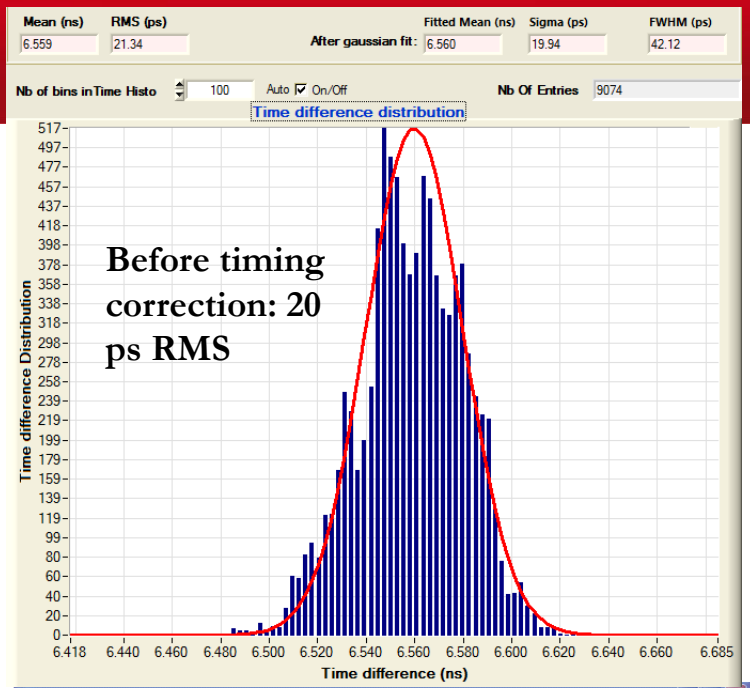
S-curve with 3kHz activity.
- 1ns pulse - 150mV amplitude

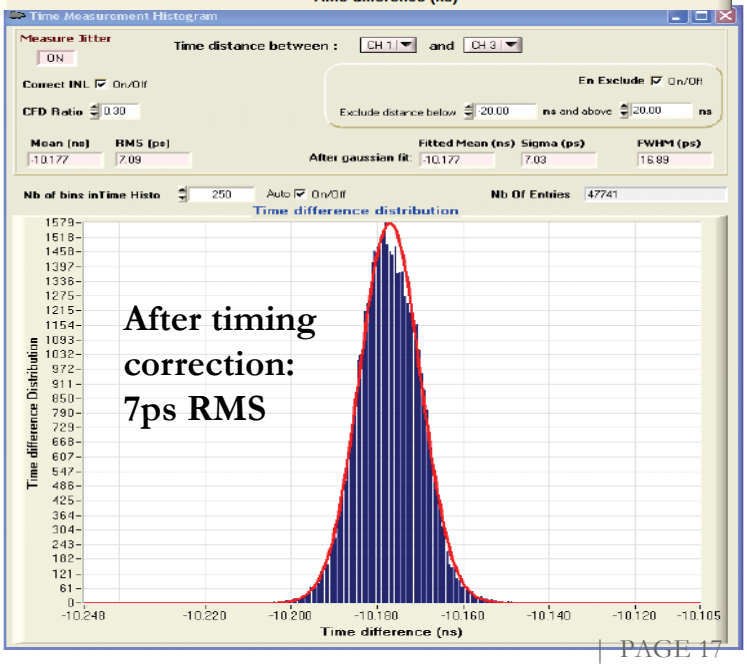




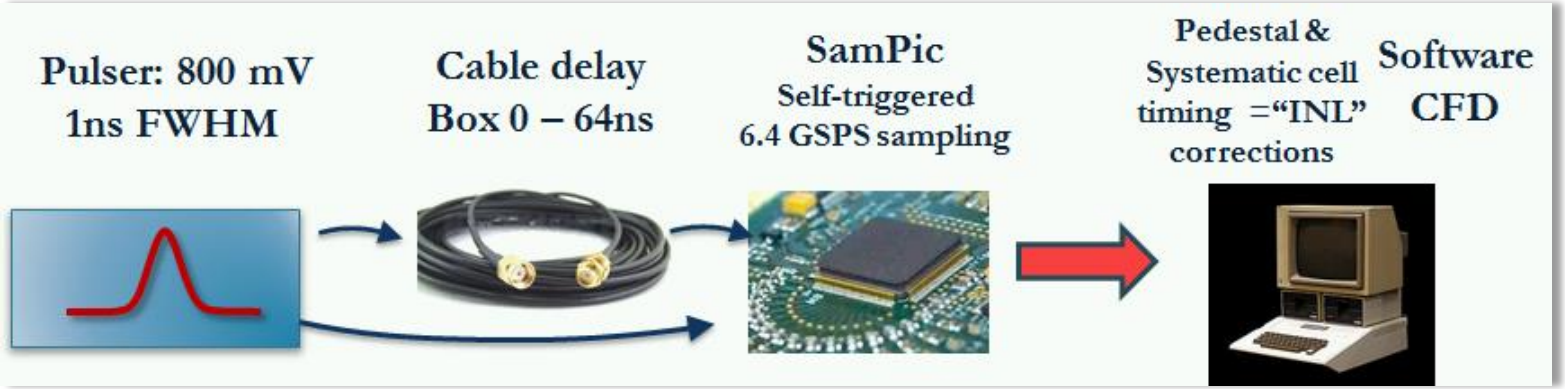
TIMING RESOLUTION

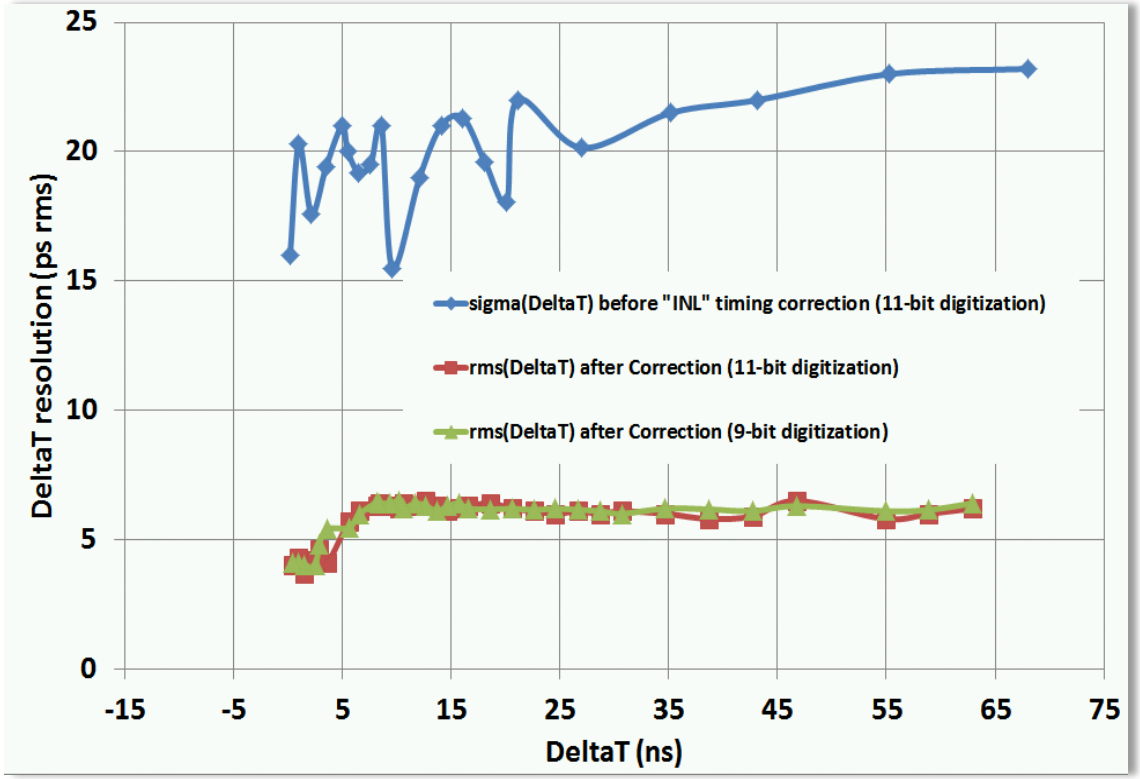
- First measurement: 2 pulses with 10ns distance. 3 kHz rate
- Measurement performed for 6.4 GPSPS sampling
- **20 ps RMS resolution on Delta T before any correction**
- **7 ps RMS after INL timing correction only**
- No tail in the distribution.
- No hit "out of time" due to mestabilities, etc…





FIRST RESULTS ON TIMING: DELTAT MEASUREMENTS





- <15 ps RMS = (22/√2) timing resolution without any timing calibration (short DLLs)
- <5 ps RMS timing resolution after timing "INL" correction
- Probably setup-limited.
- Same results in 9-bit/400ns mode
- Probably different with smaller pulses
- Correction of ADC gain spread and non-linearity not applied yet

WORK PLANNED OR IN PROGRESS

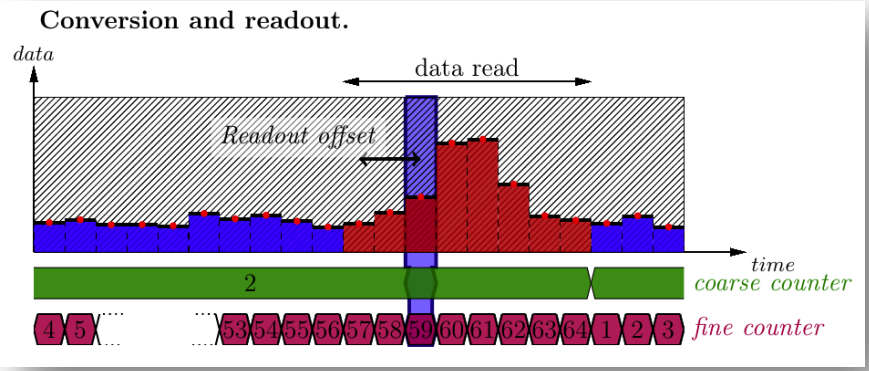
- Herve's PhD's defense (Dec 3rd 2013).
- Improvement of Firmware and DAQ software for:
  - Higher readout clock frequency
  - Better DAQ stability for Fs > 8 GSPS
- Offline-ADC nonlinearity correction
- Timing characterization with detectors/ test beams (2 setup are available)
- Characterization in fastest conversion/less resolution mode
- New submission planned for Dec 2013 or beg. Of 2014 with only minor corrections:
  - Fix of the 3 identified bugs, Improvement on ADC linearity
  - Improved "central trigger"
  - (Pseudo)-differential input ?, Plastic packaging for easier handling
- DeadTimeLess chip: end of 2014 or later

SAMPIC0: SUMMARY

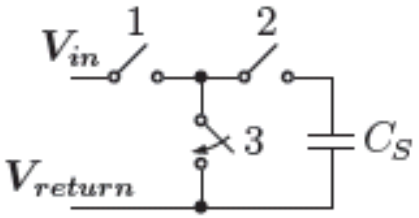
		Unit
Technology	AMS CMOS 0.18µm	
Number of channels	16	
Power consumption	180 (1.8V supply)	mW
Discriminator noise	2	mV rms
SCA depth	64	Cells
Sampling Speed	<3-8.4 (10.2 for 8 channels only)	GSPS
Bandwidth	1.6	GHz
Range (Unipolar)	1	V
ADC resolution	8 to 11 (trade-off time/resolution)	bit
SCA noise	<1.3	mV rms
Dynamic range	9.6	Bit rms
Conversion time	0.2-1.6 (8bit-11bit)	µs
Readout time (can be probably be doubled)	25 + 6.2/sample	ns
Time precision before correction	15	ps rms
Time precision after timing INL correction	< 5	ps rms

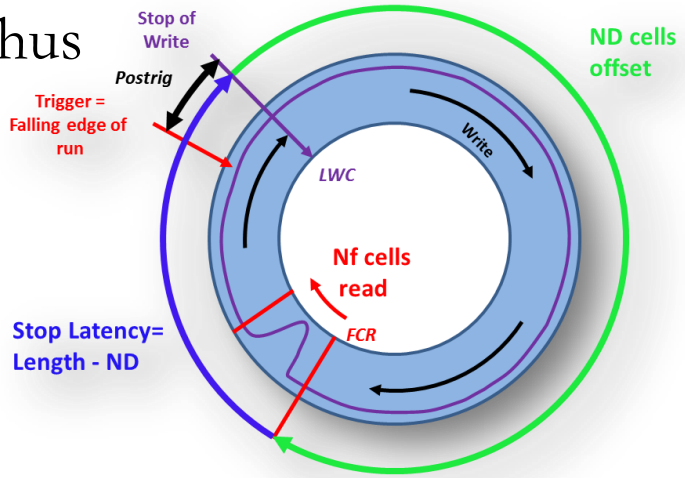
BACKUP SLIDES

SCA



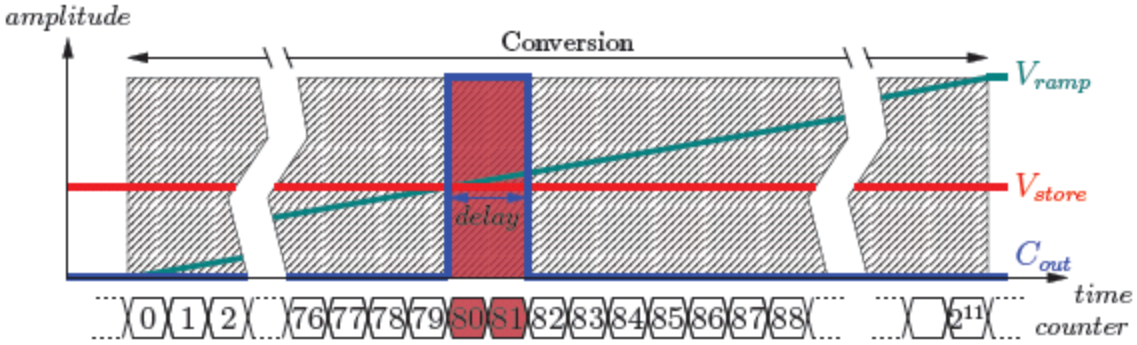
- No input buffer.
- 64 Cells/1.5 GHz BW.
- 1V usable range
- Cell structure to avoid leakages and ghosts.
- Continuously writing until triggering.
- « TDC » like trigger position marking
- Special design ensuring good quality (constant bandwidth) over all the 64 samples (even thus after trigger).
- Optional Region of Interest Readout for deadtime minimization.





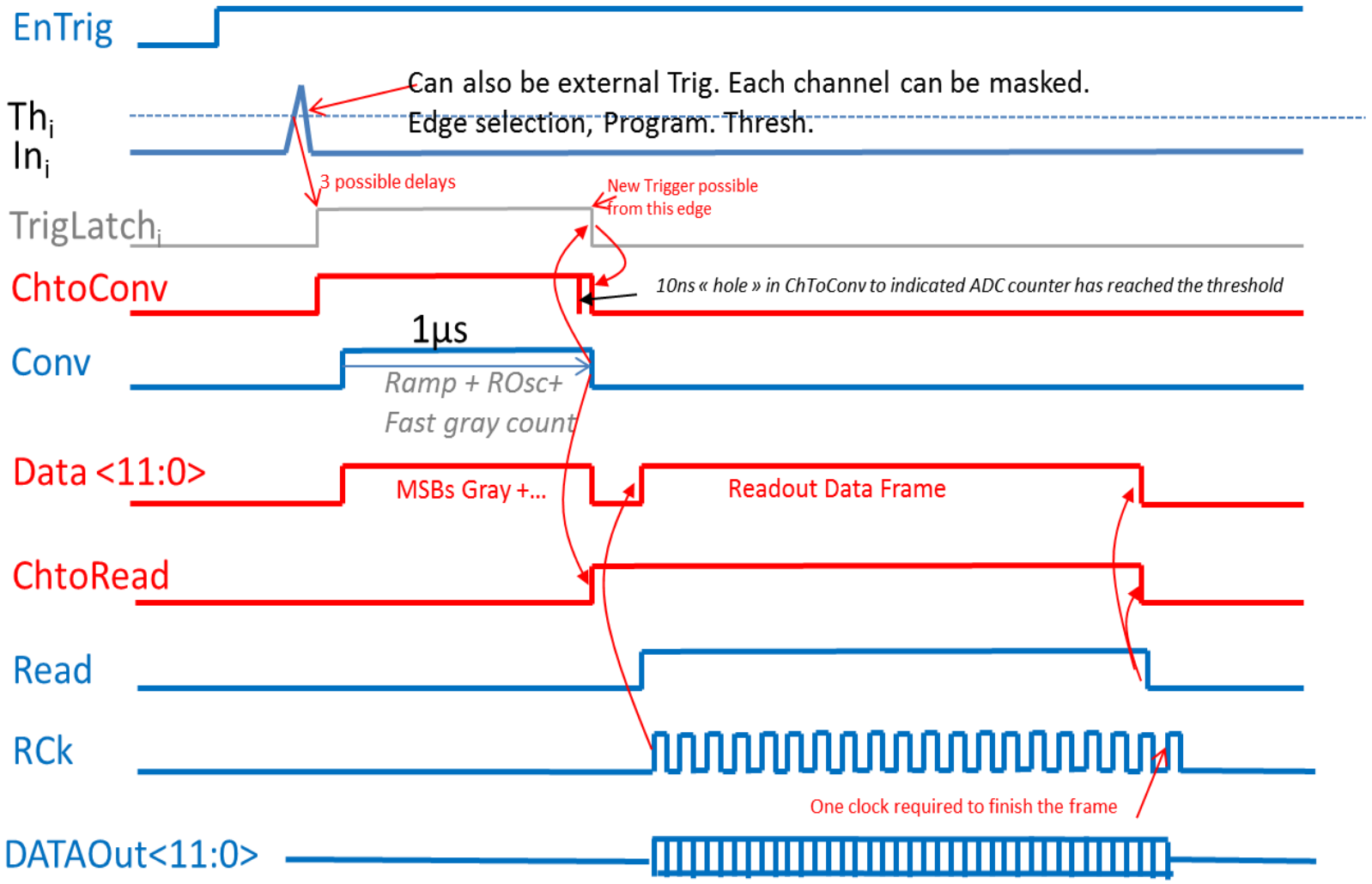
Digitization

- **1 Wilkinson ADC/cell:**
  - 1.3 GHz gray counter (clock provided by an internal oscillator)
  - 1V range , 11 bit max.
  - Conversion time depends on the required resolution:
    - Slope of the ramp is tunable
    - **1.6µs for 11bit, 800 ns for10 bit, 200ns for 8 bit**

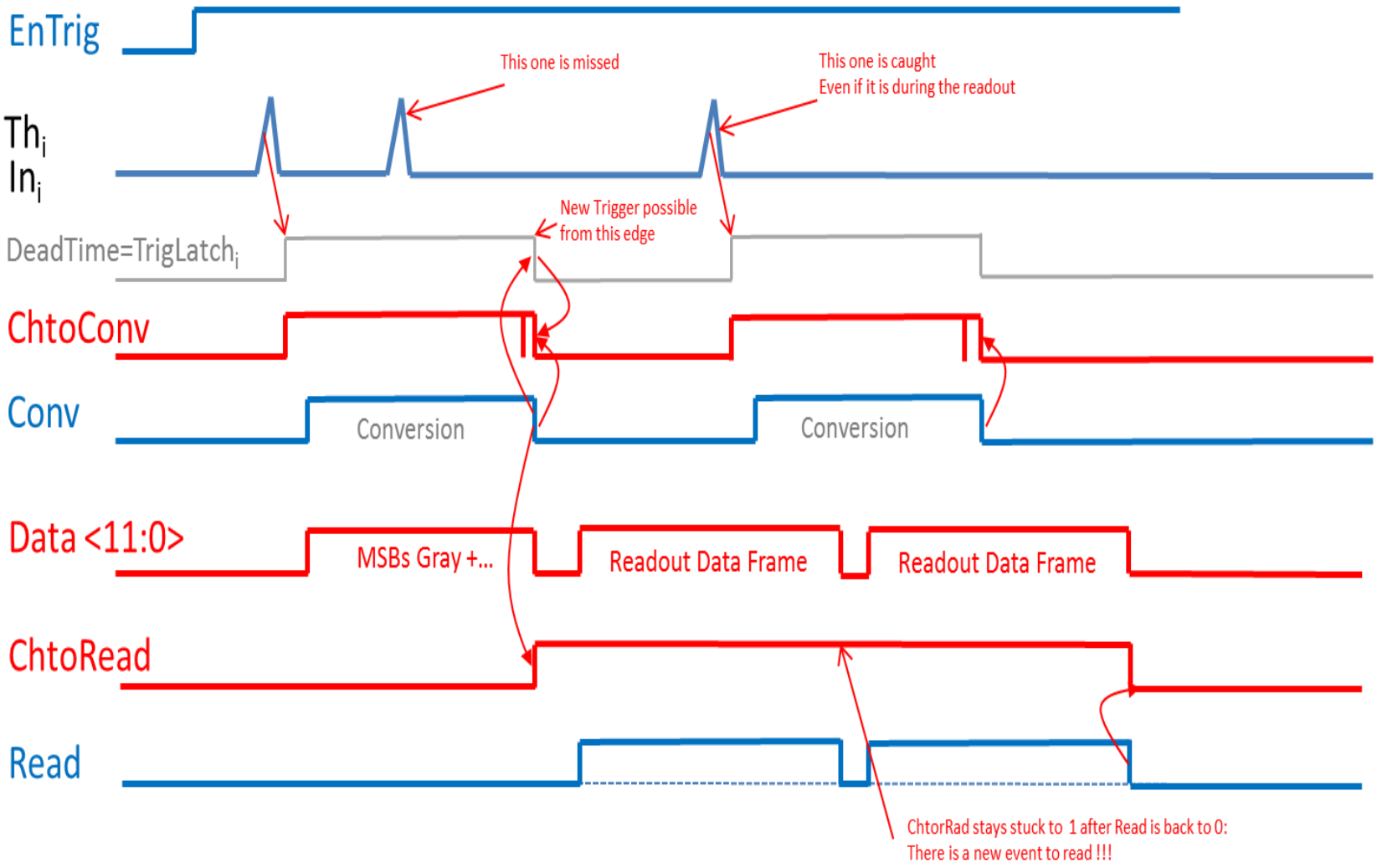


- "Convert" signal provided by the user starts the simultaneous conversion of all the cells of the triggered channels
- EOC signal sent back to the user
- Result stored in registers waiting for readout
- Once converted, a channel is already usable for a new event

SIMPLEST OPERATION: 1 HIT, 1 CHANNEL



MULTIPLE HITS, 1 CHANNEL



HITS ON 2 CHANNELS, 2 CONVERSIONS