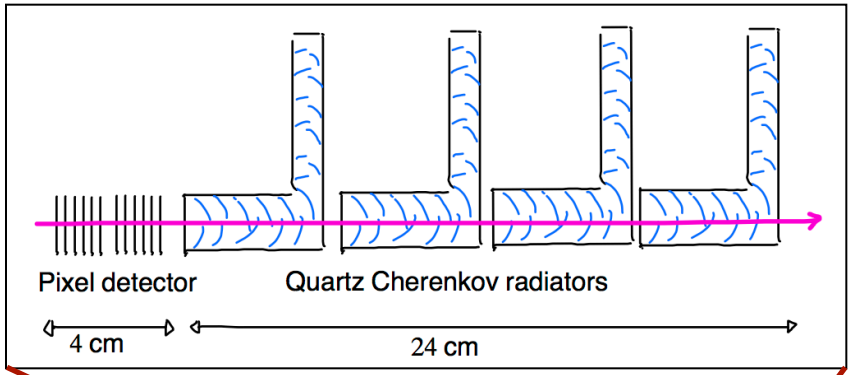
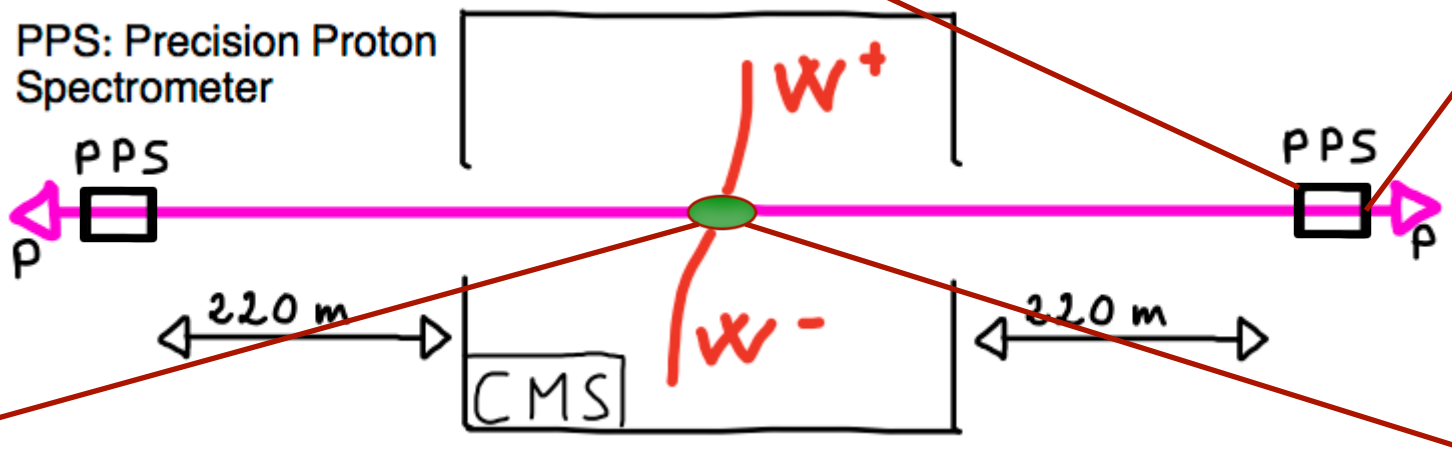
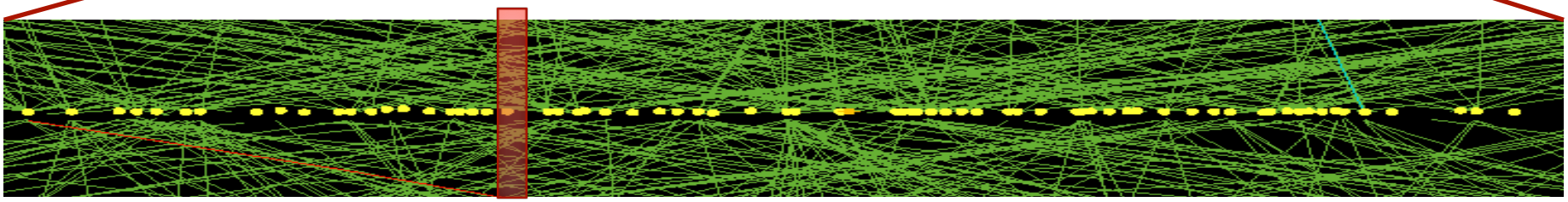
CMS - TOTEM PPS Detector

PPS goal:

- Position ~ 30 micron
- Timing ~ 10 ps



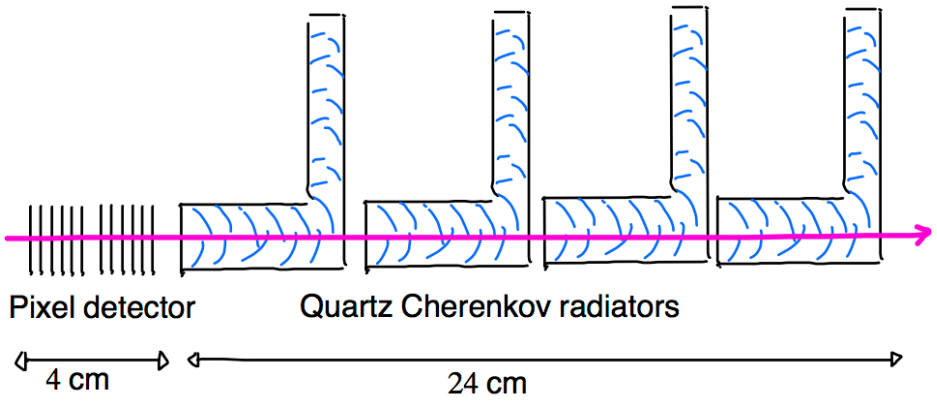




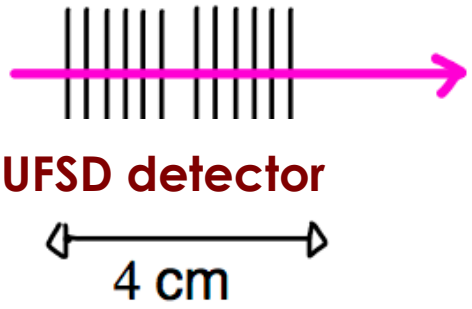
Use z-by-timing to select the right vertex

Ultra-Fast Silicon Detector

Pixel + Quartic



UFSD:
one single device



$$\sigma_T = \frac{30\,ps}{\sqrt{4}}$$

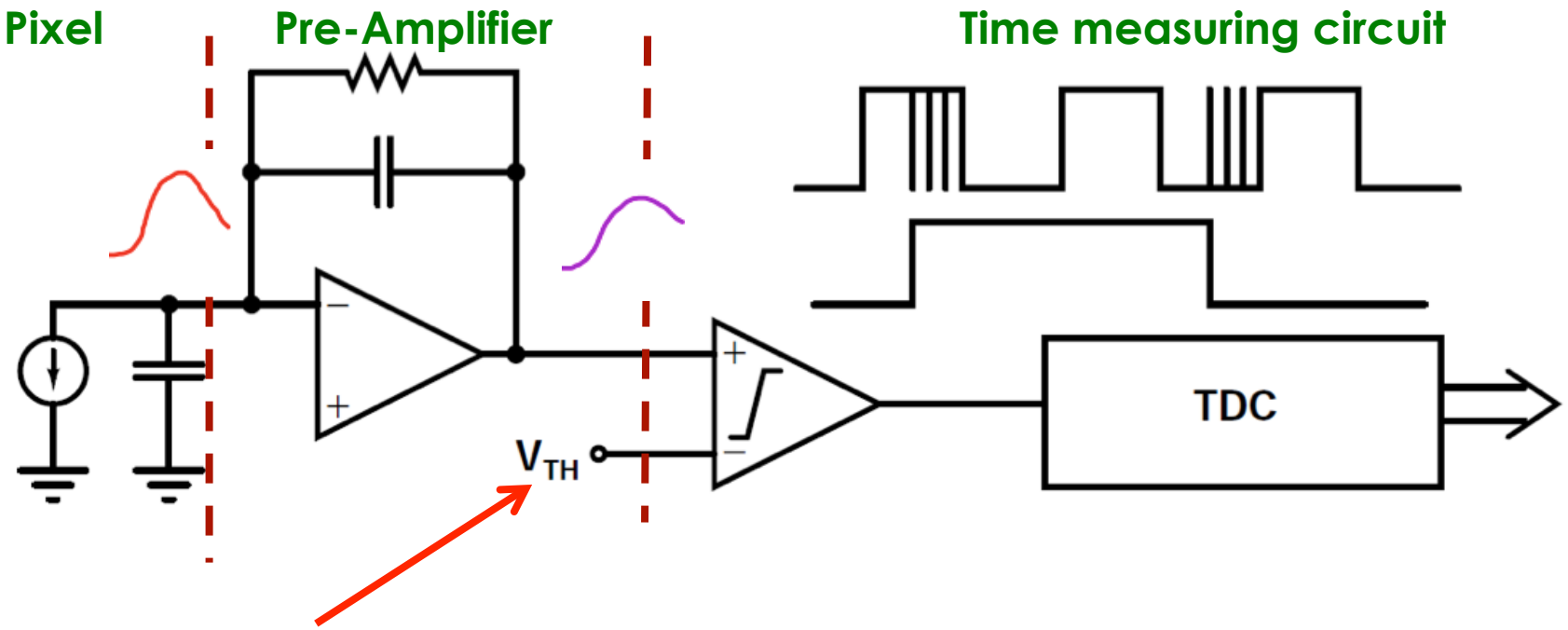
$$\sigma_T = \frac{?\,ps}{\sqrt{12}}$$

Timing capability of Silicon Detector

What is the timing precision of Silicon detectors?

Can we design a silicon detector precise enough?

UFSD: a time-tagging detector



Time is set when the signal crosses the comparator threshold

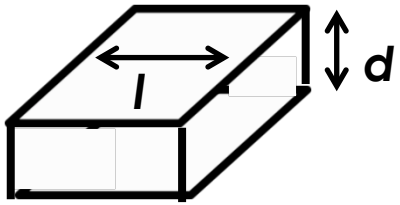
The timing capabilities are determined by the characteristics of the signal at the output of the pre-Amplifier and by the TDC binning:

$$\sigma_{Total}^2 = \sigma_{Jitter}^2 + \sigma_{Time\ Walk}^2 + \sigma_{TDC}^2$$

A parameterization of σ_t

$$\sigma_t^2 = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2 \quad (1)$$

Jitter | Time Walk | TDC



d: **detector thickness** [micron]

l: **pitch** [micron]

C: **Detector capacitance [fF]**
Depends on the pitch and thickness

N: **Noise at preamp.**
Dominated by the voltage term

S: **Signal**

t_{rise}: Pre-Amp Shaping time

V_{th}: Comparator threshold
Depends on the noise level

TDC:Width of the TDC LSB [ps]

$$C_{Det} = \varepsilon\varepsilon_o \frac{l*l}{d} + 0.2*4l + 50$$

$$N \propto \frac{C_{Det}}{\sqrt{t_{rise}}}$$

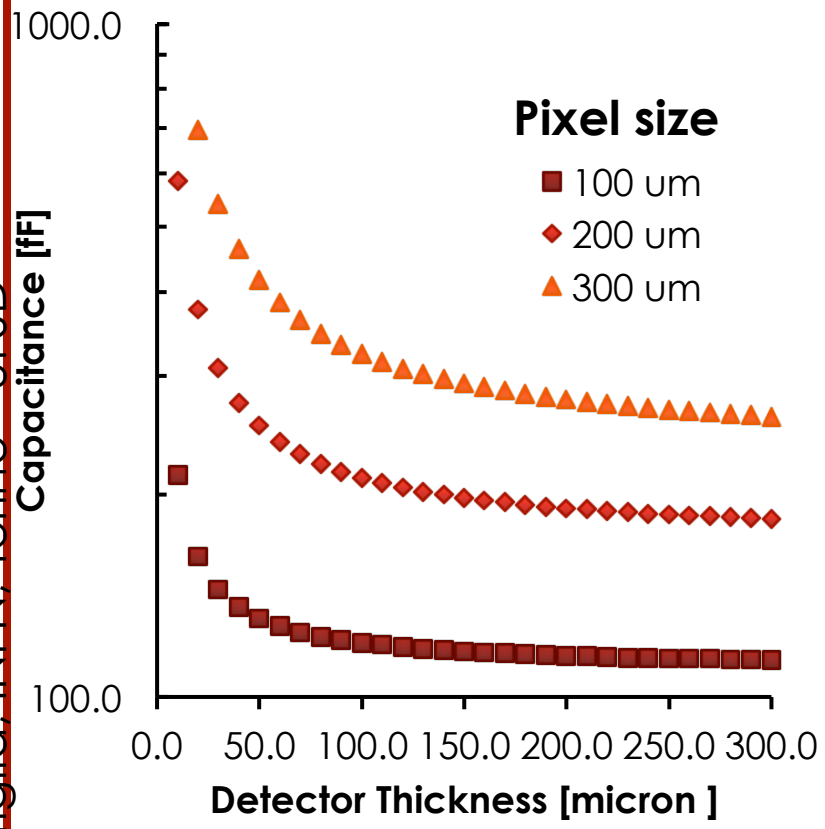
Use eq. slide (7)

$$V_{th} = 10*N$$

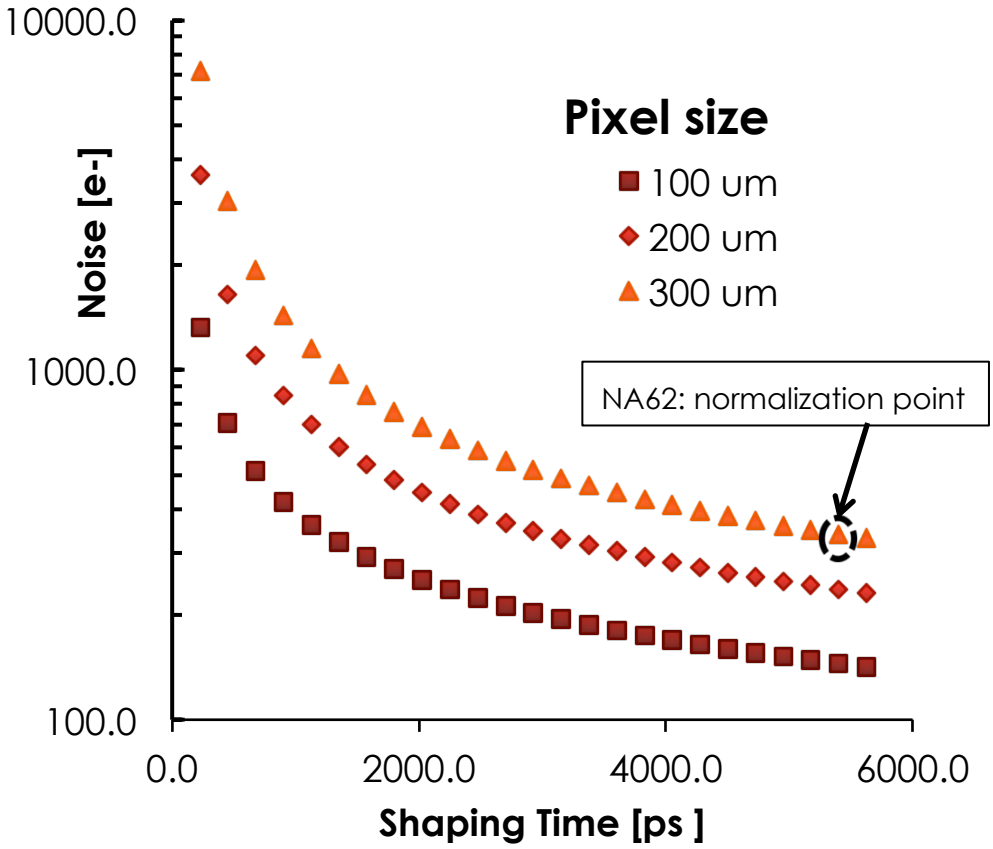
$$LSB = 20$$

Values used in the parameterization

Capacitance vs Thickness



Noise vs Shaping Time



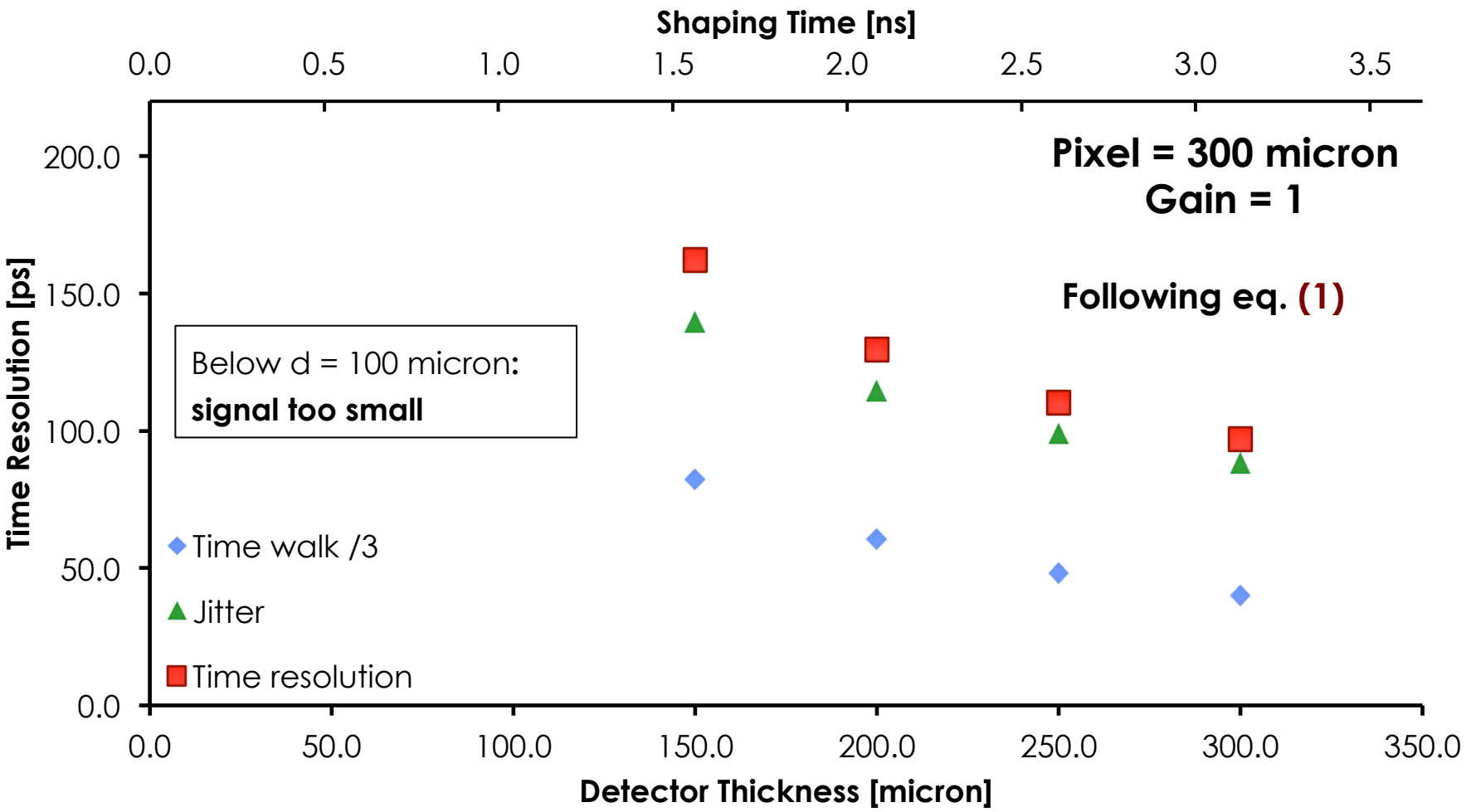
Capacitance:

backplane + 0.2 fF/μm (perimeter)
+ 50 fF (fix term)

Noise normalized to NA62:

Shaping time ~ 5500 ps,
noise ~ 300 e-

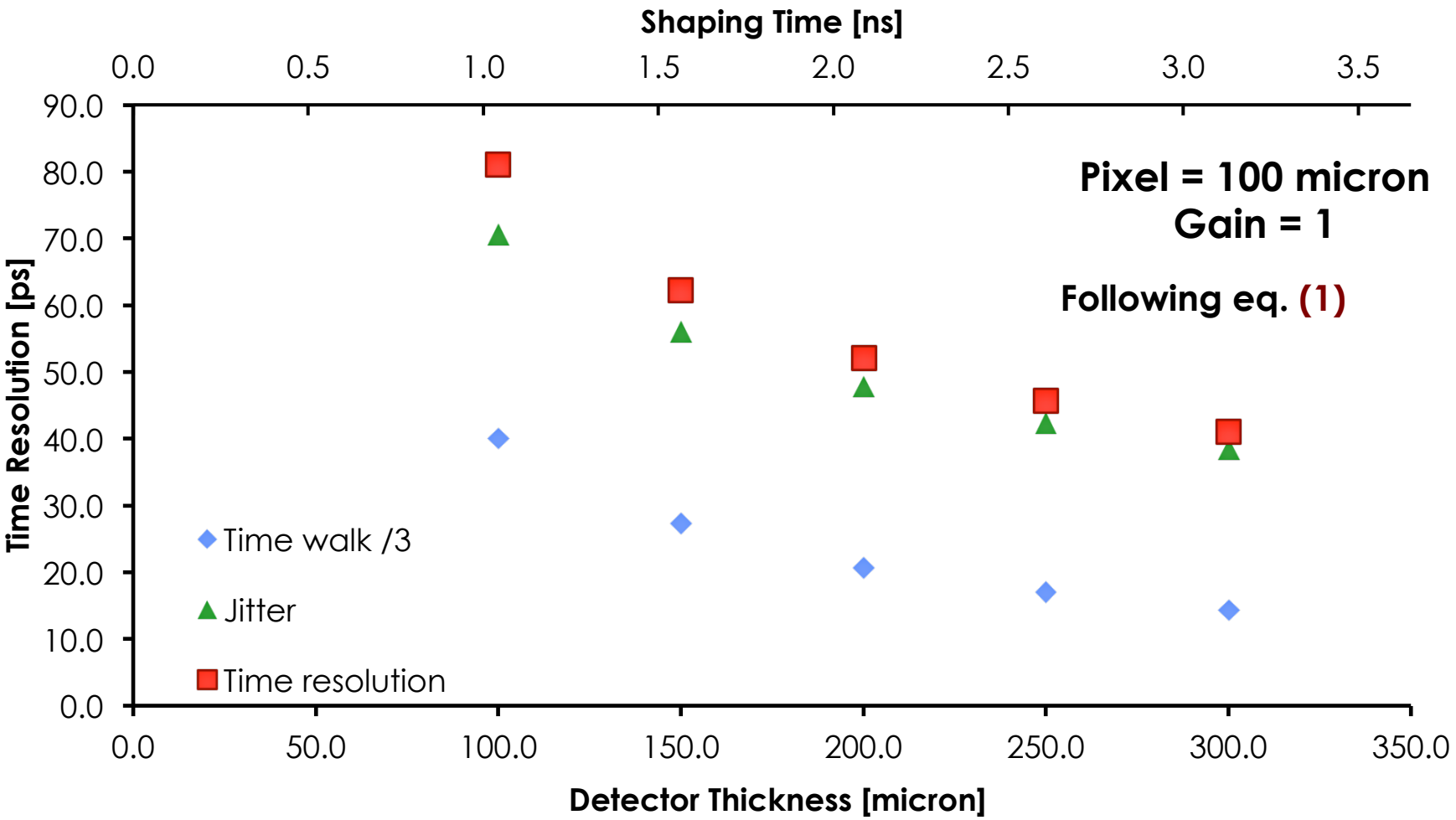
State of the Art



Best resolution achievable: ~ 100 ps

(assuming Time Walk reduction of ~ 3)

State of the Art



Best resolution achievable: ~ 50 ps

(assuming Time Walk reduction of ~ 3)

How can we do better?

$$\sigma_t^2 = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2$$

Boost the signal: **introduce gain** $S => G * S$

Impact ionization model: if the electric field is high enough, the carriers are multiplied according to:

$$N(\ell) = N_0 * e^{(\alpha * \ell)} = G * N_0$$

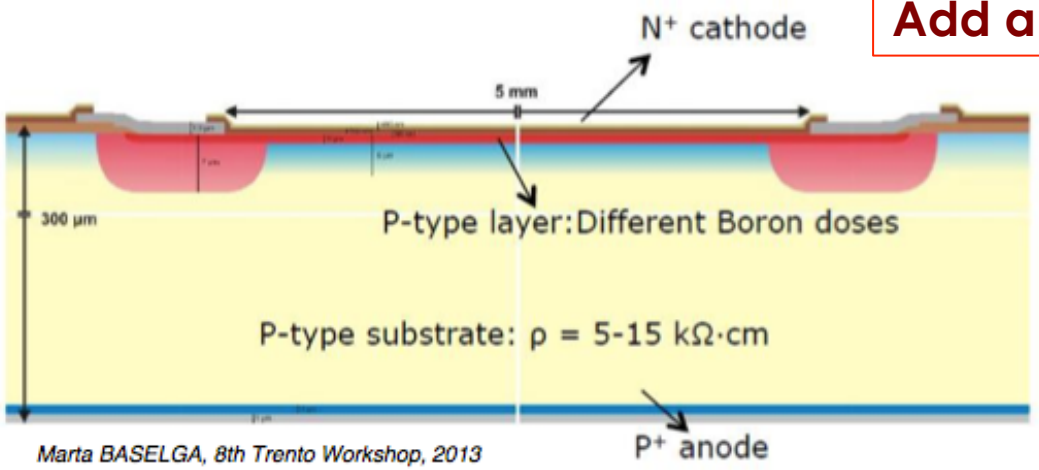
In Silicon, at 270kV/cm:

- $\alpha_e \approx 0.7$ pair/μm
- $\alpha_h \approx 0.1$ pair/μm

(see backup slides for details)

A new design of silicon detector

Add a layer of doping to obtain gain

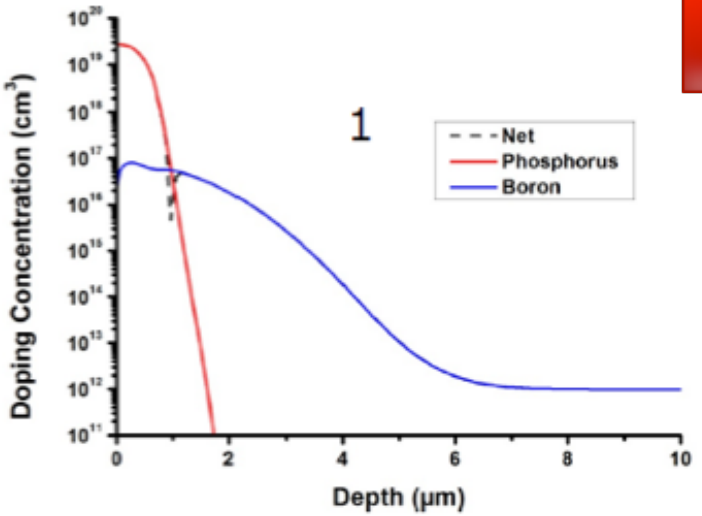


Marta BASELGA, 8th Trento Workshop, 2013

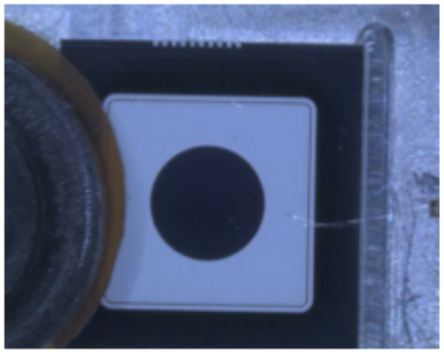
n^{++} - p^{+} - p – p^{+} stucture

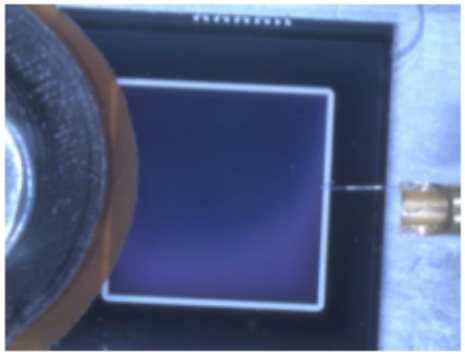
$10^{16\text{-}17}$ cm^{-3} – much larger than in the bulk. Large N_{eff} provokes avalanche multiplication by impact ionization.

V_{FD}



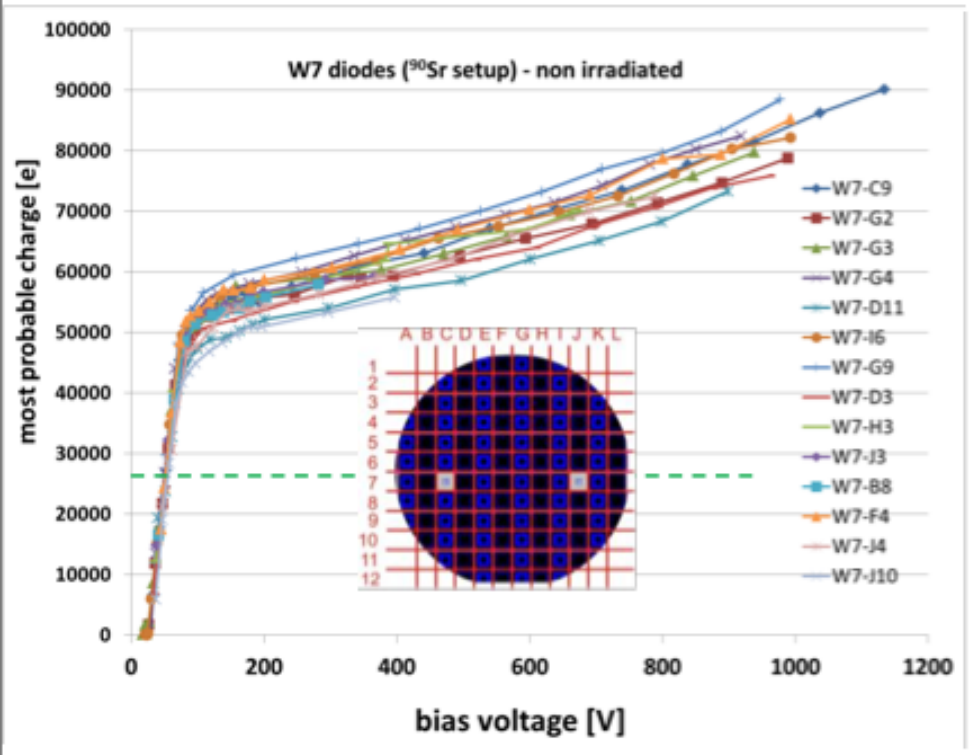
Prototype Detectors exist!

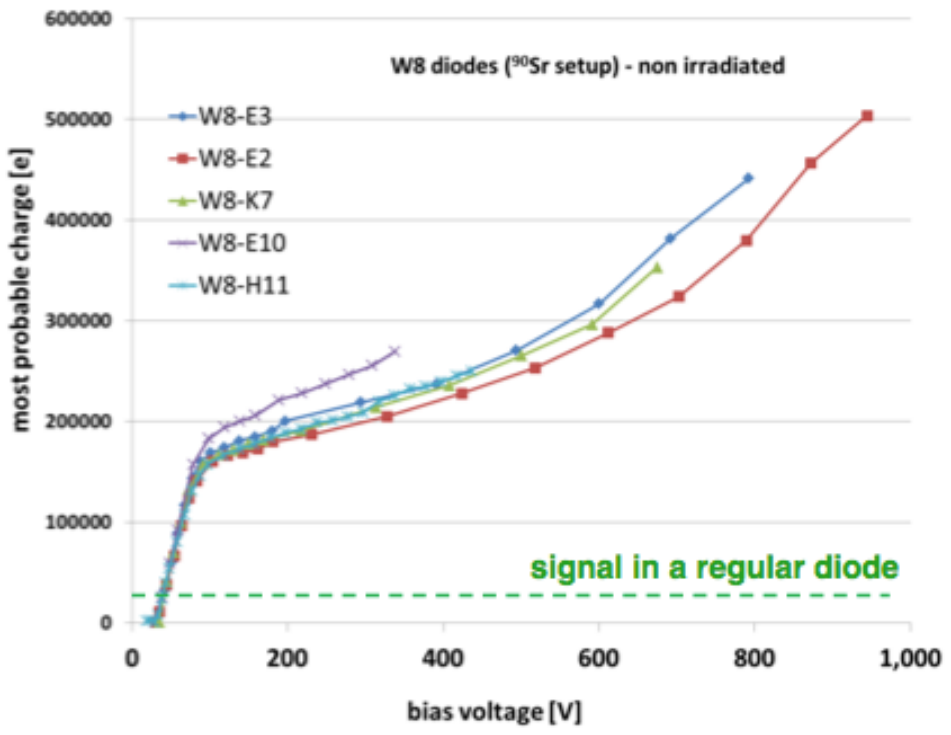




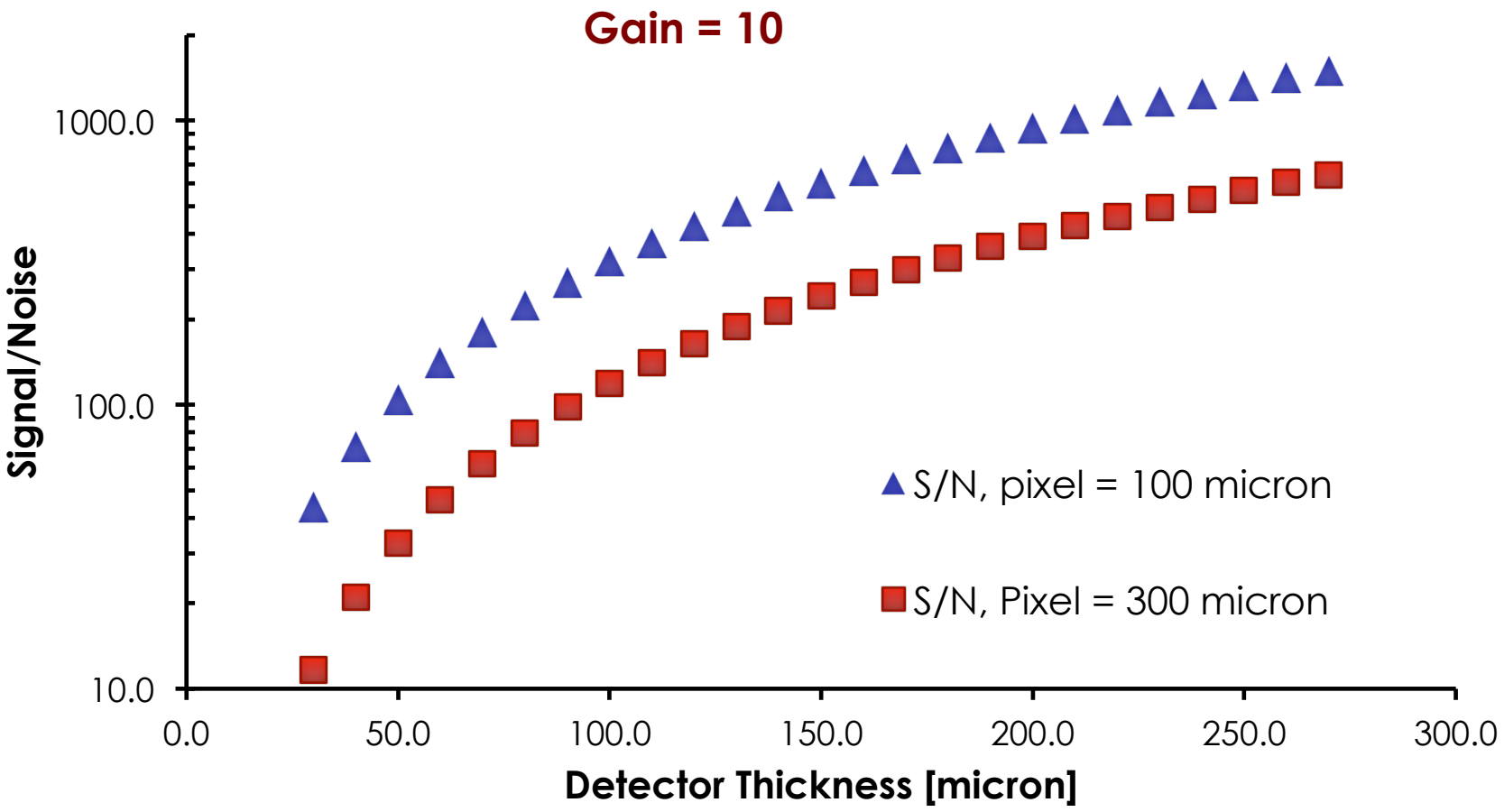
Results from Ultra – Fast silicon detector

Two sets of detectors, with gain 3 and 10



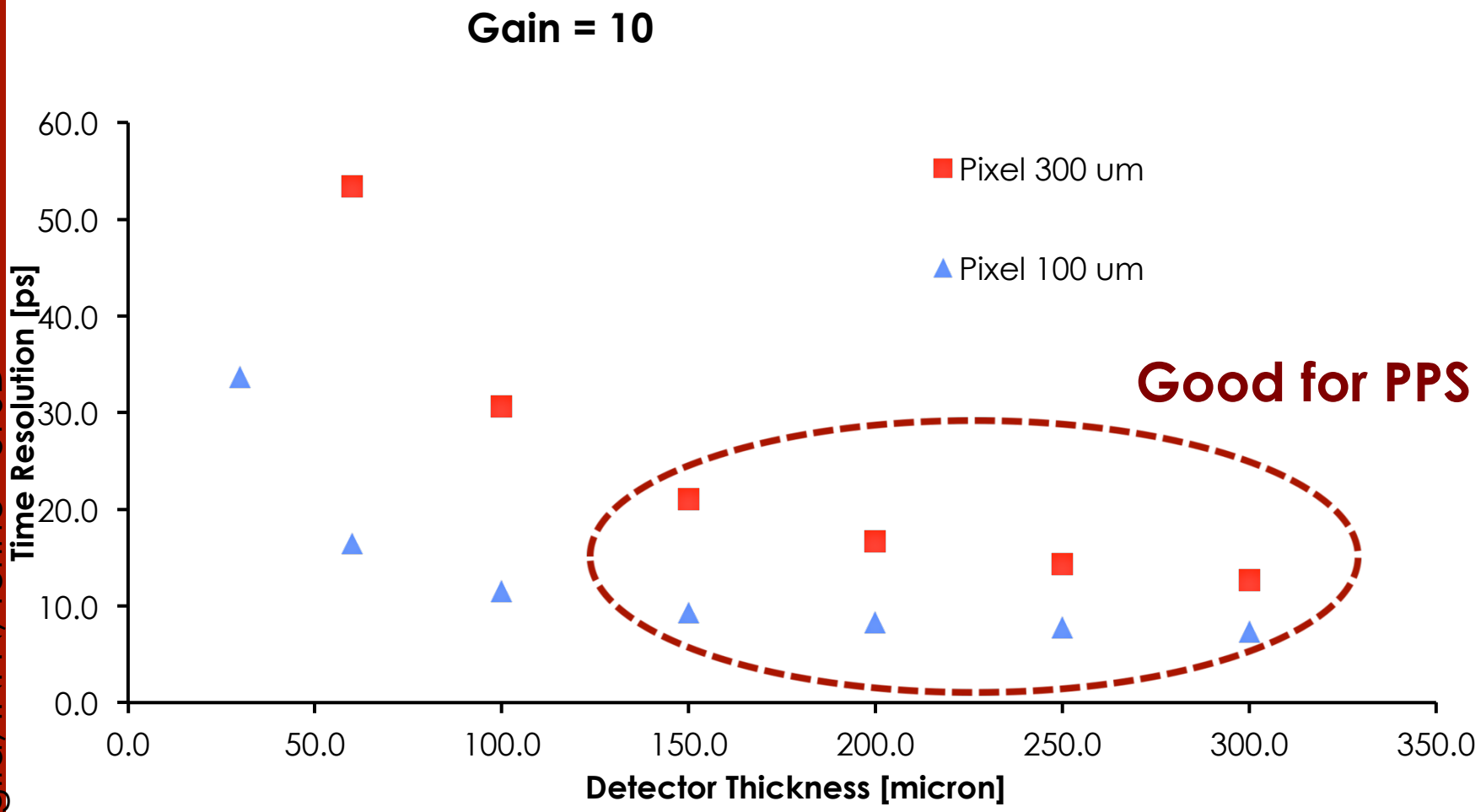


UFSD: Signal-to-Noise



UFSD offers an excellent S/N ratio even with very thin detectors

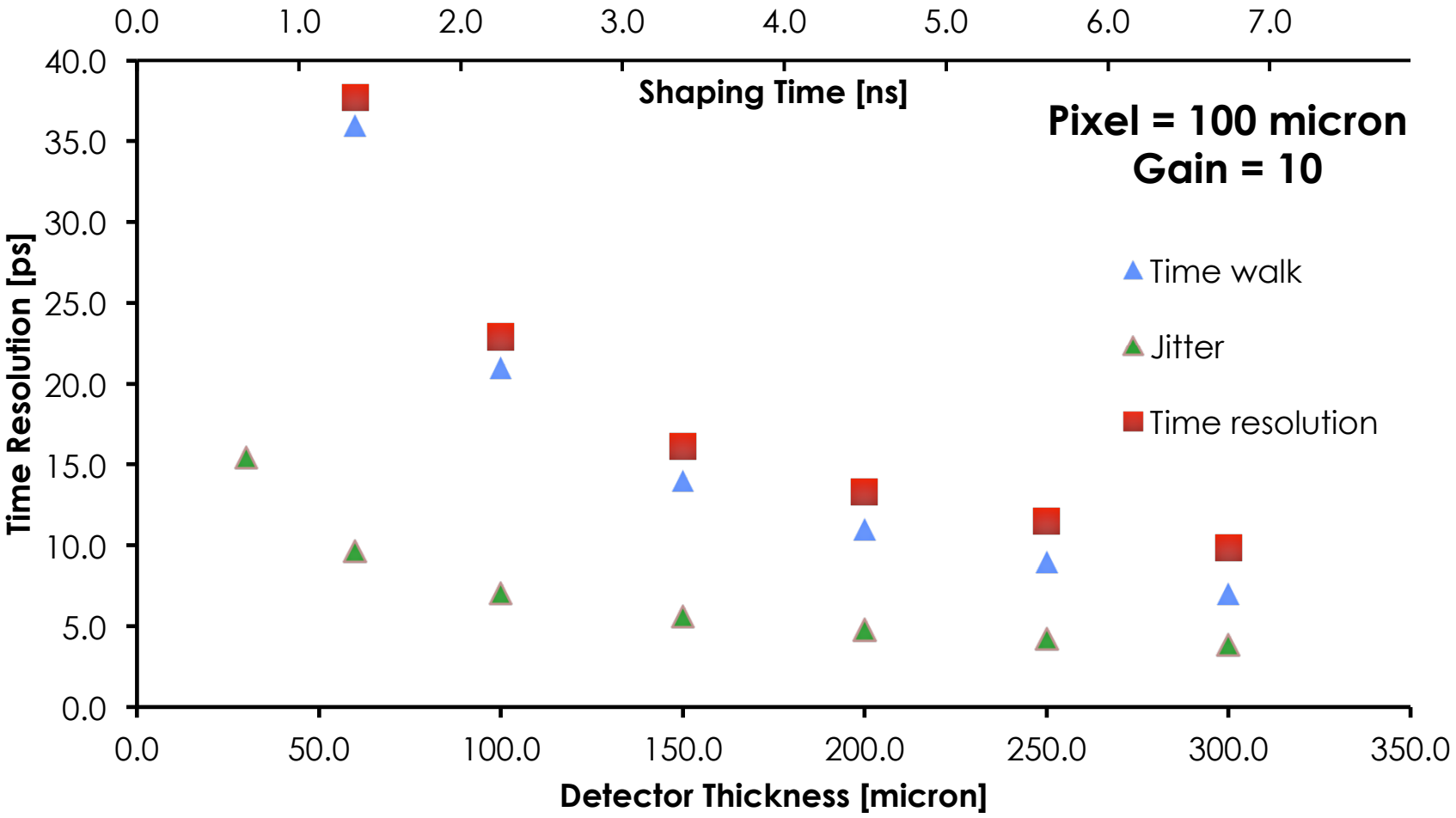
Resolution for 100 and 300 μm pixel



Excellent time resolution requires **thicker detectors**

Nicolo Cartiglia, INFN, Torino - UFSD

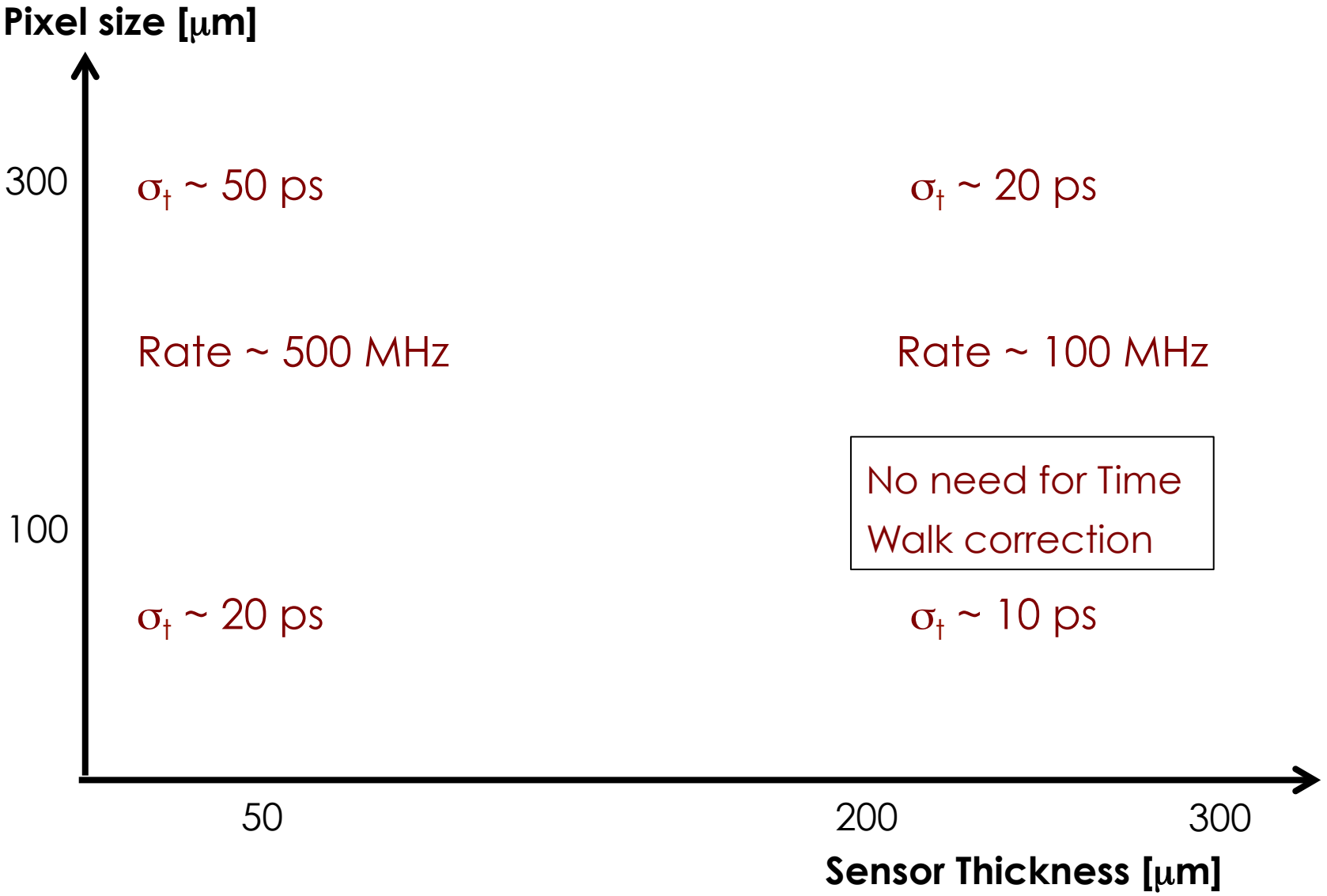
No Time Walk Correction



Excellent timing resolution even **without Time Walk correction**

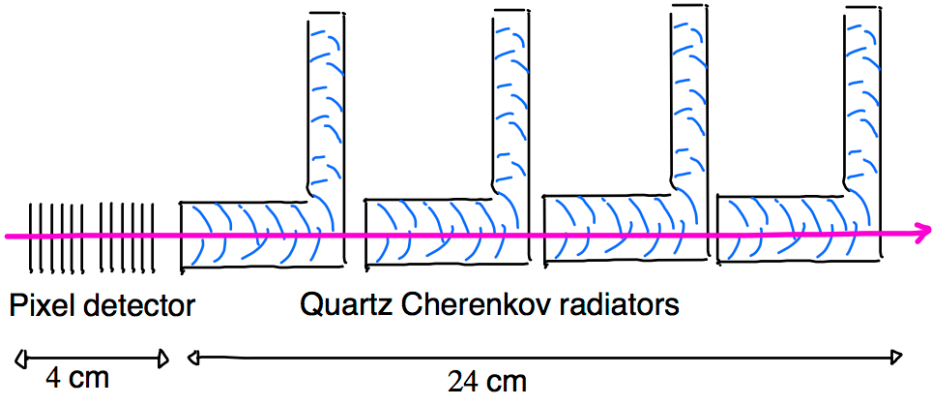
➔ Much simpler electronics

UFSD - Summary

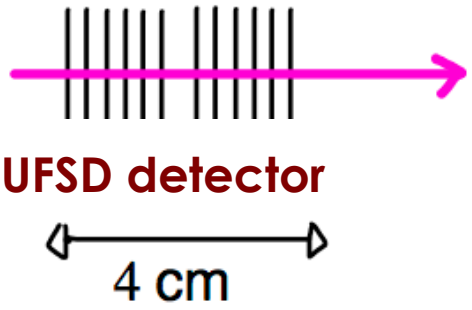


Conclusion

Pixel + Quartic



UFSD:
one sinale device



$$\sigma_T = \frac{30\,ps}{\sqrt{4}}$$

$$\sigma_T = \frac{20\,ps}{\sqrt{12}}$$

1. Silicon detector with gain of ~ 10 are well suited for combining excellent position and timing resolution
2. First prototype very promising

Back - up

What is the best shaping time (t_{rise}) ?

$$N \propto \frac{C_{Det}}{\sqrt{t_{rise}}}$$

$$S \propto \begin{cases} t_{rise} \xrightarrow{if} t_{rise} \le t_{col} \\ Const \xrightarrow{if} t_{rise} > t_{col} \end{cases}$$

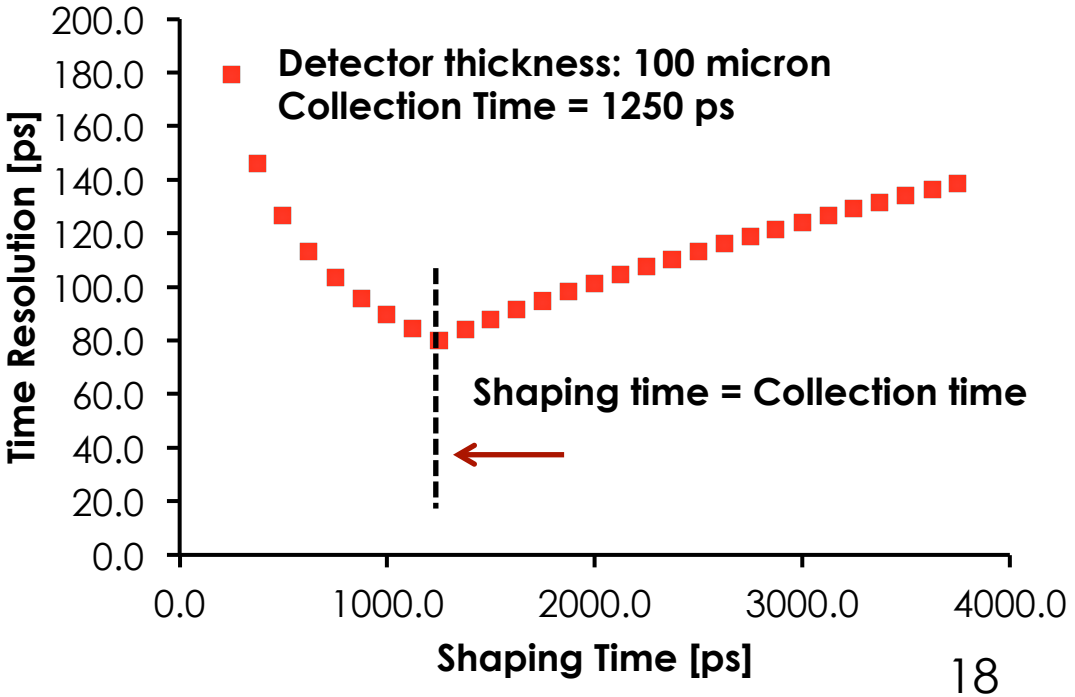
$$V_{th} \propto N$$

$$\Rightarrow \sigma_t \propto \begin{cases} \frac{C_{\det}}{\sqrt{t_{rise}}} \xrightarrow{if} t_{rise} \le t_{col} \\ C_{\det} * \sqrt{t_{rise}} \xrightarrow{if} t_{rise} > t_{col} \end{cases}$$

To minimize time resolution:

$$t_{rise} \sim t_{col}$$

Note: This value also minimizes fake signals in neighboring pixels.

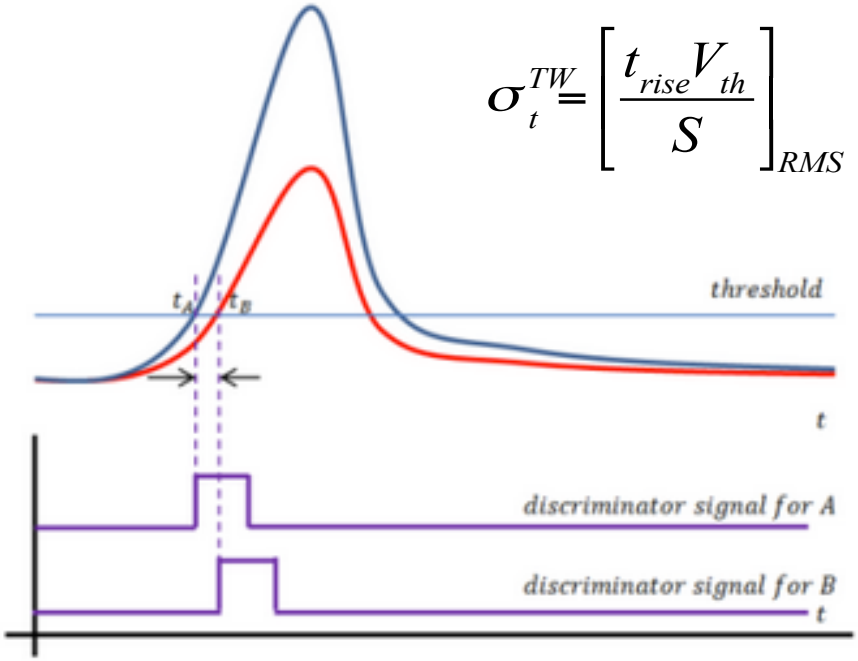


Time walk and Time jitter

Time walk: the voltage value Vo is reached at different time for signal of different amplitudes

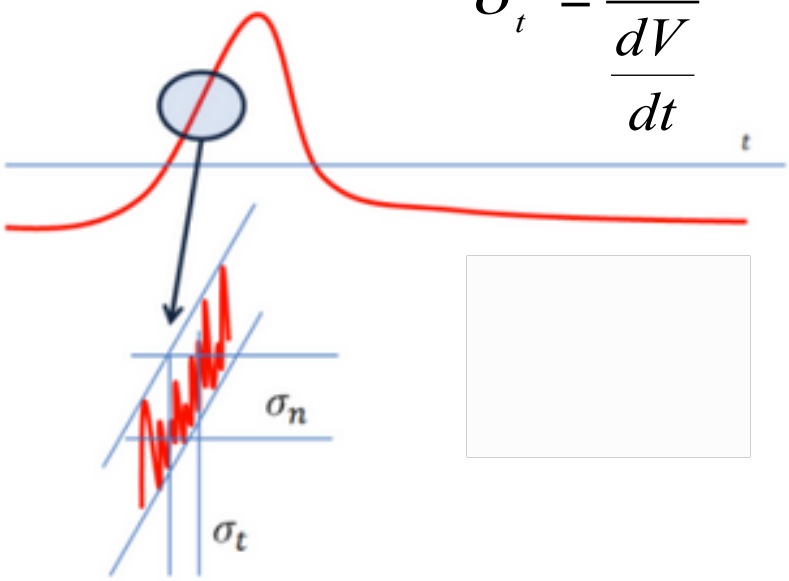
Jitter: the noise is summed to the signal, causing amplitude variations

$$\sigma_t^{TW} = \left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}$$



Time walk effect

$$\sigma_t^J = \frac{N}{\frac{dV}{dt}}$$



Jitter effect

Due to the physics of signal formation

(see backup slides for full calculation and reduction techniques)

Mostly due to electronic noise

(see backup slides for capacitance and noise values used)