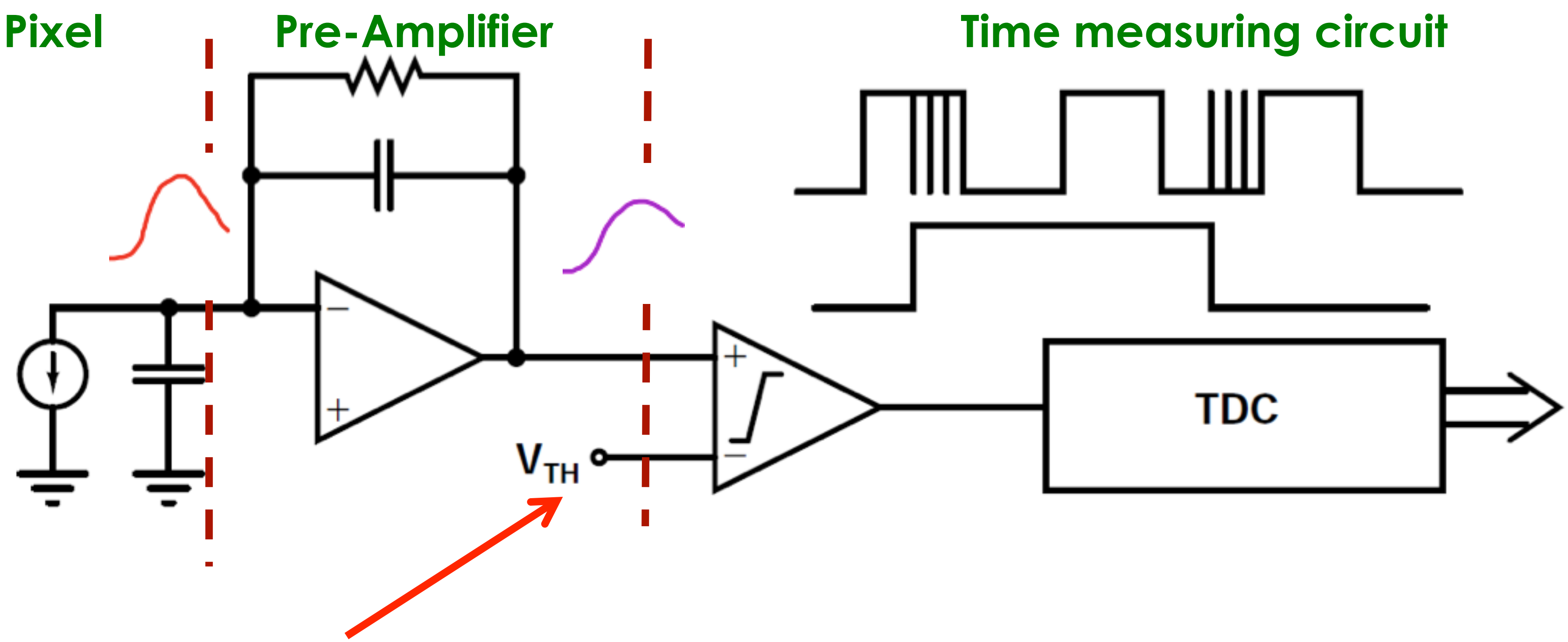
Timing capabilities of Ultra-Fast Silicon Detector

- A parameterization of time resolution
- A program to calculate Time resolution
- UFSD Timing capabilities
- How to measure Time resolution

Nicolo Cartiglia

With
F. Cenna, F. Marchetto, A. Picerno F. Ravera, H. Sadrozinski, A. Seiden, A. Solano, A. Vinattieri, N. Spencer, A. Zatserklyaniy

UFSD: a time-tagging detector



Time is set when the signal crosses the comparator threshold

The timing capabilities are determined by the characteristics of the signal at the output of the pre-Amplifier and by the TDC binning:

$$\sigma_{Total}^2 = \sigma_{Jitter}^2 + \sigma_{Time\ Walk}^2 + \sigma_{TDC}^2$$

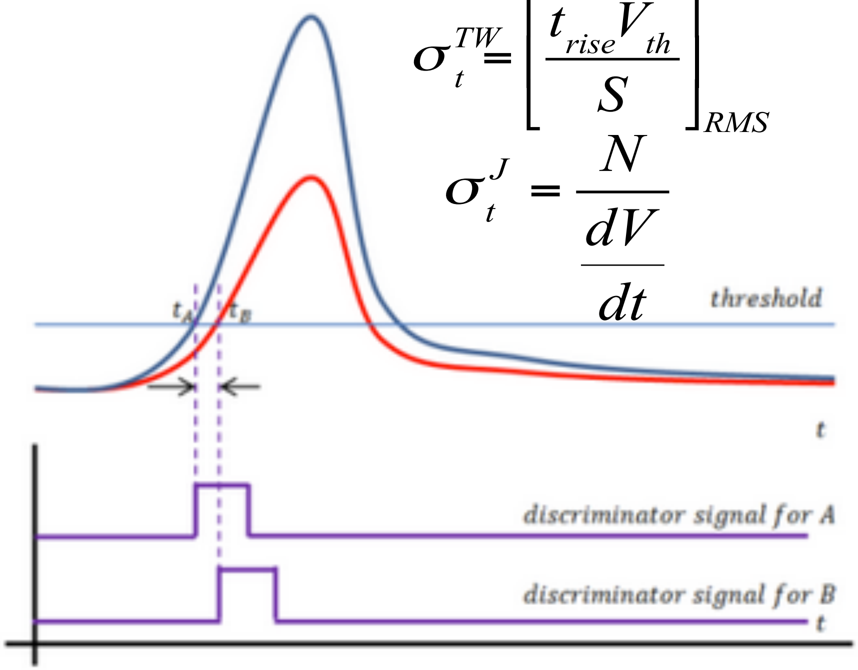
Time walk and Time jitter

Time walk: the voltage value Vo is reached at different time for signal of different amplitudes

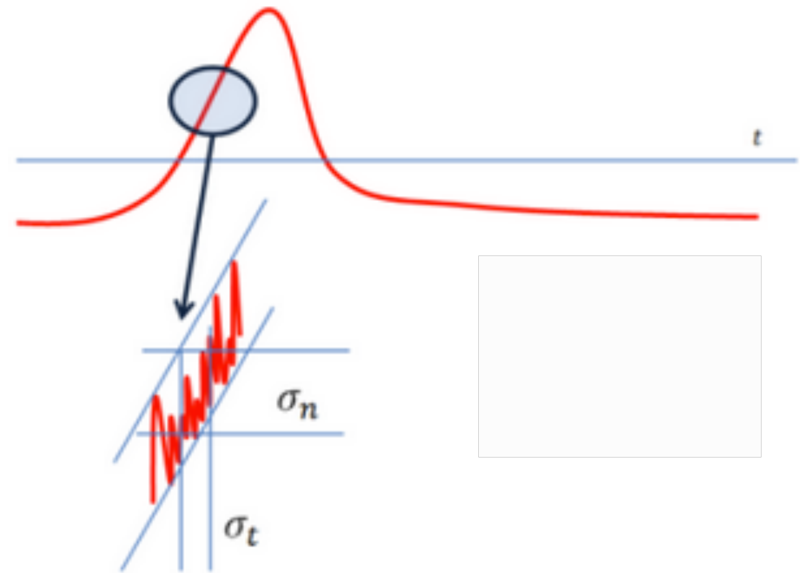
Jitter: the noise is summed to the signal, causing amplitude variations

$$\sigma_t^{TW} = \left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}$$

$$\sigma_t^{J} = \frac{N}{\frac{dV}{dt}}$$



Time walk effect



Jitter effect

Due to the physics of signal formation

(see backup slides for full calculation and reduction techniques)

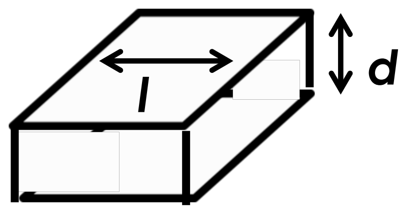
Mostly due to electronic noise

(see backup slides for capacitance and noise values used)

A parameterization of σ$_t$

$$\sigma_t^2 = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2 \quad (1)$$

Jitter — Time Walk — TDC



d: detector thickness [micron]

l: pitch [micron]

C: Detector capacitance [fF]
Depends on the pitch and thickness

$$C_{Det} = \varepsilon\varepsilon_o \frac{l*l}{d} + 0.2*4l + 50$$

N: Noise at preamp.
Dominated by the voltage term

$$N \propto \frac{C_{Det}}{\sqrt{t_{rise}}}$$

S: Signal

t_{rise}: Pre-Amp Shaping time

V_{th}: Comparator threshold
Depends on the noise level

$$V_{th} = 10*N$$

TDC:Width of the TDC LSB [ps]

$$LSB = 20$$

What is the best shaping time (t_{rise}) ?

$$N \propto \frac{C_{Det}}{\sqrt{t_{rise}}}$$

$$S \propto \begin{cases} t_{rise} \xrightarrow{if} t_{rise} \le t_{col} \\ Const \xrightarrow{if} t_{rise} > t_{col} \end{cases}$$

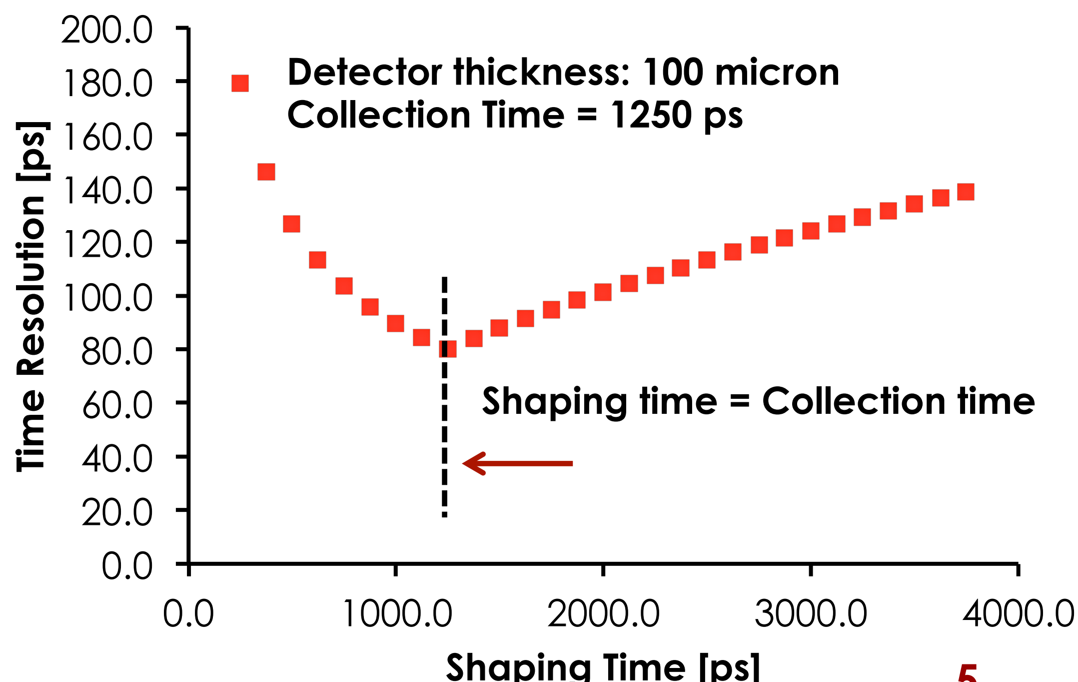
$$V_{th} \propto N$$

$$\Rightarrow \sigma_t \propto \begin{cases} \frac{C_{det}}{\sqrt{t_{rise}}} \xrightarrow{if} t_{rise} \le t_{col} \\ C_{det} * \sqrt{t_{rise}} \xrightarrow{if} t_{rise} > t_{col} \end{cases}$$

To minimize time resolution:

$$t_{rise} \sim t_{col}$$

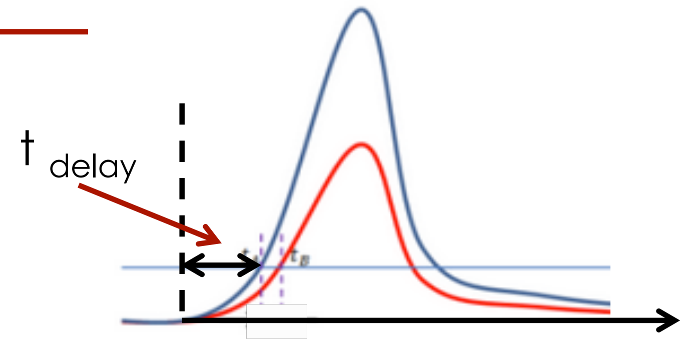
Note: This value also minimizes fake signals in neighboring pixels.



Time walk

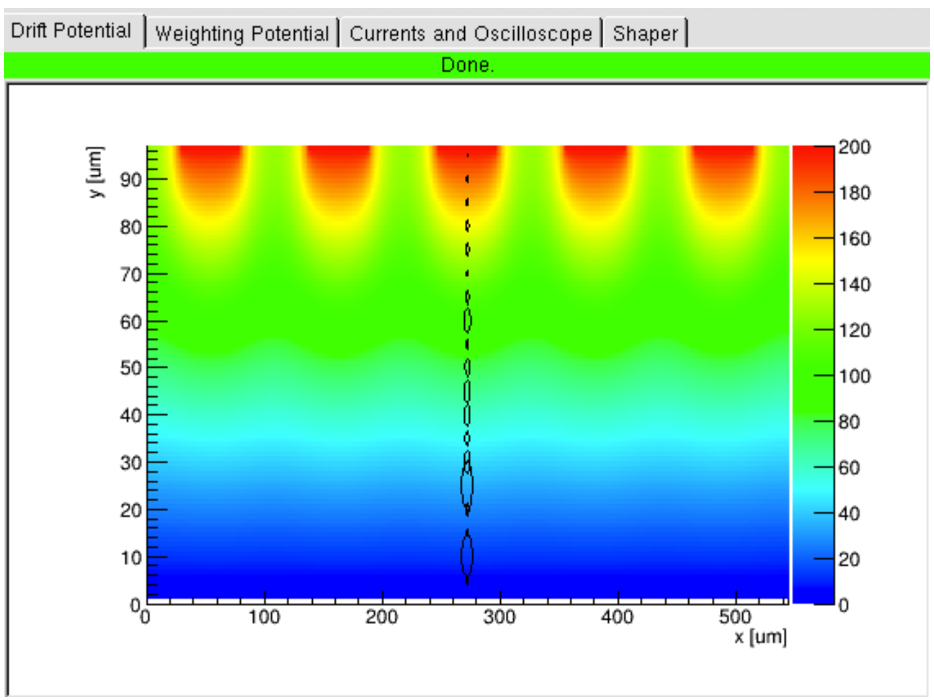
Signals cross a given threshold with a delay that depends on their amplitude, on the rise time and on the value of the threshold:

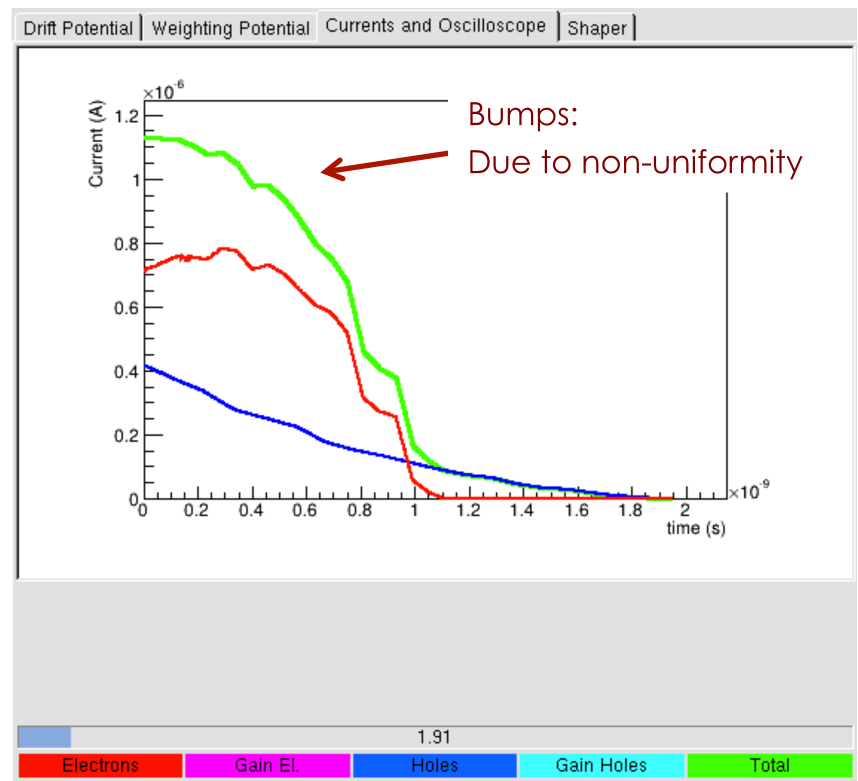
$$t_{delay} = t_{rise} \frac{V_{th}}{V}$$



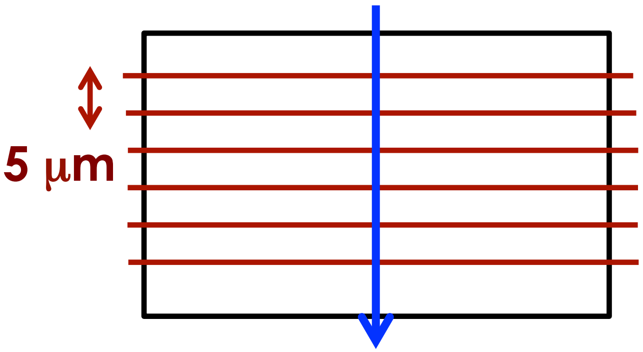
Time walk has 2 different source:

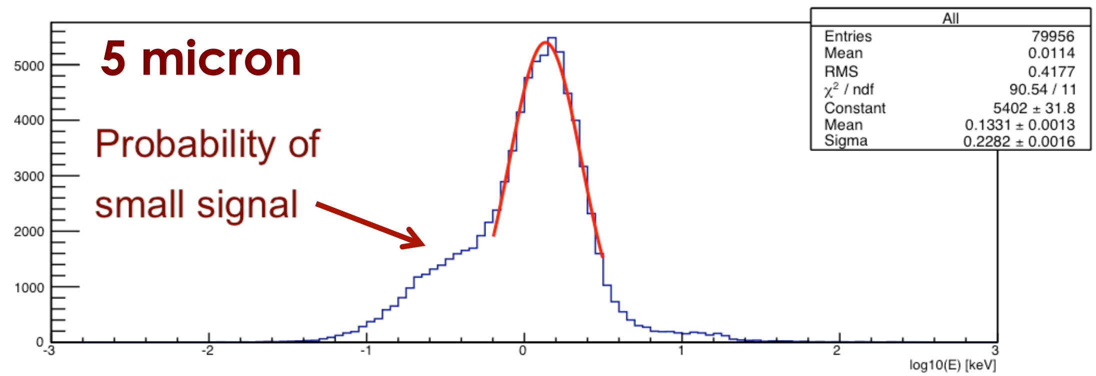
1. Amplitude variation (Landau distributed)
2. Non-uniformity charge deposition





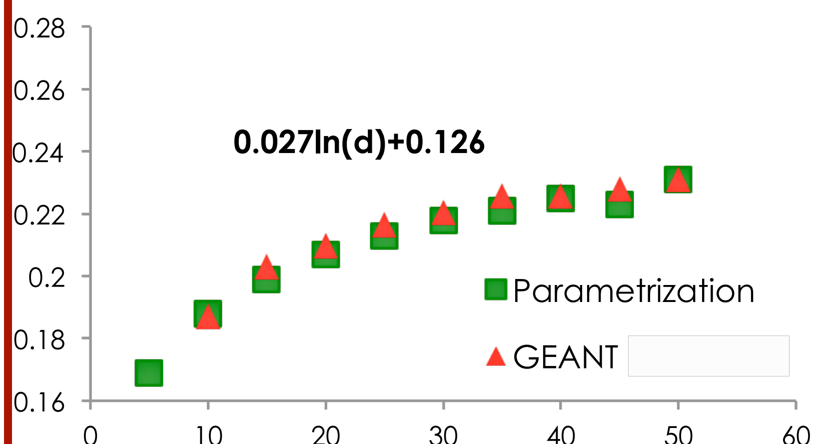
Aside: Non-Uniform Energy deposition

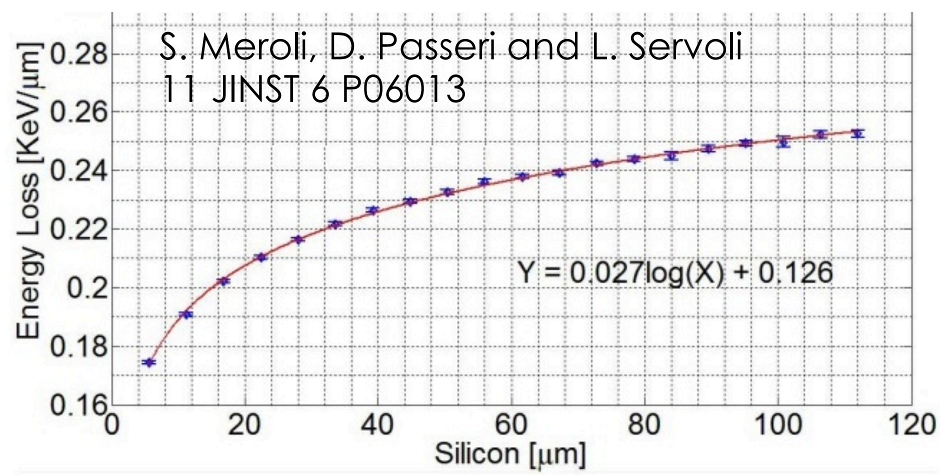




We have created, using GEANT4, a library of the energy depositions of a MIP in silicon, every 5 micron. Using this library, we can predict the value in any thickness

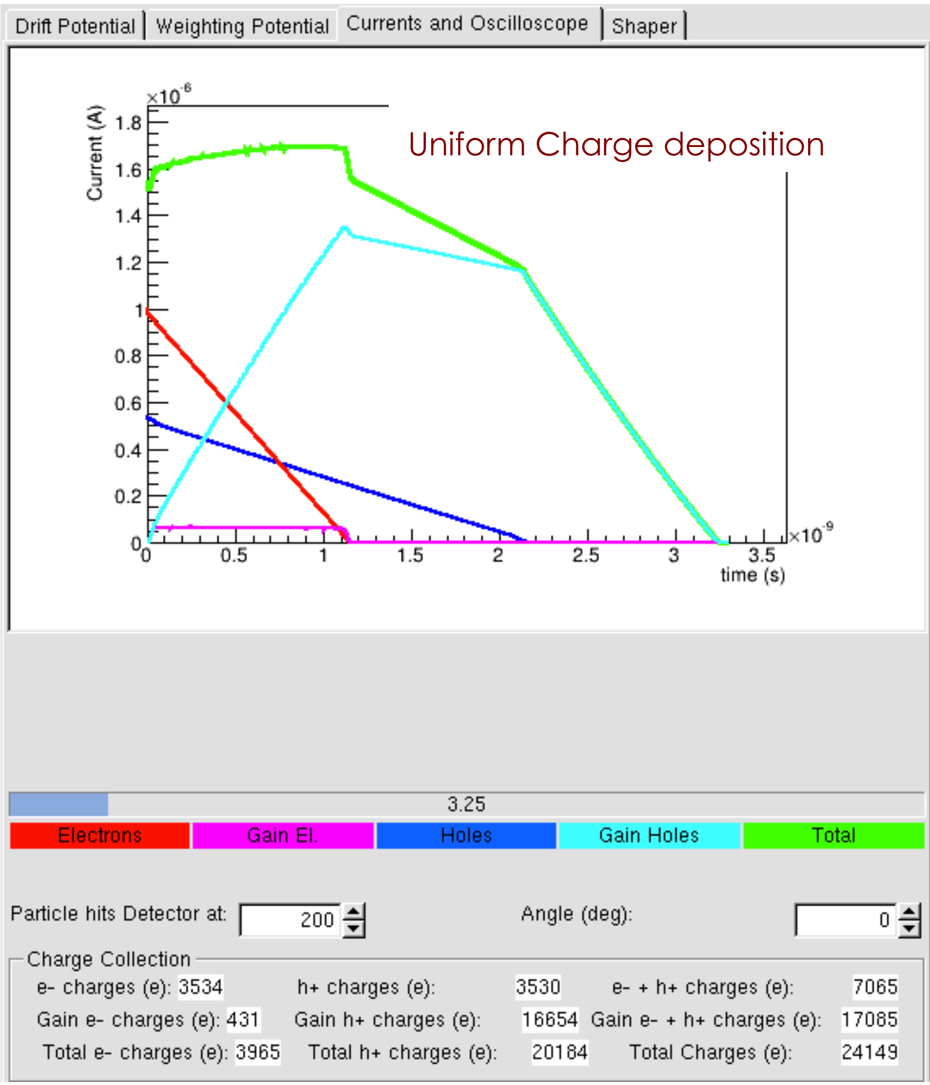
Comparison with the measurement presented in 2011 JINST 6 P06013

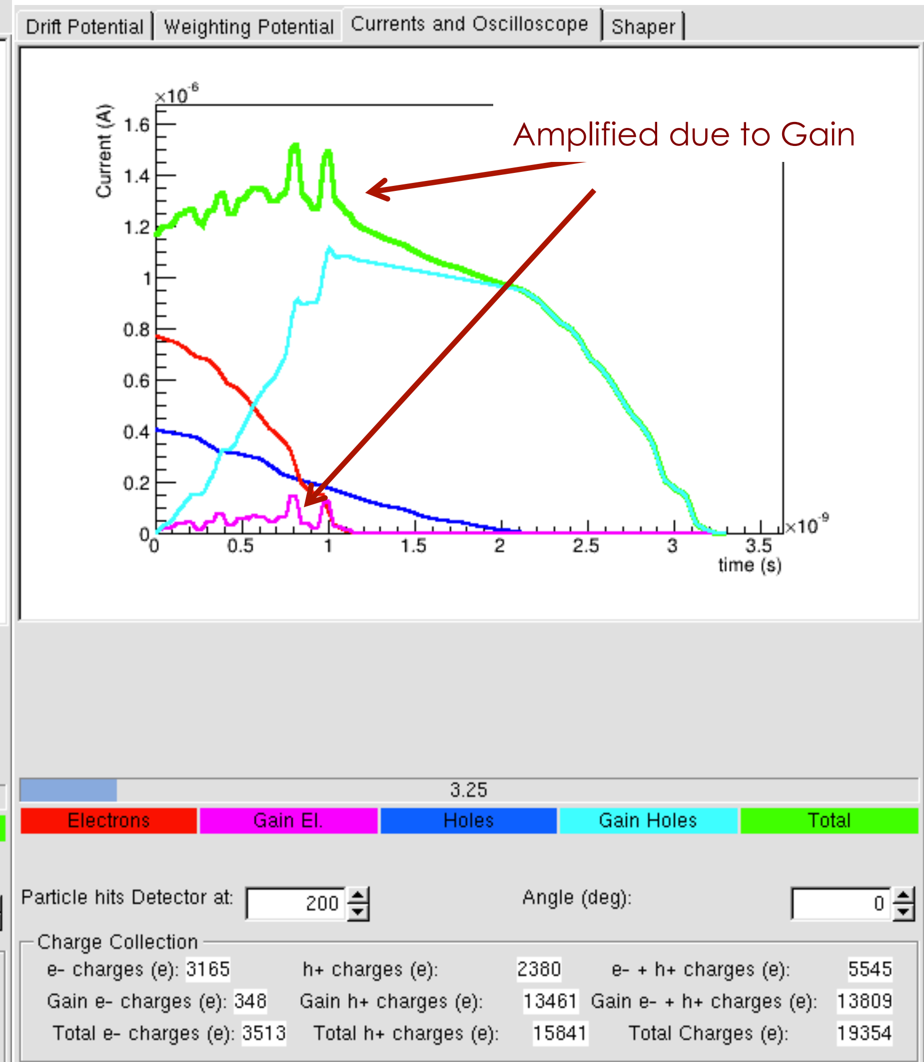




Time walk and Gain

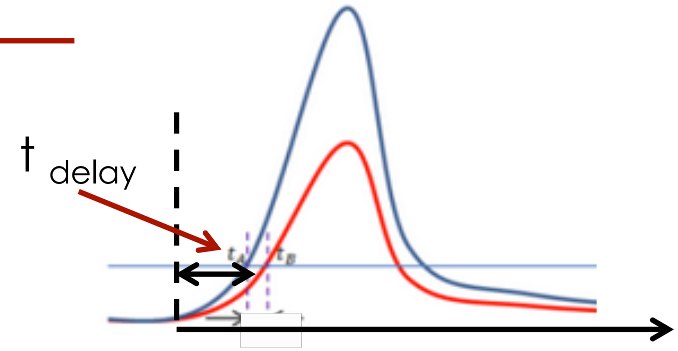
Unfortunately gain enhances the non-uniformity of charge deposition:
MIP, 100 micron detector, without and with gain (g ~ 4)





Time walk Calculation

1) We use Weigthfield to generate a lot of events in any given geometry:

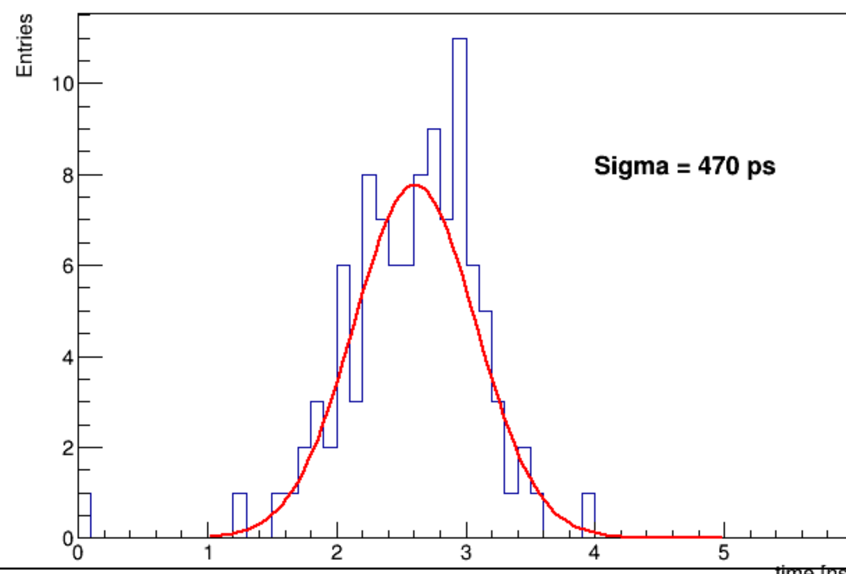


2) We simulate a shaper with t_rise = t_collection

3) We calculate the time when the signal crosses 10*Noise

t_delay = t(Vout = 10 Noise)

4) The time walk is the RMS of the t_c



Example:

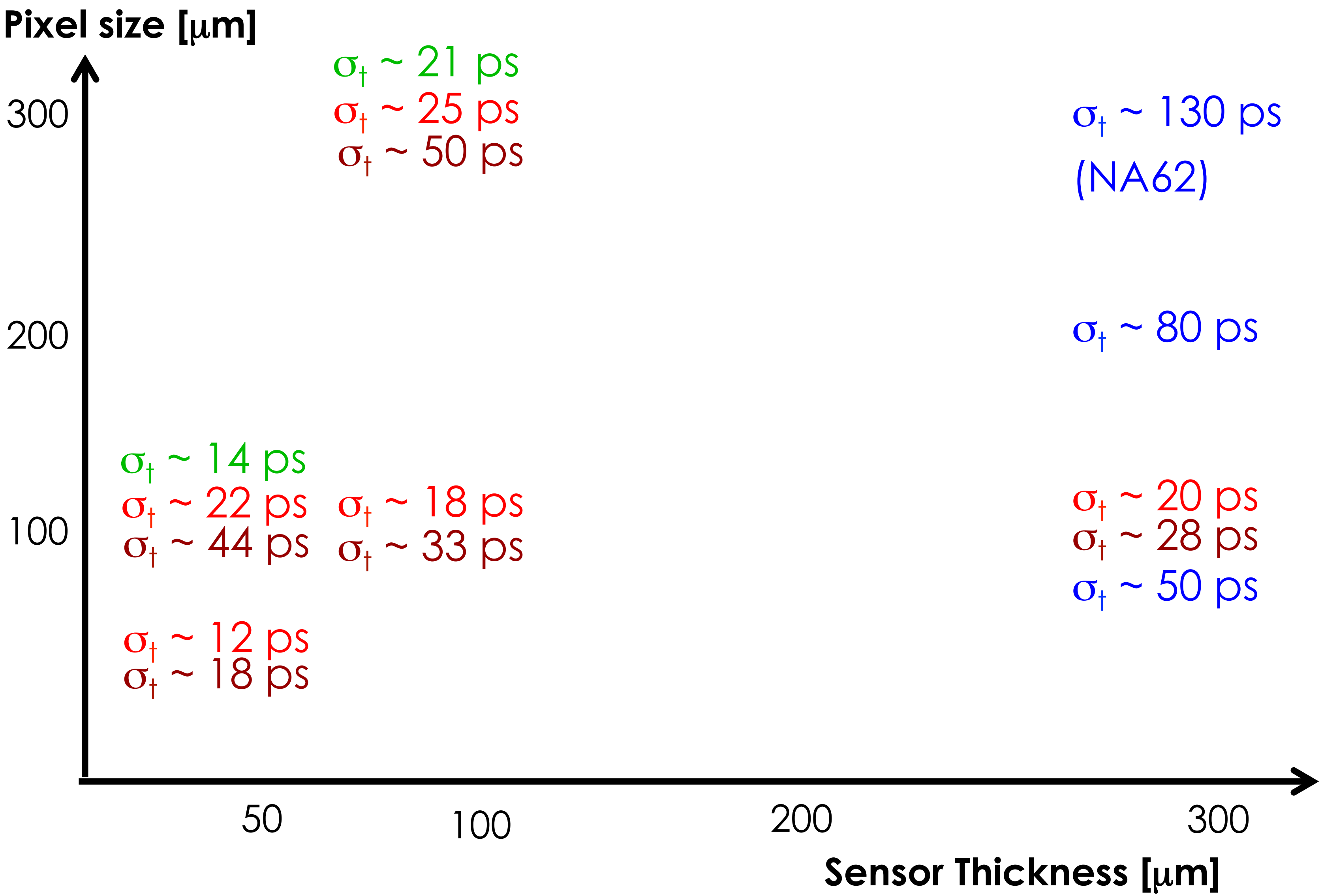
200 micron pixel

300 micron thick

TW = 470 ps

The electronics reduces time walk by compensating circuits (CFD, ToT). In the following we assume a reduction of 10

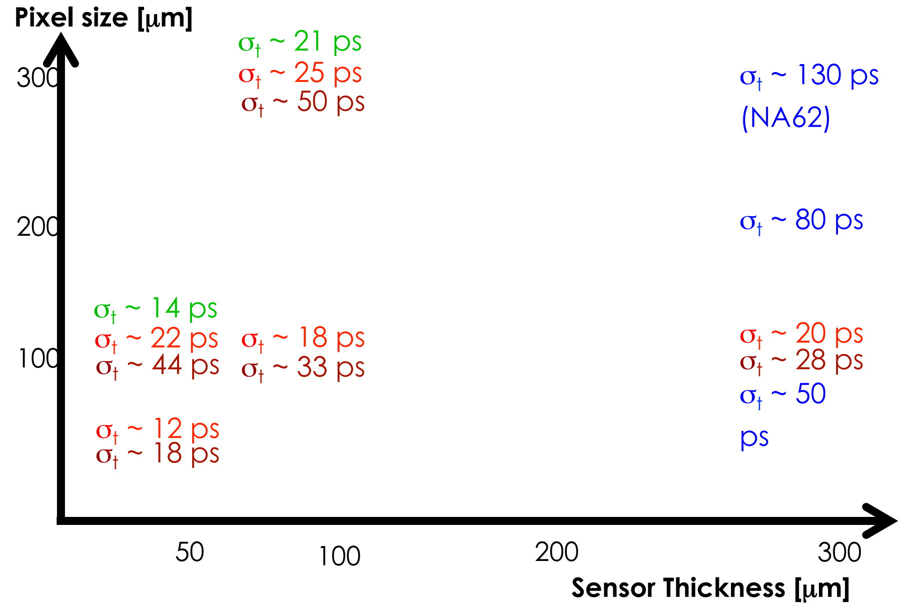
UFSD – Timing Capability



No Gain   Gain = 4   Gain = 10   Gain = 15

A plan to measure UFSD – Timing Capability

Non uniform charge deposition dominates the time resolution when we go below 50 ps



Is this true?

We need to validate this model

The road ahead:

- Have detector of different thicknesses
- Have detector with different gains
- Have dedicated very low noise electronics
- Sample the waveform per event, compare to average

UFSD – Summary

We are just starting to understand the timing capability of UFSD

We developed a program, **Weightfield2.0**, that seems to be able to predict the major feature of the problem.
(available at http://personalpages.to.infn.it/~cartigli/Weightfield2.0/)

Gain is the key to excellent timing, however it exacerbates the effect of non uniform charge deposition.

We need to measure the signal "bumpiness" of the output signal: detector production is ahead of electronics characterization. We need to invest in this aspect.

10 ps looks really difficult, 20 ps looks 1/4 as difficult, 30 ps 1/9 …