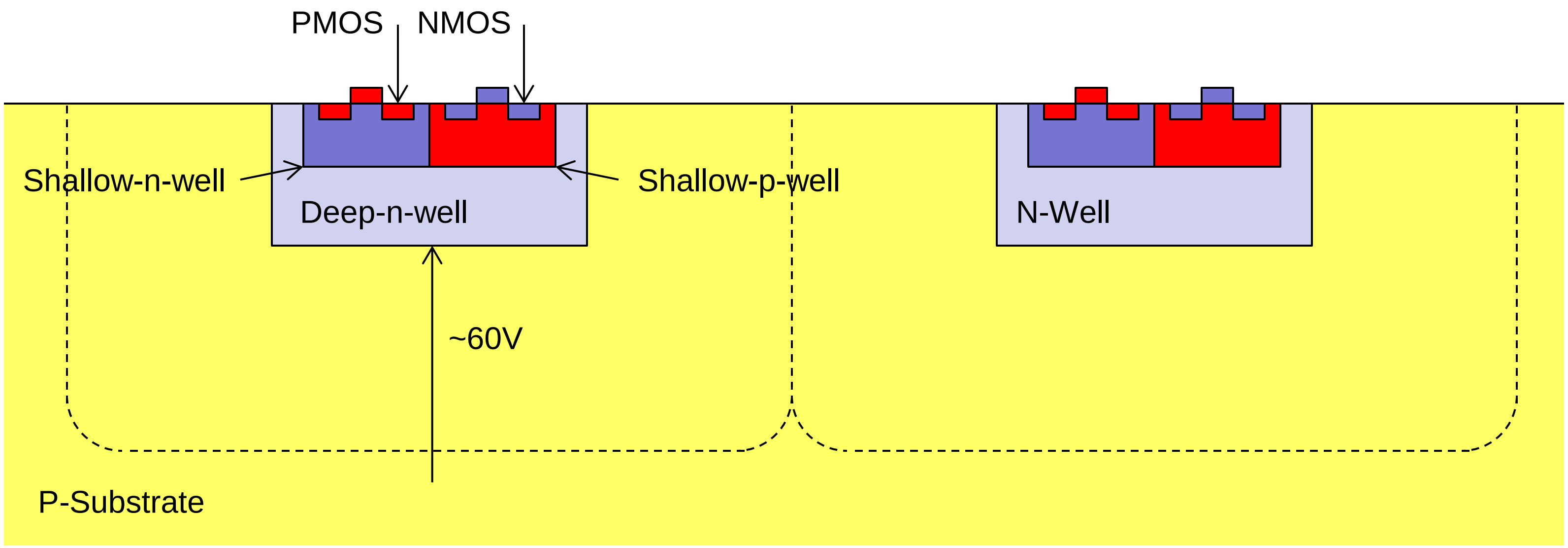
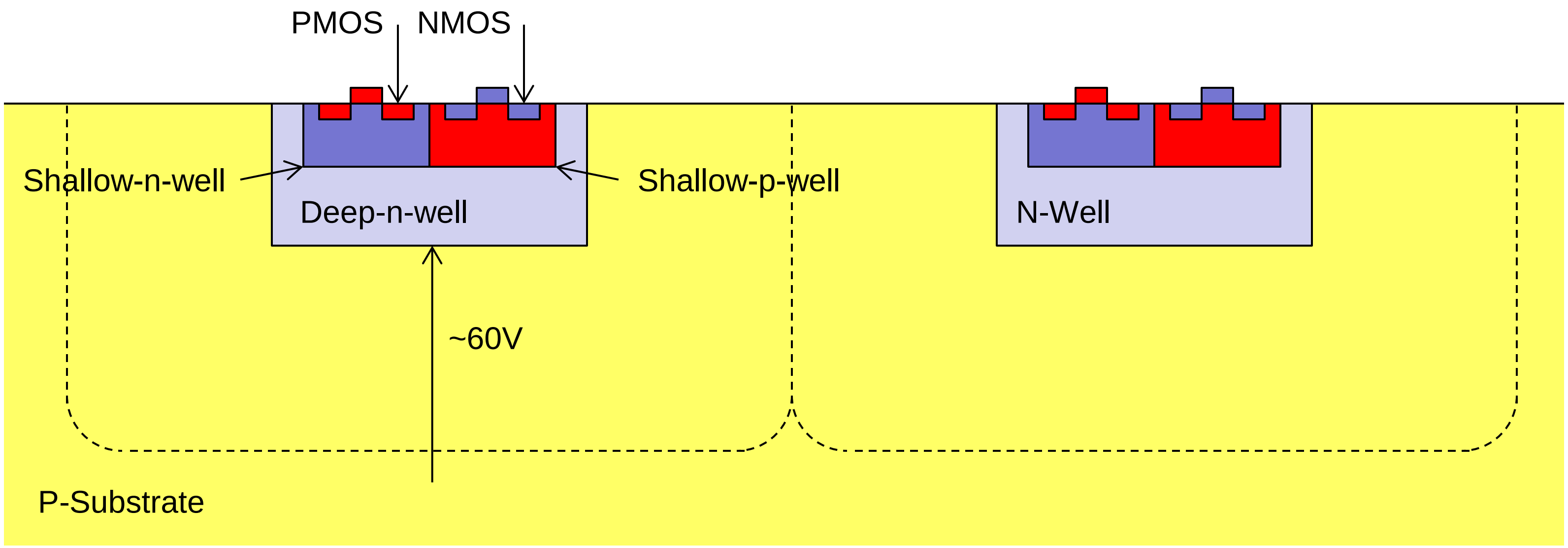
HV-CMOS Overview

Ivan Peric

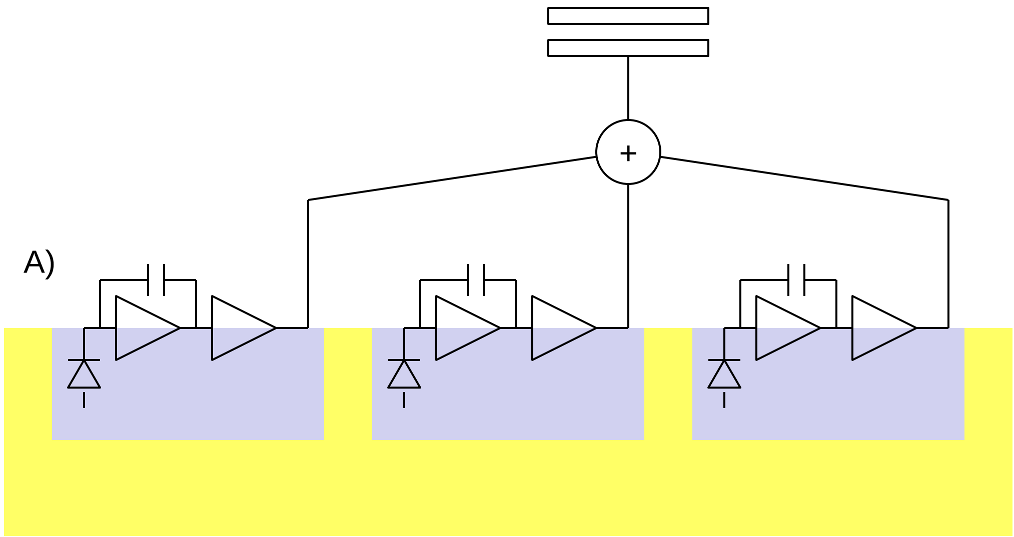
- Ideas:
- Use the standard (HV)CMOS technologies to implement particle detectors
- Use a high voltage to deplete the sensor volume – charge collection by drift
- Original implementation: CMOS electronics inside the deep n-well-collecting electrode
- “Smart diode”

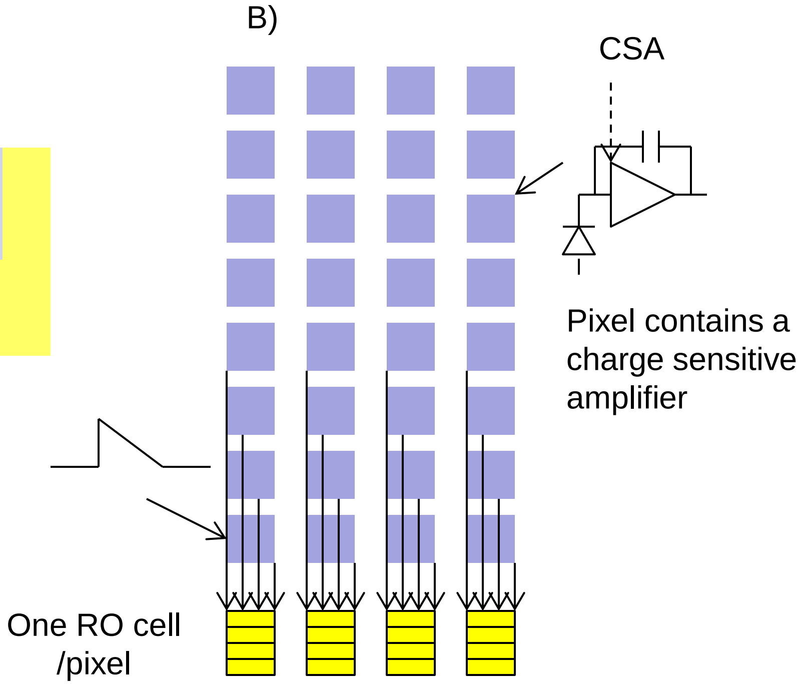


- Some drawbacks:
- The standard substrates are relatively low resistive (~20 Ωcm)
- The depleted region is up to ~15 µm thick – MIP signals are relatively weak ~ 1800 e
- The collection electrode is, at the same time, the PMOS bulk – there is a strong capacitive crosstalk from PMOS transistors to the detector input.
- General drawback of monolithic sensors: Complex in-pixel electronics leads to increased detector capacitance or to decreased electrode-/pixel-size ratio

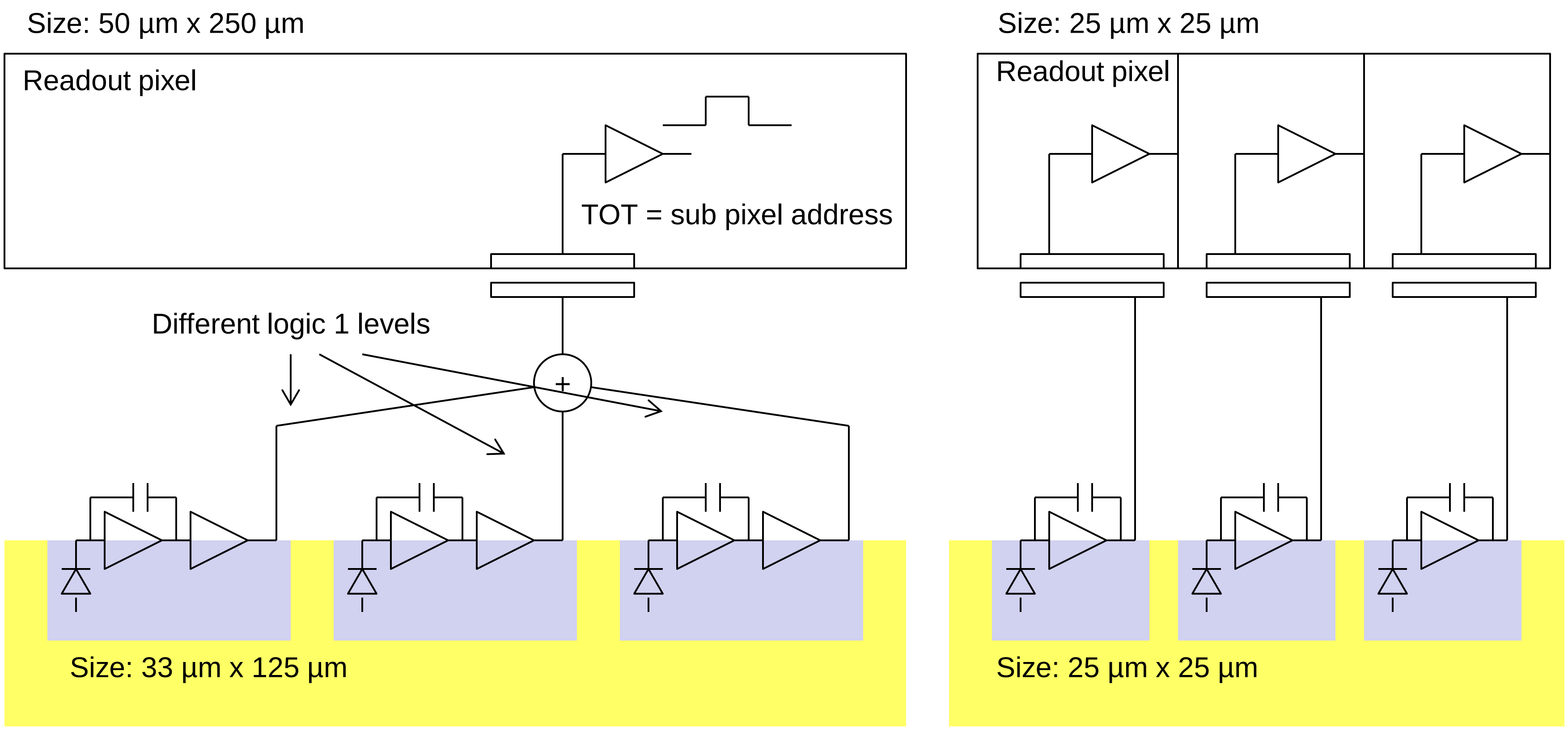


- We investigate two detector structures:
- A) Hybrid detector with a “smart” HVCMOS sensor and capacitive signal transmission to the readout ASIC (capacitively coupled pixel sensor - CCPD)
- B) Monolithic pixel detector with digital signal processing on the chip periphery



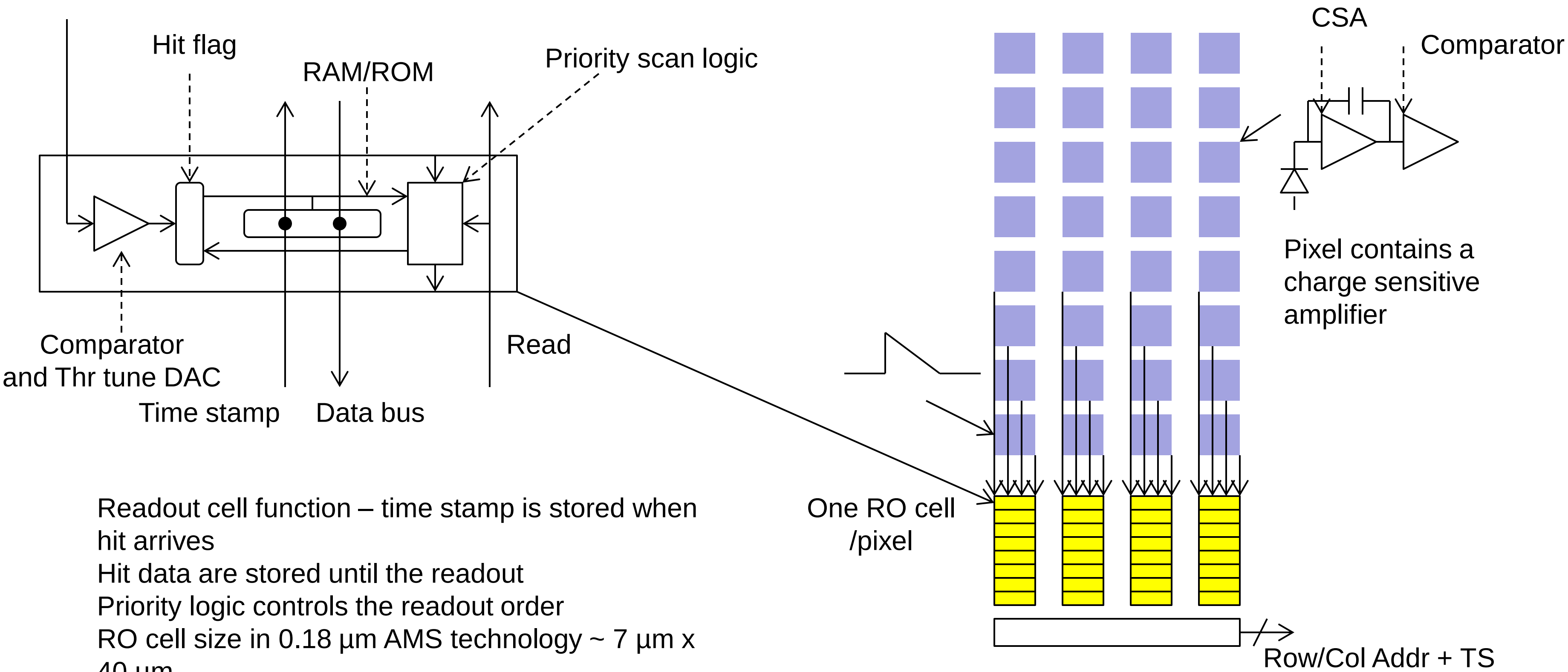


- CCPD
- ATLAS-pixel “style”: digital outputs of three pixels are multiplexed to one pixel readout cell
- HVCMOS pixel contains an amplifier and a comparator
- CLIC “style”: every HVCMOS pixel has its own readout cell
- HVCMOS pixel contains only an amplifier



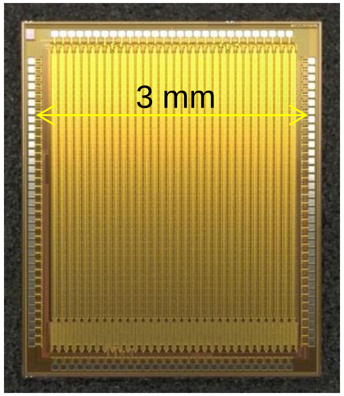
Monolithic HVCMOS pixel sensor for Mu3e experiment

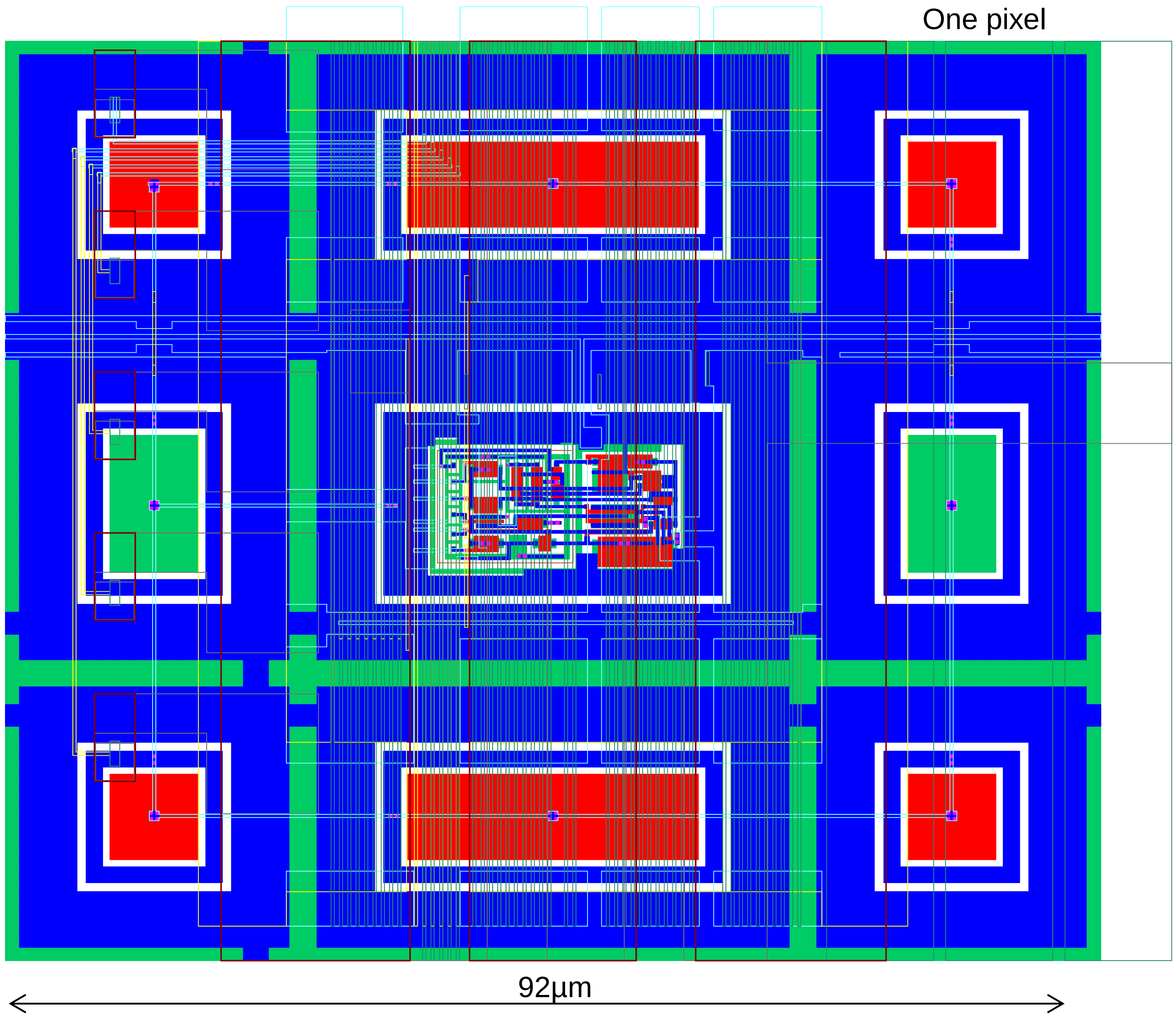
Concept: Every pixel has its own readout cell, placed on the chip periphery

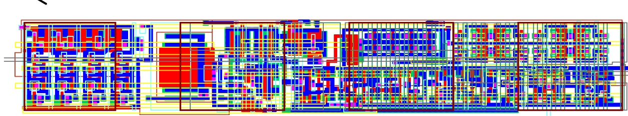


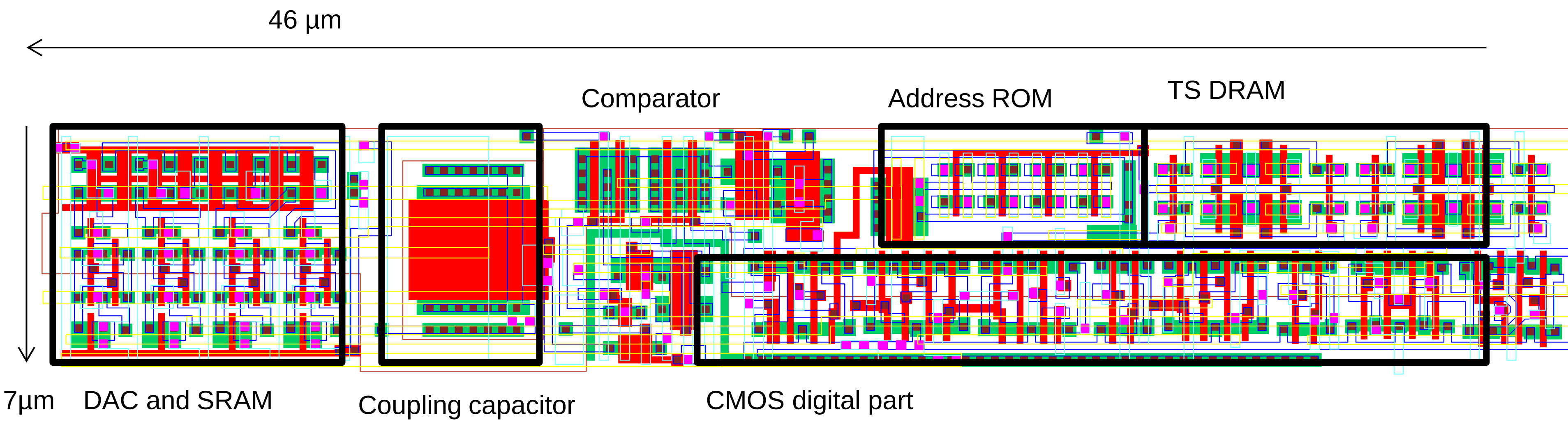
Readout cell function – time stamp is stored when hit arrives
Hit data are stored until the readout
Priority logic controls the readout order
RO cell size in 0.18 µm AMS technology ~ 7 µm x 40 µm
(with comparator and threshold-tune DAC)

Monolithic HVCMOS pixel sensor for Mu3e experiment

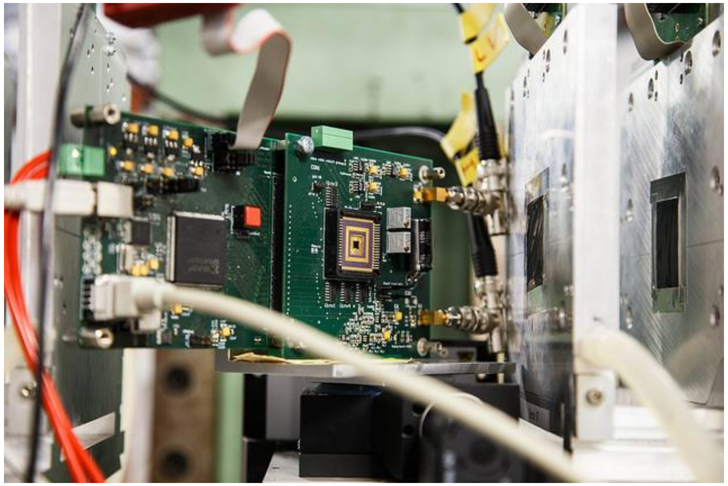


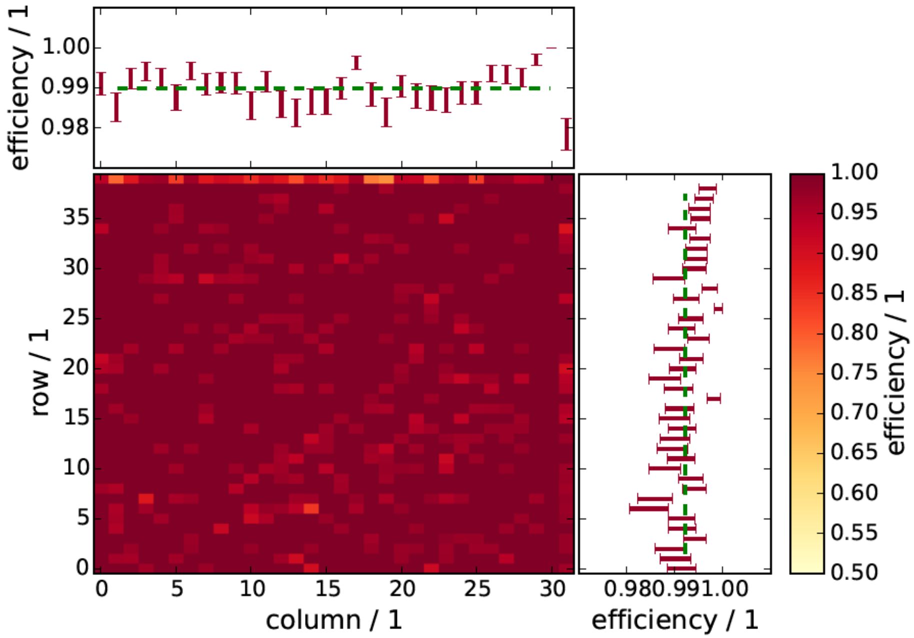


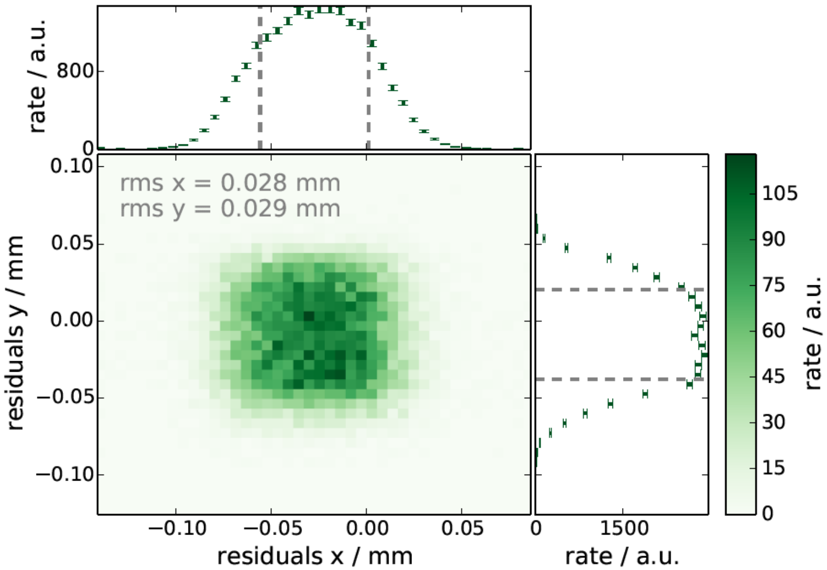



46 µm
Comparator
Address ROM
TS DRAM
7µm
DAC and SRAM
Coupling capacitor
CMOS digital part

- Test-beam measurement February 2014 DESY
- Performed by our colleagues from Institute for Physics in Heidelberg
- Plots: Moritz Kiehn, Niklaus Berger







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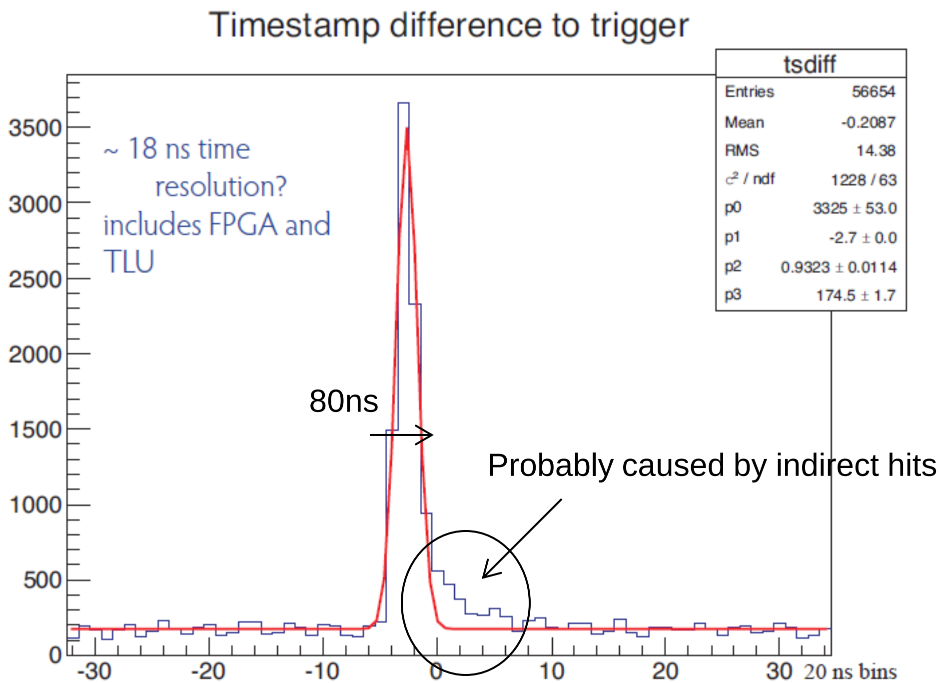
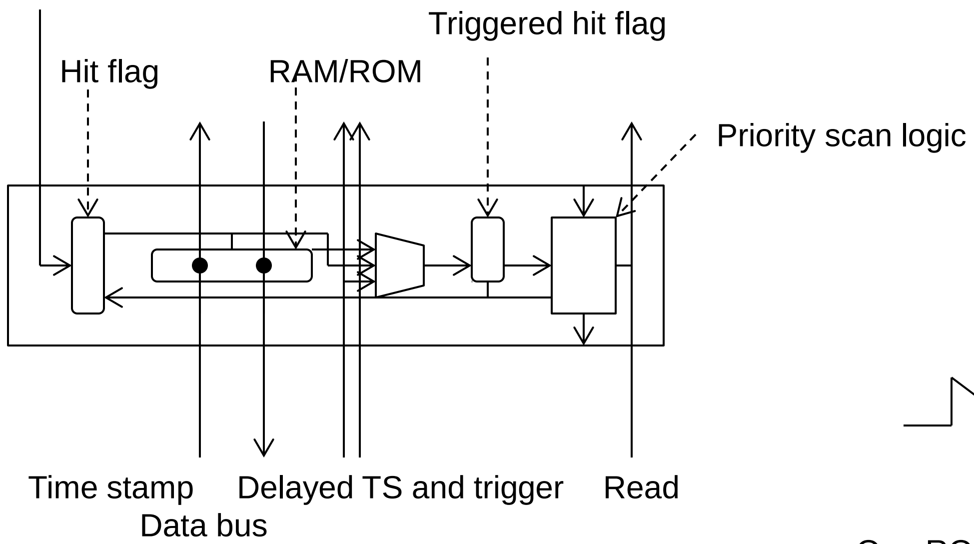
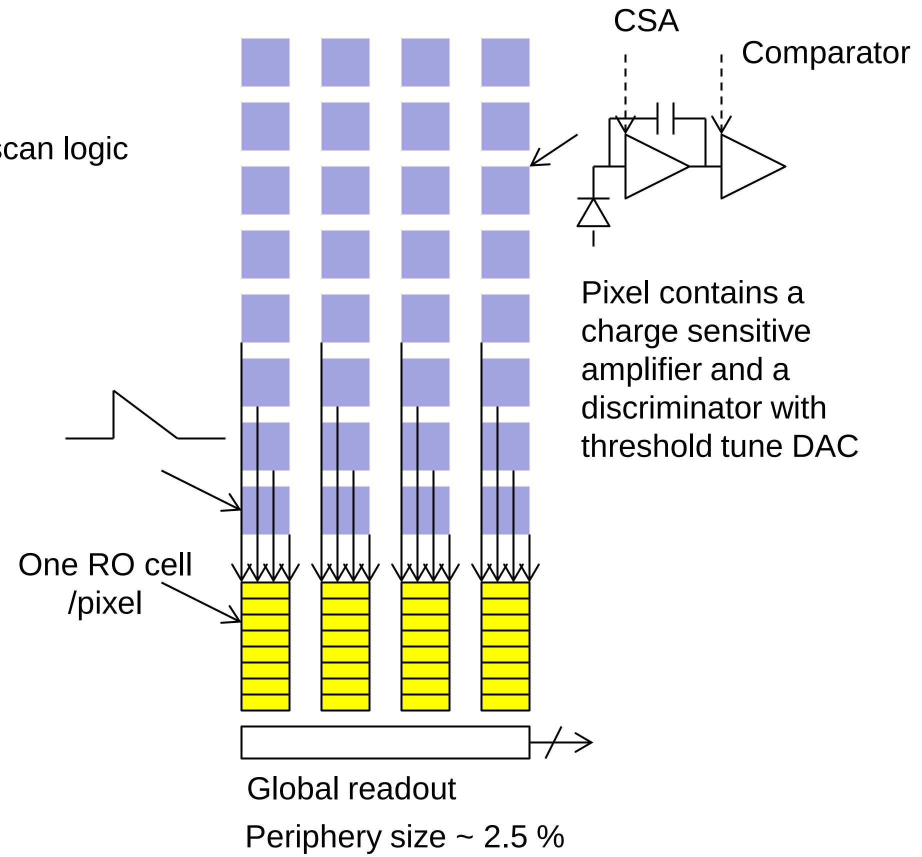


Concept: Every pixel has its own readout cell, placed on the chip periphery



Readout cell function – time stamp is stored when hit arrives
The stored time stamp is compared with the current time stamp
If trigger arrives with the correct latency, the triggered hit flag is set
Priority logic controls the readout order
Estimated cell size in 0.18 µm AMS technology without comparator ~ 7 µm x 50 µm
Example: Pixel size 50 µm x 250 µm
Chip size: ~ 2 cm x 2 cm
Number of pixels: 400 x 80
Size of periphery without comparator:
2 cm x 560 µm (~ 2.5%)



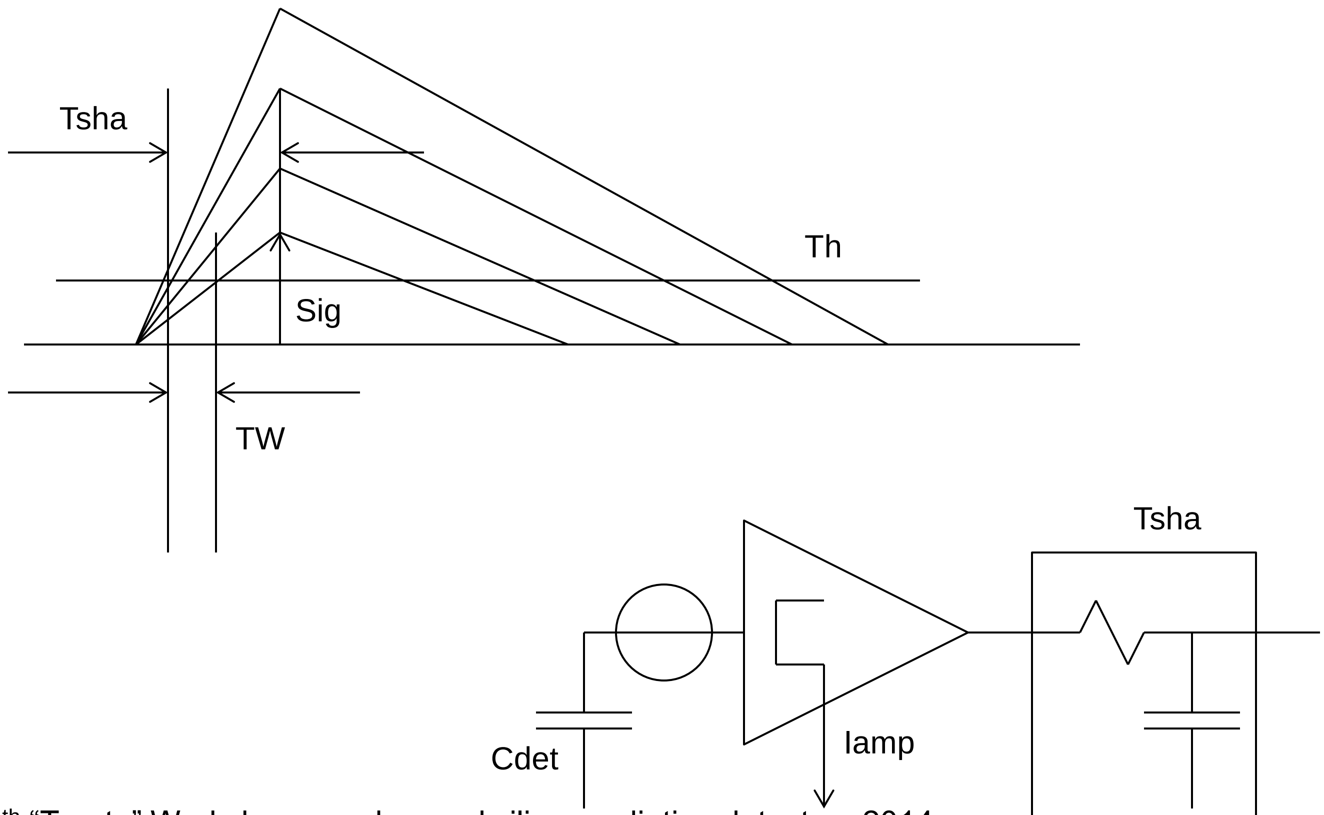
HVCMOS pixel sensor for ATLAS

Further steps

- We need to improve time walk
- We need to improve SNR of CCPDs for ATLAS, especially after irradiation
- Three strategies:
- 1) optimize present design
- 2) invent more clever electronics
- 3) improve the detector structure and technology

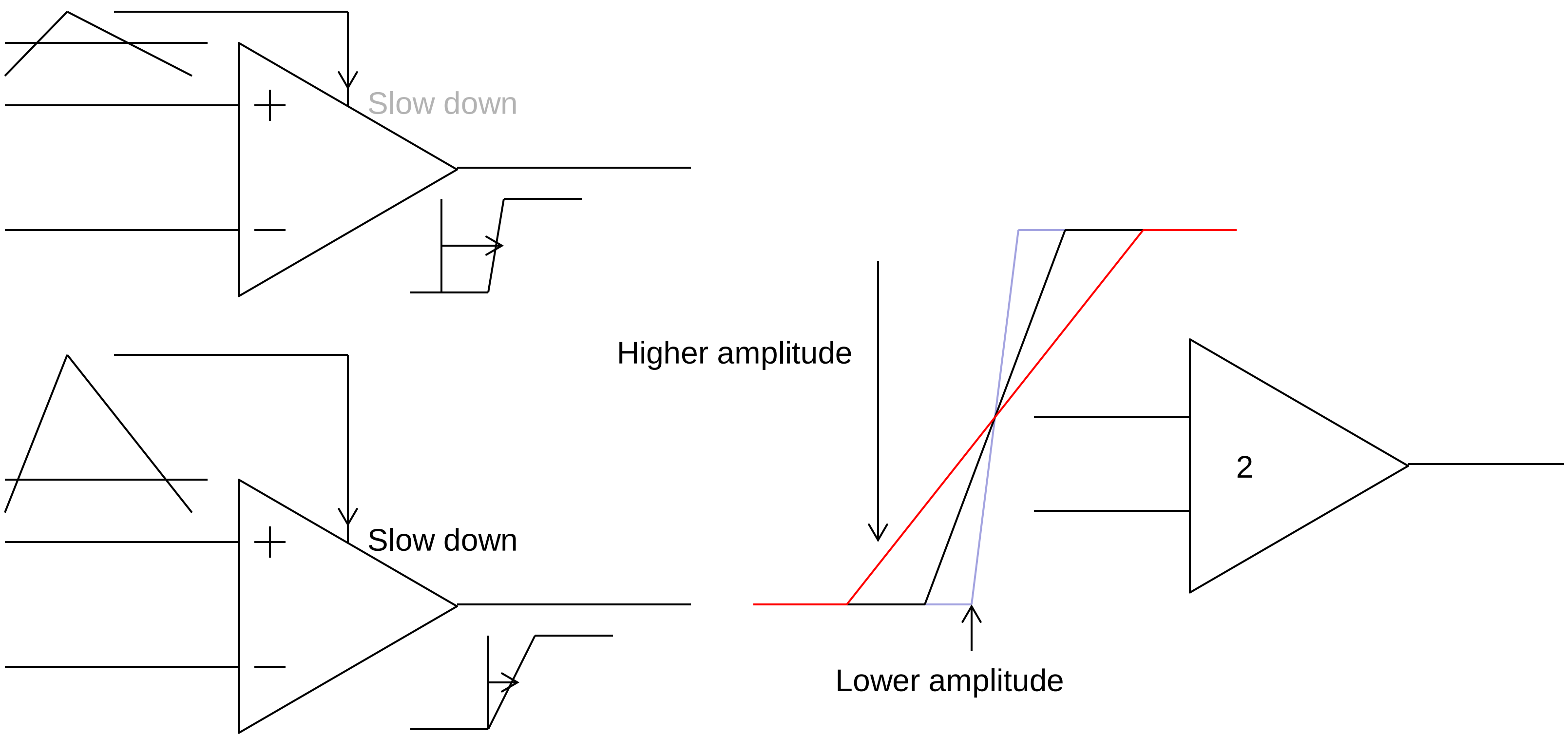
Time Walk Compensation

- The idea: Adding of low-pass filter decreases the noise without increasing the power consumption
- => Better SNR, lower threshold
- However: a slow output signal leads to a time-walk
- Time walk is caused 1) by the fluctuations of the input signal and 2) by the low and signal-dependent response speed of the electronics
- Can we compensate for time walk, without decreasing the shaping time constants?

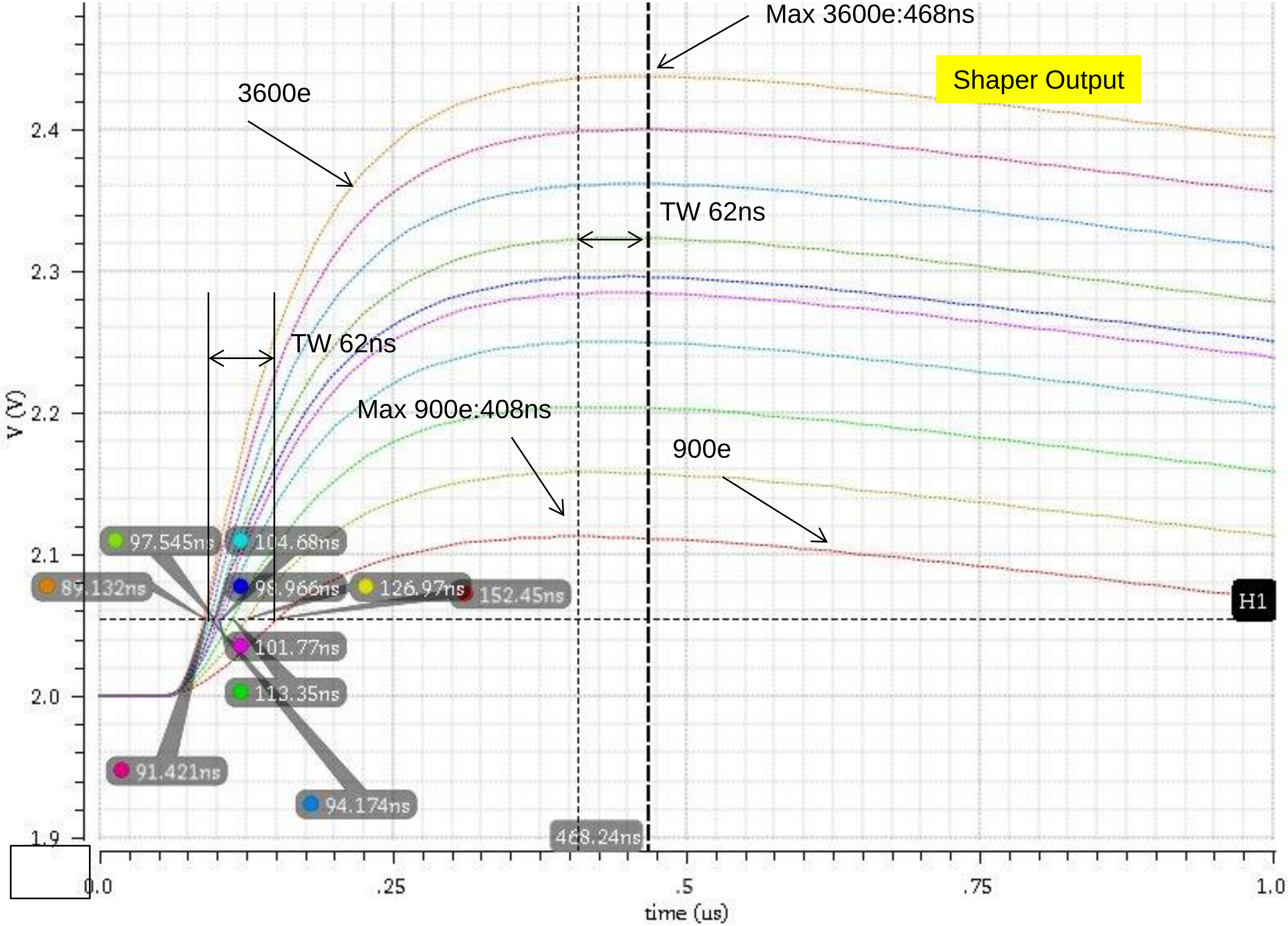


Time Walk Compensation

- Imagine a comparator which has the output zero-to-one transition speed, that depends on the input signal “overdrive”
- High amplitude signal – faster threshold crossing but slower 0-1 transition
- Low amplitude signal – slower threshold crossing but faster 0-1 transition
- Result: the threshold-crossing- and the transition time skews compensate each other
- Second comparator generates time-walk free signal



- Noise=8.8mV, Thr=55mV, Bias current=10µA, Pixel size = 50x250µm, Ifoll=10, amplifier power **200mW/cm²**



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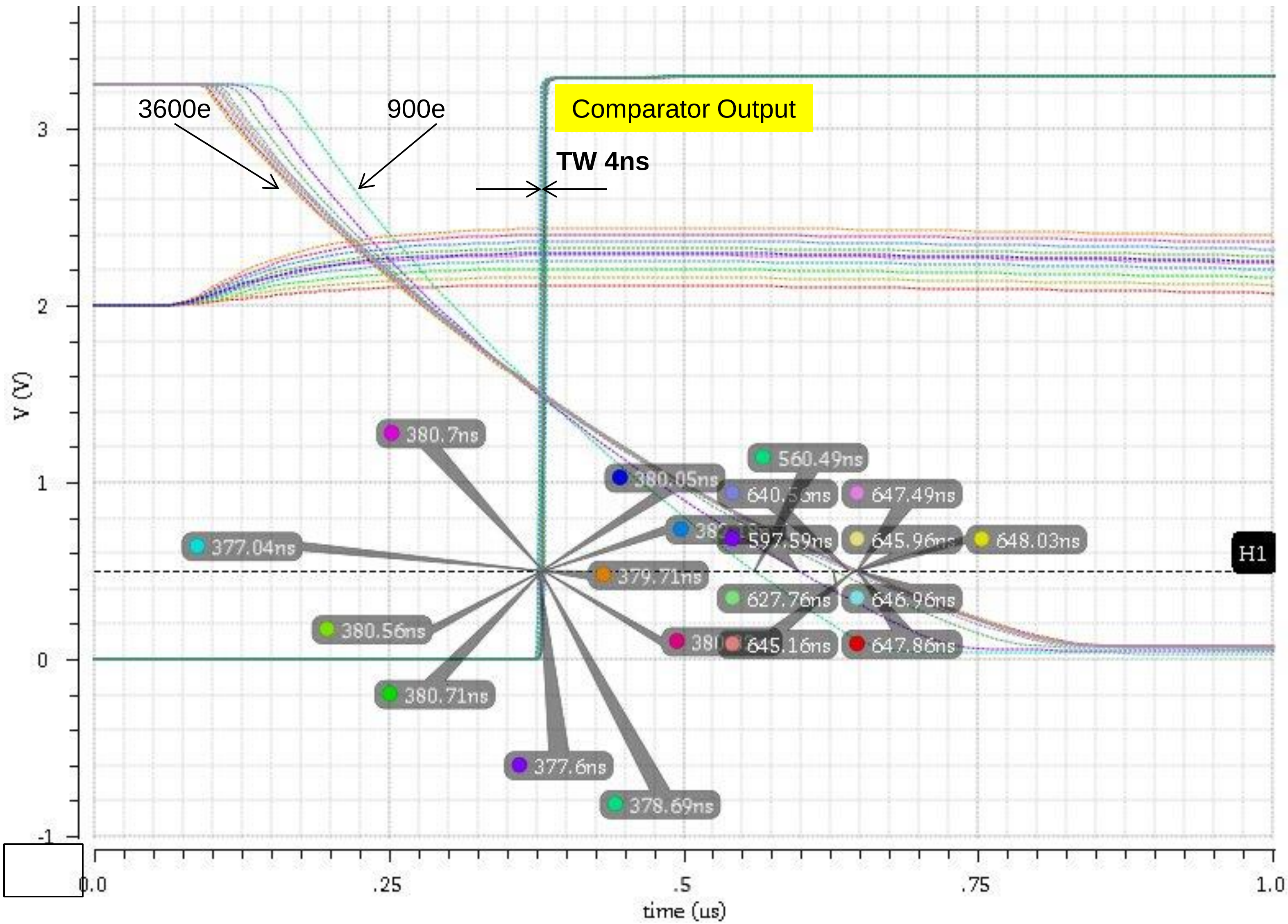
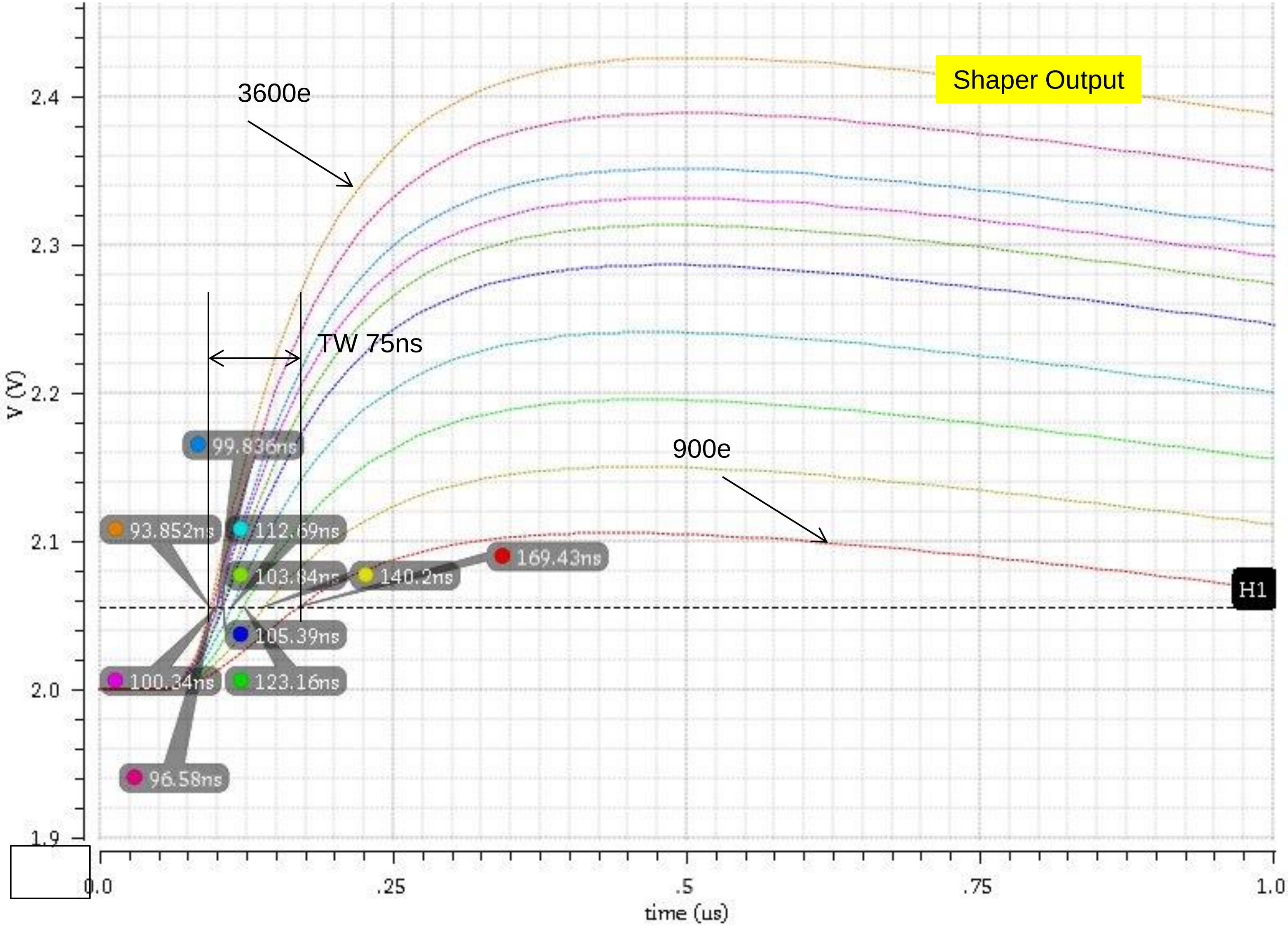
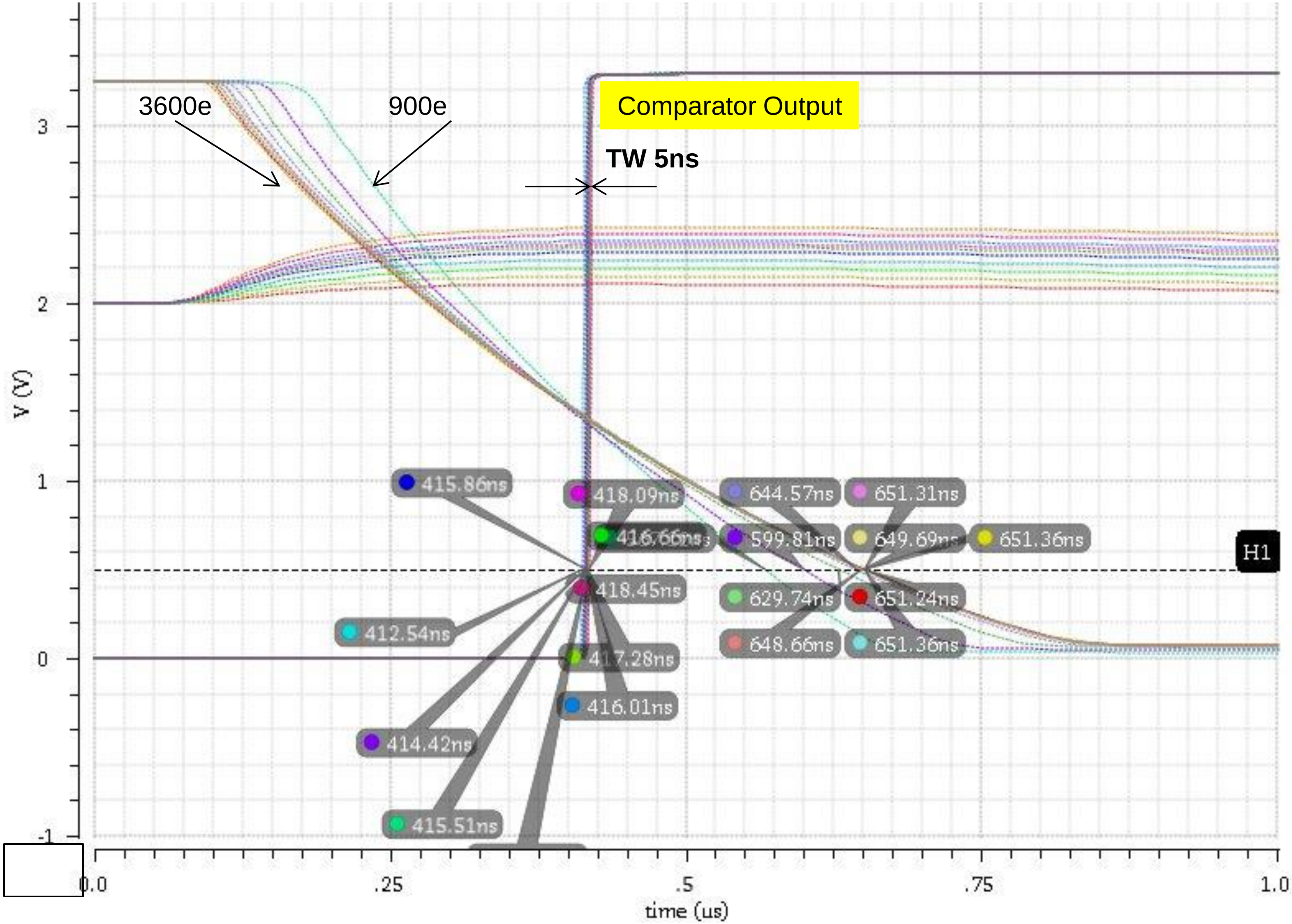


- Noise=8.0mV, Thr=55mV, Bias current=10µA, Pixel size = 50x500µm, Ifoll=7, amplifier power **100mW/cm²**

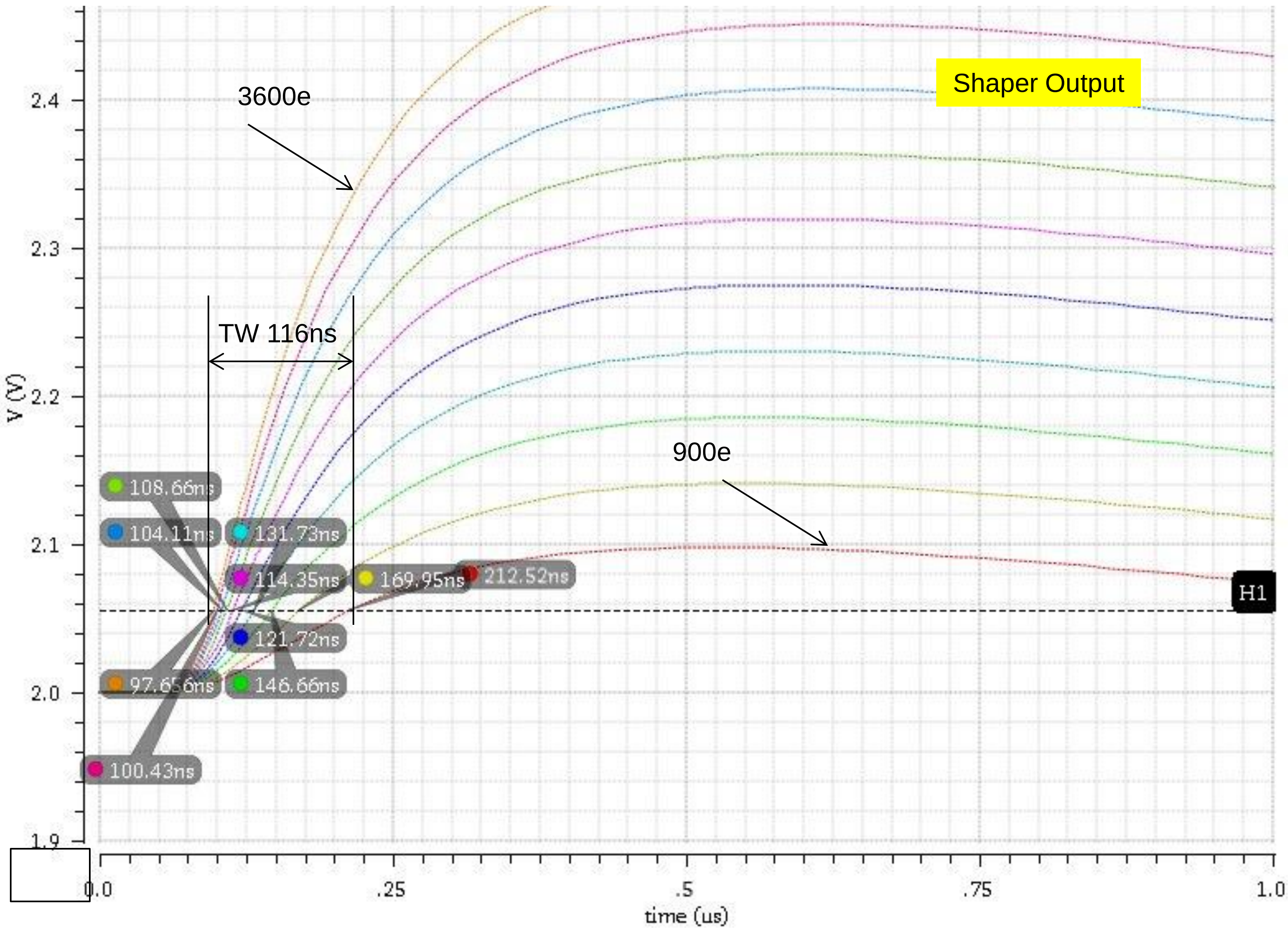


Time Walk Compensation

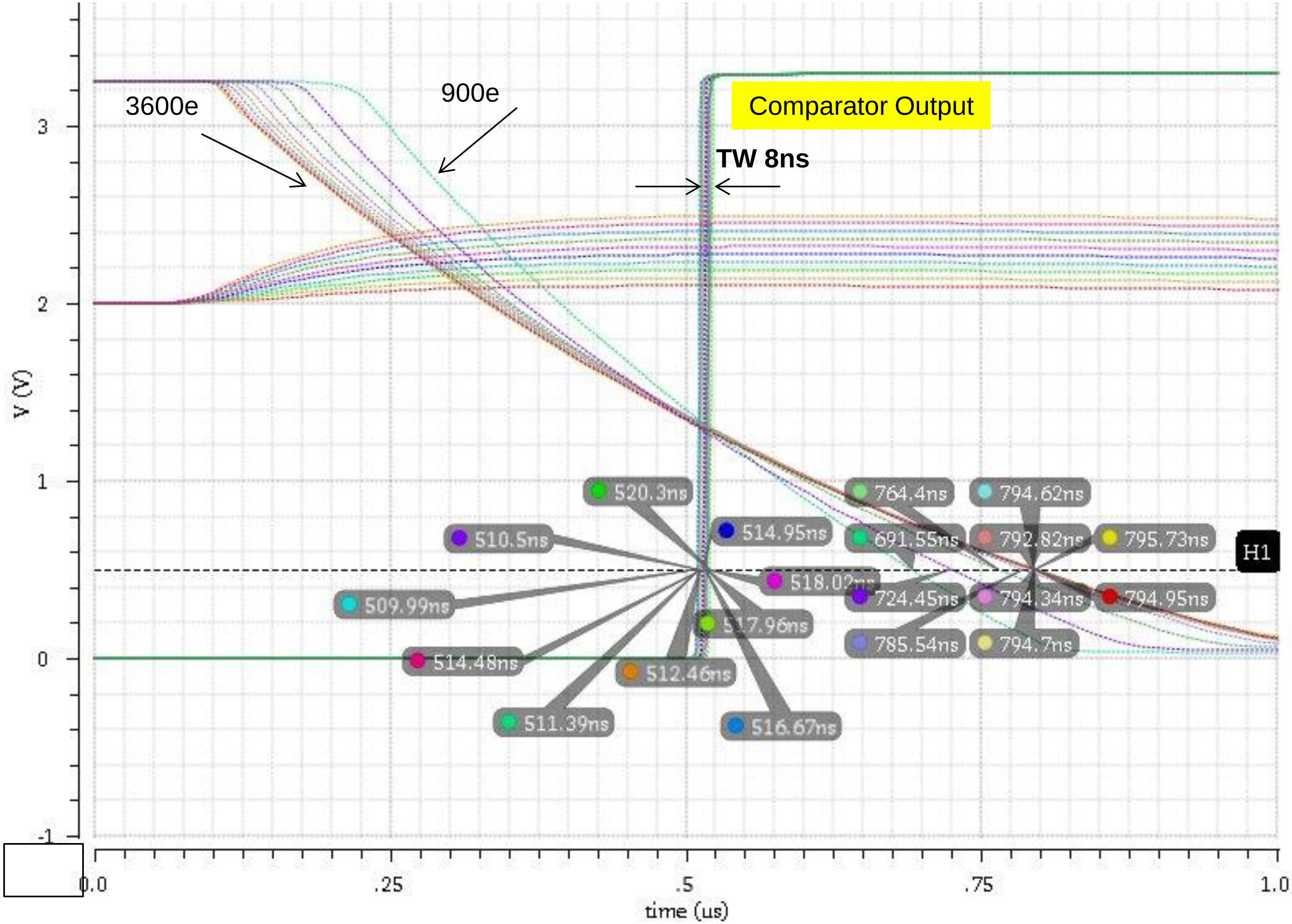
- Noise=8.0mV, Thr=55mV, Bias current=10µA, Pixel size = 50x500µm, Ifoll=7, amplifier power **100mW/cm²**



- Noise=7.9mV, Thr=55mV, Bias current=5µA, Pixel size = 50x500µm, Ifoll=5, amplifier power **50mW/cm²**

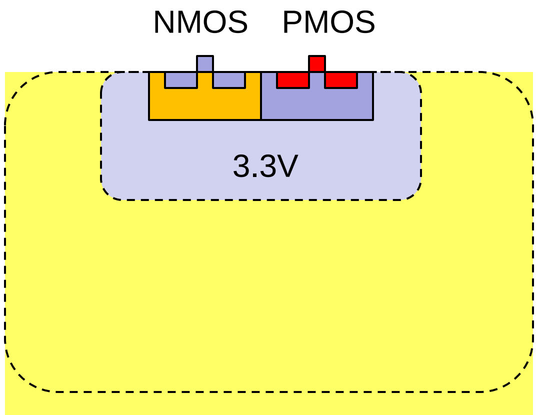


- Noise=7.9mV, Thr=55mV, Bias current=5µA, Pixel size = 50x500µm, Ifoll=5, amplifier power **50mW/cm²**

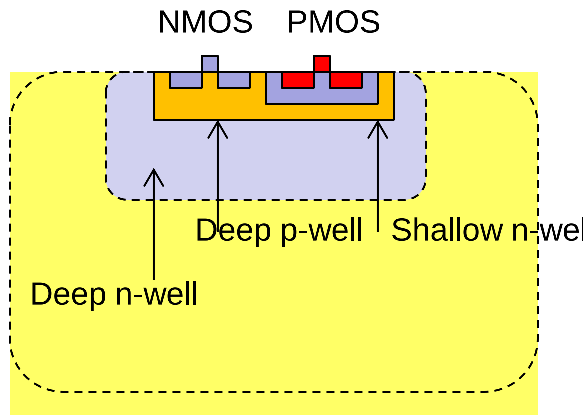


Detector structure improvements

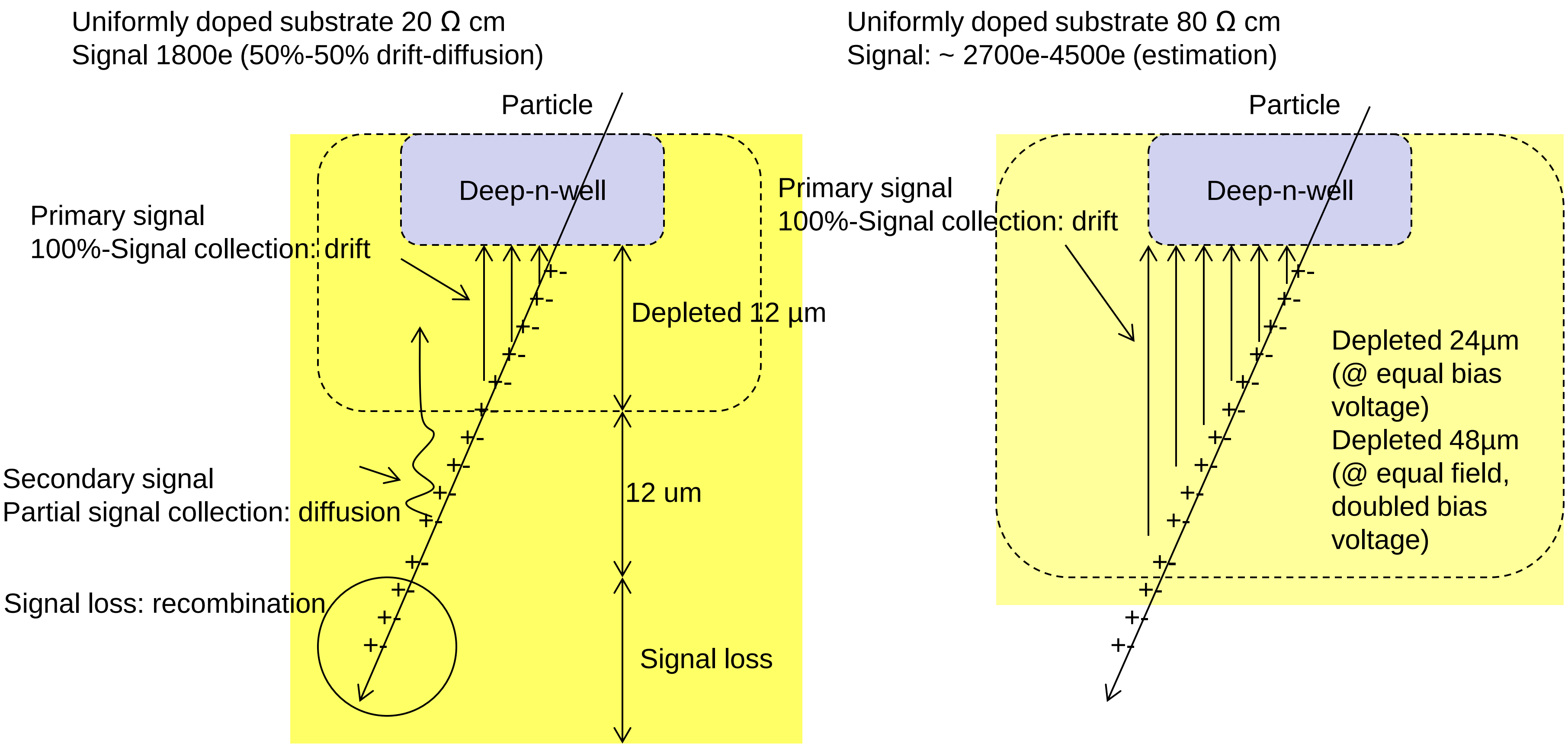
- Detector structure improvements:
- Isolated PMOS
- Eliminates PMOS to sensor crosstalk, allows more freedom when pixel electronics is designed



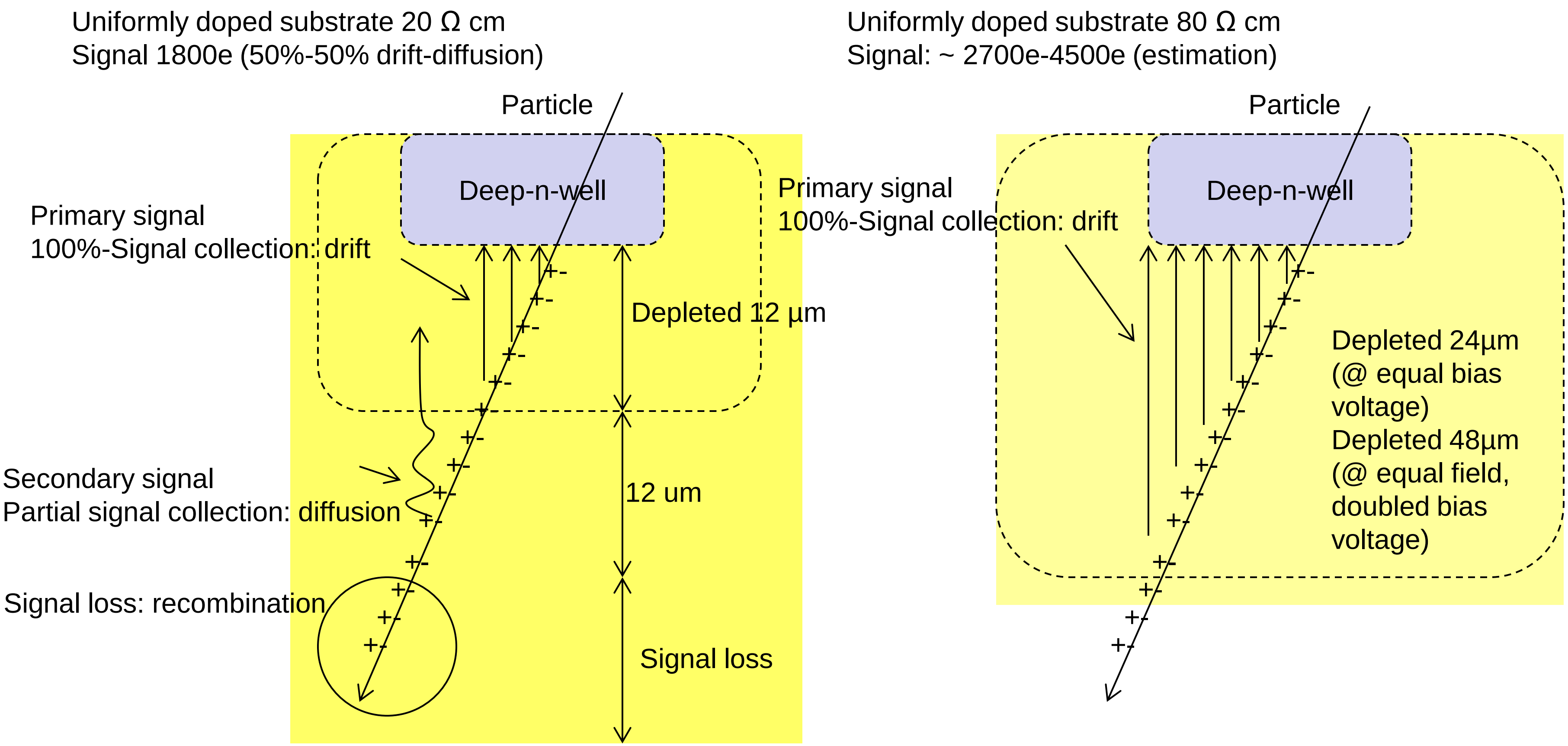
Improvement:



- Detector structure improvements:
- High resistive substrates

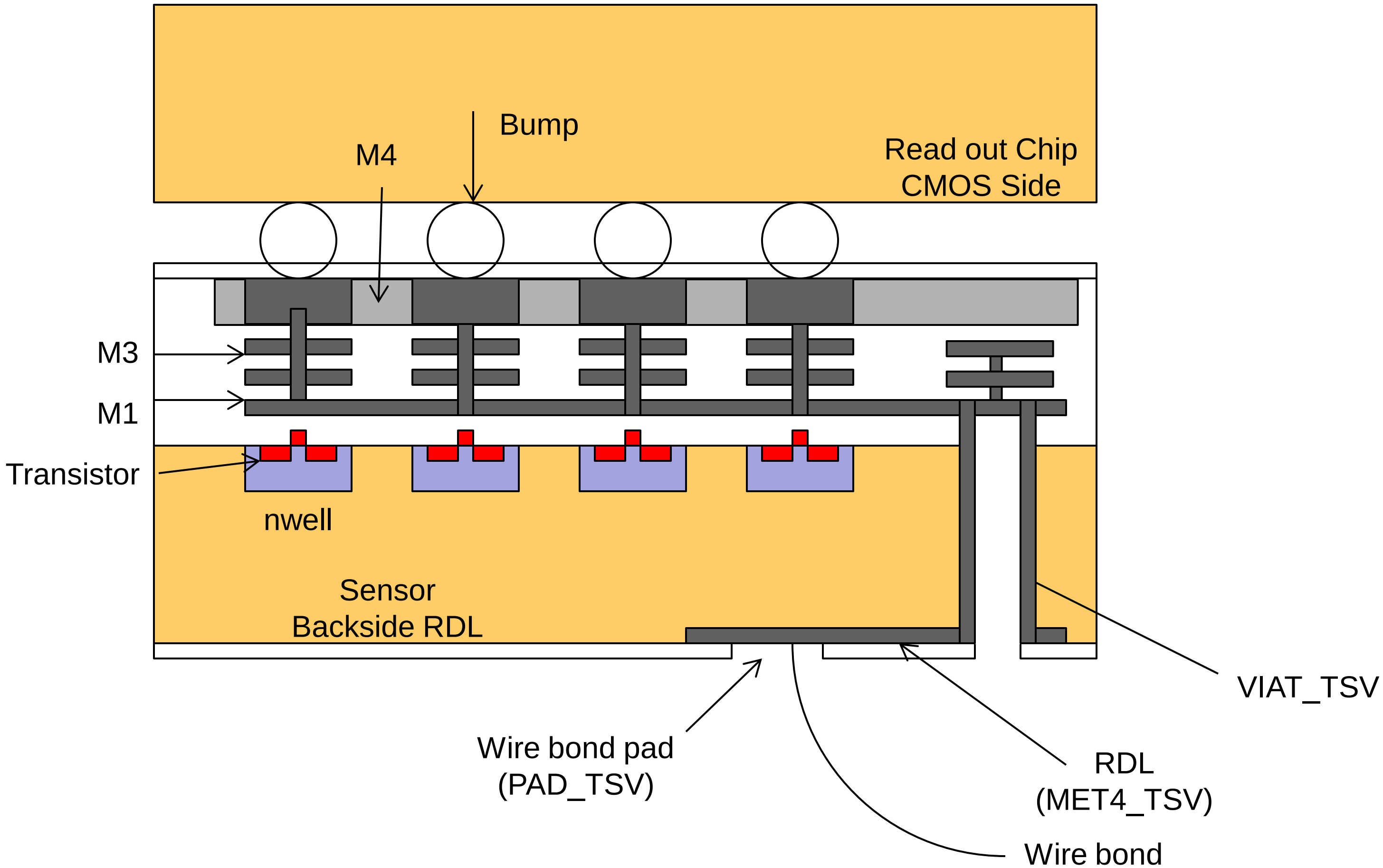


- Detector structure improvements:
- High resistive substrates
- **These improvements are possible within AMS- and LFoundry processes**
- AMS agreed to use substrates of up to 3000 Ωcm (350nm process H35)



AMS TSV process

- AMS offers through silicon vias and wafer bonding (so far only for H35, from end of 2015 for H18 as well)
- Backside redistribution layer and backside pads are possible
- TSV pitch 260 µm
- Very important for the module construction



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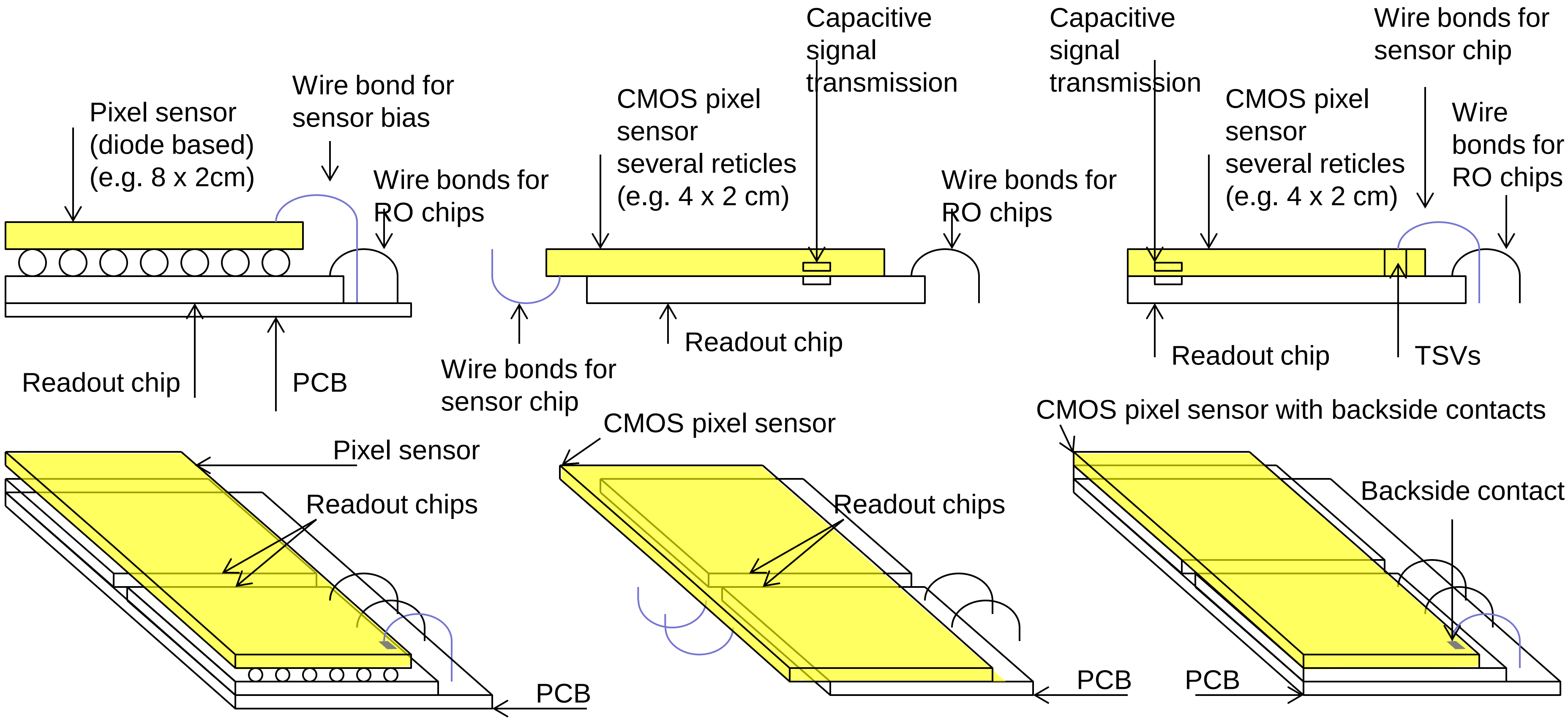
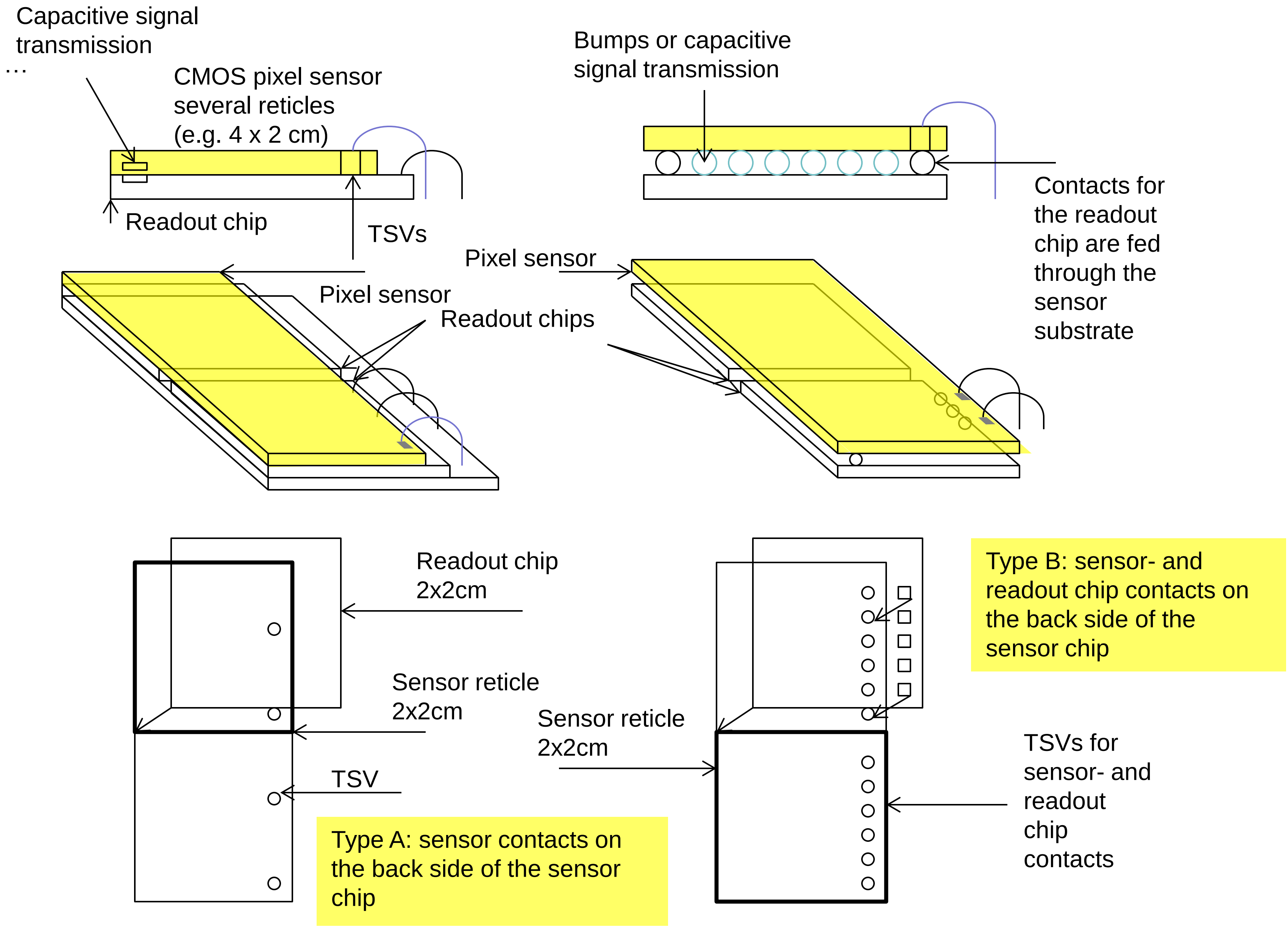


Detector as it is done now:
Diode based pixel sensor bump-bonded to readout ASICs

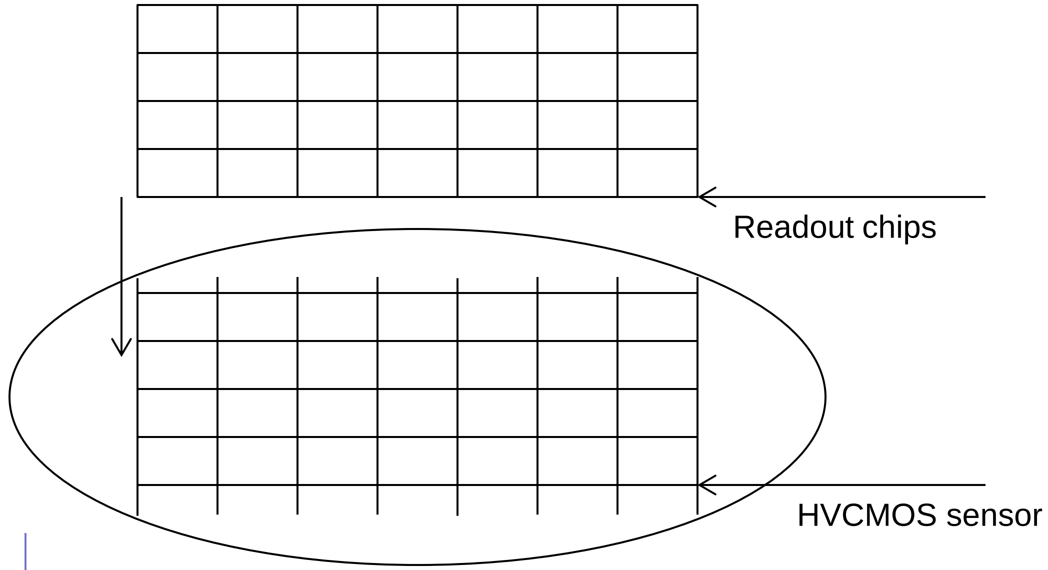
Present development:
CMOS pixel sensor capacitively coupled to readout ASICs

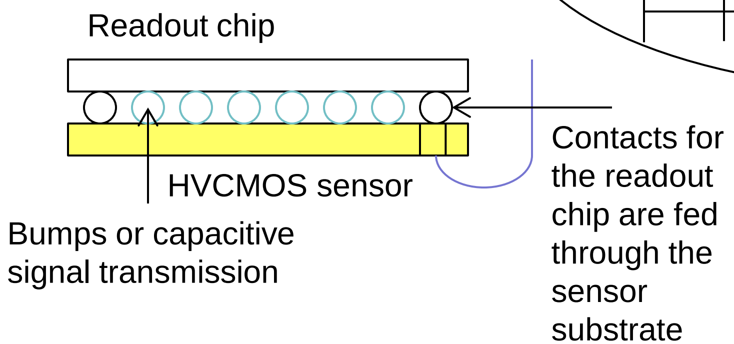
With TSVs
CMOS pixel sensor with backside contacts capacitively coupled to readout ASICs

Pixel detectors with TSVs



- Type B: sensor- and readout chip contacts on the back side of the sensor chip
- Allows readout chip- to sensor-wafer bonding
- If backside RDL is used, it allows, in theory, large area hybrid detectors
- About 1.5% of the area may be covered by the test structures; lateral signal collection from these regions is probably possible



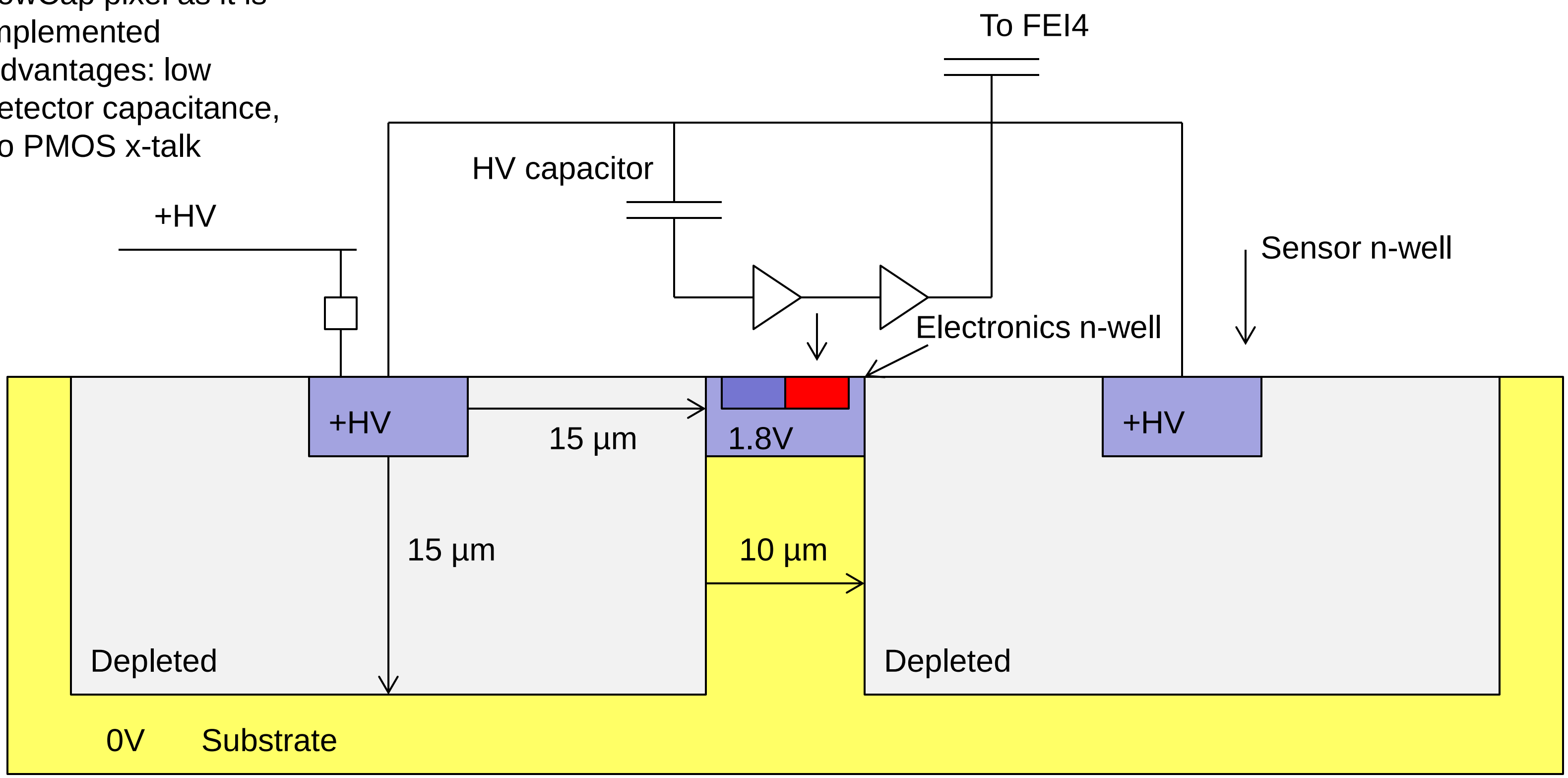


Developments ongoing

New H18 CCPD chip

- The new CCPD test chip in AMS H18 technology has been produced last week
- The chip contains test matrices with three types of pixels
- Type A – improved standard pixel from previous prototypes, we expect better threshold uniformity, lower noise, faster response
- TypeB - new type of pixel (LowCap-Pixel or HVMAPS) with separated electronic and electrode, sub pixel size 25 µm x 125 µm
- CLIC pixels, size 25 µm x 25 µm

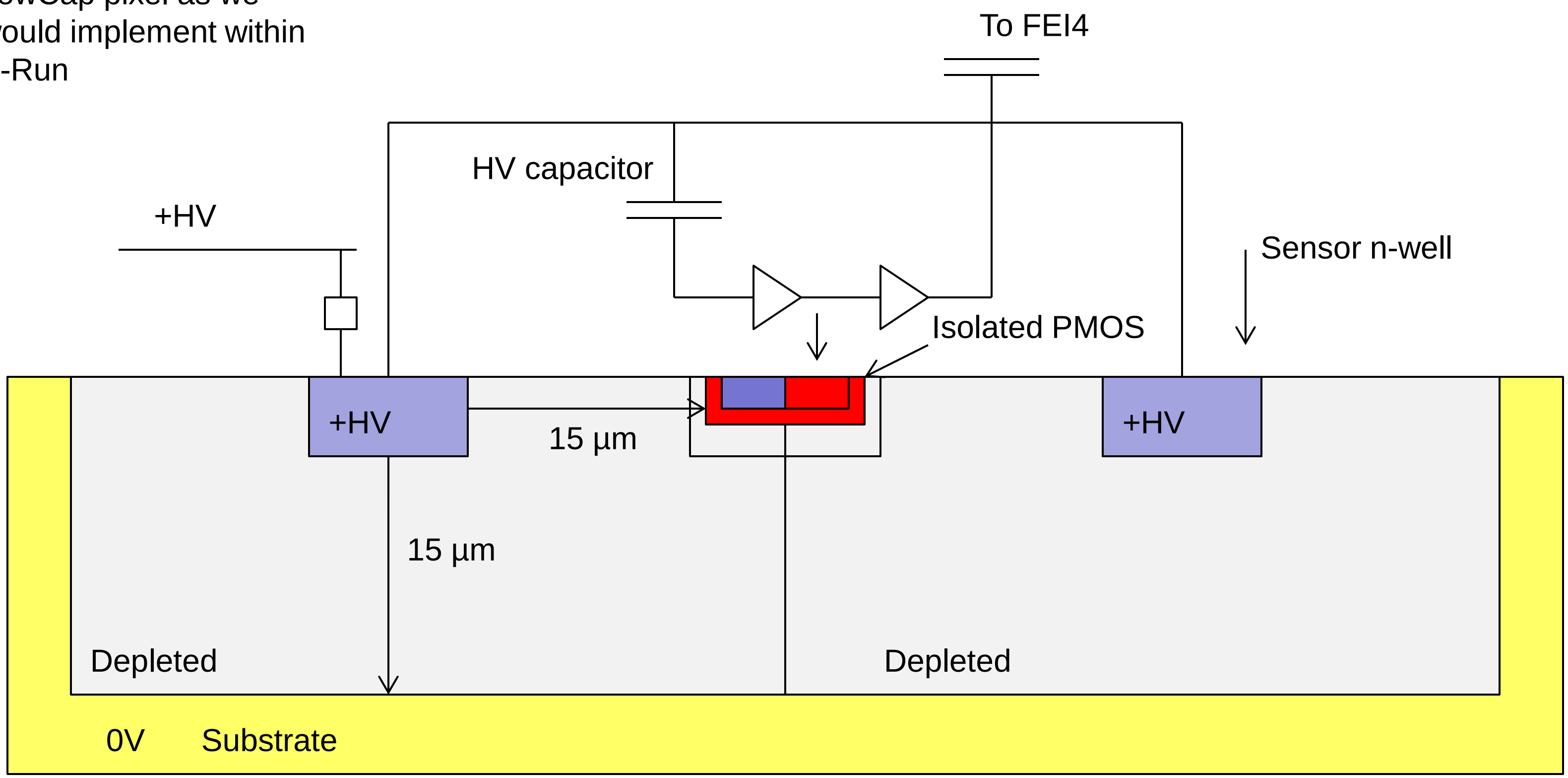
LowCap pixel as it is implemented
Advantages: low detector capacitance, no PMOS x-talk



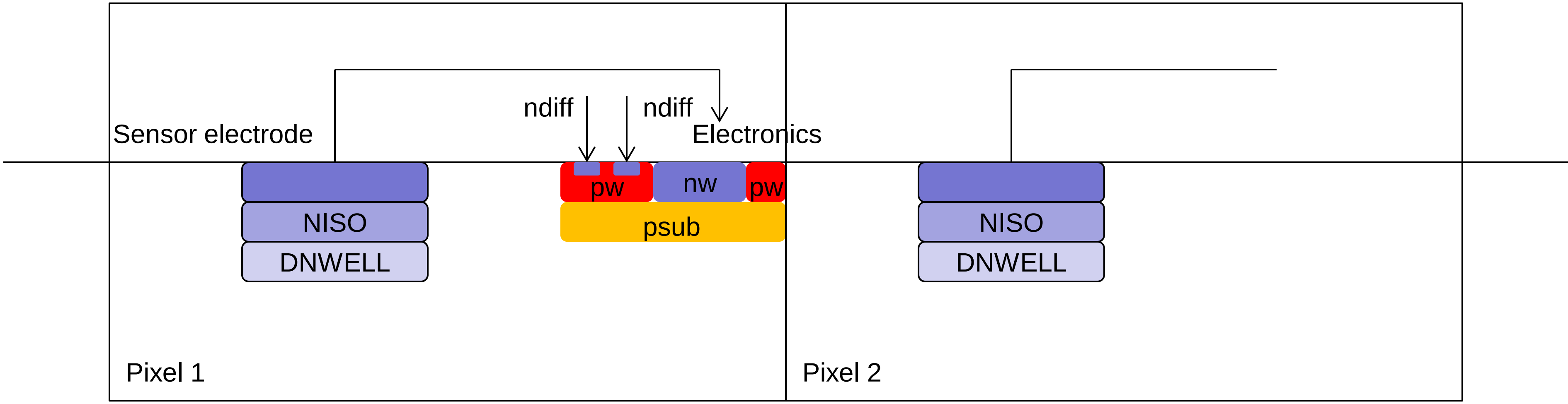
New H18 CCPD chip

- We are planning an engineering run in ~June 2014 within DEPFET project
- DEPFET does no need entire area
- A good opportunity to share the costs with DEPFET and submit larger area HVCMOS test structures
- Price per area would be 450 € + tax which is much less than within a MPW (1100 €)
- Several pixel types could be implemented: the standard one, standard with the time walk compensation, the Mu3e-type, the CLIC-type and the low-capacitance pixel

LowCap pixel as we would implement within E-Run



- LFoundry 0.13 µm technology is very interesting since it allows high-resistive substrates and PMOS isolation
- 1cm x 1cm test chip is currently being designed mostly by Bonn and CPPM



Pixel detectors with TSVs

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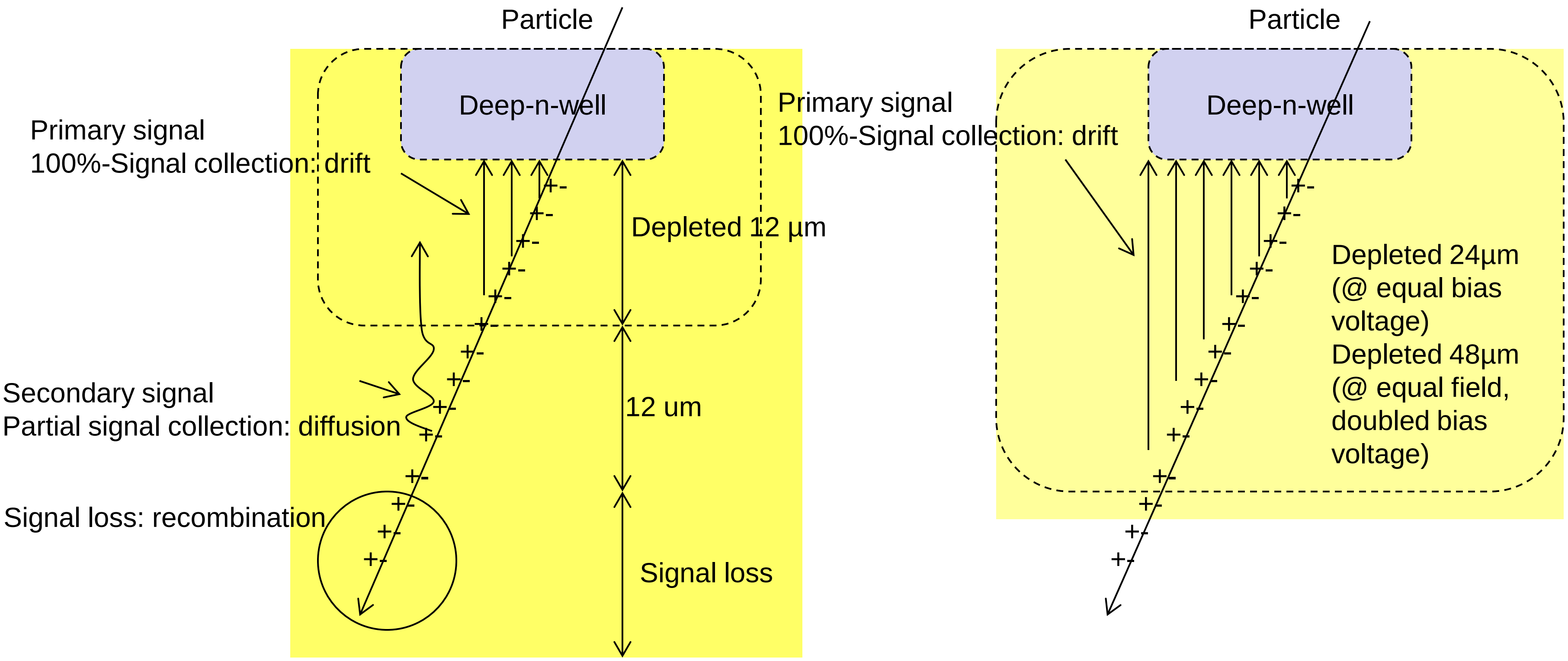
- Price per area wwould be 450 € + tax which is much less than within a MPW (1100 €)

High resistive substrates

- Detector structure improvements:
- High resistive substrates
- **These improvements are possible within AMS- and LFoundry processes**
- AMS agreed to use substrates of up to 3000 Ωcm (350nm process H35)

Uniformly doped substrate 20 Ω cm
Signal 1800e (50%-50% drift-diffusion)

Uniformly doped substrate 80 Ω cm
Signal: ~ 2700e-4500e (estimation)

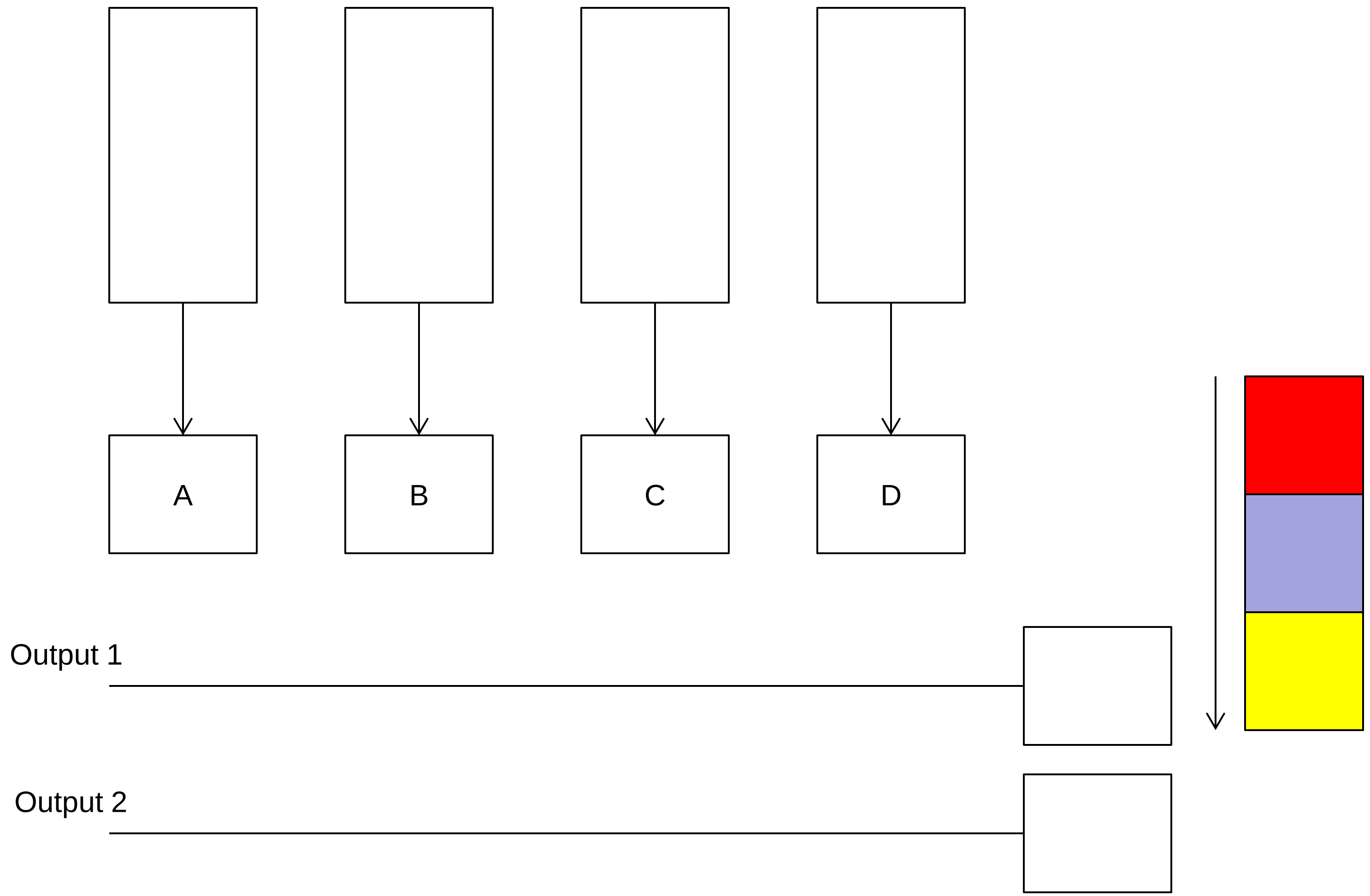


Summary

- Collaborations have been formed with the goals to develop HVCMOS sensors for ATLAS- and Mu3e experiments, as well for CLIC
- The Mu3e prototype detector (technology AMS 0.18 µm H18) (design Heidelberg) is a fully monolithic sensor with untriggered time-stamp based readout
- Detection efficiency of >99% has been measured in a beam test, time resolution (time walk) is ~ 70 ns.
- The ATLAS prototypes in AMS 0.18 µm (H18) (design HD) and GF 0.13 µm (design CPPM, HD) technologies are capacitively coupled smart sensors that can be readout using FE-I4 chip
- Irradiations and test beam measurements have been performed on the H18 chip
- The H18-chip is operational after 880 MRad and 10^{16} n_{eq}/cm^2
- A test beam measurement has been performed with the test-setups which are still not optimized and in development stage – the threshold uniformity was poor
- The uniradiated H18-detector had a detection efficiency of >90% in the regions with lower threshold
- The detector irradiated to $10^{15} n_{eq}/cm^2$ had a non-uniform efficiency (in some regions >90%) which is still not understood. Time resolution is ~70ns

Summary

- We need to improve the time walk and the detection efficiency
- Three approaches:
- 1) Optimization of the present design
- 2) Use of low-pass filter and the time-walk compensation circuit
- 3) Detector structure improvements (isolated PMOS) and the use of substrates of higher resistivity
- Chip producers AMS and LFoundry allow such "extra features" within their processes
- Combined monolithic-CCPD prototype detector is currently being designed mostly by Bonn and CPPM in LFoundry 0.13 µm process on a high resistive substrate
- AMS additionally offers through silicon vias and wafer bonding (so far only for H35, from end of 2015 also for H18 process)
- Backside redistribution layer and the backside pads are possible
- Backside contacts may be very important for module construction
- We are also investigating the use of HVCMOS sensors (segmented strips) for the ATLAS strip layers
- Constant delay lossy multiplexing can be used – every hit is transmitted to one of n outputs with a constant delay of ~60 ns.
- Hit loss occurs only if there are more than n simultaneous hits within one bunch crossing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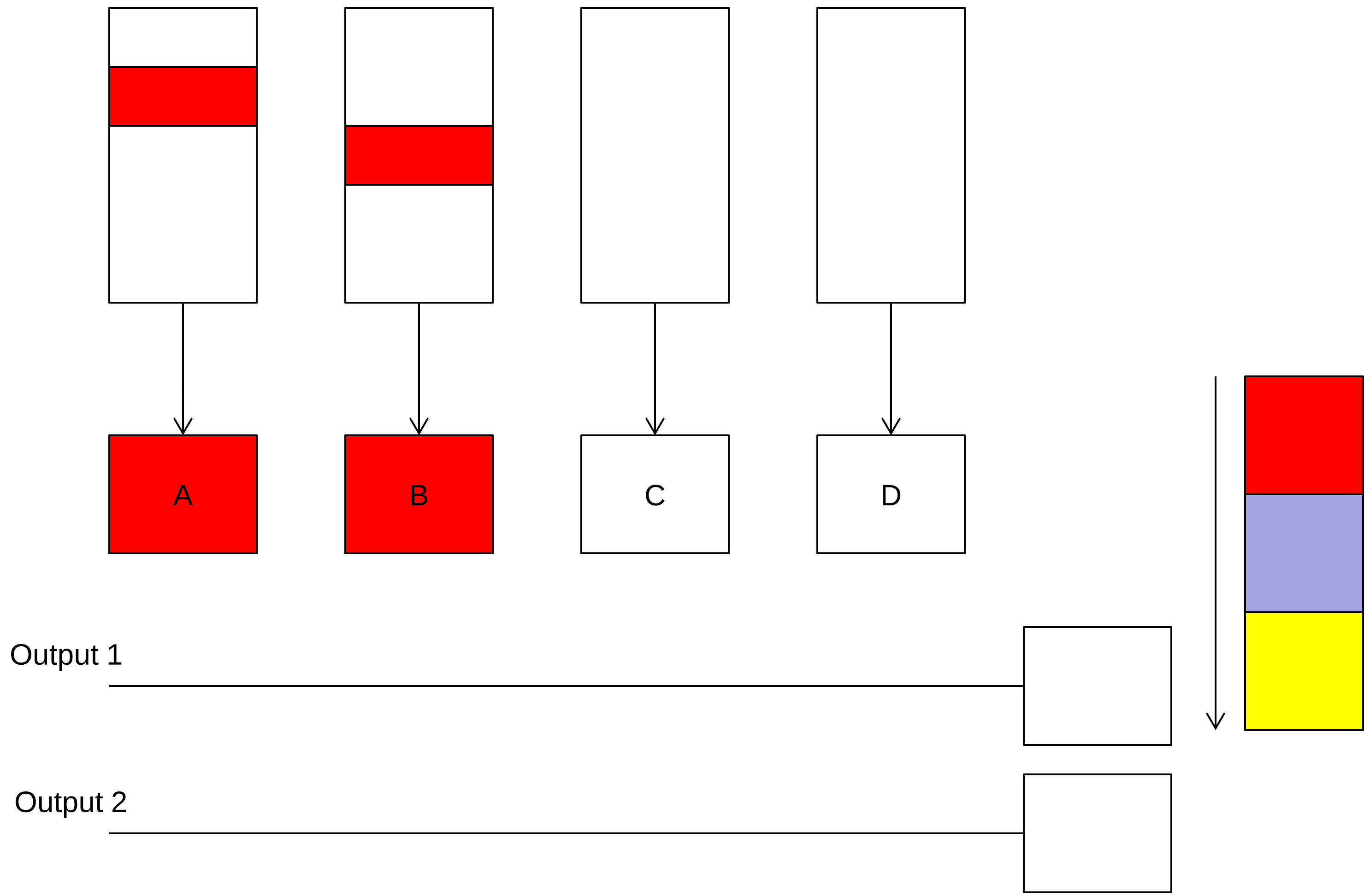
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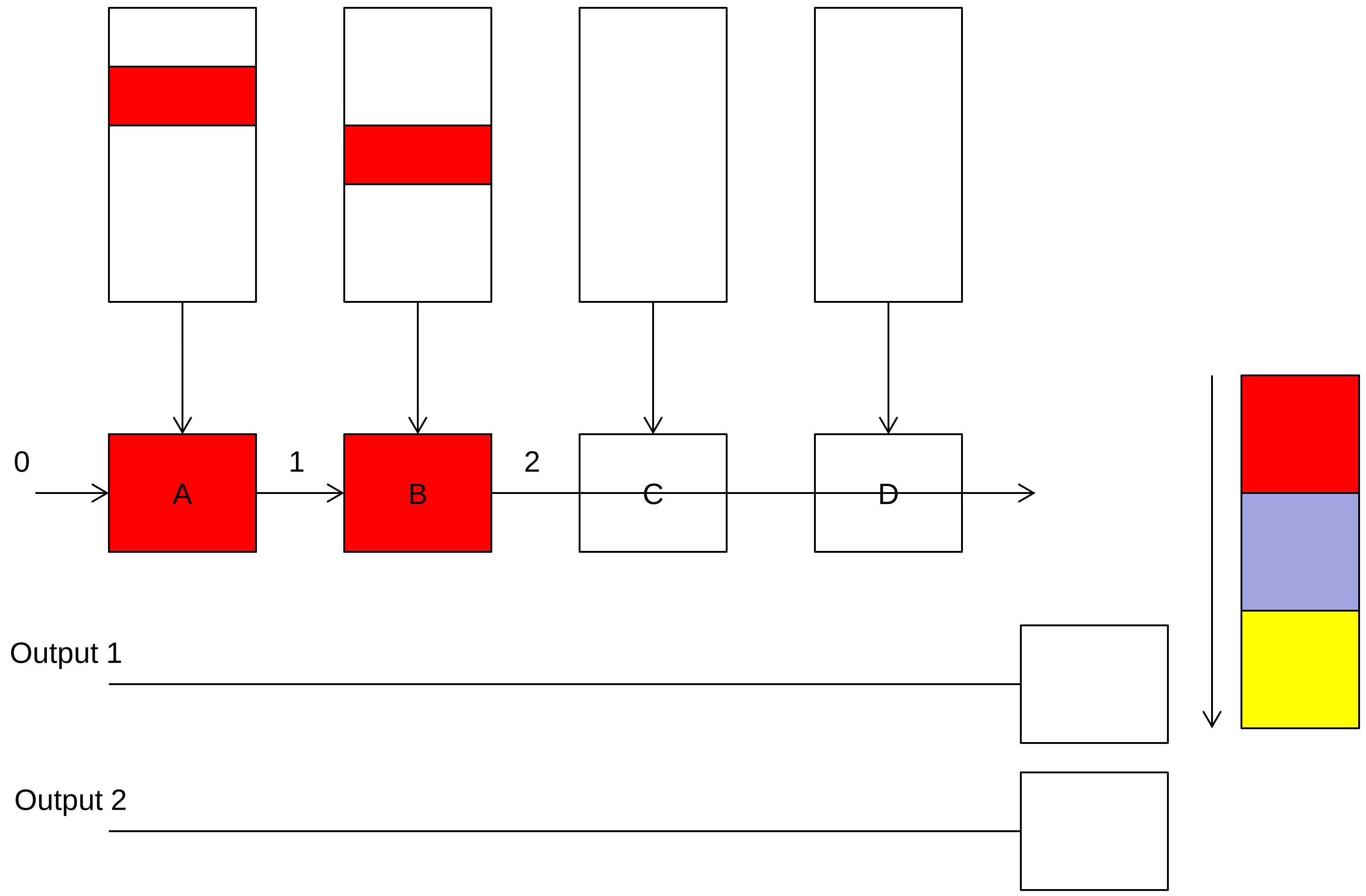
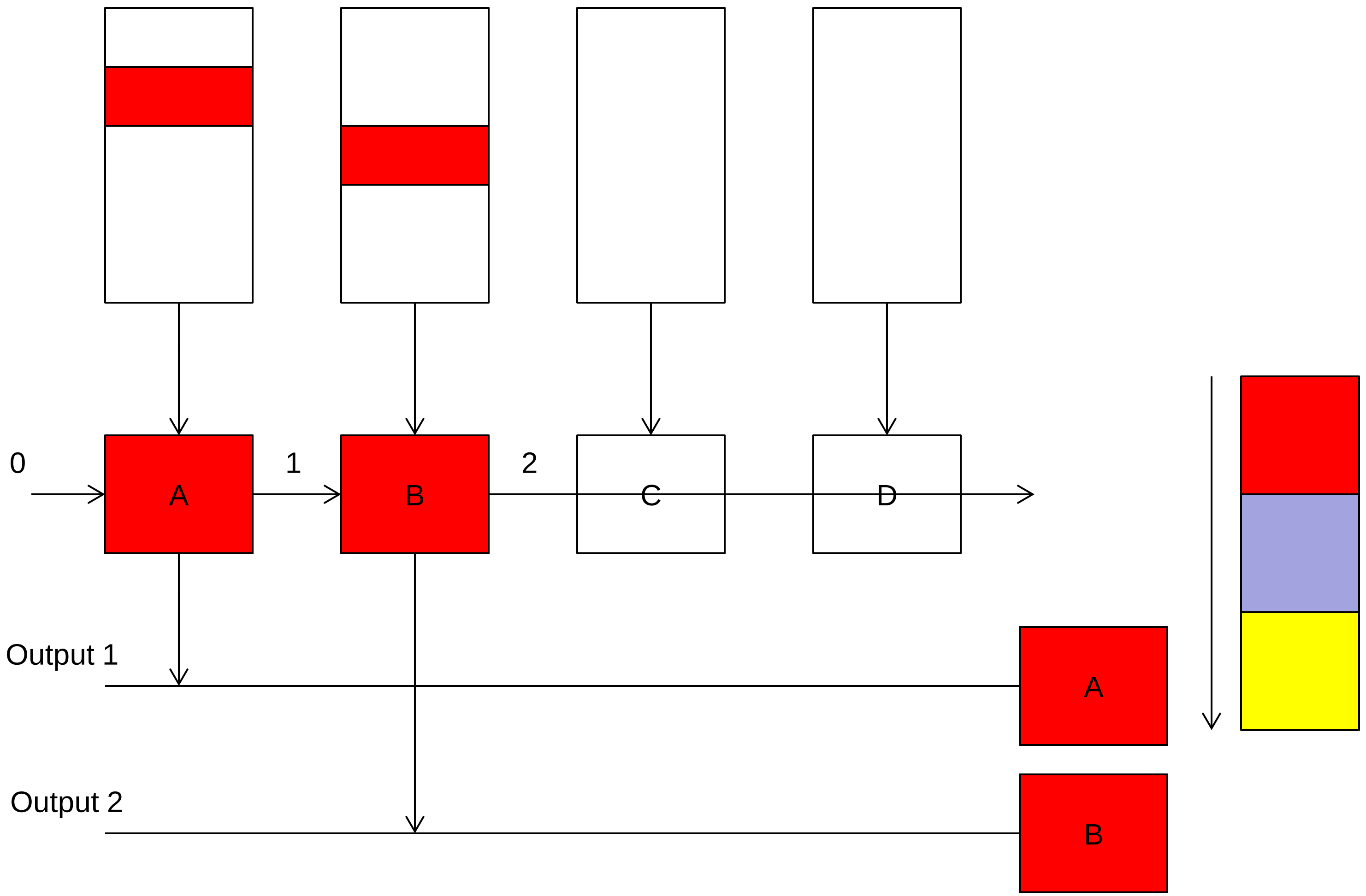
Segmented strip detector with lossy constant-delay-multiplexing





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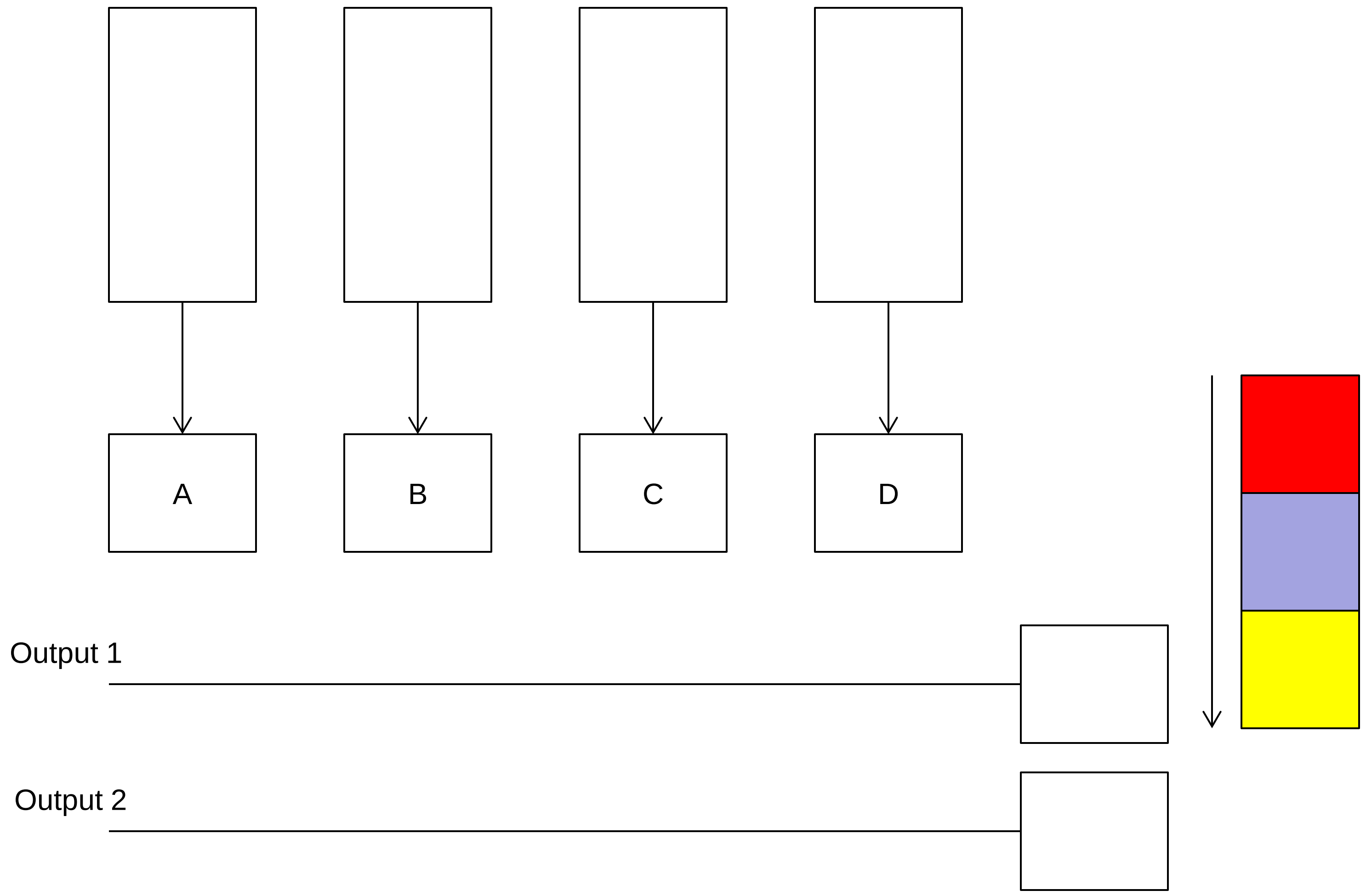
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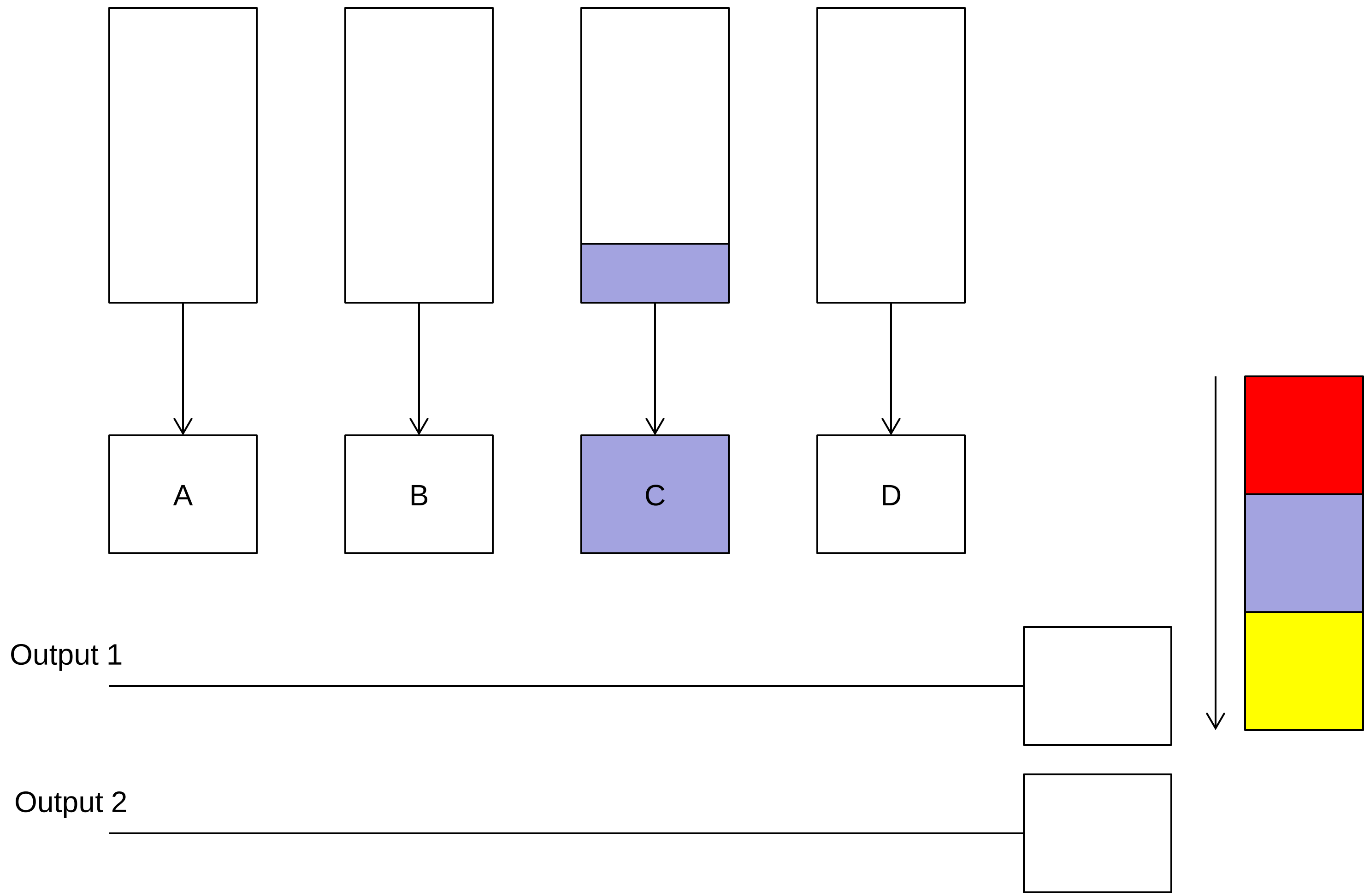
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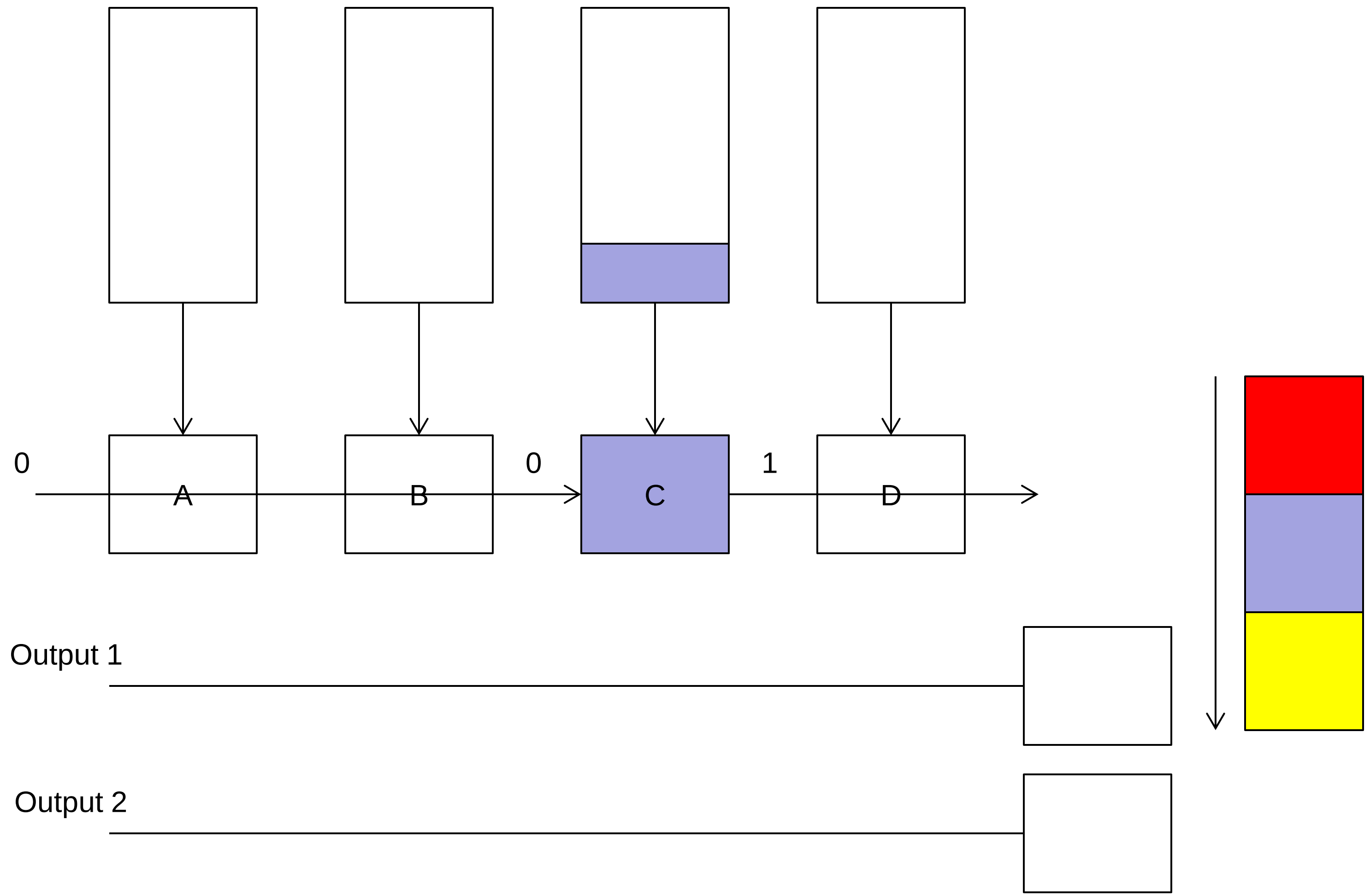
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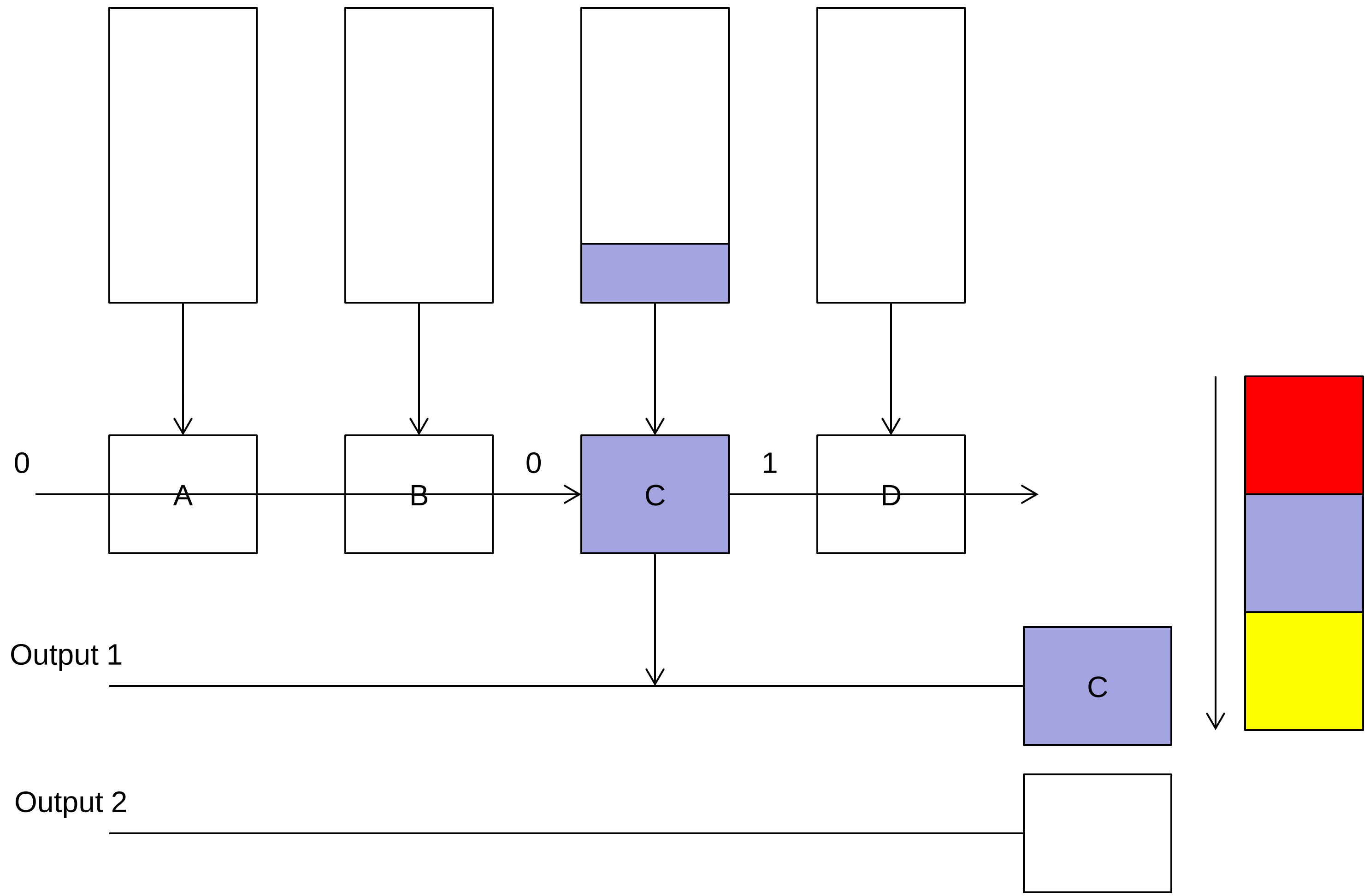
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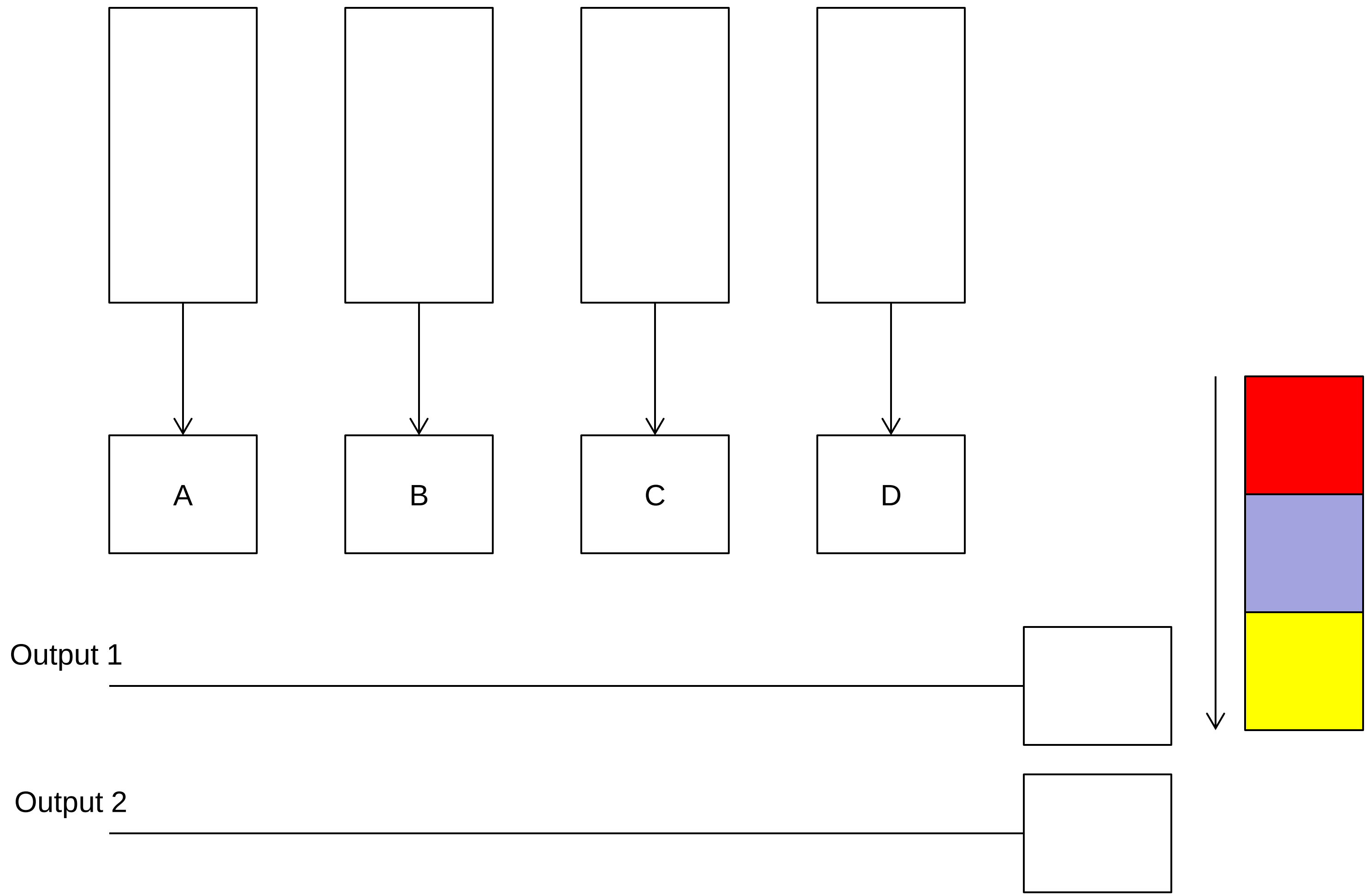
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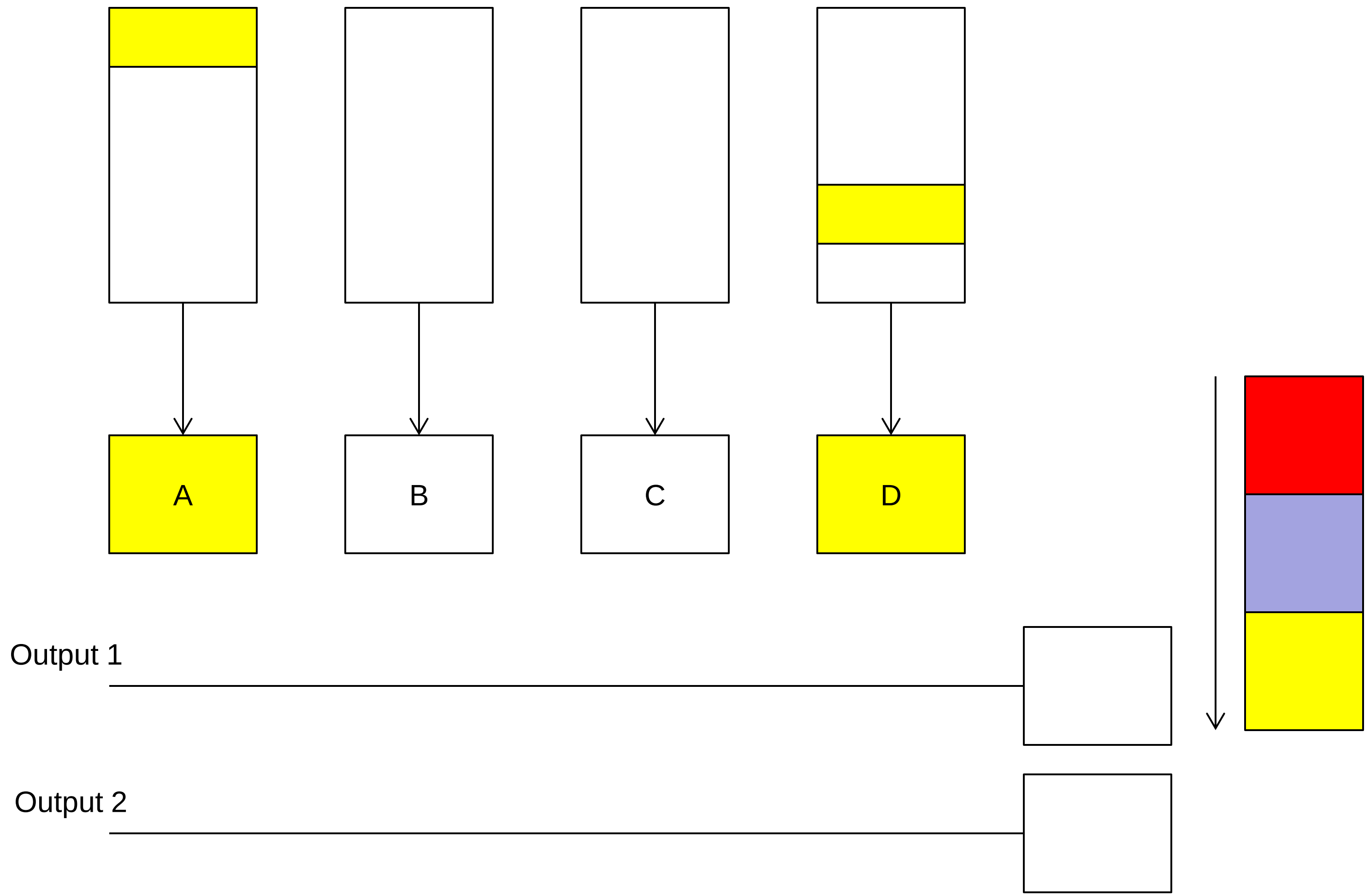
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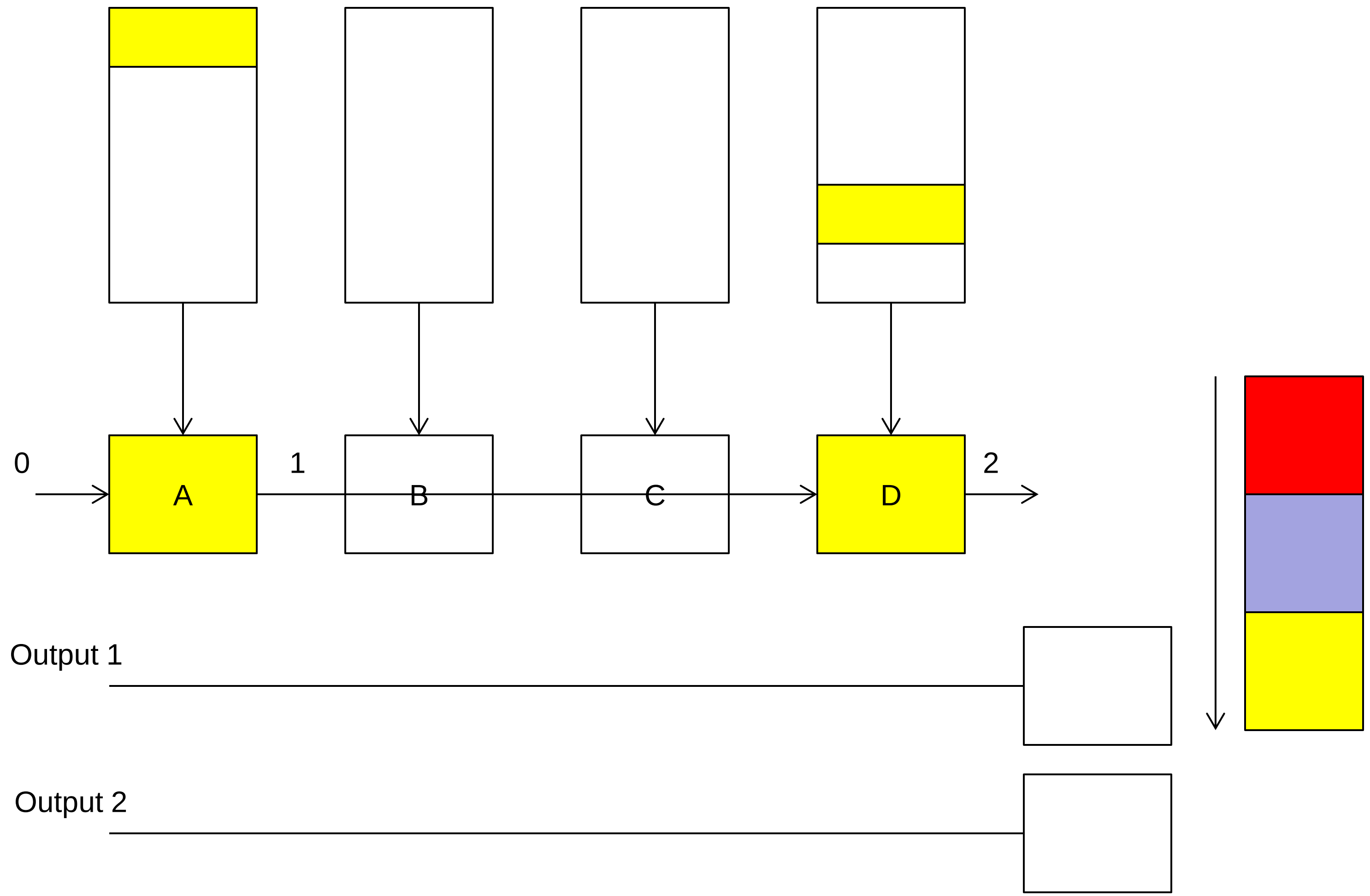
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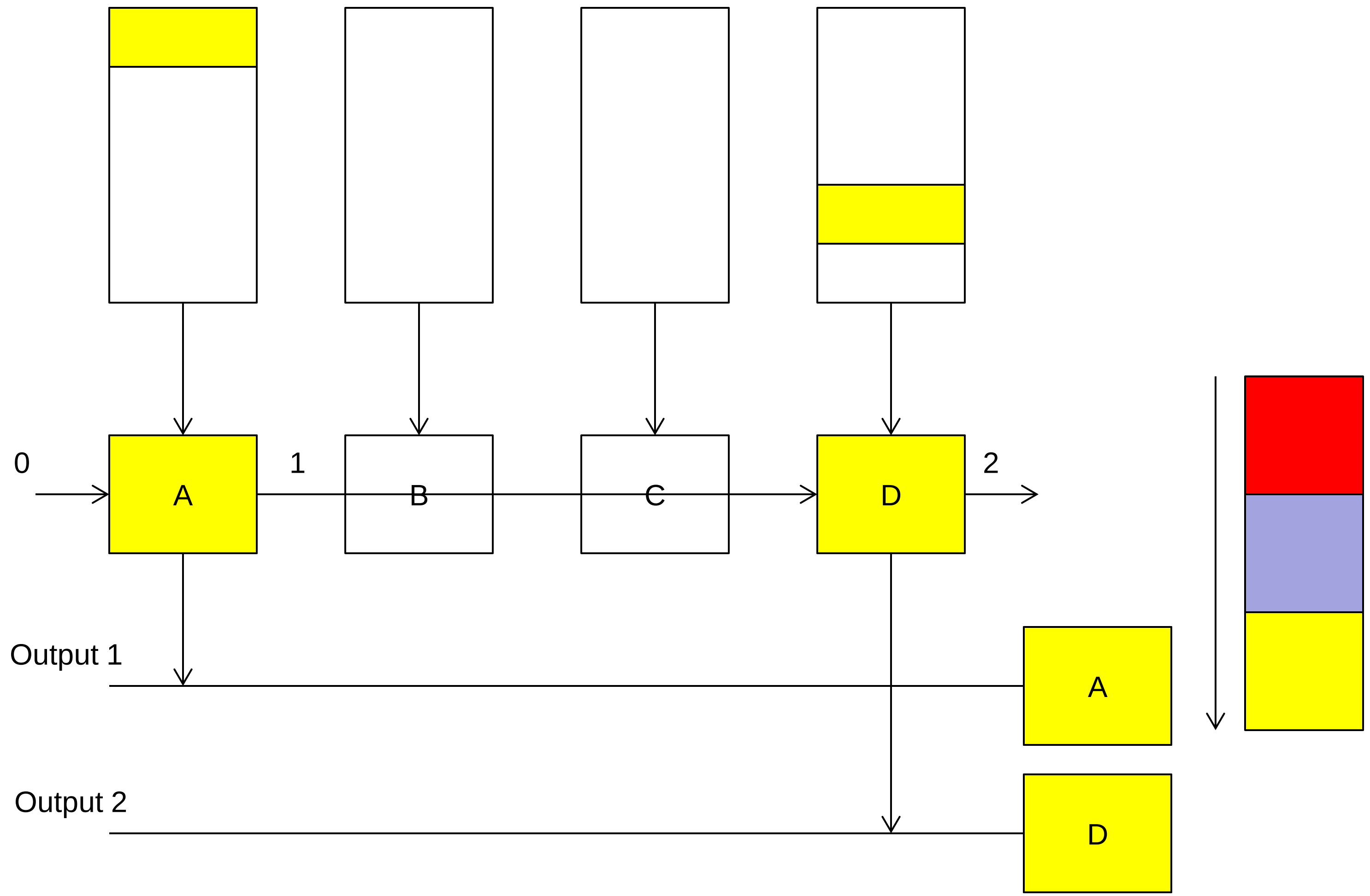
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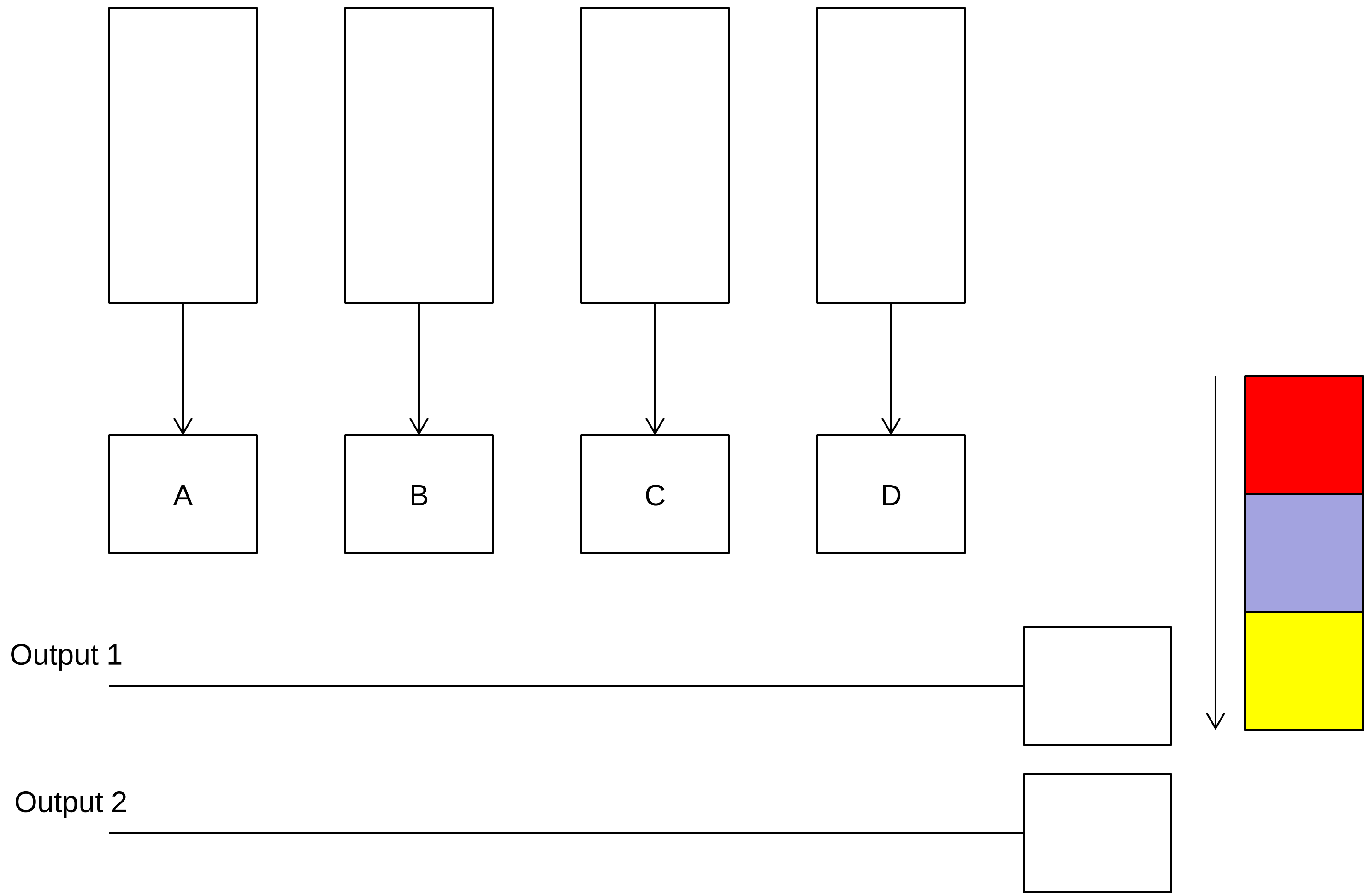
A
B
C
D
Output 1
Output 2