Development of thin pixel modules using novel 3D Processing techniques

9th Trento Workshop, Genoa 2014

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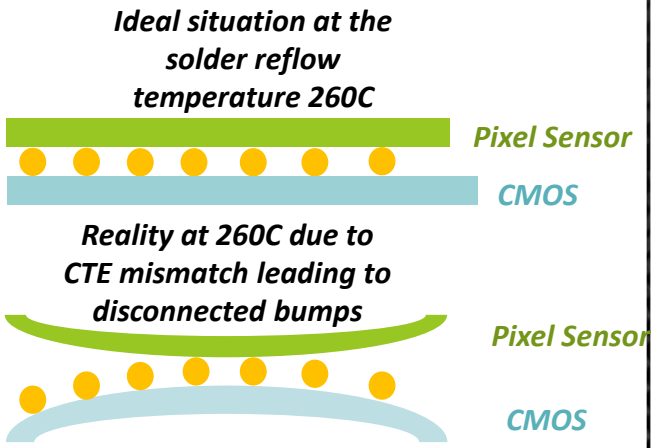
Outline

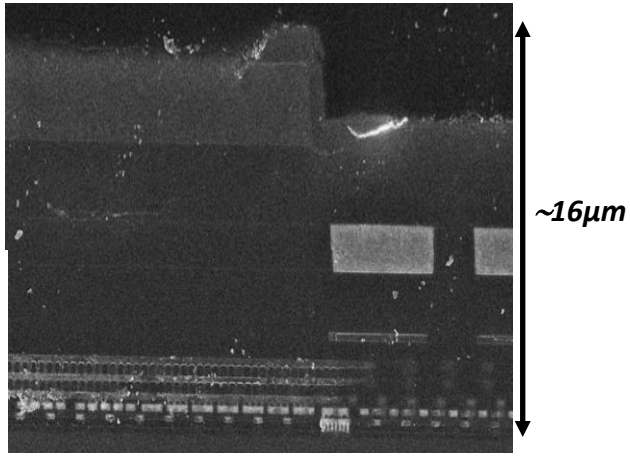
- *Introduction*
- *CEA LETI Open 3D overview*
- *Process flow*
- *Front-side bump processing*
  - *Full thickness bump yield*
- *Backside processing*
  - *Backside stack*
  - *Thermal cycling of single die*
- *Summary*

Introduction

- *One of the main objectives for the pixel upgrade is to develop an approach towards low mass modules and thus reducing radiation length.*
- *Develop an alternative wafer level back-side process that compensates for the CTE mismatch of the CMOS front-side stack*
- *From the module perspective this can be achieved by thinning both the sensor and the CMOS ROIC*
- *The thinning of these devices leads to low bump yield (26,880 bumps in 80 columns) at the solder reflow stage and hence poor device resolution due to bad co-planarity of the two chips*
- *Begin by thinning the ROIC from the standard 300um to 100um using the Open 3D technology offered at CEA-LETI*
- *Identify new foundry with 200-300mm capacity for bump processing and wafer thinning*

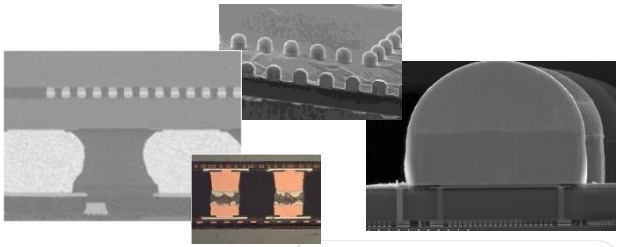


Cartoon depicting the pixel sensor and CMOS dynamics at the solder reflow temperature

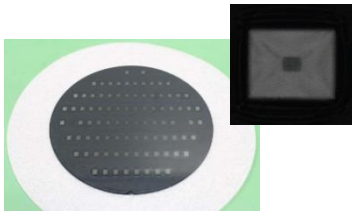


SEM x-section of FE chip showing the full front-side CMOS stack and differing metal densities through the layers

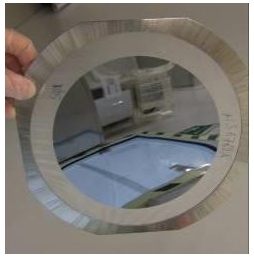
3D Packaging Lab / Core competencies at CEA-LETI

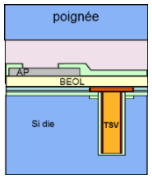


µ-bumps and SAC copper pillars

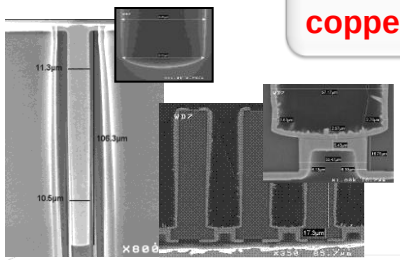


Molding & underfilling

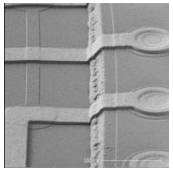


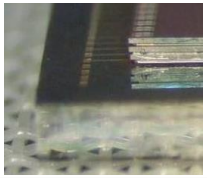


Temporary bonding on 100 µm thk 200mm wafer including small or large copper pillars



Through Silicon Via (TSV). Cu filled. AR3-10

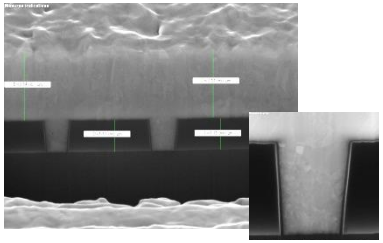




F2F and B2F Thin die stacking (30um thk). Conformal routing

3D

INTEGRATION

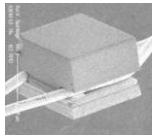


2 to 4 layers routing Damascene thick Copper Routing on organic

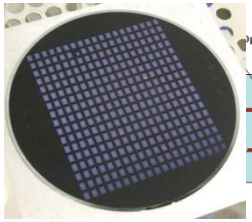
Thinning 80 – 100 µm

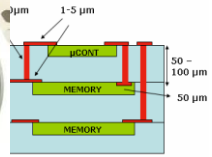
Internal stress monitoring

Warp management



Silicon on wire





Organic/silicon rebuilt wafer

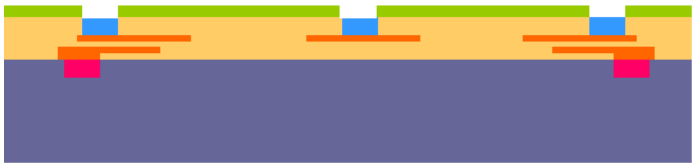
Routing and via (TPV)

Strata stacking and connecting

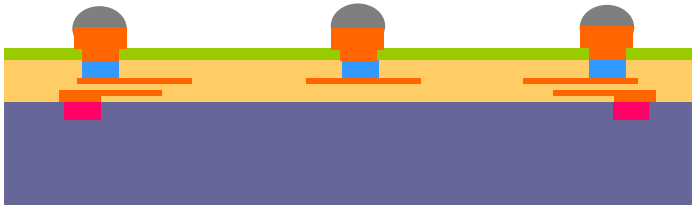
University of Glasgow

cea leti OPEN 3D

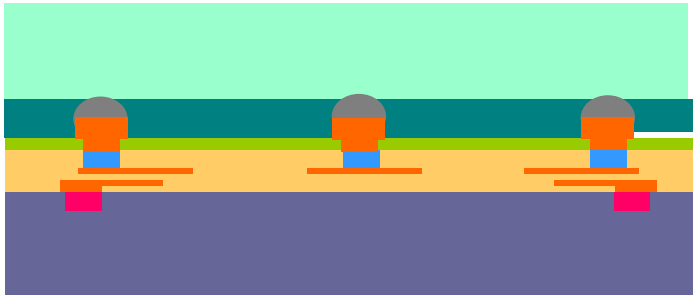
Processing overview
Basic flow



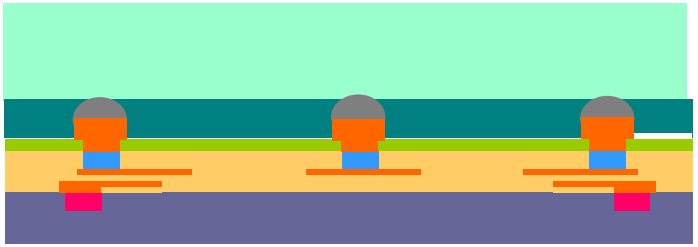
Incoming wafers



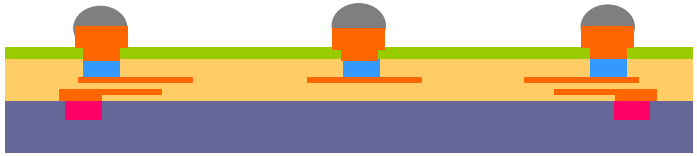
Front side µbumps



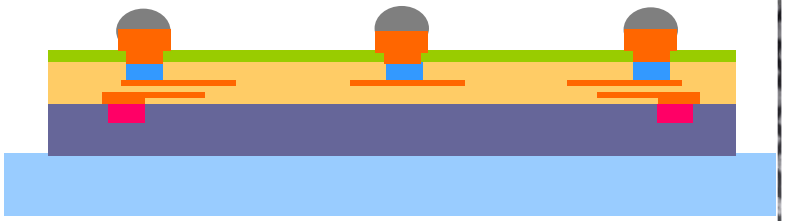
Temporary bonding



Thinning to 100 µm
Once thinned runs 3, 4 and 5 will have backside compensation material deposited prior to de-bonding



Debonding



Taping & deliver to ADVACAM for dicing

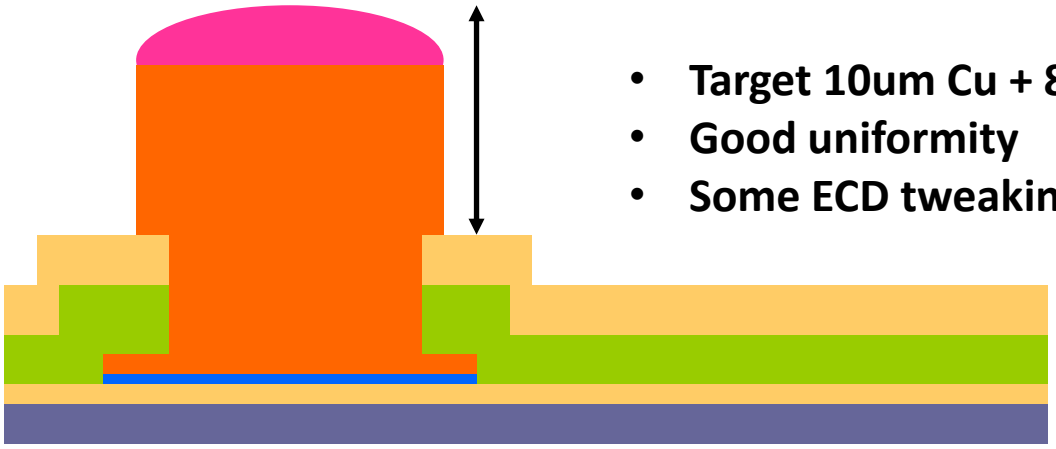
µBump ECD
Process control – Height measurement

			16.64					
		16.59	16.92	17.27				
18.57		17.33	17.16	17.7	17.9			
		17.15	17.23	17.19				
			17.66					
			P24					

mean=17.33µm – unif = 3.18%

			16.76					
		16.92	17.57	16.02				
18.4		17.21	17.49	17.1	18.6			
		17.85	17.55	17.46				
			18.36					
			P25					

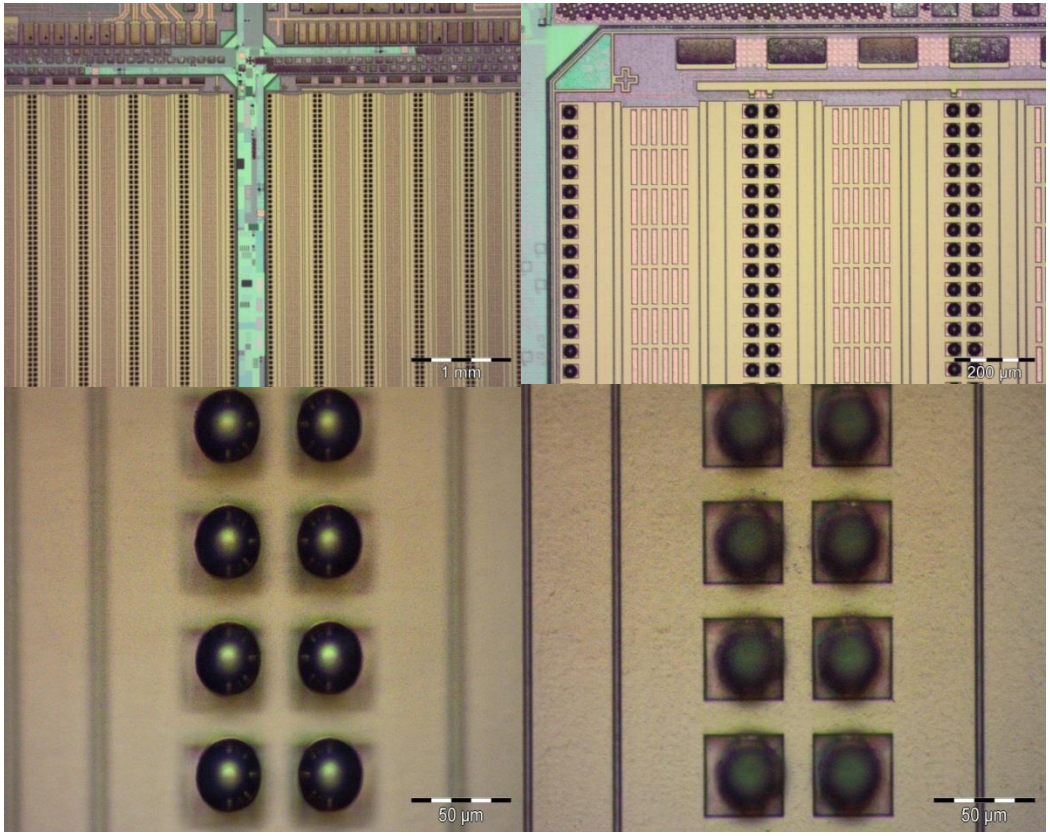
mean=17.48 – unif=4.08%



- **Target 10um Cu + 8um solder**
- **Good uniformity**
- **Some ECD tweaking would improve this more**

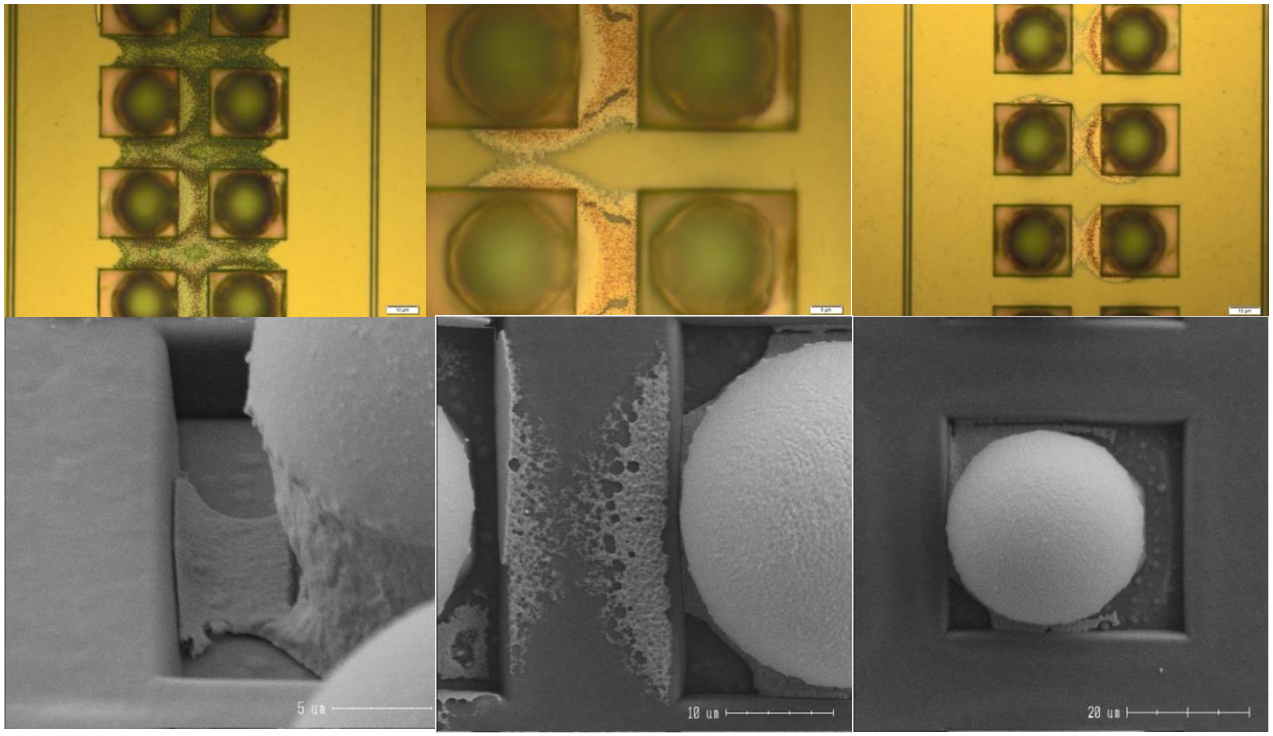
ECD = Electro-Chemical Depostion

Wafer inspection post µBump solder reflow and seed etch



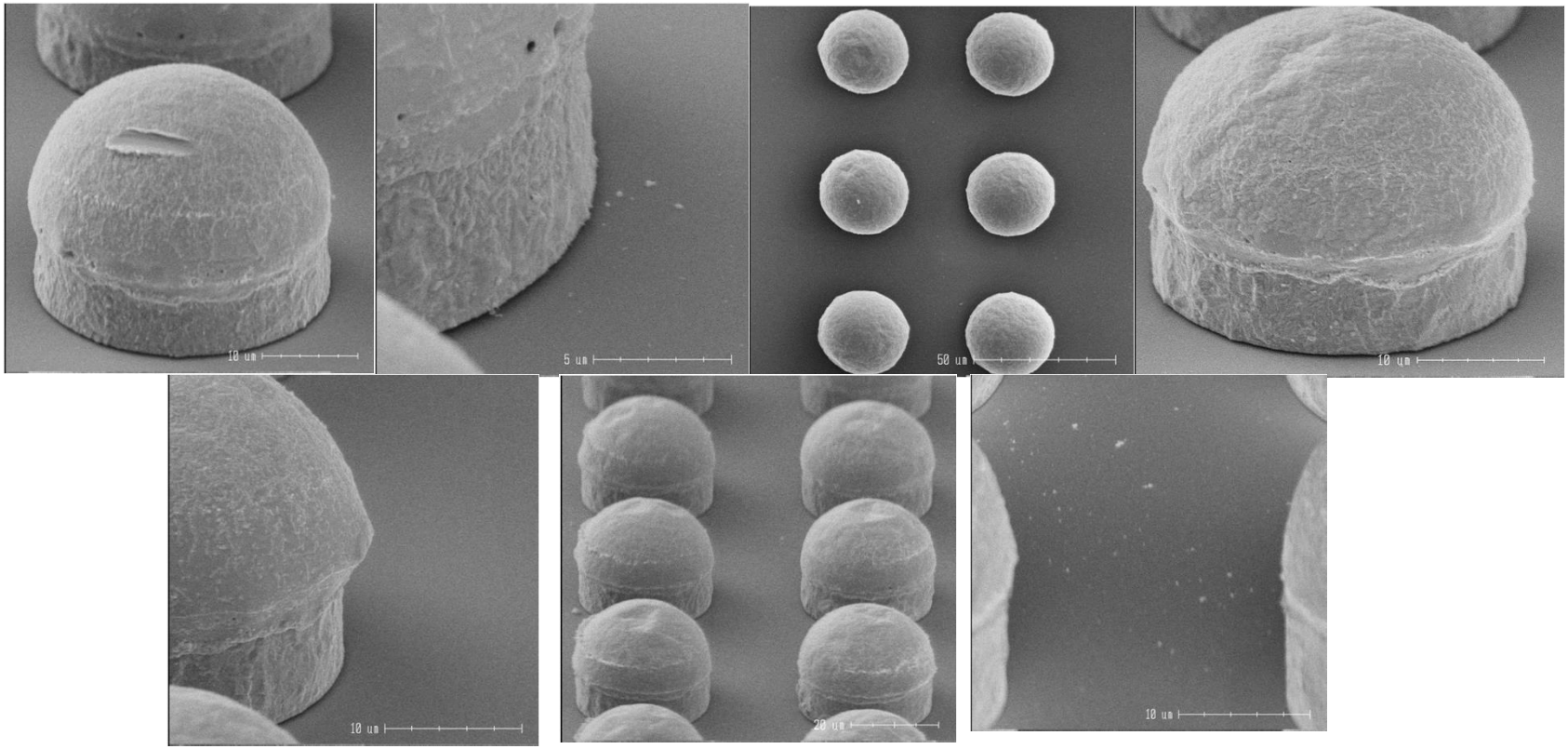
- **Seed layer etch + reflow**
- **2 probes resistance measurement =~2.5 Ohm on 2 µbump chain on top metal**
- **Both wafers looked good with seed etch clear in fields and no metalic residue between bumps**

Process defects as observed optical and SEM defect gallery



- **Residual metal observed between bumps both on FEI4Bs and blank process monitors**
- **Localised to the centre of the wafer only**
- **Lead to shorting between bumps**
- **All processing was put on hold on FEI4B and all work transferred to wafer blanks to resolve the problem**
- **Seed layer etch conducted in a cassette loaded bath (all wafers etched together)**
- **2 out of 13 wafers were affected by this.**

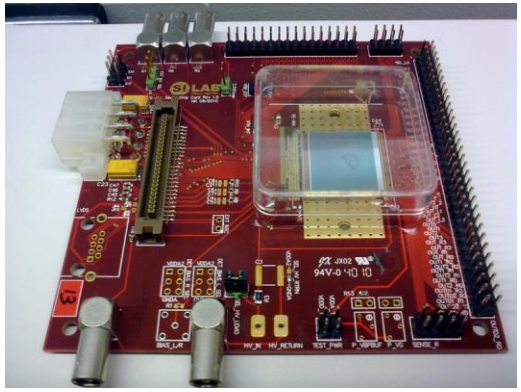
Short loop results on planar Si wafers
SEM defect Gallery



- **Residual metal issue resolved with a combination of improved resist strip and Cu/Ti seed etch optimisation**
- **Some remaining isolated metal particles but no shorting between bumps**
- **Agreement to release FEI4B wafer processing and resume project**
- **LETI will continue to improve their processes in the background**
  - **They also believe that bump density plays a role**

Module Results for full thickness FEI4b chips

- Flip chipping conducted at ADVACAM to demonstrate front side processing and bump-bonding
- Boarding mounting and testing at Liverpool*
- Threshold tuning of all the available working modules to date
- Data at 3200e used for estimating the number of dead, unconnected, noisy and stuck pixels in these modules.



Module ID	*Dead pixels*	*Cut = 30*
ADV-DC-1	**2**	**3**
ADV500-DC-2	**2**	**3**
ADV2000-DC-2	**1**	**0**
ADV2000-DC-1 *untuned*	**4**	**9**

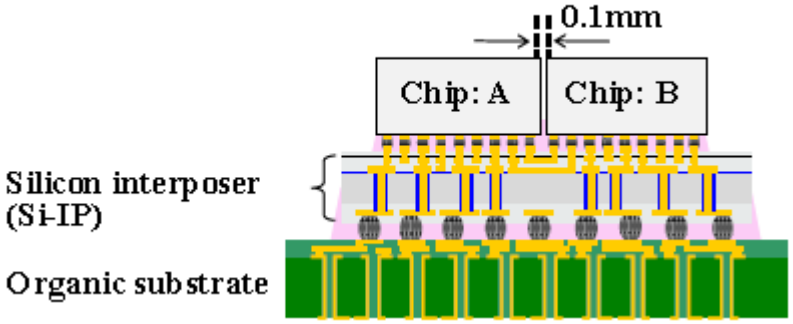
Defect rate of 0.04% observed so far we will have more module data soon

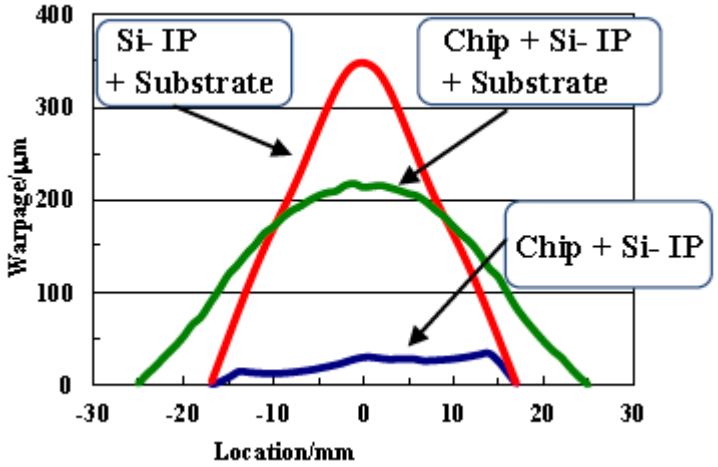
Marko Milovanovic et al. Pixelfest Manchester 2013

Papers already published by LETI using their Si-IP technology

Warpage Control of Silicon Interposer for 2.5D Package Application

Kei Murayama1, Mitsuhiro Aizawa1, Koji Hara1, Masahiro Sunohara1, Ken Miyairi1, Kenichi Mori1, Jean Charbonnier2, Myriam Assous2, Jean-Philippe Bally2, Gilles Simon2 and Mitsutoshi Higashi1
1 SHINKO ELECTRIC INDUSTRIES CO., LTD.
2 CEA, Leti





Overall package	Item	Dimension
Chip	Size	10x10x0.75mm
	micro bump(Pitch/Solder)	50μm/SAC305
Silicon interposer	Size	26x26x0.1mm
	TSV(Diameter/Pitch)	10/50μm
	Metal layer(Chip side)	2 layers
	Metal layer(Substrate side)	1 layer
Organic substrate	Size	40x40x1.0mm
	Core thickness	0.8mm
	FC bump(Pitch/Solder)	500μm/Sn57Bi
	BGA Pitch	1mm

The full assembly was successfully processed using conventional mass reflow process and assembly equipment.

Three kinds of warpage control technique as below were performed and they were found to have small warpage and to show high reliability.

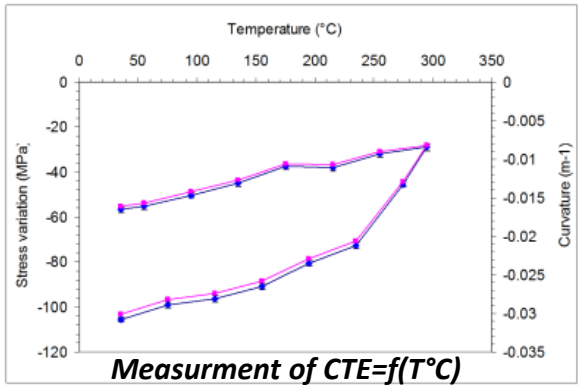
-Chip first process for silicon-interposer assembly.

-Using underfill material of low Tg and high storage modulus for 0 level assembly.

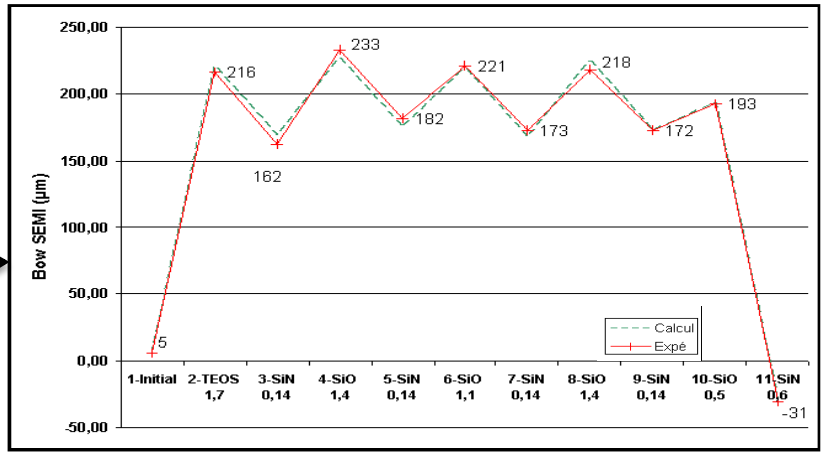
-Using Sn57 Bi solder joining for 1 level assembly.

Stress compensation studies at Leti

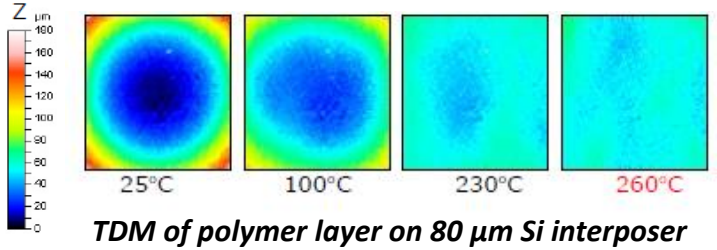
- **Basic characterization of thin film material:**
  - **CTE measurement vs temperature with RX diffraction (high sensitivity and accuracy method)**
  - **Young modulus extraction with nano-indention method**
- **Work at wafer level: measurement and modeling of bow evolution with temperature with stacked deposition layers**
- **Work at die level (20x20 mm to 30x30 mm): Topography and Deformation Measurement (TDM) to vaildate the behavior of die bow with temperature**



Measurment of CTE=f(T°C)

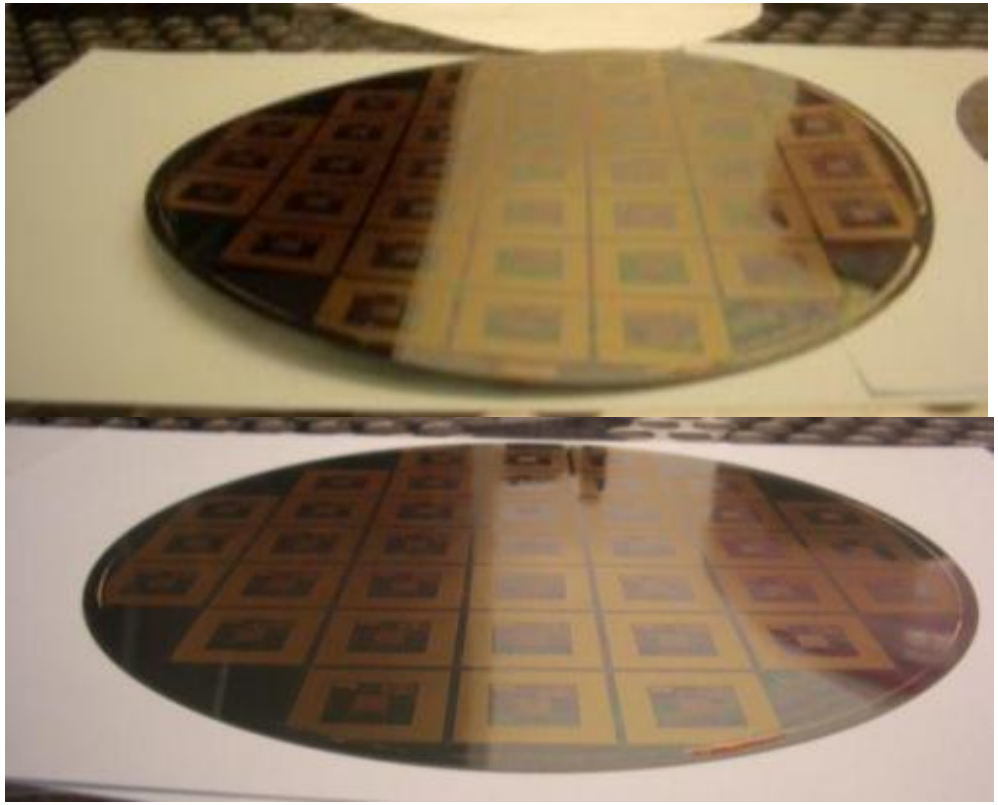


Modeling vs experiment of interposer

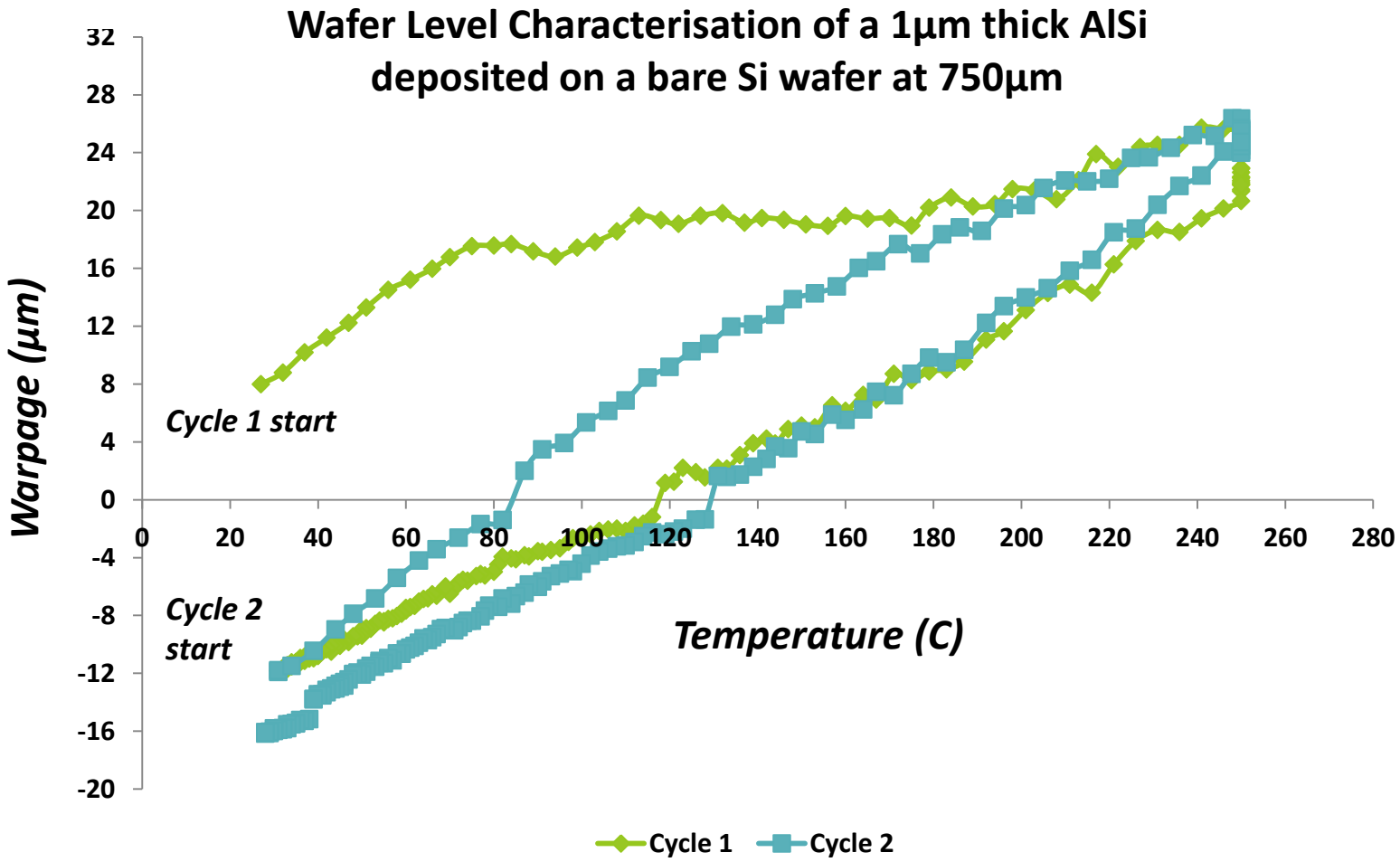


TDM of polymer layer on 80 µm Si interposer

CEA-LETI Interposer with backside compensation



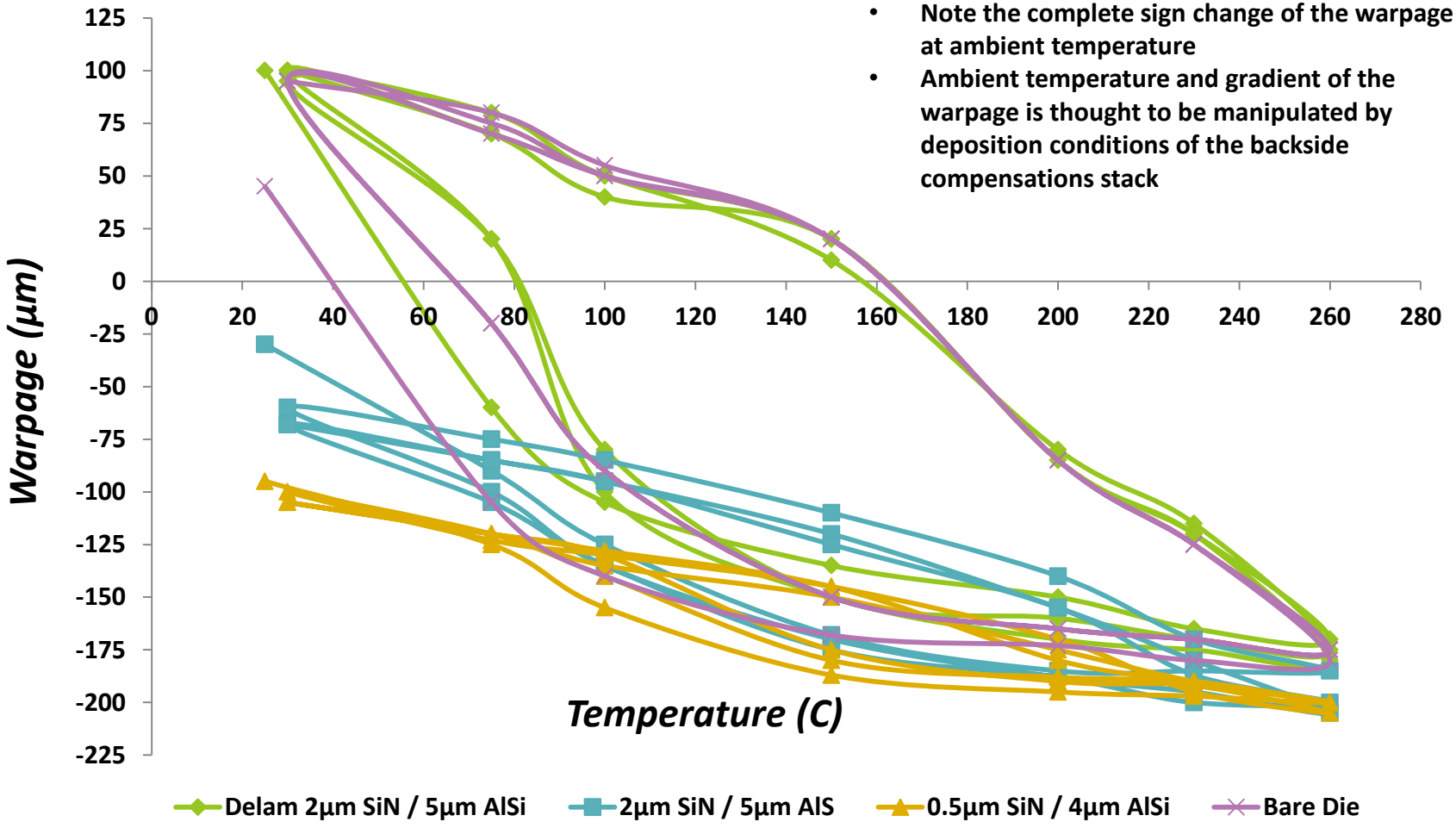
- **5.5mm bow after front-side processing on a 50um thick wafer**
- **Wafer pulled flat after backside compensation applied**



- AlSi plastic deformation during initial temperature ramp up
- Good linear behavior during second thermal cycle
- Modulus (from nanoindentation measurement) = 45 Gpa, CTE is estimated ~ 18 ppm
- Wafer level measurements conducted using a Flexus

TDM Measurements of 100µm thick FEI4B Die thermally cycled to 260C

- Warpage amplitude greatly reduced by almost 3x
- Note the complete sign change of the warpage at ambient temperature
- Ambient temperature and gradient of the warpage is thought to be manipulated by deposition conditions of the backside compensations stack



Summary

- >99% yield demonstrated for bumps on full thickness wafers
  - Some residual effects at seed etch that requires finer process tuning but doesn't affect module performance
- Front-side processing of FEI4B wafers at LETI has been successful on 11 of the 13 FE-I4b wafers
  - More wafers are needed to help LETI develop and fine tune their processes
- Initial back side stack shows promising results to compensate for the CMOS front-side CTE mismatch on chips with a 100µm thickness
- Development still under way
  - Backside stack starting bow and thermal cycle gradient is believed to be tuneable by the deposition conditions
- Back-side compensation is good for production:
  - Wafer level approach
  - Less expensive than single module mechanical approach
  - Higher throughput
- Back-side compensation ought to make the module more robust against any thermal excursions in the experiment
  - Modules could be affected by this as both ROIC and sensor become thinner
- We believe LETI to be a viable vendor for this type of work and collaboration will be on-going to further develop this approach and fine tune the processing on the FE-I4b wafers.