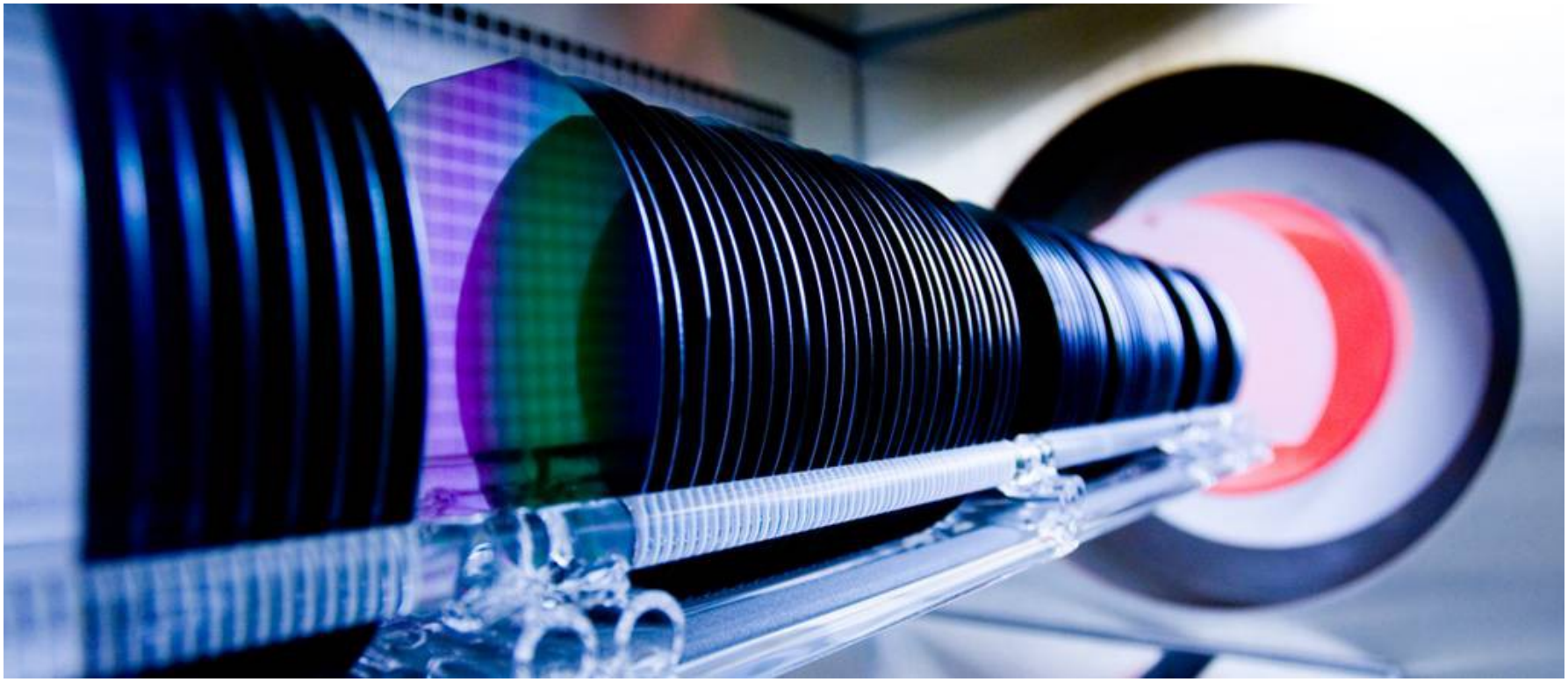

Future Sensor Production and Sensor-Chip Packaging Technologies at CiS

Forschungsinstitut für **Mikrosensorik** und **Photovoltaik** GmbH

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Tobias Wittig, 9th Trento Workshop Genova, 26.02.2014

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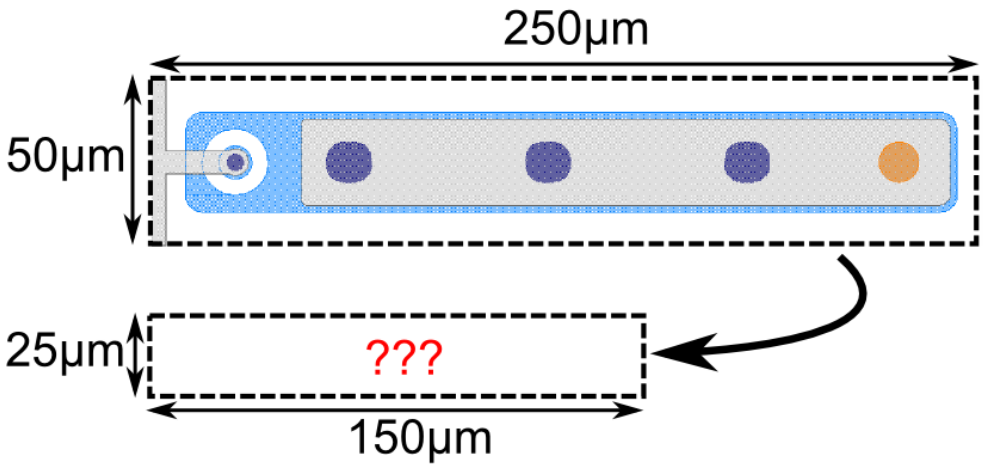
in cooperation with

technische universität dortmund

challenges under HL-LHC-conditions e.g. ATLAS

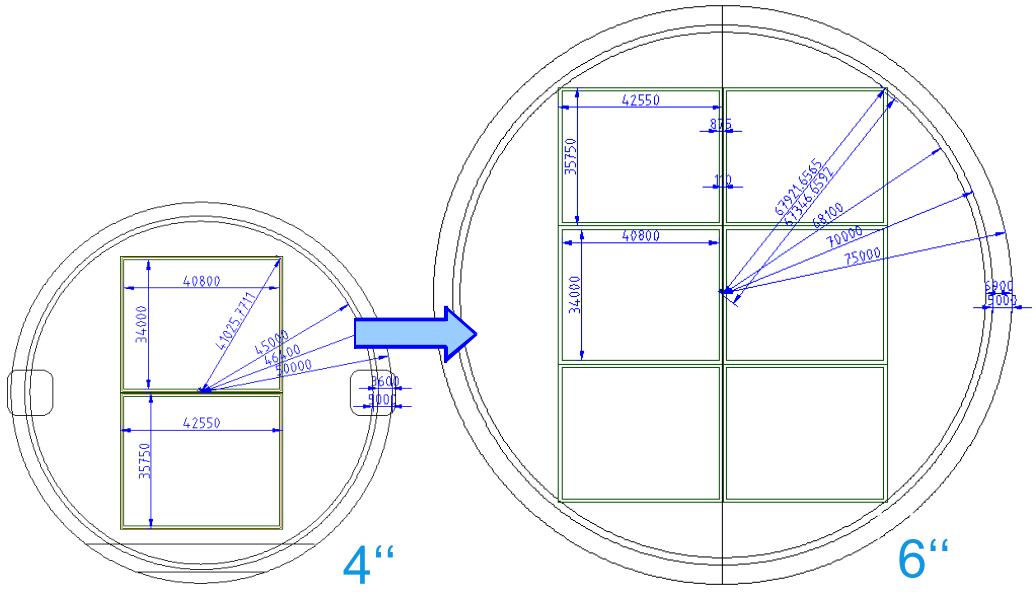
inner layers

- massive irradiation exposure
  - smaller thicknesses for planar sensors
  - design optimization
  - defect engineering
- small pixel dimensions
  - pitch of 25um
  - design minimization



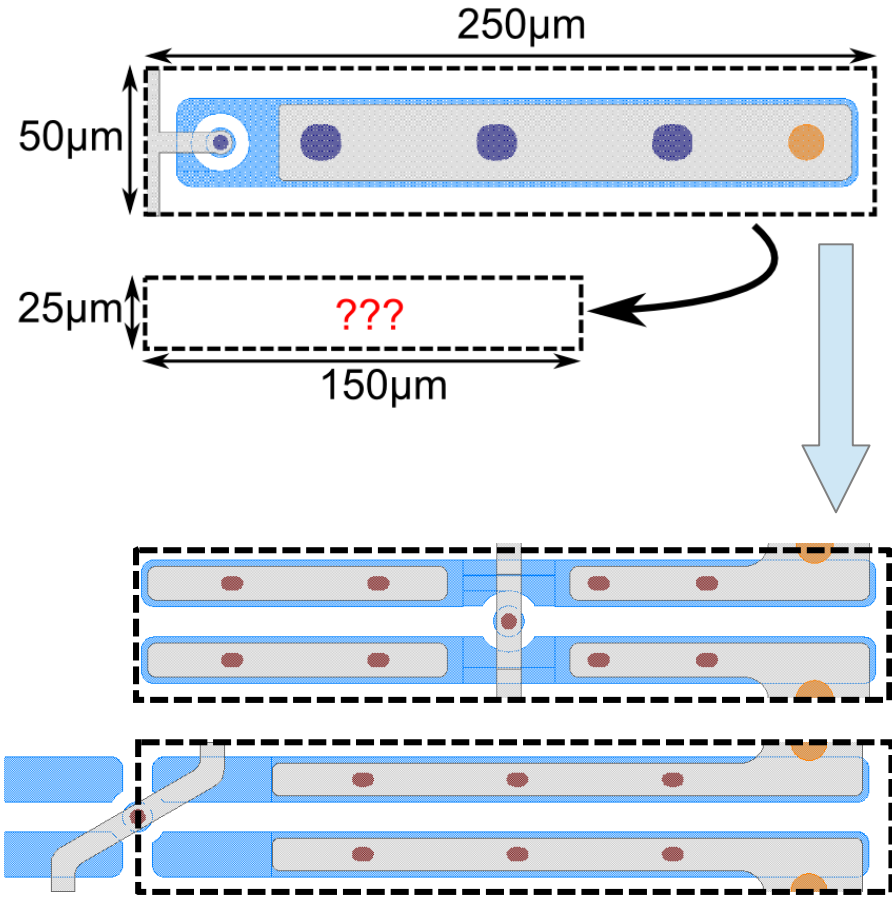
outer layers

- production of large area silicon
- possible areas:
  - pixel detector: 8.2m²
  - strip detector: 193m²
- cost reduction by production on 6“ wafers
  - relatively less non-used area



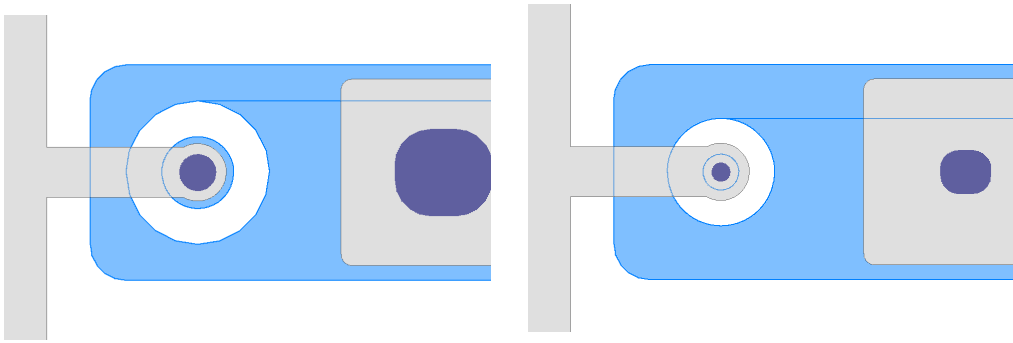
sensor design challenges

- smaller pitch aswell represents challenge to future sensor designs
- esp. conventional bias grid is not usable anymore
- testing different bias grid versions on current wafer productions
- variations of
  - bias dot position
  - bias dot diameters
  - pixel implant width



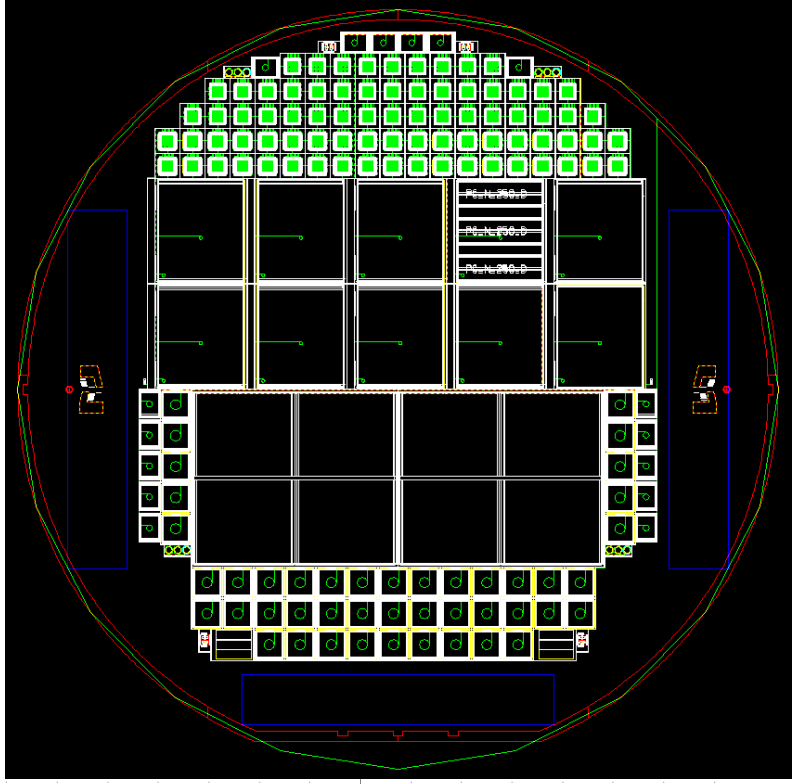
laser direct imaging (LDI)

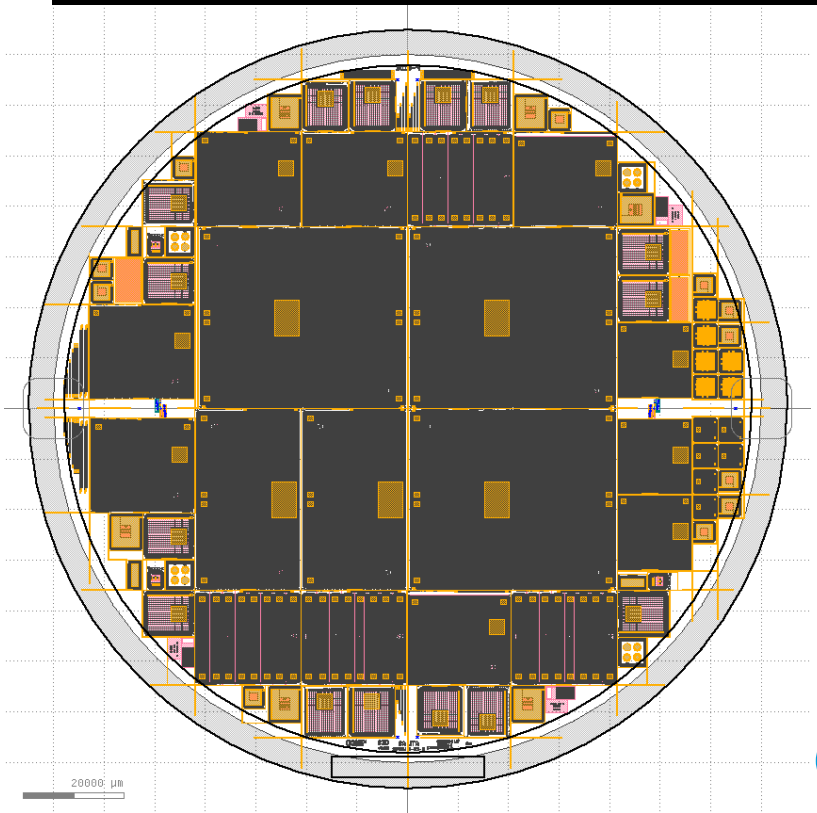
- alternative to the currently used projection exposure
- no masks necessary anymore
- expect to be able to process smaller dimensions (O(2-3um))
  - implantations
  - oxide openings
- current production combines projection exposure and LDI



6‟ productions

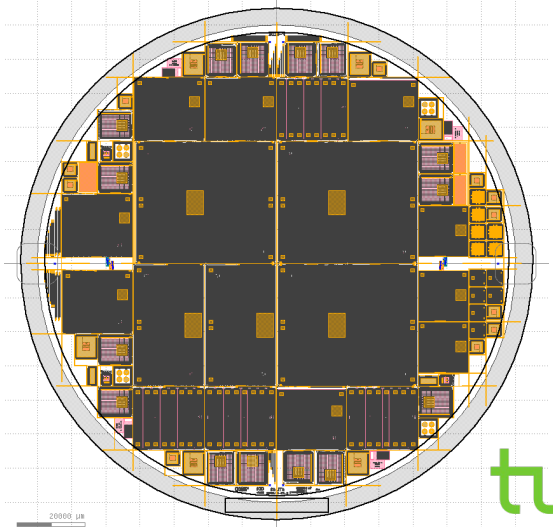
- changeover to a 6‟ processing line is inevitable for a cost efficient large scale sensor production
- first steps are already done at CiS
  - first 6‟ n-in-p production for MPP Munich processed and delivered
    - 270um thickness
  - first 6‟ n-in-n production started right now (see next slide)
- at the time being, several processing steps are outsourced (MPI Halle)
- planned to conduct as many steps as possible in-house in the future





6" n-in-n production

- 500um thickness
- predominantly ATLAS pixel sensors
  - FE-I4 Quads, Alpines, pseudo-Hex possible
  - FE-I4 SCS, several versions
    - bias grid variations
    - extreme slim edge design
      - investigate if inactive edge of 50um is possible
- MediPix/TimePix & DosePix sensors
- test structures
  - systematic variations of bias grid dimensions
  - find out the minimal structure size which can be reached
    - with conventional projection exposure
    - with laser direct imaging



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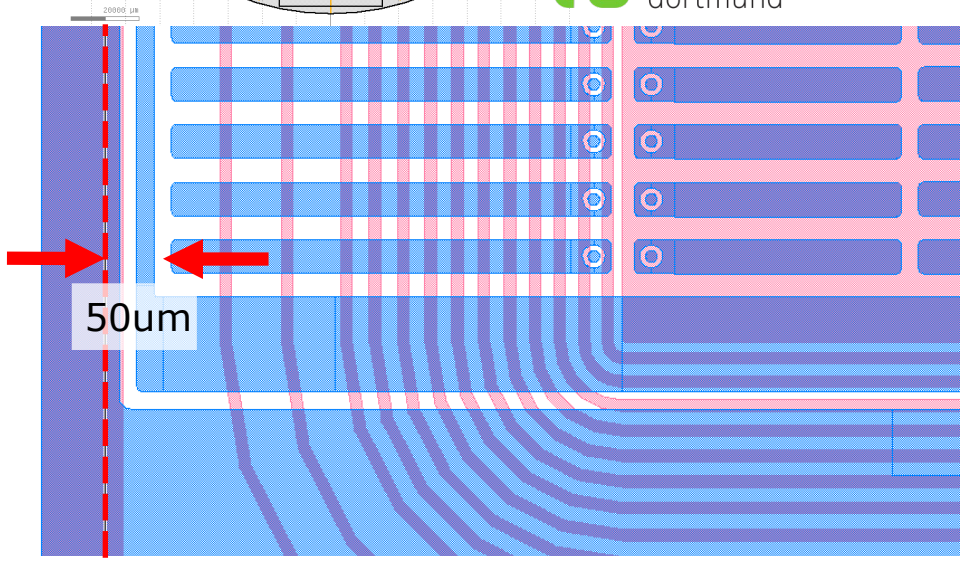
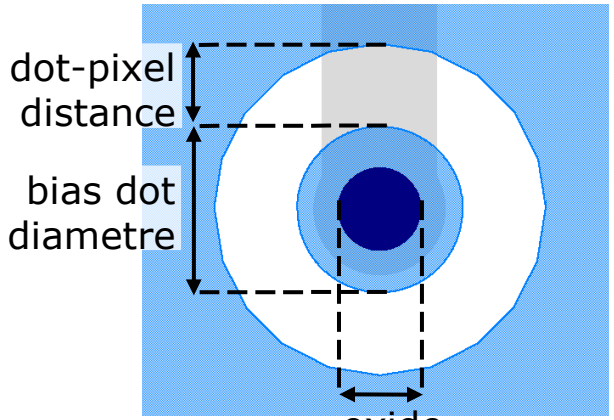
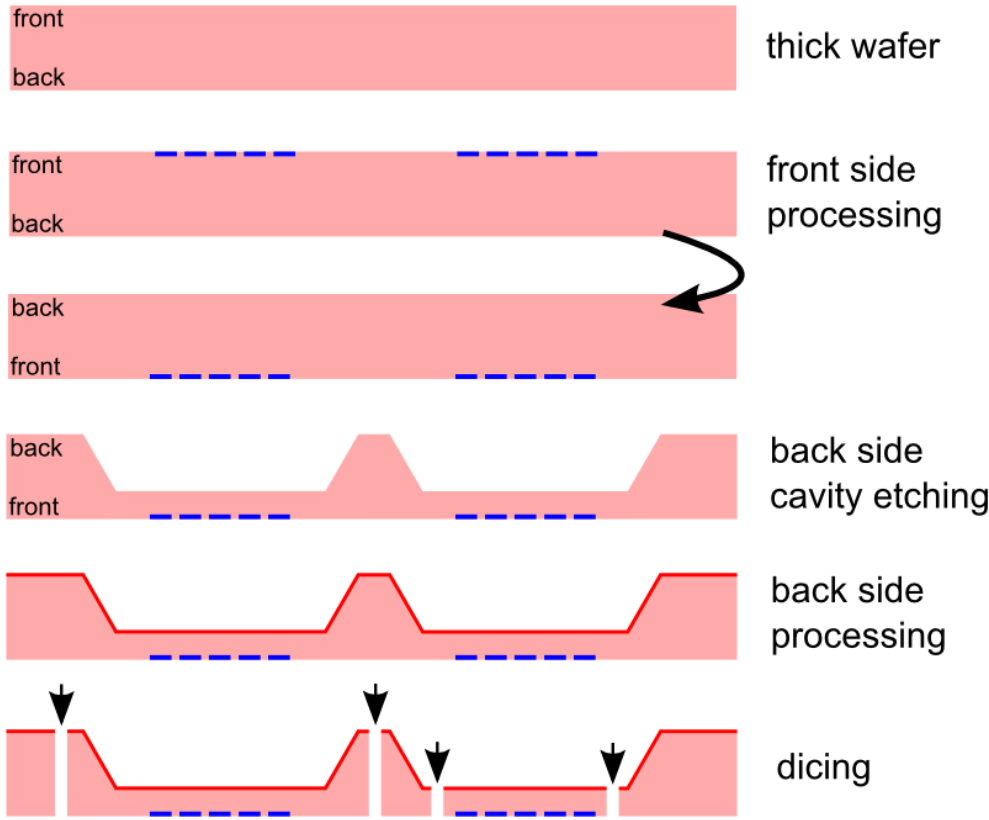




reduction of sensor thickness

- smaller thickness is advantageous for planar sensors after high irradiation
- wafers getting extremely fragile with thicknesses <150um, esp if 6“ sizes are desired
- alternative to handling wafer can be etching of cavities to backside (<100> bulk)
- guarantees stability on wafer level by thick frames at the sensors edges
- sensitive area is located at the ‚membrane‘: thickness down to 50um should be feasible
- dicing can be done at the thick frames or within the cavity
- technology well known from pressure sensors
- process should work out for single sided sensors
- challenging to structure back side within the cavity (for double sided sensors)



3D sensors

- geometrical advantages of 3D sensors compared to planar sensors are obvious
  - large volume of charge generation
  - small drift distances
- should technically result in a better radiation hardness
- CiS is planning to do initial steps towards the processing of 3D sensors
- new project in preparation, plans:
  - simulation/optimization of the layouts
  - determine challenges
    - etching of pillars (ICP etcher)
    - homogeneous doping of the pillars
    - properties of the interface within the pillars
  - maybe alternatives to Poly-Si deposition?
    - Spin-On
    - vapor deposition
  - concept of testability on wafer level

- cooperations with other institutes/universities very welcome

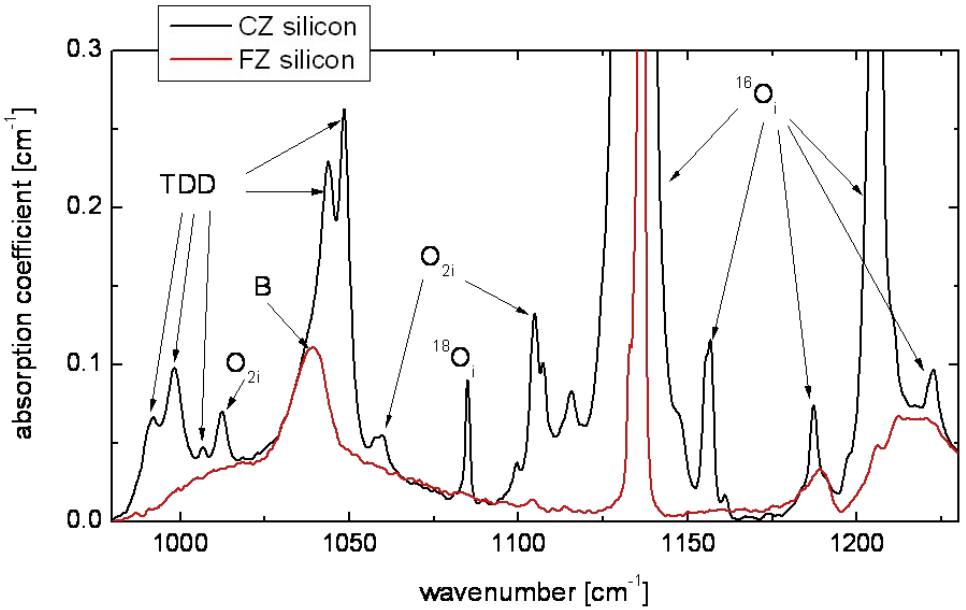
defect engineering

new project in preparation:

- improvement of the radiation hardness of silicon sensors by defect engineering

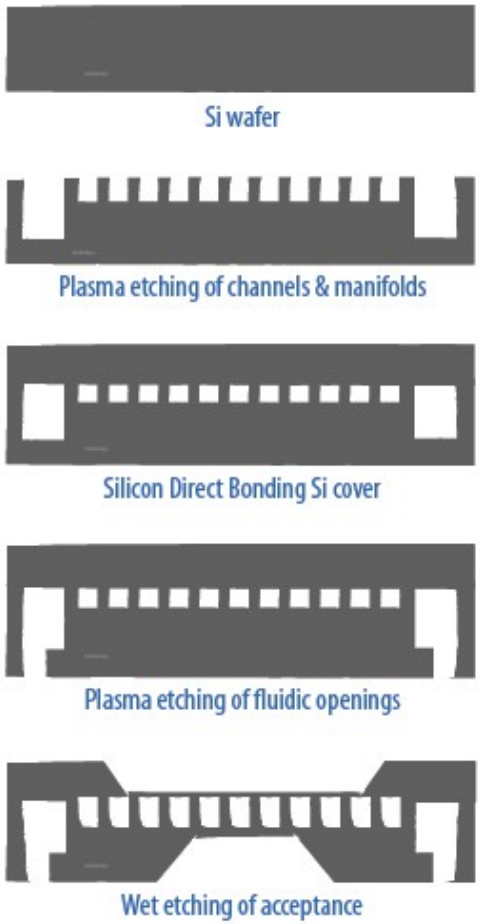
plans:

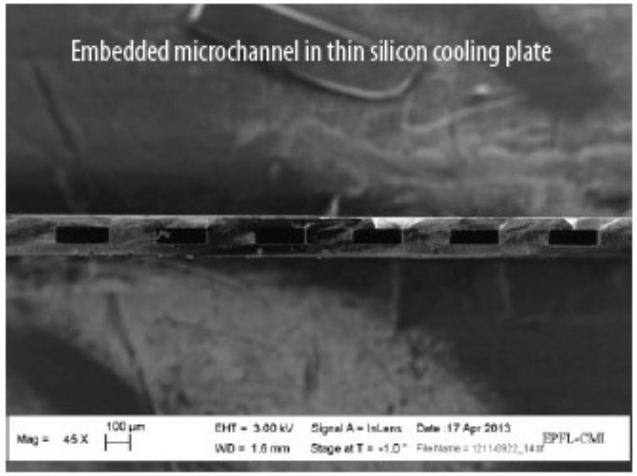
- analysis of defects in silicon during and after the processing, possibly also after irradiation
- investigation of the reason for increase of radiation hardness by oxygen
- optimize the defect configuration
  - investigate effect of other elements for bulk enrichment
  - adaption of essential process steps
    - influence of thermal budget to the oxygen defect configuration
    - influence of thermal donors
    - tempering
    - dielectrical layers
- tools:
  - simulation
  - charge carrier life time
  - low-temperature FTIR
  - DLTS

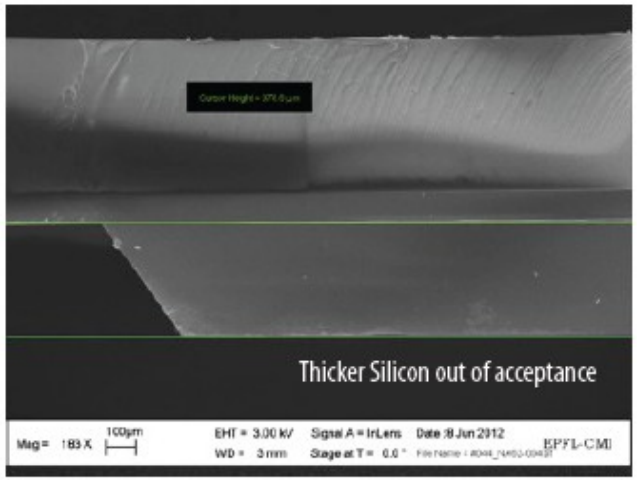


micro channel cooling

- etching of pipes into wafer should be possible at the end of this year (ICP etcher)
- technologies for remaining steps are already existing
- long-term research project is planned

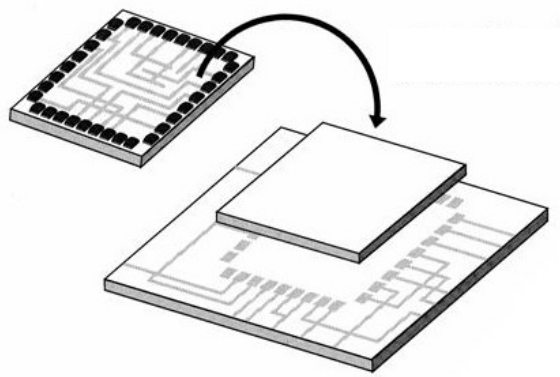






sensor chip packaging

- involvement of CiS ended after wafer production
- idea: participate at the sensor/module processing as long as possible, i.e. up to bump bonding assembly step
  - technological requirements are present
    - outsourcing
    - in-house
  - reduction of unnecessary steps: packaging, shipments
  - technological value added
  - possibility of providing
    - flip-chip-able sensors
    - complete sensor-chip assemblies



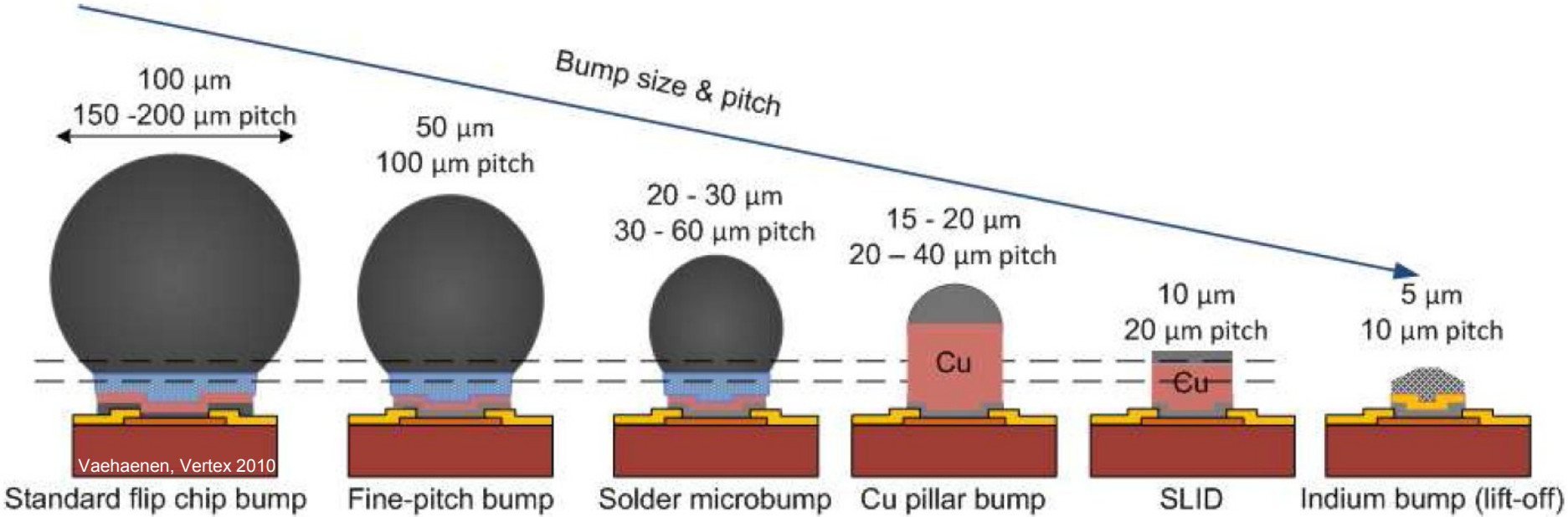
challenges for future bump bonding concepts

large radii

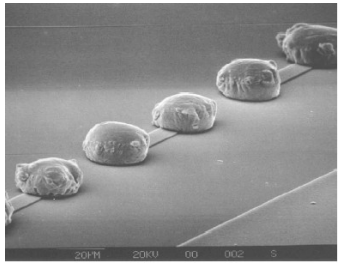
- bump bonding still one of the main cost driver
- cost reduction is essential
- batch wise processes preferable
- minimization of dimensions is secondary

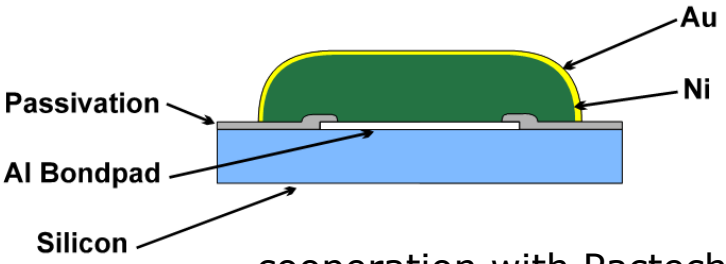
small radii

- minimization of bump size & pitch
- e.g. ATLAS:
  - pitch 50µm -> 25µm
  - => bump size < 25µm
- radiation hardness

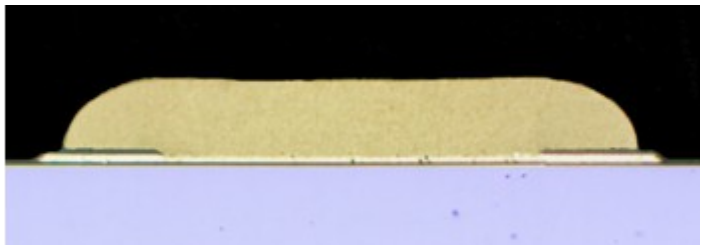


bump bond technologies



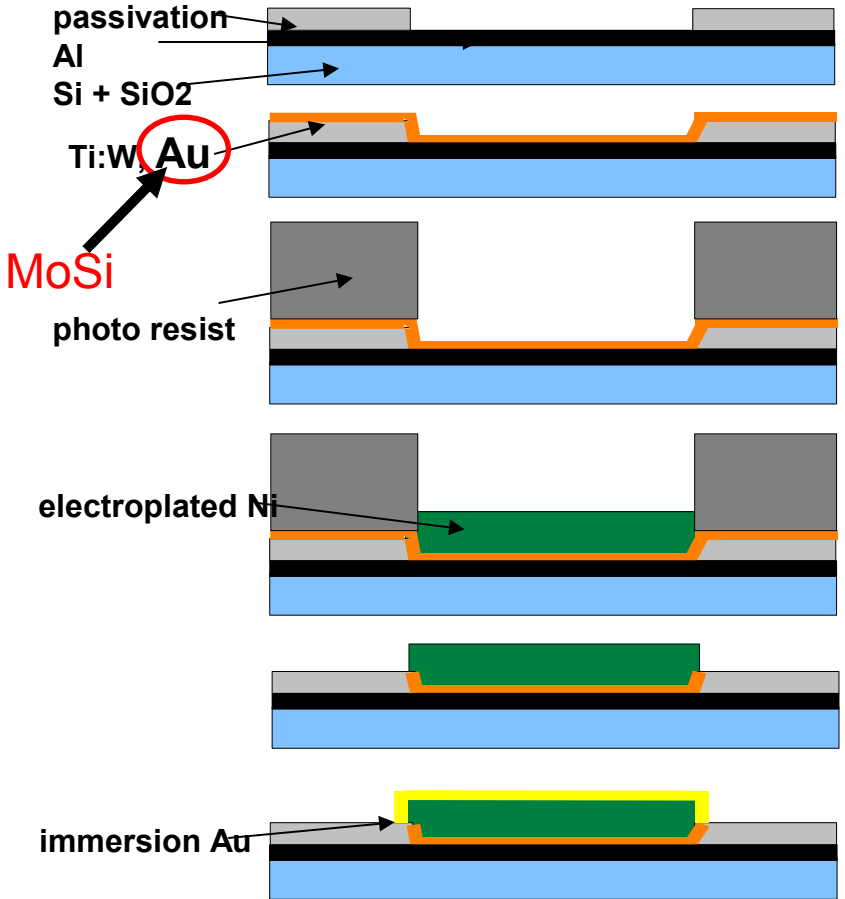


cooperation with Pactech



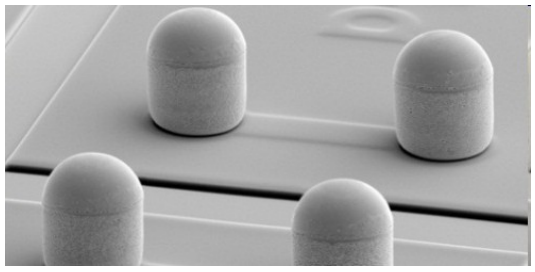
electroless Ni-UBM + solder ball bumps

- wet-chemical
- passivation is used as a mask, no additional mask necessary
- optimizations of
  - AlSi quality
  - pretreatment steps
  - Ni-electrolyte for very small pad openings



MoSi based electroplating

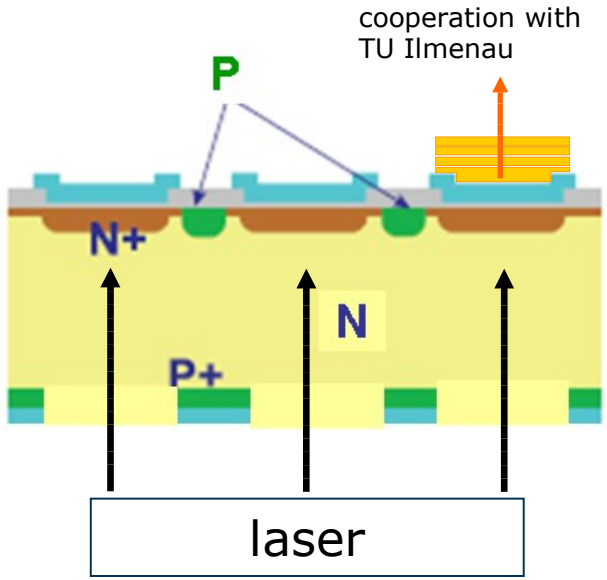
- Au/Cu plating base can be replaced by MoSi
  - properties are expected to be similar
- process could be conducted completely in-house



bump bond technologies

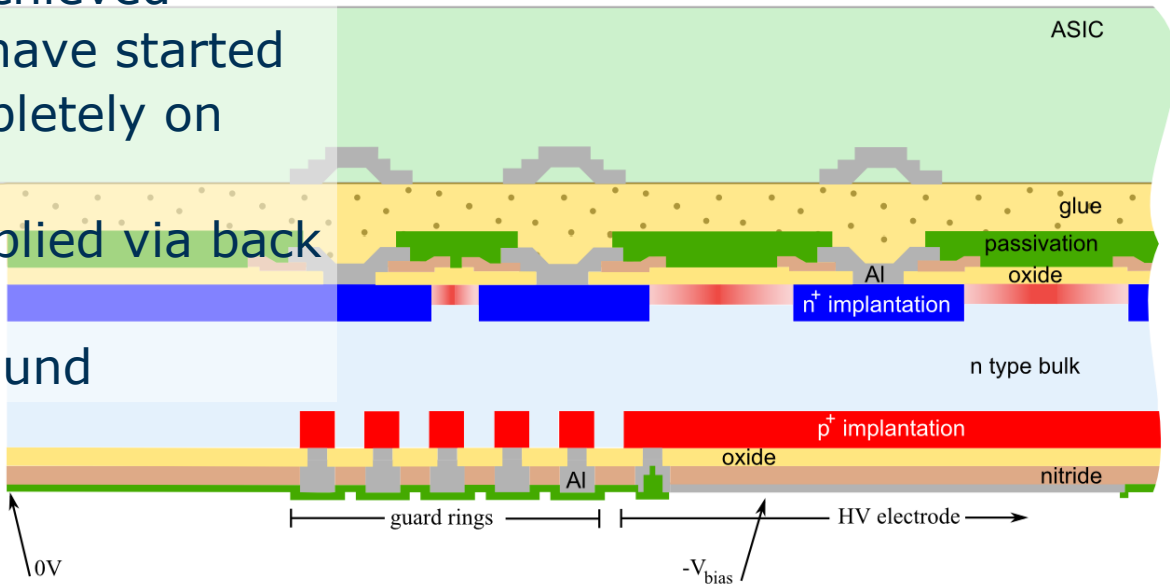
LIP-Ni - light induced plating

- concept from photovoltaics sector
- epitaxial growth of the UBM is stimulated by a laser
- UBM is only growing on the passivation openings
- no additional process steps necessary
  - no plating base / resist
  - no stripping / etching
- less cost & time consuming



capacitive coupling

- sensor and ASIC are glued together
- significant cost reduction could be achieved
- initial tests with CiS n-in-n sensors have started
  - advantage that pixel side is completely on ground potential
  - HV & ground potential can be applied via back side
  - Uni Bonn, Uni Geneva, TU Dortmund



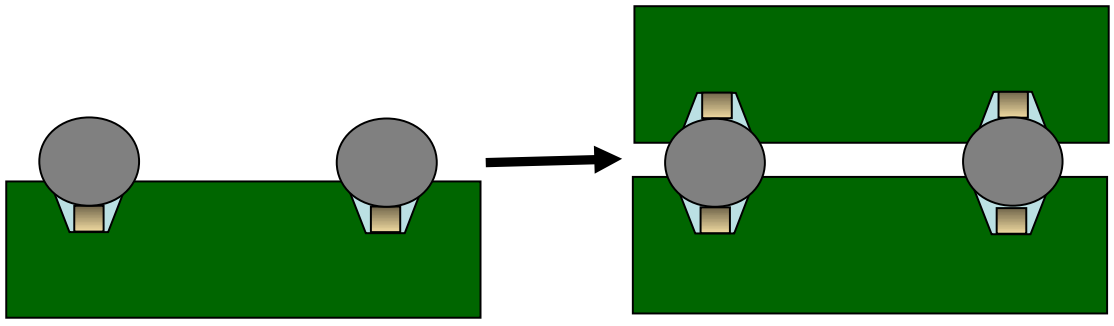
conclusion

- CiS is planning to deal with various challenges of future HEP experiments
  - sensor technology
    - 6“ production
    - design minimization
    - thin planar sensors
    - defect engineering for radiation hardness
    - 3D sensors
  - sensor chip packaging technology
    - cost reduction
    - minimization of the bump dimensions
    - various technological approaches are planned
    - as many process steps as possible should be done in-house
    - the possibility to produce complete sensor-chip assemblies is given

Backup

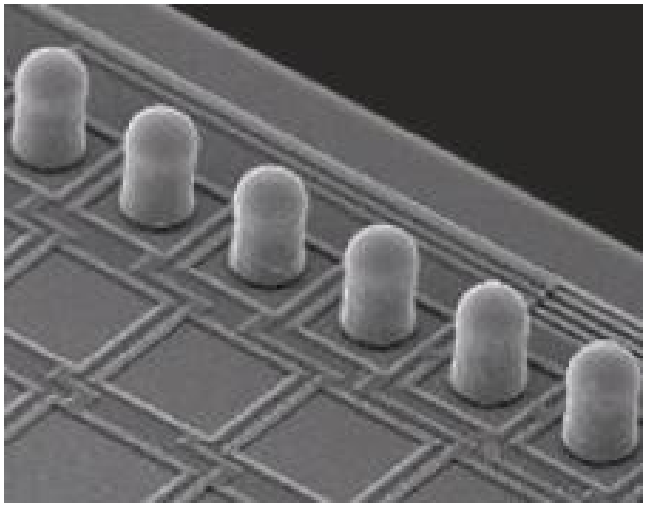
bump bond technologies
cavities

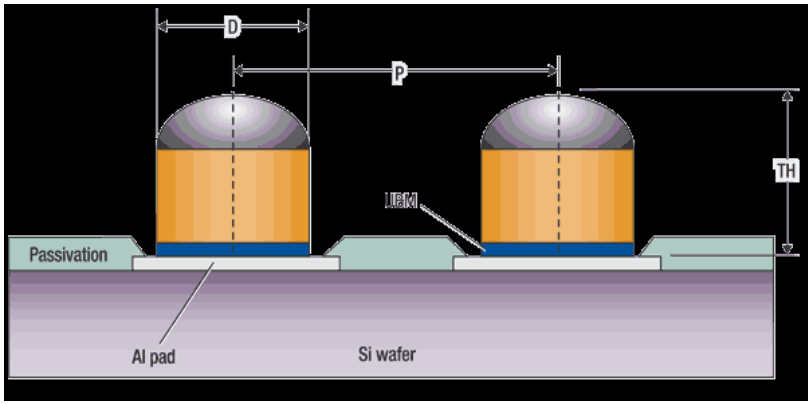
- option to place contact pads into a cavity
- simplification for flip-chip positioning? esp. if aiming at small dimensions
- if lowering of pads in cavities prove to be an advantage for flip chip positioning, cavities could also be implemented on ASIC by polymer layers
- experiences are existing at CiS from MST

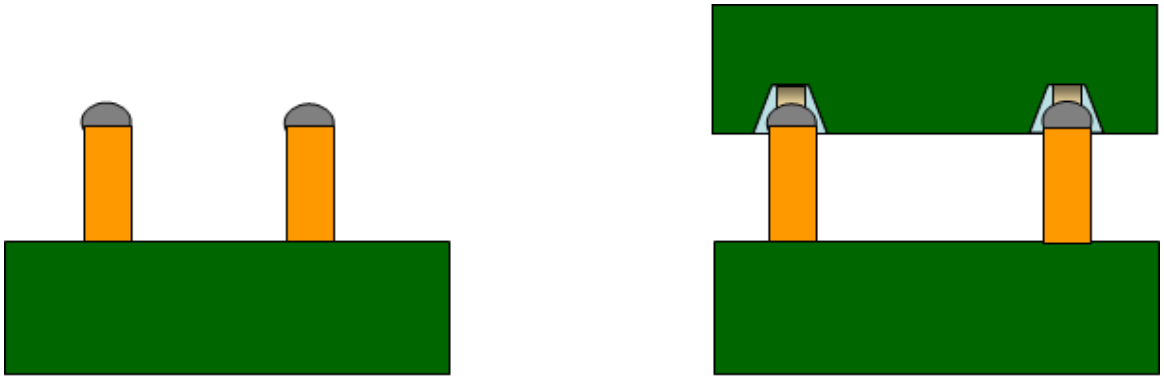


bump bond technologies
copper pillars

- building of pillars by combination of thick film lithography and electroplated copper deposition
- top is tin-coated, act as solder
- small diameter feasible
- esp. advantageous in combination with cavity contacts

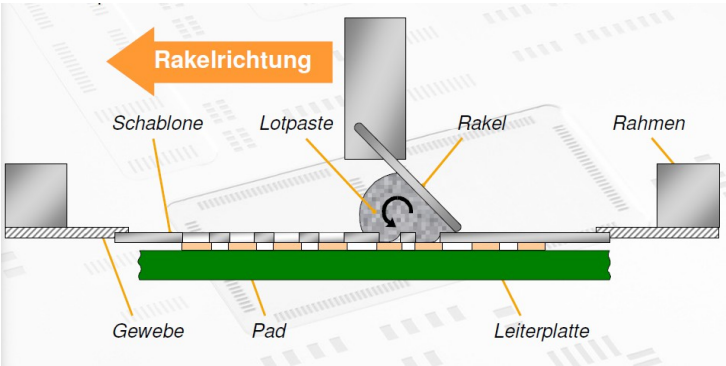






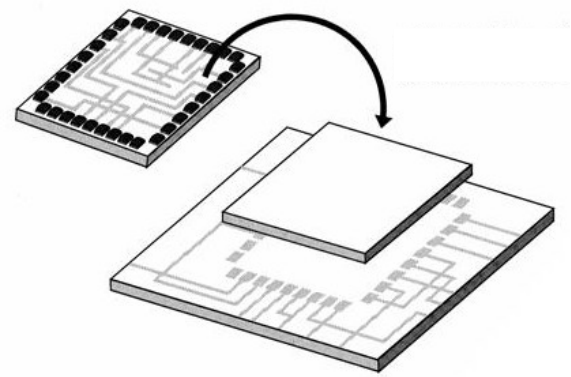
bump bond technologies
mechanical alternatives

- studbumping
  - e.g. on ASIC side in combination with Ni-UBM & Sn bump on sensor
- minimization of screen printing
- optimization of stencil printing
  - already available with 20µm openings
  - investigation of very fine-grained powder as solder paste



strategy for flip chipping

- testing of flip chip process itself
  - daisy-chain dummies
  - real sensors & ASICs



- testing of reliability
  - defect engineering
    - establish automatical optical inspection
  - stress tests
    - operation at low temperatures
    - fast temperature cycles
    - irradiations up to HL-LHC fluences