9th "Trento" Workshop on Advanced Silicon Radiation Detectors
Genova, February 26-28, 2014

Development of monolithic silicon pixel sensors for the ALICE ITS upgrade

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for the ALICE collaboration

Outlook

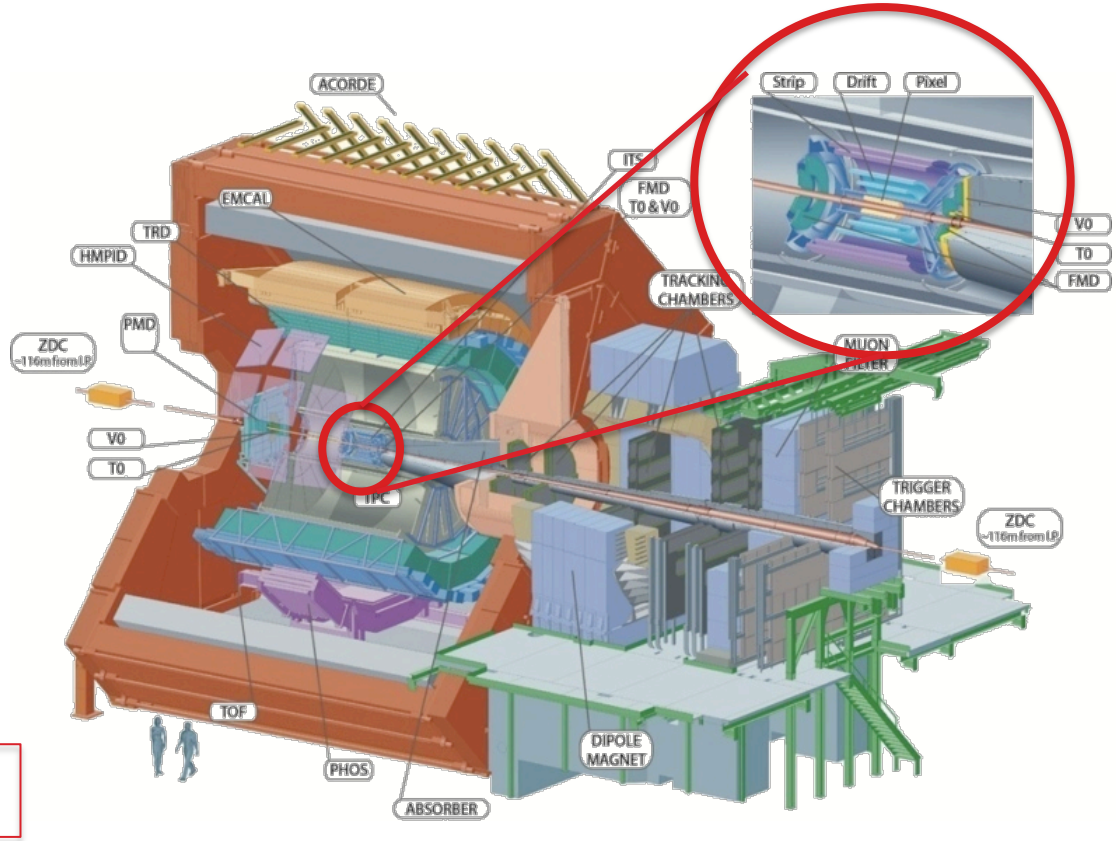
- The upgrade of the ALICE Inner Tracking System (ITS)
- Monolithic silicon pixel sensors for the ALICE ITS
- Recent results on prototype sensors

ALICE Upgrade

The ALICE upgrade during LS2 will allow doing high **precision measurements of rare probes at low p_T**, which cannot be selected with a trigger, require a **large sample of events recorded on tape** and **improvement on vertexing and tracking capabilities**.

→ Upgrade of ALICE readout and online systems

→ Upgrade of the Inner Tracking System



ALICE ITS Upgrade

Improve impact parameter resolution by a factor of ~3 (r-phi)

- Get closer to IP (39 mm) → 21 mm (layer 1)
- Reduce material budget (1.14 % X_0) → 0.3 % X_0 (inner layers)
- Reduce pixel size (50 µm x 425 µm) → O(30 µm x 30 µm)

High standalone tracking efficiency and p_t resolution

- Increase granularity and radial extension → 7 pixel layers

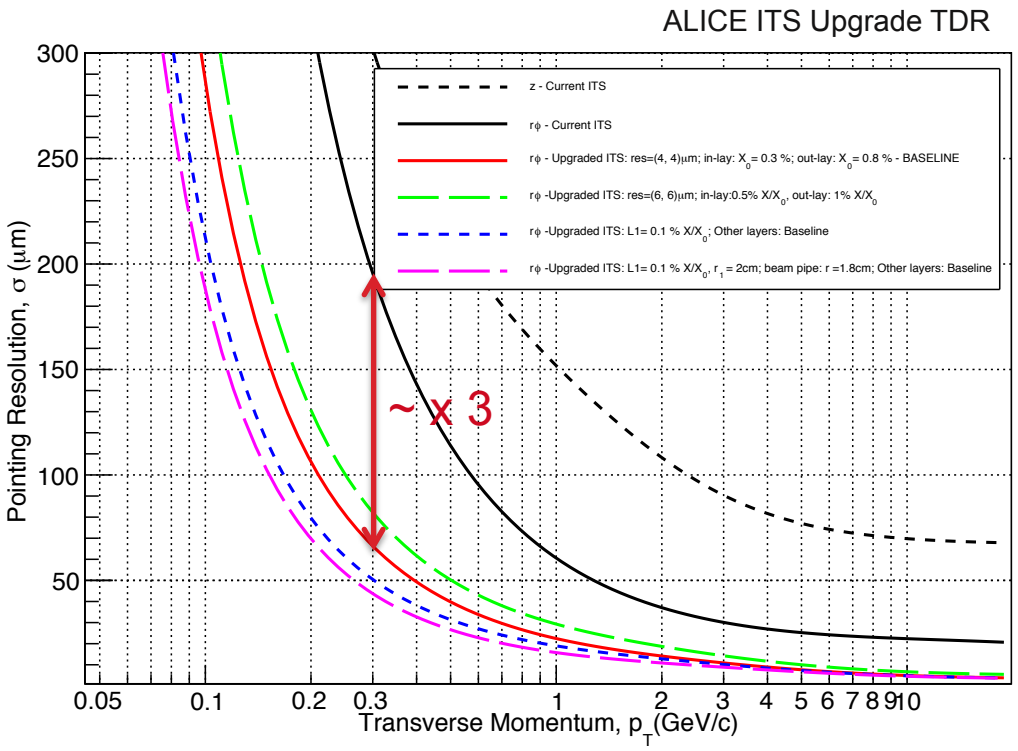
Fast readout

- Readout of Pb-Pb interactions at >50 kHz and pp interactions at several 10^5 Hz (now limited to 1 kHz with full ITS, and ~ 3 kHz without silicon drift)

Fast insertion/removal for yearly maintenance

- Possibility to replace non functioning detector modules during yearly shutdown

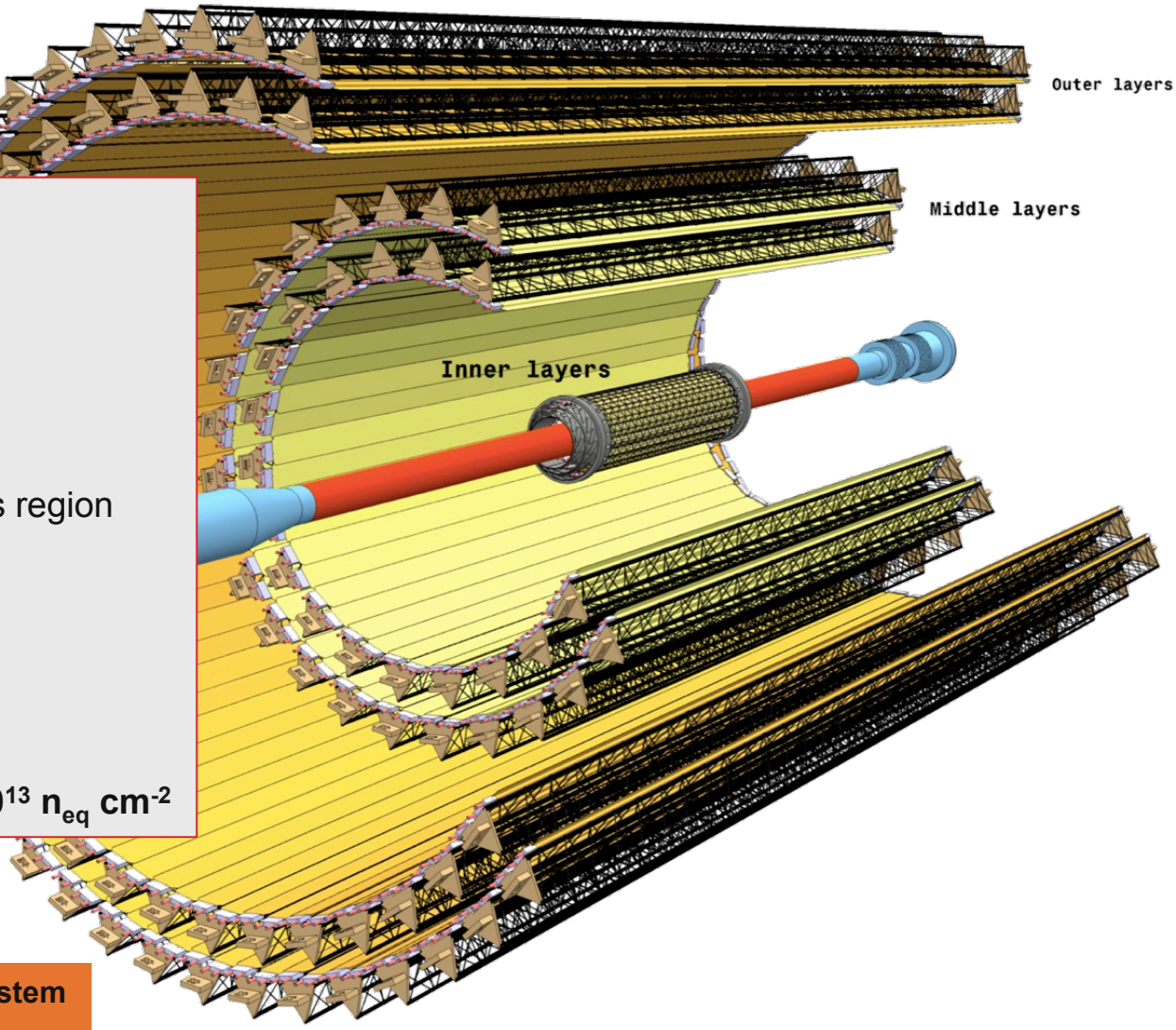
ALICE ITS Upgrade



- Very thin sensors
- Very high granularity
- Large area to cover
- Modest radiation levels

Monolithic silicon pixel detectors

ALICE ITS Upgrade



3 Inner Barrel layers (IB)
4 Outer Barrel layers (OB)

Radial coverage: 21-400 mm

~ 10 m^2

$|\eta|<1.22$ over 90% of the luminous region

0.3% X_0/layer (IB)
0.8 % X_0/layer (OB)

25 Giga-pixel tracker

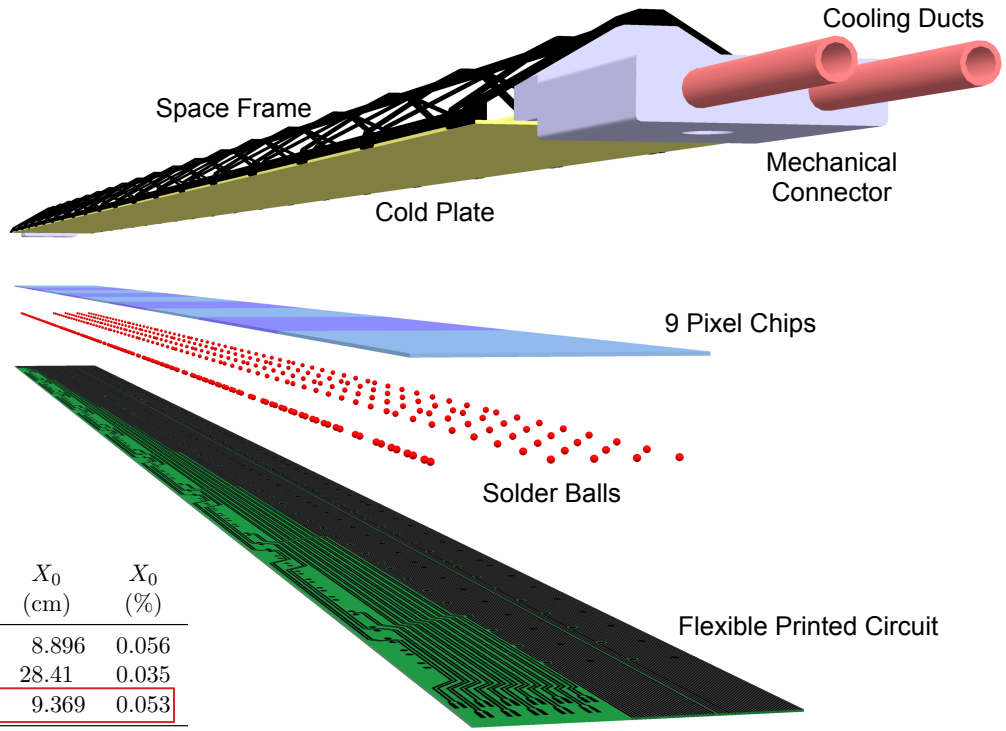
Radiation level (L0): 700 krad/10^{13} n_{eq} cm^{-2}

Upgrade of the ALICE Inner Tracking System
CERN-LHCC-2013-024 ; ALICE-TDR-017

ALICE ITS Upgrade

Light weight, compact modules:

- 50 µm silicon sensors connected via solder points to a 2-layer Al-polyimide flex cable



Inner barrel stave
ALICE ITS TDR

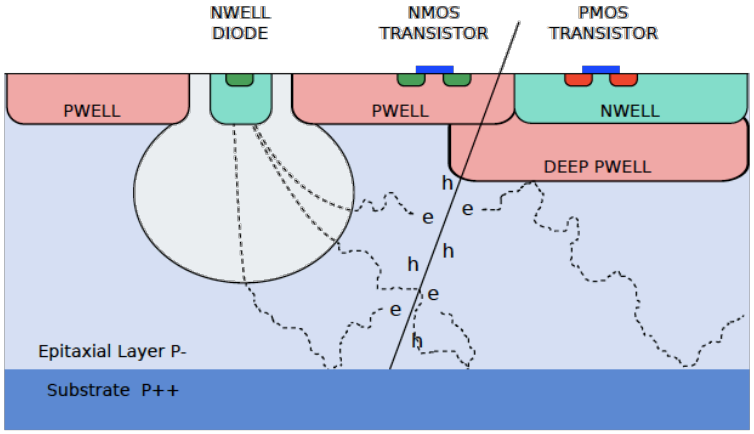
Stave element	Component	Material	Thickness (µm)	X_0 (cm)	X_0 (%)
HIC	FPC Metal layers	Aluminium	50	8.896	0.056
	FPC Insulating layers	Polyimide	100	28.41	0.035
	Pixel Chip	Silicon	50	9.369	0.053
Cold Plate		Carbon fleece	40	106.80	0.004
		Carbon paper	30	26.56	0.011
	Cooling tube wall	Polyimide	25	28.41	0.003
	Cooling fluid	Water		35.76	0.032
	Carbon plate	Carbon fibre	70	26.08	0.027
	Glue	Eccobond 45	100	44.37	0.023
Space Frame		Carbon rowing			0.018
Total					**0.262**

ALICE ITS Sensor Technology

0. 18 µm CMOS imaging sensor process (TowerJazz)

- **High resistivity epi layer** on p-type substrate
- **Special deep-p-well layer** to shield PMOS

  → true CMOS circuitry in the pixel



Schematic cross-section of CMOS pixel sensor
(*ALICE ITS Upgrade TDR*)

- Nwell diode output signal = Q/C

  → minimize charge spread over different pixels

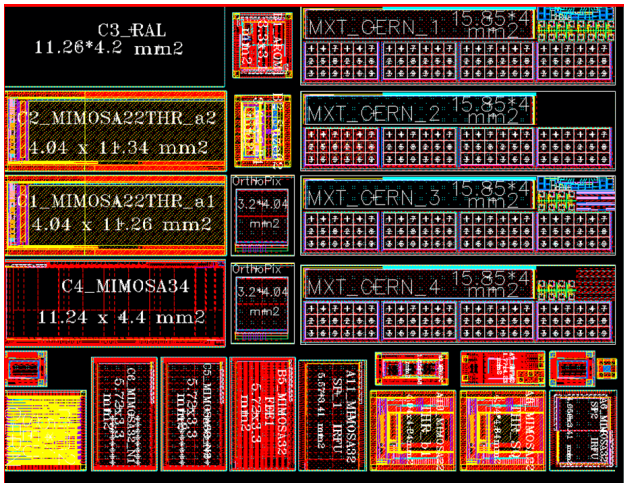
  → minimize capacitance

  → small diode surface (~ 100x smaller than pixel area) and large depletion volume

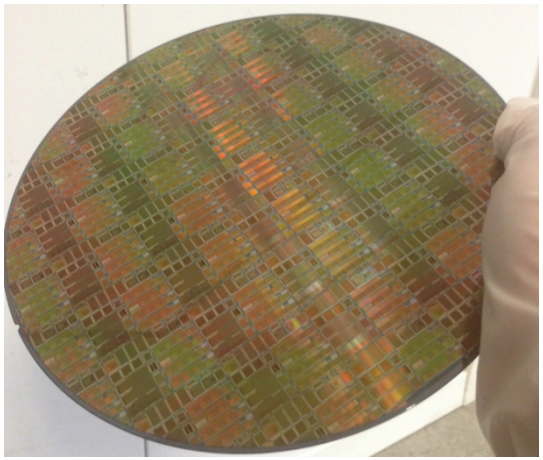
ALICE ITS Sensor Development

Prototype chips produced on a variety of starting wafers:

- Dedicated engineering run (March 2013)
  - 26 different dies in one reticle (23.5 x 31 mm) to study different architectures
- New engineering run submitted in Jan. 2014



Reticle layout and wafer engineering run 03/2013



Evaluation of the different prototype chips (thinned to 50 µm) using source tests (Fe55) and test beams.

Special thanks to the team at DESY who provided help & support during 60 days of testbeam in 2013!

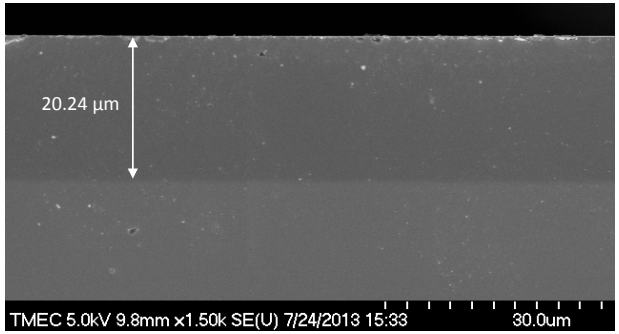
Measurements before and after irradiation to 0.25, 1 and 3 x 10^{13} 1 MeV n_{eq} cm^{-2}.

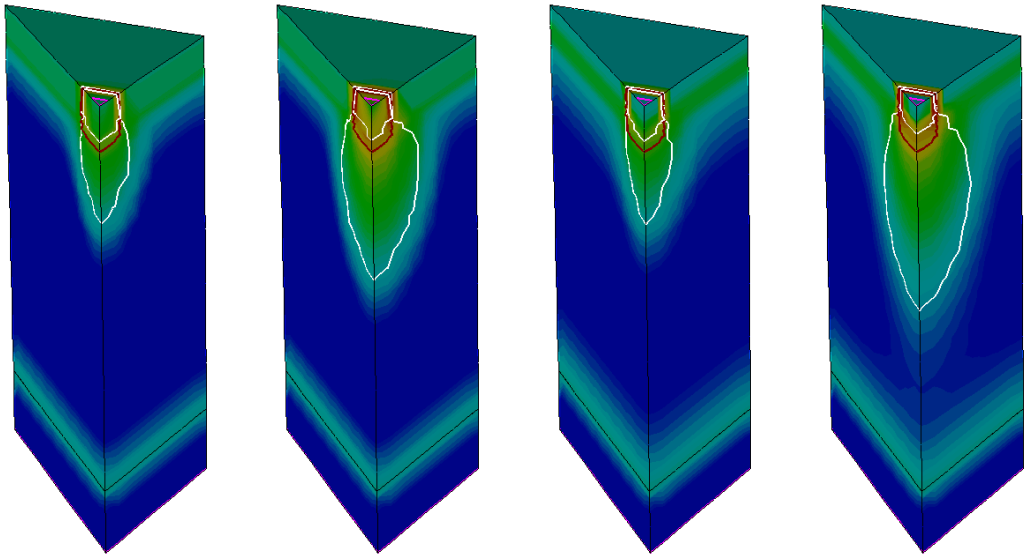
ALICE ITS Sensor Development

Starting wafers used in the engineering run 03/2013 (ALICE ITS TDR):

Type	Number of wafers	Epitaxial Thickness (µm)	Resistivity (kΩ cm)
1 (LR-12)	3	12.0 ± 0.5	0.03
2 (HR-18)	4	18.0 ± 1.5	>1
3 (HR-30)	3	30.0 ± 0.3	≈1
4 (HR-40A)	3	40.0 ± 0.6	≈1
5 (HR-20)	6	20.0 ± 1.9	6.2
6 (HR-40B)	3	40.0 ± 1.9	7.5
7 (CZ)	3	CZ	>0.7

SEM: epi layer and substrate thickness





(a) $-1\,\mathrm{V}$, $10^{13}\,\mathrm{cm}^{-3}$ (b) $-6\,\mathrm{V}$, $10^{13}\,\mathrm{cm}^{-3}$ (c) $-1\,\mathrm{V}$, $10^{12}\,\mathrm{cm}^{-3}$ (d) $-6\,\mathrm{V}$, $10^{12}\,\mathrm{cm}^{-3}$

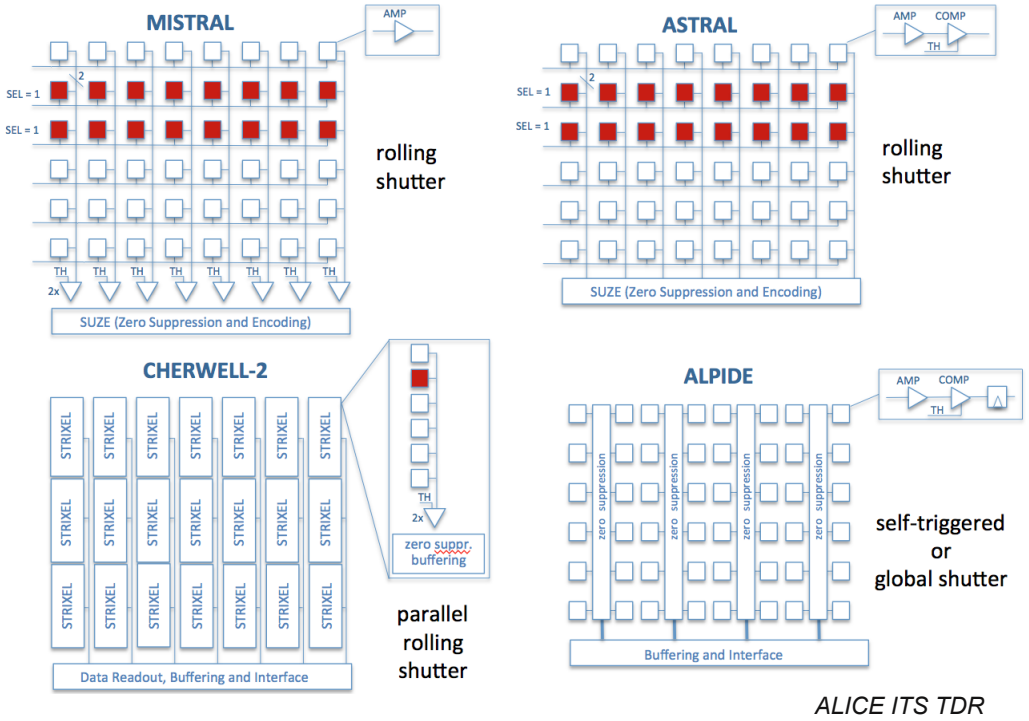
ALICE ITS TDR

TCAD simulation of an n-well diode (3 µm x 3 µm):

- using 2 different doping levels for the epi-layer and
- two reverse bias settings
- logarithmic colour scale of the electric field
- White line shows depletion region

ALICE ITS Sensor Development

- **4 different architectures under study**
  - Selection for the final chip planned for end 2014
- **Prototype chips** available for each architecture
- In the following a selection of results is presented from:
  - MIMOSA22THR, MIMOSA32ter (MISTRA/ ASTRAL)
  - Explorer0 and Explorer1 (ALPIDE)



ALICE ITS TDR

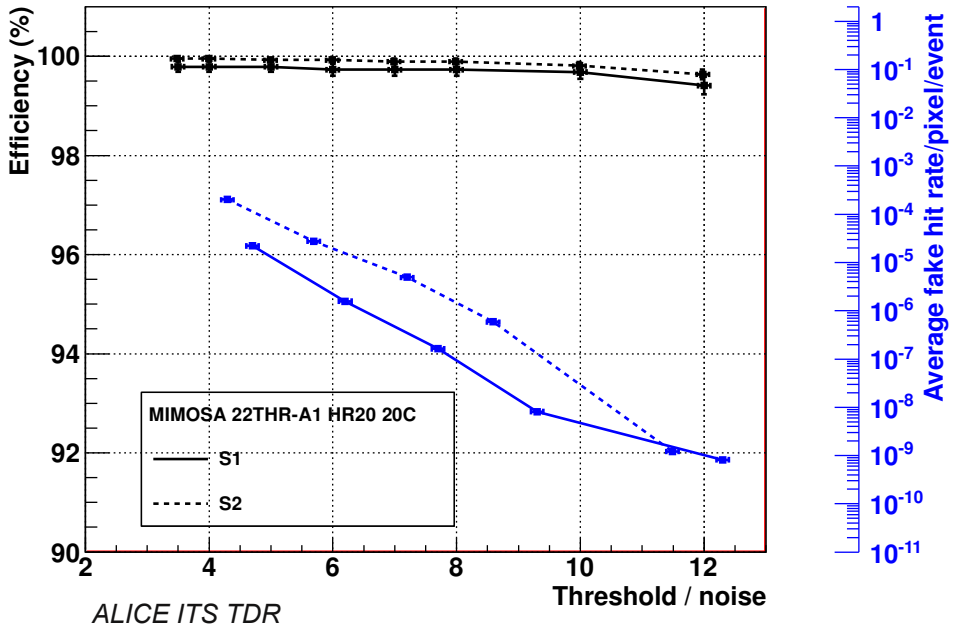
Architecture (discriminator, read-out)	Pitch ($r\phi \times z$) (μm^2)	Integration time (μs)	Power consumption ($mW\,cm^{-2}$)
MISTRAL (end-of-column, rolling-shutter)	22×33.3	30	200
ASTRAL (in-pixel, rolling-shutter)	24×31 36×31	20	85 60
CHERWELL (in-strixel[a], rolling-shutter)	20×20	30	90
ALPIDE (in-pixel, in-matrix sparsification)	28×28	4	< 50

[a] A strixel is a 128-pixel column over which the electronics are distributed.

MIMOSA22THR

Prototype chip of the MISTRAL/ASTRAL family **with pre-amplifier and CDS in pixel circuitry and parallel column readout with offset compensated discriminators at the end of column.**

- Used to validate the upstream part of the MISTRAL and most of the ASTRAL readout.
- **Version a:** single row rolling shutter, **version b:** double row rolling shutter.
- Noise measurements: 19 e^- ENC (a), 20-23 e^- ENC (b)



ALICE ITS TDR

MIMOSA22THRa test beam measurement

HR20 wafer (20 µm epi layer thickness)
Pixel size: 22 µm x 33 µm

Explorer 0 and Explorer 1

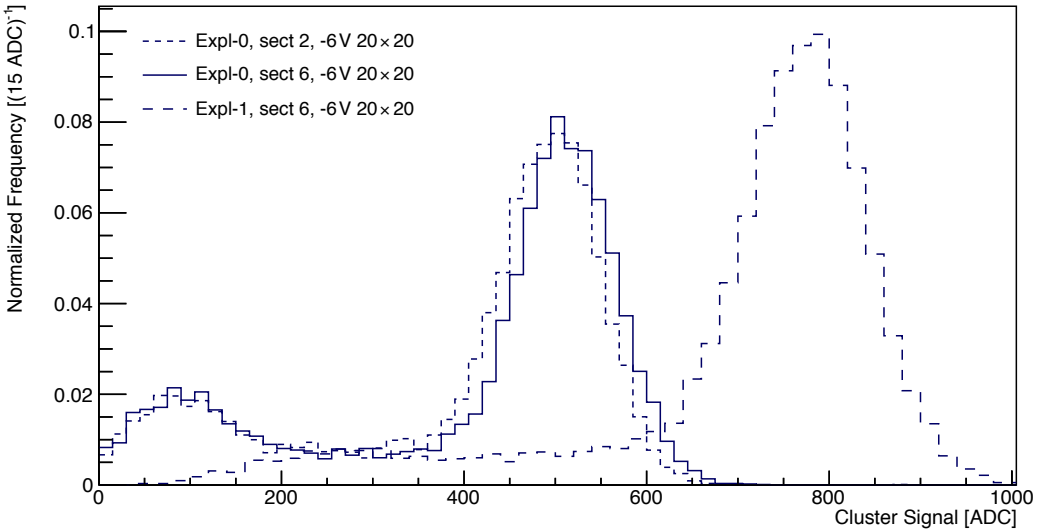
Prototype chips of the ALPIDE family **to study the charge collection and diode layout as well as the effect of back-biasing.**

- 2 sub-matrices (20 µm x 20 µm and 30 µm x 30 µm pixels)

Sector	Shape	Diameter [µm]	Spacing [µm]
1		1.13	3.035
2		2	2.6
3		3	2.1
4		1.13	3.035
5		2	2.6
6		3	2.1
7		1.13	0.635 (top)
8		1.13	0.635 (top)
9		2	2.6

Explorer 1, ALICE ITS TDR

ALICE ITS TDR, Fe55 measurement



Different **n-well diode areas and spacing** to the surrounding p$^+$ring:

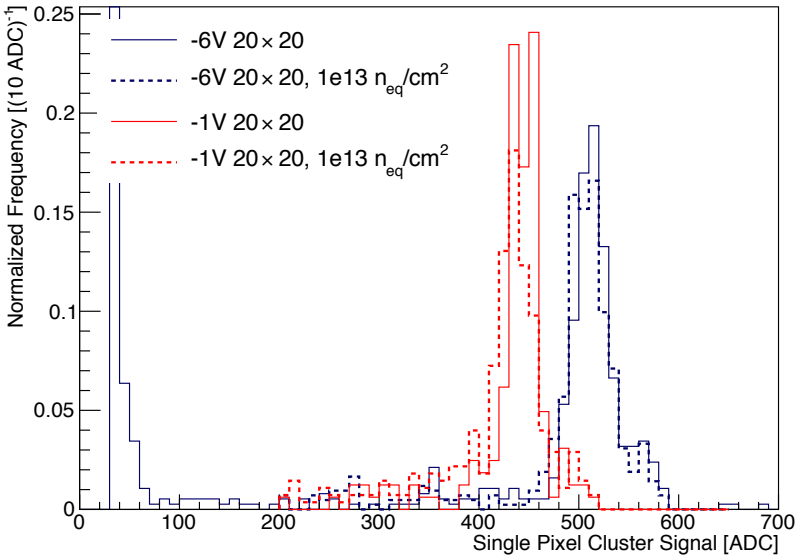
- Explorer 0: sector 2: 7.6 µm^2 diode, no spacing
- Explorer 0: sector 6: 7.6 µm^2 diode, 1.04 µm spacing
- Explorer 1: sector 6: 7.6 µm^2 diode, 2.1 µm spacing

Explorer 0 before/after irradiation

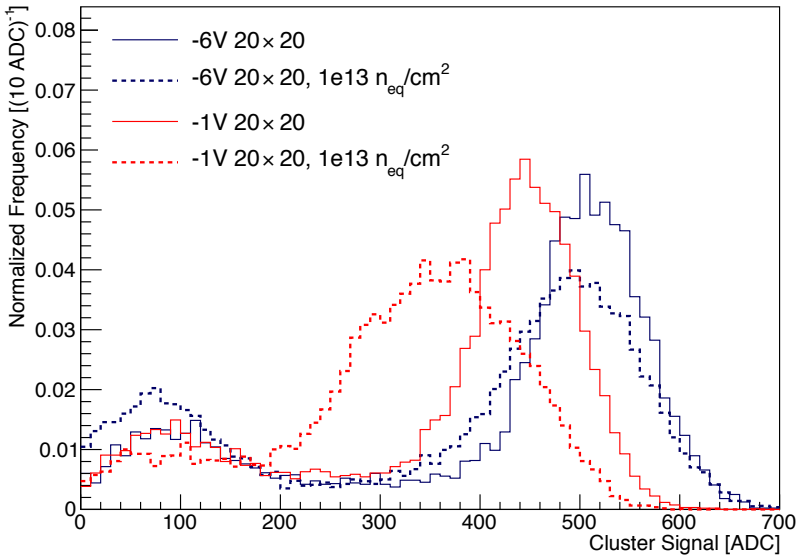
Explorer 0 irradiated to 1x10^{13} 1MeV n_{eq} cm^{-2}

- 2 bias settings (-1V, -6V)
- N-well diode: 7.6 µm2 with 1.04 µm spacing
- Noise increases by 5-15% (different pixel sizes and diode geometries)

ALICE ITS TDR, Fe55 measurement



(a) Single-pixel cluster signal

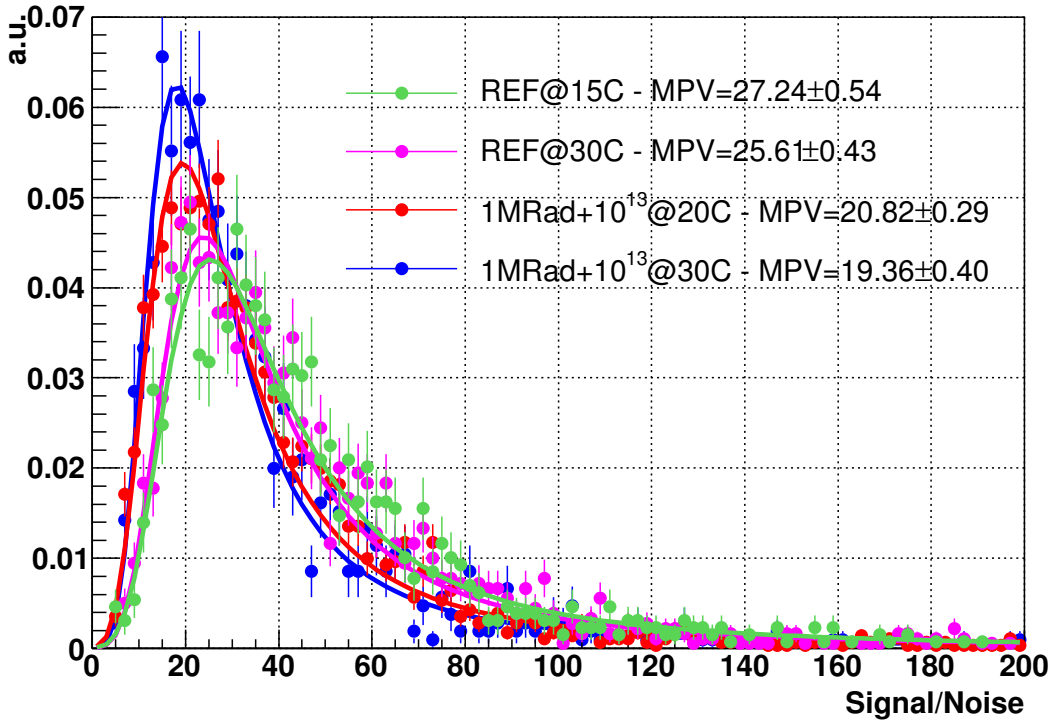


(b) Cluster signal (sum of 5×5 matrix around seed pixel)

MIMOSA32ter

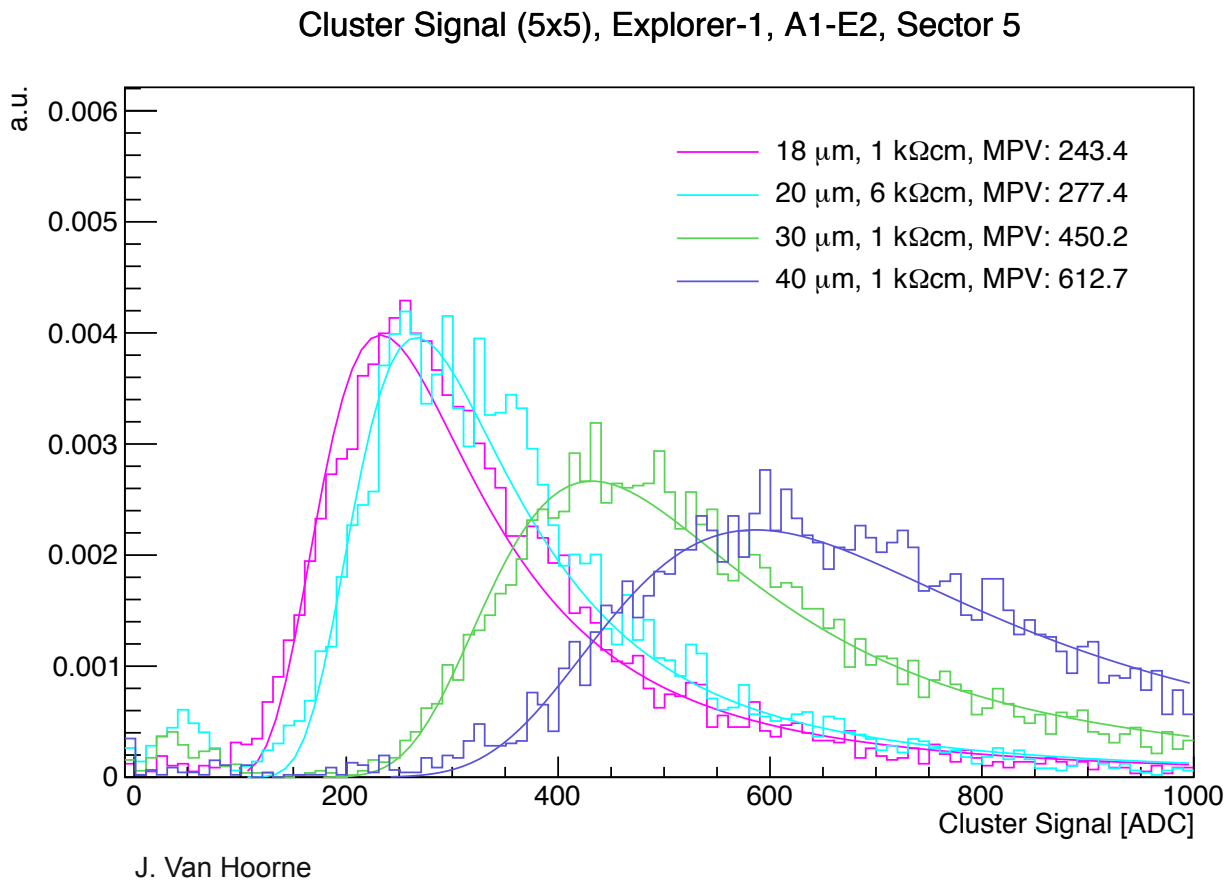
S/N measured in the SPS testbeam for **MIMOSA32ter chips before and after irradiation** (combined irradiation 1 Mrad TID + 10^{13} 1 MeV n_{eq} cm^{-2})

- S/N decrease due to noise increase after irradiation
- Cluster signal remains unchanged



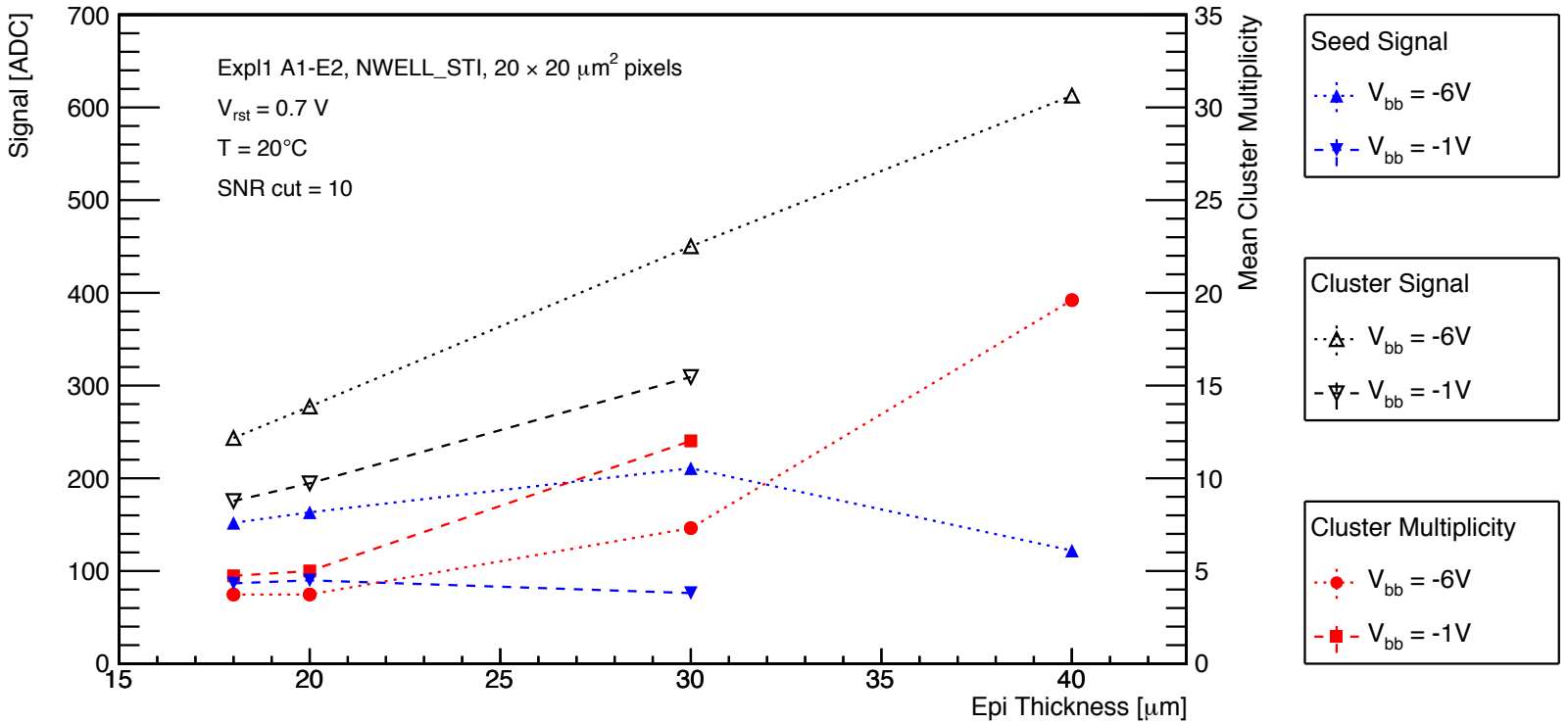
Explorer 1

Study of different starting materials (pixel size 20 µm x 20 µm), Desy testbeam 2013:



Explorer 1

Study of different starting materials (pixel size 20 µm x 20 µm), Desy testbeam 2013:



2 competing processes:

- Cluster charge increases linearly with the epi layer thickness
- Cluster size increases for thicker epi layer thicknesses

Best SNR: 30 µm @ -6V
20 µm @ -1V

Summary

- A new ALICE ITS will be installed during LS2, replacing the present silicon tracker with 7 layers of monolithic silicon pixel detectors.
- Different architectures are under study in testbeams and laboratory measurements using prototype chips.
- Several starting materials have been included in a recent engineering run, allowing to study the effects of different epi layer thicknesses and resistivities.
- Radiation tests up to the levels expected for the innermost layer in the new ITS show no signal degradation in the prototype chips and a noise increase between 5 and 15%, depending on the pixel and diode geometry.