Pixel Detectors – on the brink to a new era

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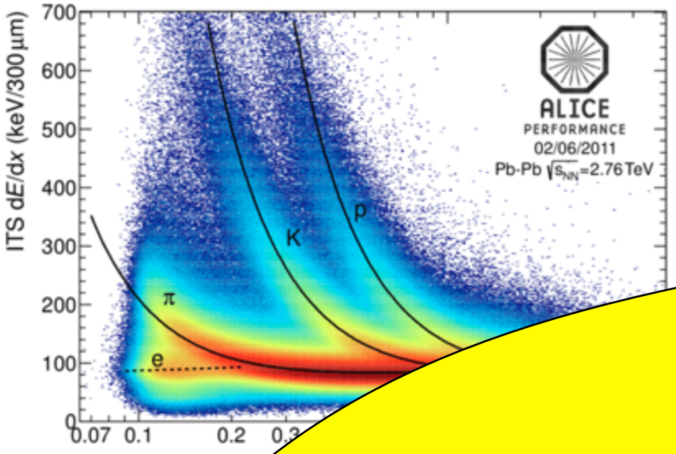
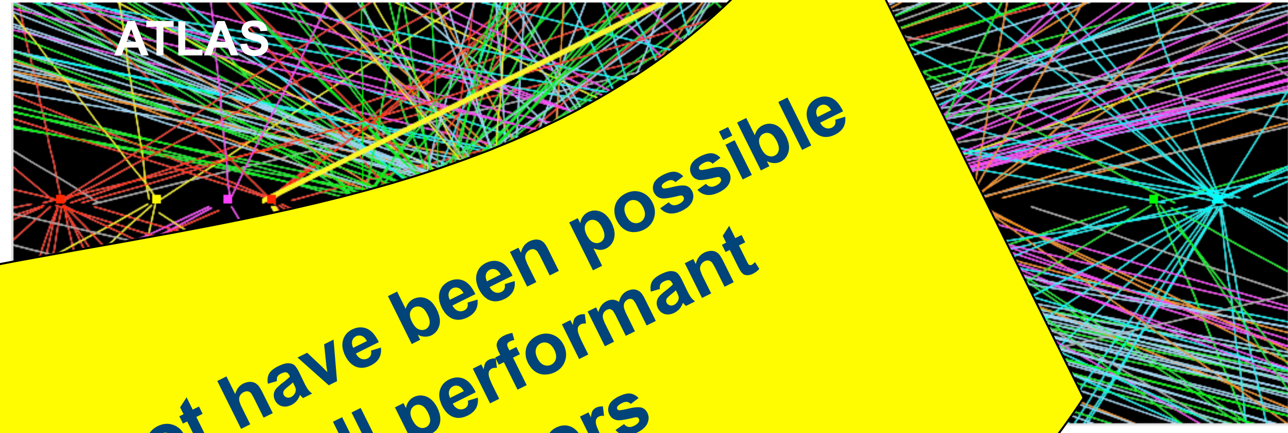
SI LAB
Silizium Labor Bonn

Looking back on 3 years of LHC running (25 /fb) ...

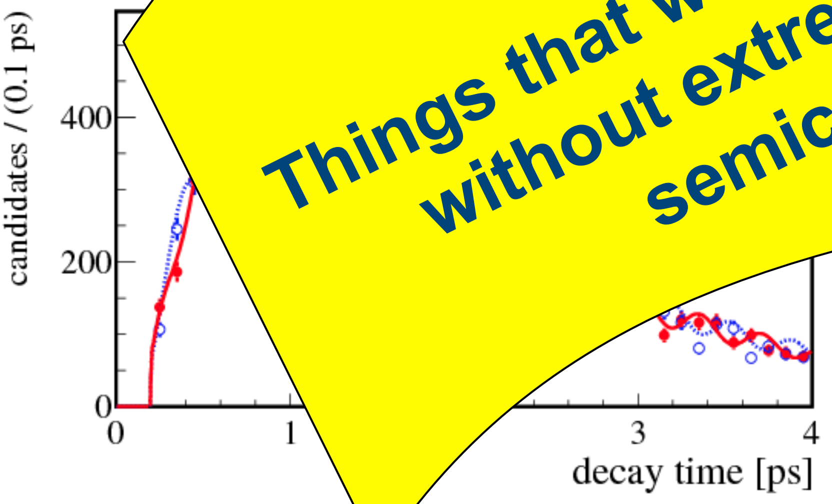
This is a definitively a success story !

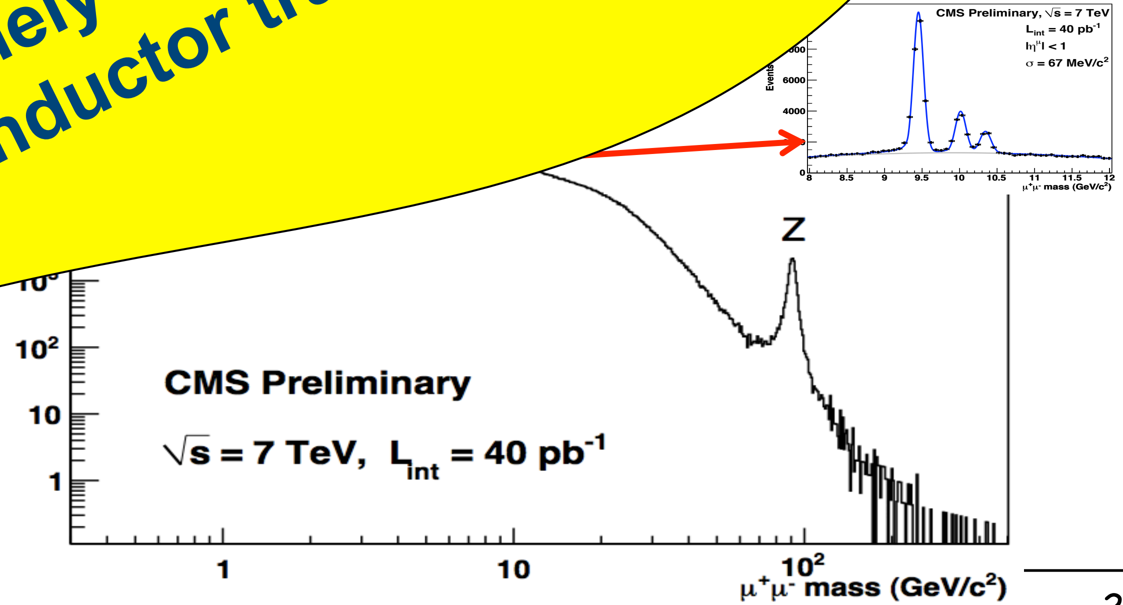


~70 interactions /BX



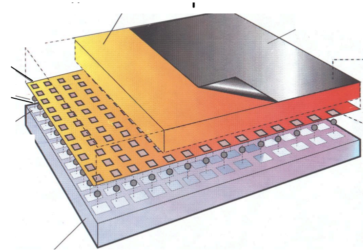
een possible



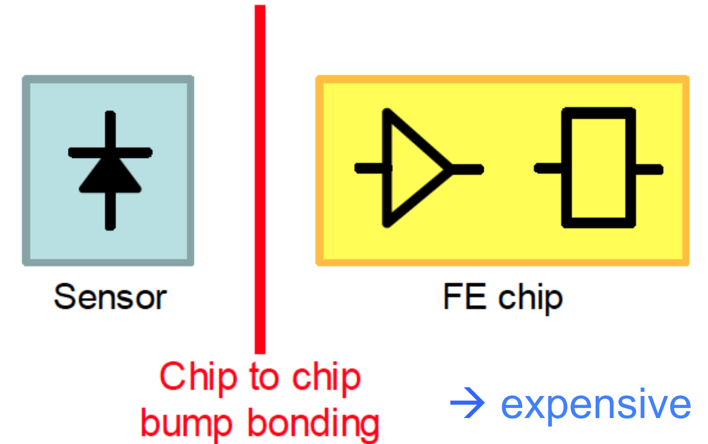


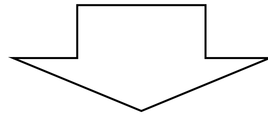
Things that would not have been possible without extremely well performant semiconductor trackers

A classification ... from HYBRID pixels to new challenges

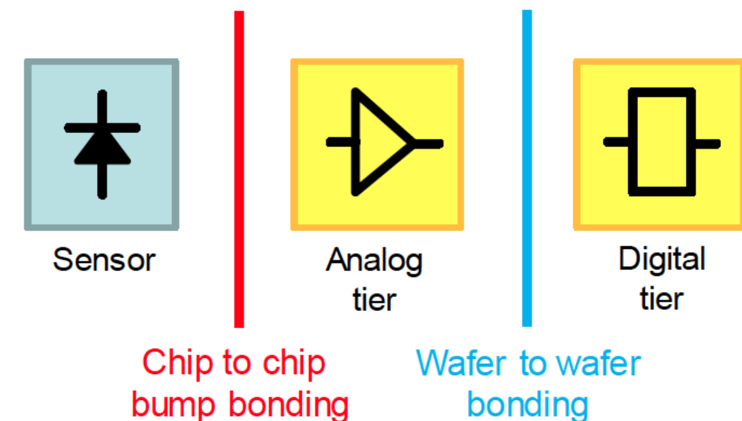


- standard HYBRID pixels
  - various sensors: planar-Si, 3D-Si, diamond
  - mixed signal R/O chip (FE-I3, FE-I4, ROC ...)





- 3D integration of CMOS Tiers
  - separate analog / digital / opto
  - FE-TC4 (Tezzaron/Chartered)



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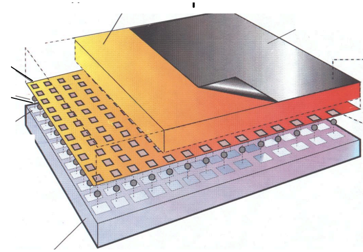

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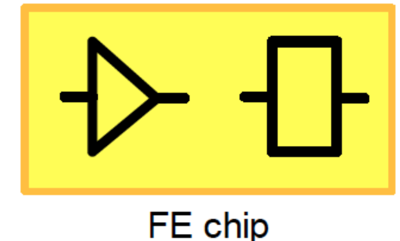
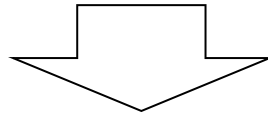
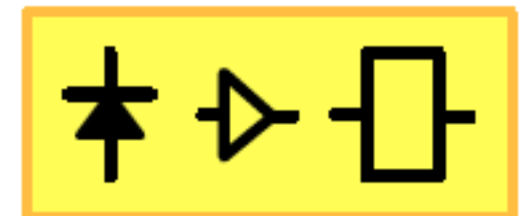


Chip to chip
bump bonding

→ expensive

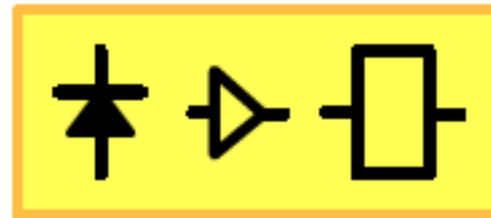


- Monolithic Active Pixel Sensors
  - MAPS using CMOS with Q-collection in epi-layer (usually by diffusion → recent advances)
  - depleted DMAPS using HR substrate and/or HV process to create depletion region: $d \sim \sqrt{\rho \cdot V}$
  - CMOS on SOI



A classification ... from HYBRID pixels to new challenges

- (D)MAPS

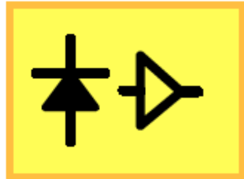


Diode + Amp + Digital

MIMOSA family
ALPINE
CHERWELL
} epi-Si

HVMAPS
T3
LePIX
DMAPS
} bulk depletion

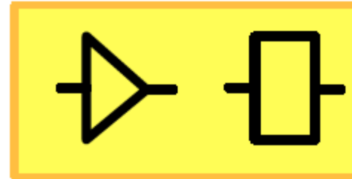
~100 trans.



Diode + preamp

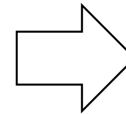
Wafer to wafer bonding

~100M trans.

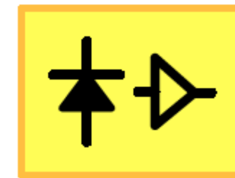


existing FE chip

or only chip to chip ??



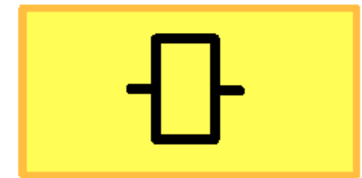
~100 trans.



Diode + full analog processing

Wafer to wafer bonding

~100M trans.



Digital only FE chip

or chip to wafer

- HYBRID pixels using "smart" sensors
  - 8" **HV** or **HR** sensor w/ few transistors
  - (voltage) signal cap. coupled to R/O-chip
  - eg. CCPD to FE-I4
- DEPFET pixels (one in-pixel transistor)

- depleted CMOS ACTIVE Sensors + digital R/O chip
  - **HR** or **HV** CMOS sensor with CSA+disc
  - dedicated digital R/O chip
  - CCPD -> DMAPS -> goal wafer to wafer

Rate and radiation challenges at the innermost pixel layers

Hybrid Pixels

	BX time	Particle Rate	Fluence	Ion. Dose
	ns	kHz/mm^2	n_{eq}/cm^2 per lifetime*	Mrad per lifetime*
LHC (10^{34} cm^{-2}s^{-1})	25	1000	2×10^{15}	79
HL-LHC (10^{35} cm^{-2}s^{-1})	25	10000	2×10^{16}	> 500
LHC Heavy Ions (6×10^{27} cm^{-2} s^{-1})	20.000	10	$>10^{13}$	0.7
RHIC (8×10^{27} cm^{-2}s^{-1})	110	3,8	few 10^{12}	0.2
SuperKEKB (10^{35} cm^{-2}s^{-1})	2	400	~3 x 10^{12}	10
ILC (10^{34} cm^{-2}s^{-1})	350	250	10^{12}	0.4

Monolithic Pixels

lower rates
lower radiation
smaller pixels
less material
better resolution

DEPFET: Belle II
MAPS: STAR@RHIC and future ALICE ITS

assumed lifetimes:
LHC, HL-LHC: 7 years
ILC: 10 years
others: 5 years

Hybrid Pixels

An experimenter's dream

- good S/N
- µm space resolution
- ~ns time resolution
- > 10 MHz / mm^2 rate capability
- radiation hard to 1 Grad
- radiation length per layer < 0.2% X_0
- all in one monolithic pixel "chip"

Reality

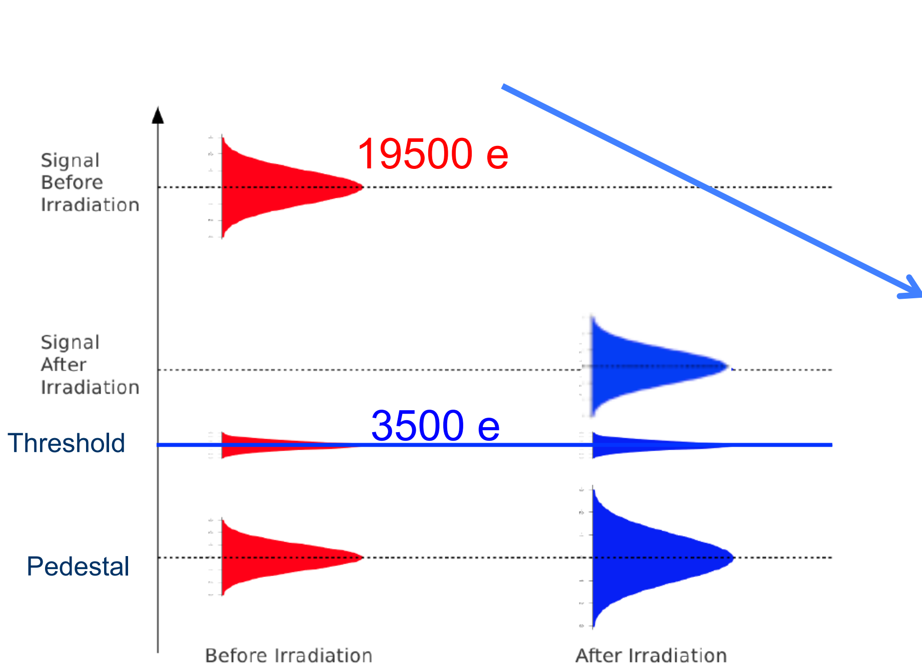
hybrid pixels

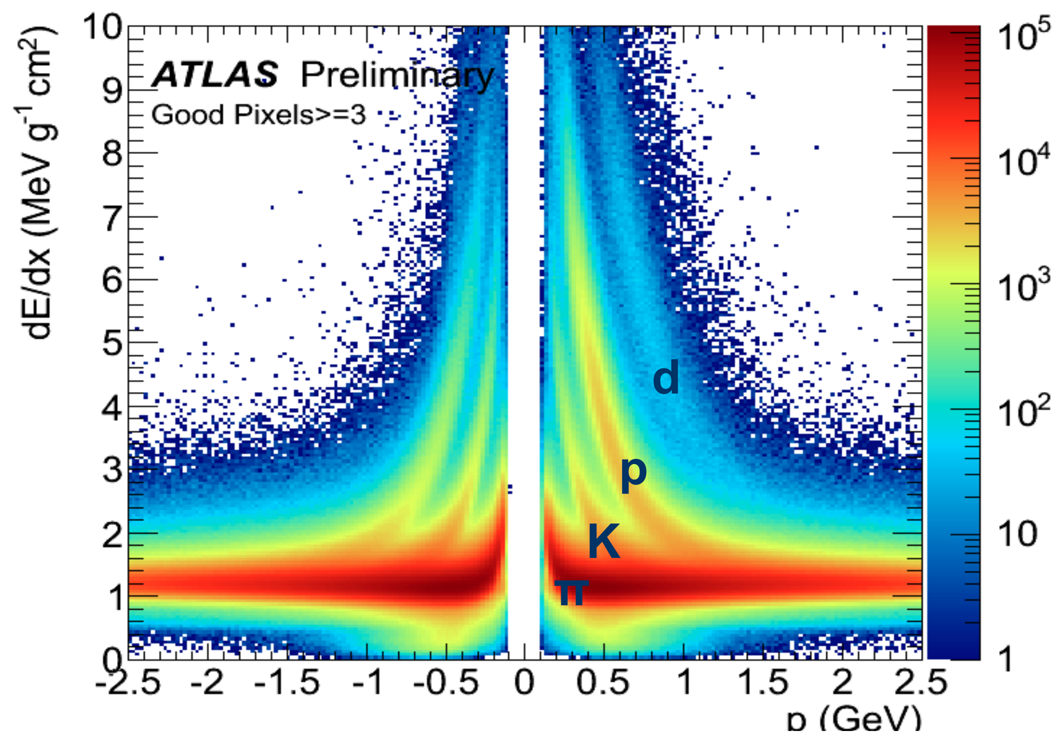
- good S/N — ✓ (fully) depleted
- µm space resolution — ➢ ~10 µm
- ~ns time resolution — ✓ obtained at LHC
- > 10 MHz / mm^2 rate capability — ✓ tbd for HL-LHC
- radiation hard to 1 Grad — ✓ tbd for HL-LHC
- radiation length per layer < 0.2% x/X_0 — ➢ 3.5% → 1.7%
- all in one monolithic pixel “chip” — ➢ no, hybrid

Performance (typical ... here ATLAS)

Signal of a high energy particle ≙ 19500 e⁻ → <10000 e⁻ after irrad.

- Discriminator thresholds = 3500 e, ~40 e spread, ~170 e noise
- 99.8% data taking efficiency
- 95.9% of detector operational
- ca. 10 µm x 100 µm resolution (track angle dependent)
- 12% dE/dx resolution





ATLAS: C. Gemme et al., Physics Letters B 720 (2013)

... and abolutely convincing measured efficiencies

after 2013/14 shut down

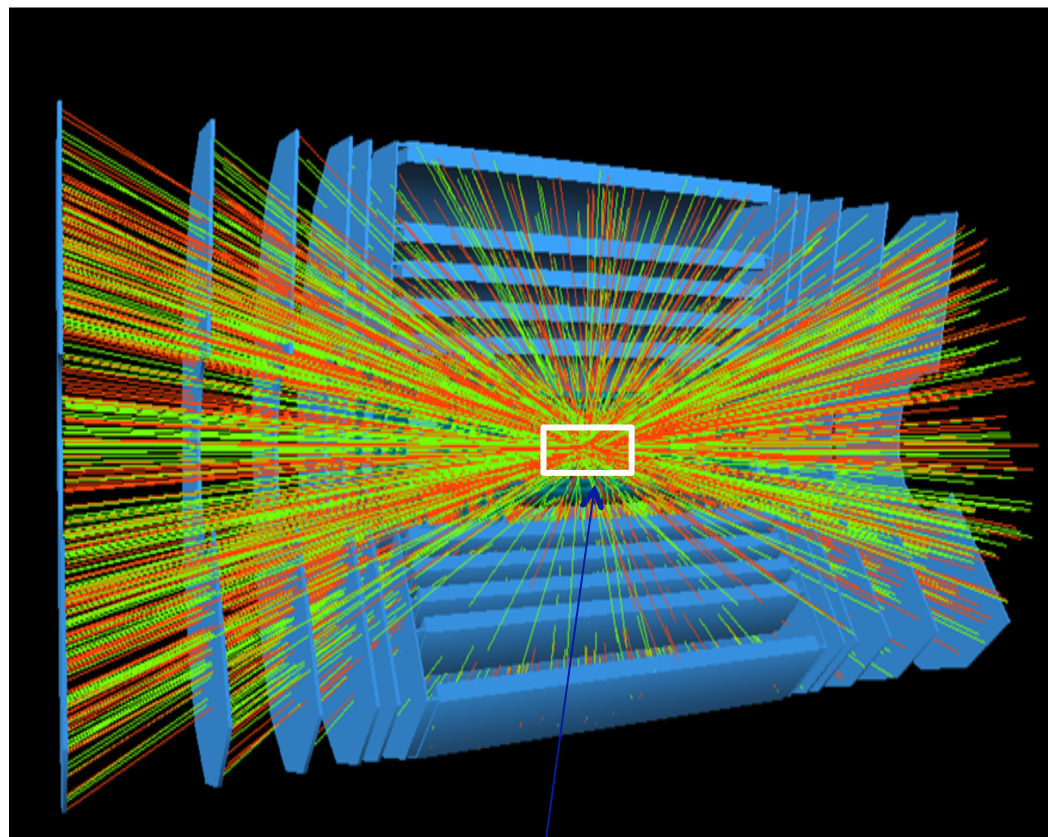
	ATLAS Pixels	ATLAS Strips	CMS Pixels	CMS Strips	LHCb	ALICE Pix	ALICE SDD	ALICE Strips
good modules	95% (→99%)	99%	96.3% (→99%)	97.5%	99%	92%	86%	91%
hit eff. of good	>99%	>99.5%	>99%	>99%	>99.3%	>99%	>99%	>99%
track eff.	99%	>99%	99% ?	99% ?	98%			
Data taking	99.9%	>99.1%	93% (overall CMS)		93%			

who would have thought in 2007 that one can operate such huge detectors w/o any access for more than 4 years with these efficiencies ?

Challenges for the LHC upgrades

Increased luminosity requires

- higher hit-rate capability
- increased granularity
- higher radiation tolerance
- lighter detectors



we are here

Radiation hardness and rate increase compared to now

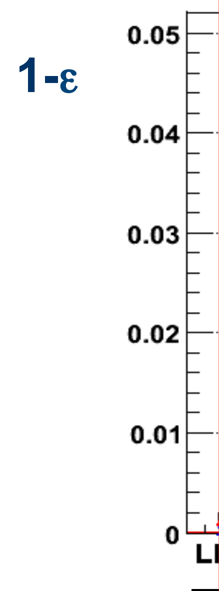
- phase 0 (2015) ≈ × 5
- phase 1 (2018) ≈ × 5-10
- phase 2 (2022) ≈ × 10-30

HL-LHC data rates

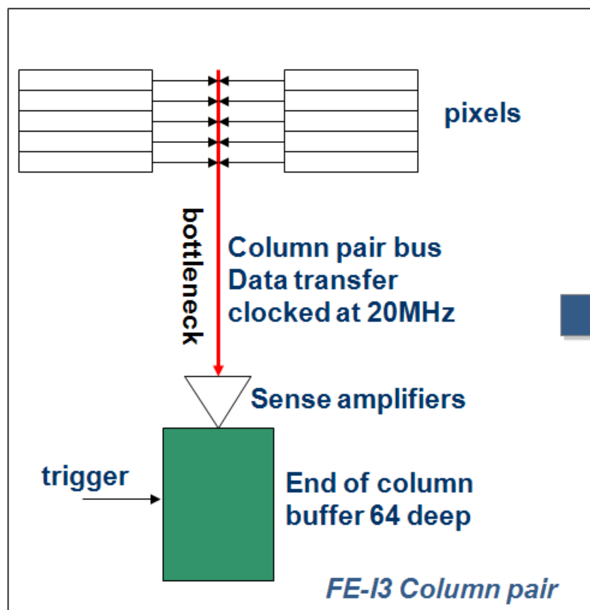
Hit inefficiency rises steeply with the hit rate

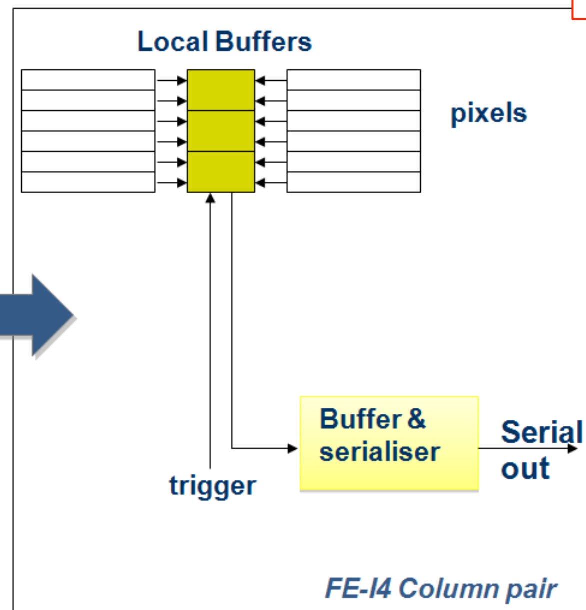
Bottleneck: congestion in (double) column readout

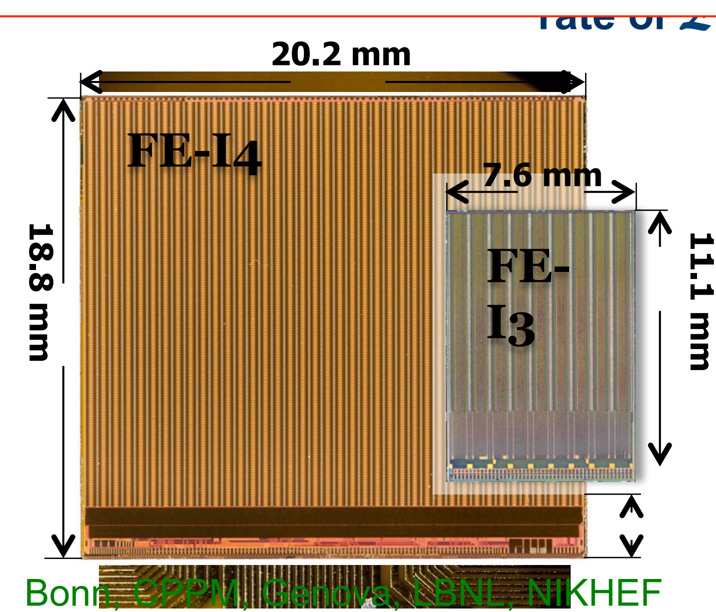
⇒more local in-pixel storage (130 nm !)
>99% of hits are not triggered
⇒ don't move them → no blocking



- IBM (130 nm)
- 70 Million transistors
- 26880 pixels (50 x 250 μm^2)
- lower noise than FE-I3
- lower threshold operation poss.
- higher rate compatibility
- radiation hard to >250Mrad
- 3+ years of design work w/ 8 designers
- working horse for current and future pixel R&D



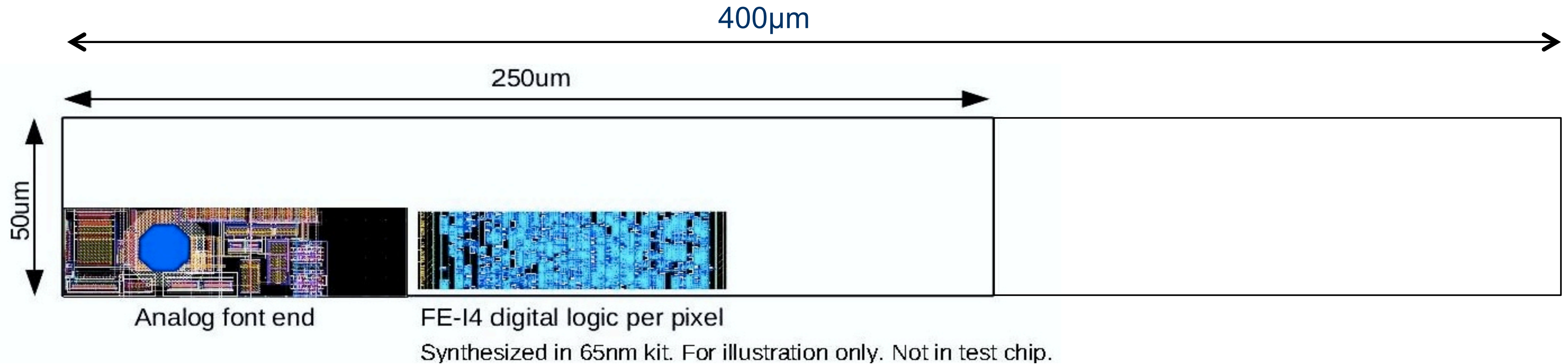




Bonn, CPPM, Genova, LBNL, NIKHEF

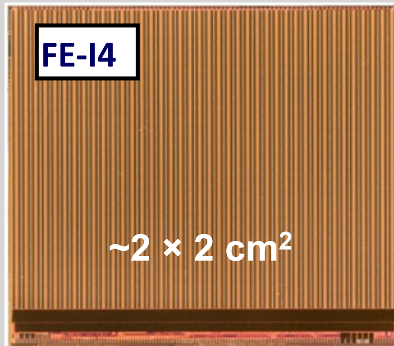
M. Garcia-Sciveres et al, Nucl.Instrum.Meth. A636 (2011) 155-159

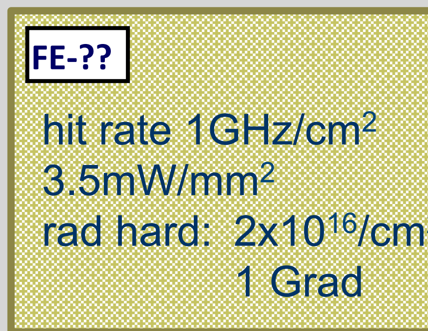
next generation based on 65 nm technology ...



ATLAS Pixel FE chips

~0.6 × 1.1 cm²





FE-I3	FE-I4	FE-??
250 nm technology	130 nm technology	65 nm technology
pixel size 400 × 50 µm²	pixel size 250 × 50 µm²	pixel size 125 × 25 µm²
3.5 M. transistors	70 M transistors	~ 500 M transistors

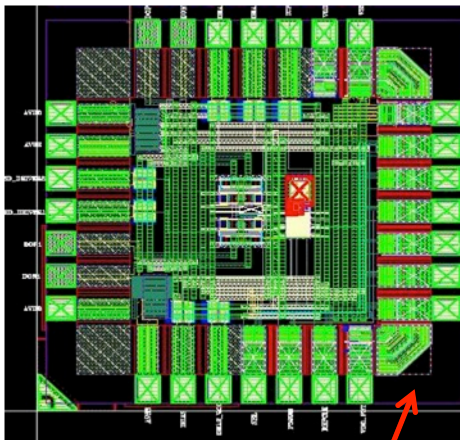
addressed by
CERN R&D collab.

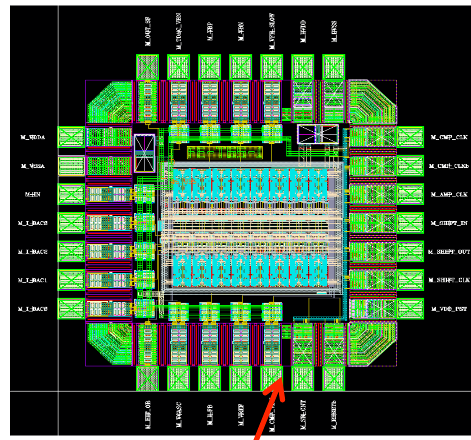
RD53

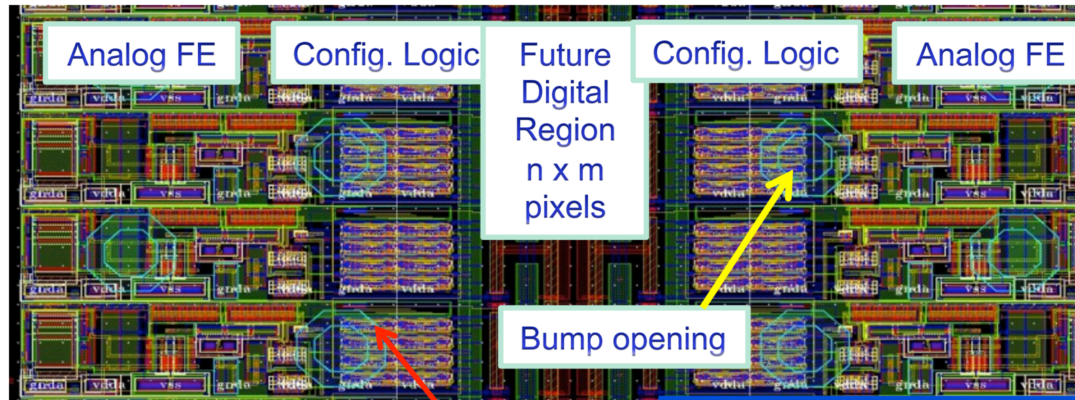
convenors:
Jorgen Christiansen
Maurice Garcia Sciveres

65 nm prototypes of analog and digital circuits submitted and successfully tested

First ATLAS prototype IC blocks in 65nm

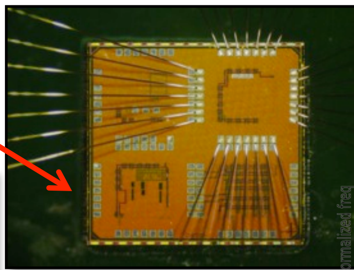




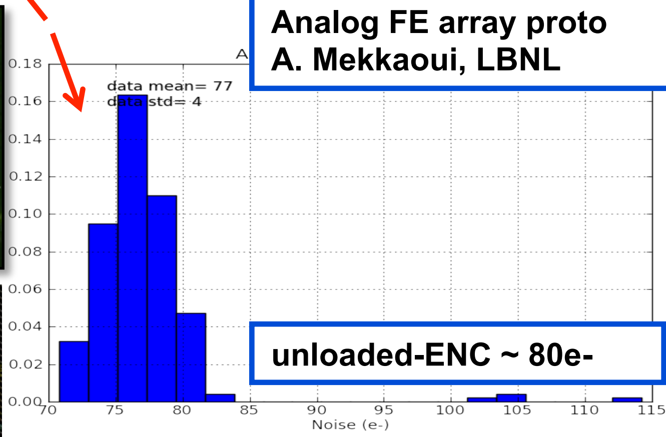


1.6 GHz PLL-PRBS-CML
T. Kishishita, Bonn

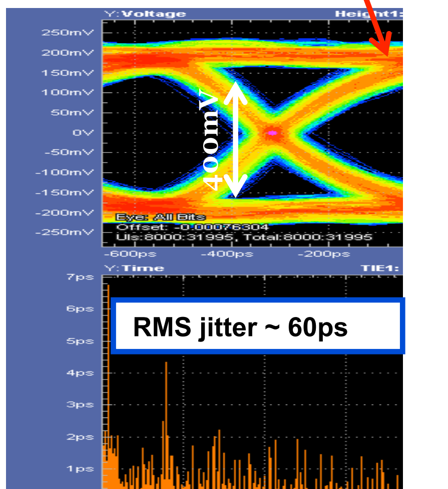
FE-T65-1,to test analog perf.
CSA + Discr. versions
M. Havranek, Bonn



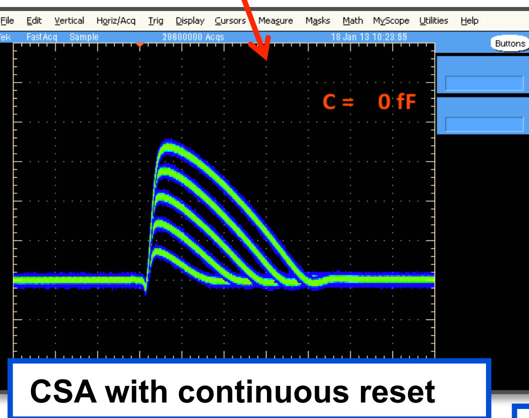
Analog FE array proto
A. Mekkaoui, LBNL



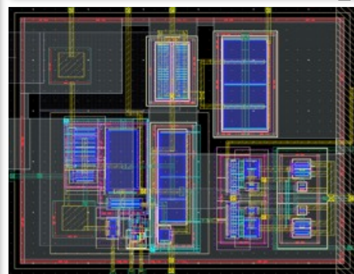
unloaded-ENC ~ 80e-



RMS jitter ~ 60ps



CSA with continuous reset



dyn. comp.: 2.4μW @40MHz

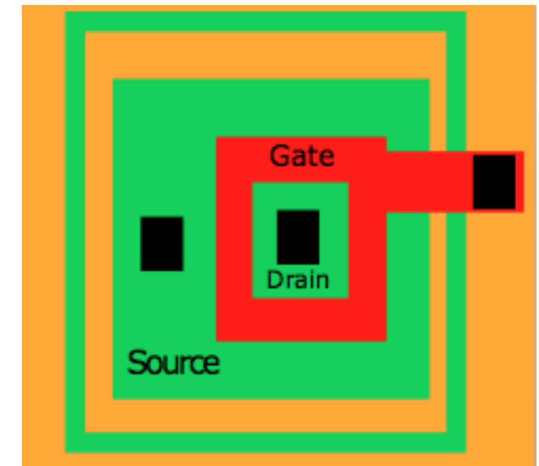
1.6 Gbps, PRBS, preamp on

other Bonn prototypes: SAR-ADC, LVDS

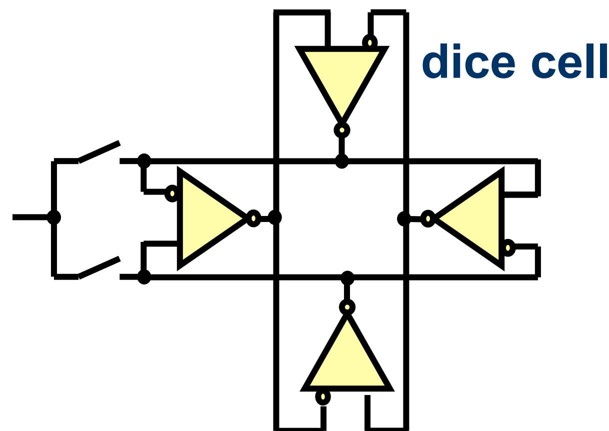
a problem still to solve: pMOS transistors don't stand more than 400 Mrad (CPPM)

Radiation hardness to HL-LHC fluences $\gg 10^{15}$ cm^{-2}

- chips are radhard … provided that …
  - deep submicron technology used (130 nm → 65 nm)
  - "round" transistors used at critical nodes
  - SEU tolerant digital logic where needed



round FET

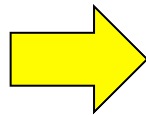


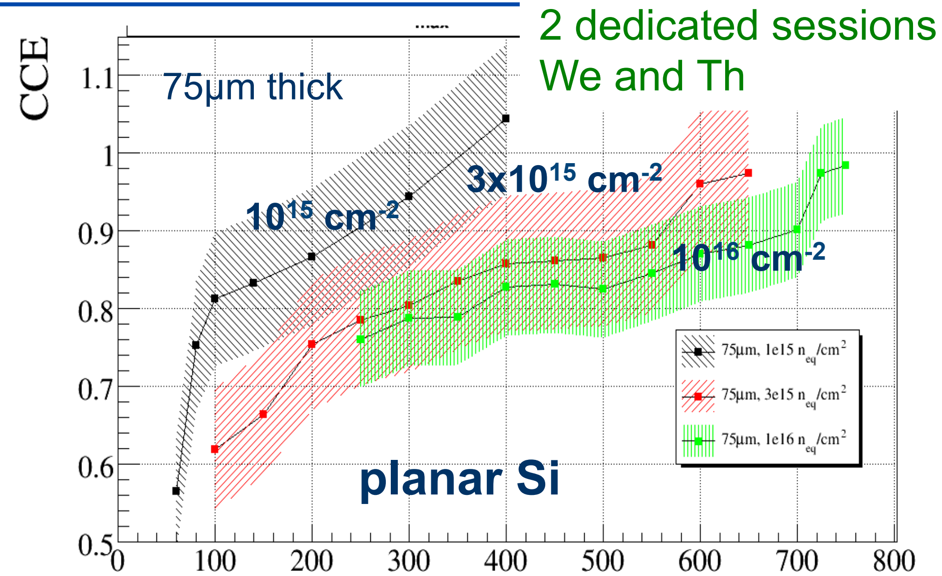
dice cell

Hybrid Pixel: radhard sensor (passive) development

Planar sensors: (PPS collab.)

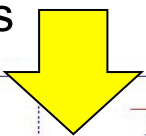
- work at $2x10^{16}$ n_{eq}/cm^2
- but need high bias voltage
- n in n (inner), n in p (outer layers)
- slim edges (guard ring optimization)



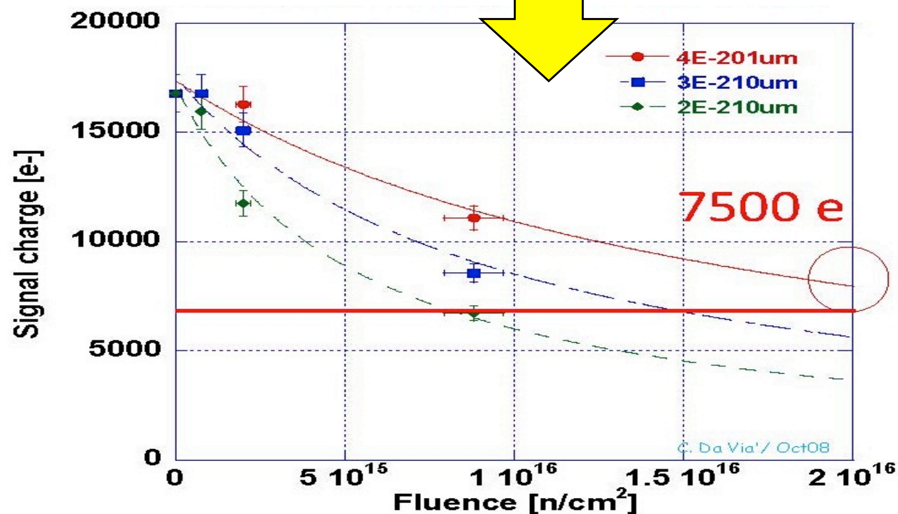


3D-Si sensors: (3D-Si collab.) → special geometry

- 50 µm electrode spacing → V_{bias} ~200 V only
- option for inner layers

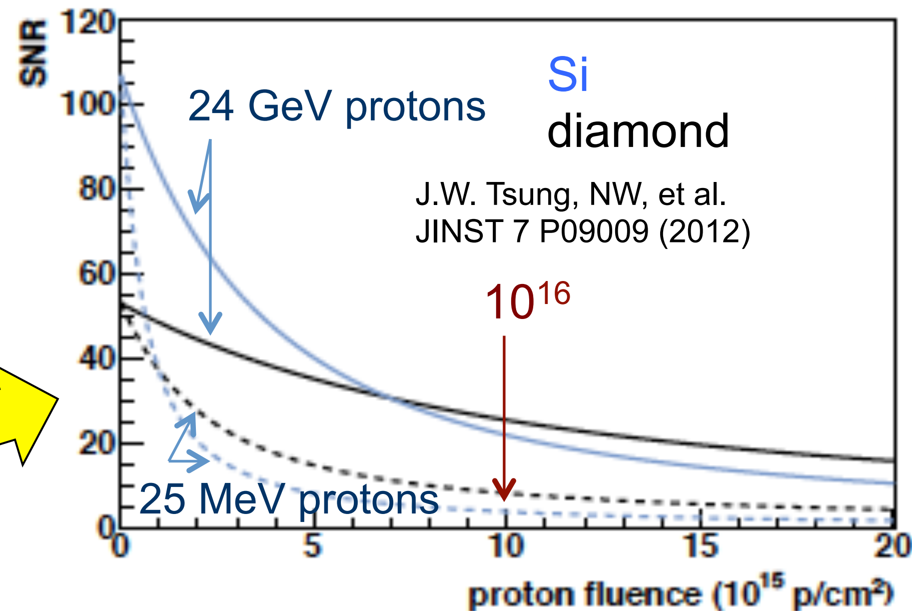


2 dedicated sessions

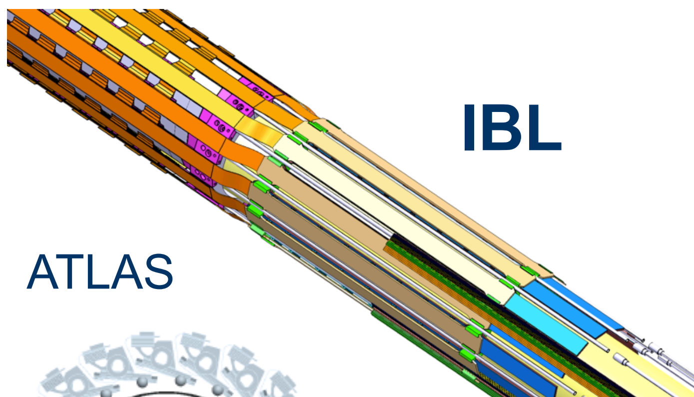


Diamond sensors: (RD42 & DBM collab)

- ~2000e at $2x10^{16}$ n_{eq} cm^2 → need low thresh.
- but S/N potentially better than Si at high fluence
- for beam monitors, option for innermost layer?

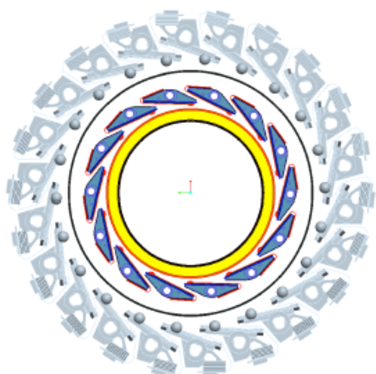


LHC upgrades .... ATLAS IBL (to be installed May 2014)

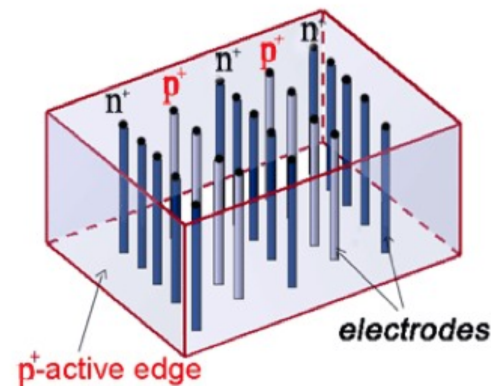


IBL

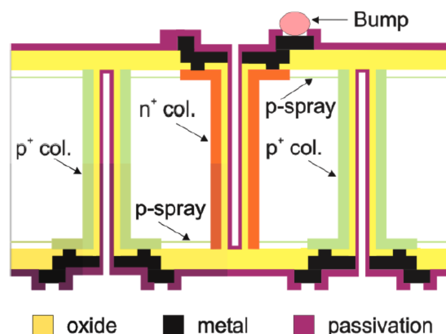
ATLAS

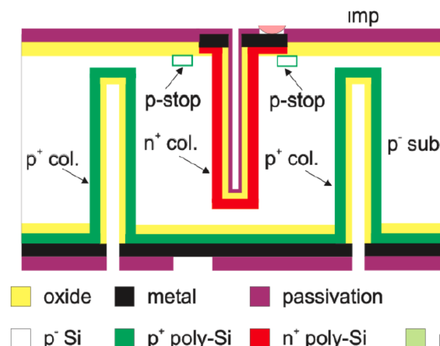


25% 3D Si sensors
75% planar Si

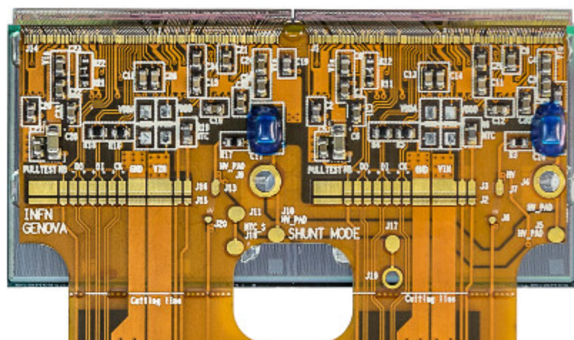


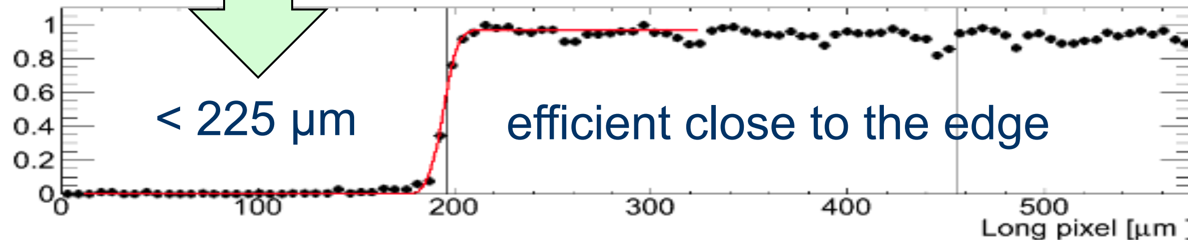
see talk by
Didier Ferrer





2-chip (FE-I4) module





a so far convincing experience with 3D sensors

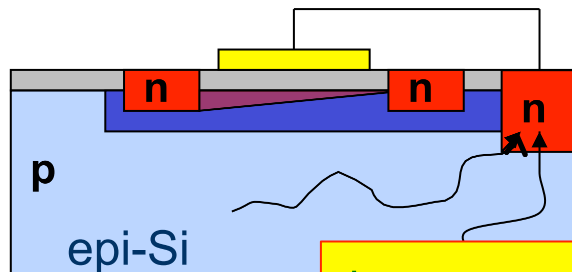
(semi) Monolithic Pixels

(Semi)- Monolithic Detectors

+ **really low mass**
+ **fewer interconnections**
– **slow (frame readout, rolling shutter)**

CMOS Sensors (MAPS) → STAR
CMOS with epi-layer as sensor

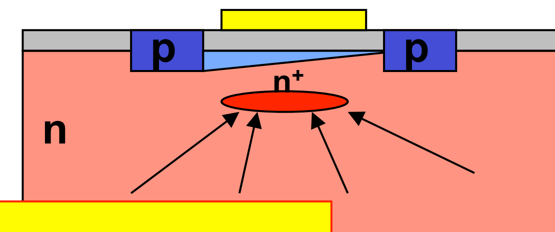
+ 'standard CMOS' process
+ CMOS circuitry, but limited to NMOS
– small signal, slow charge collection
– area limited by chip size



R. Turchetta et
NIM A458 (200

DEPFET → Belle II
FET on fully depleted bulk

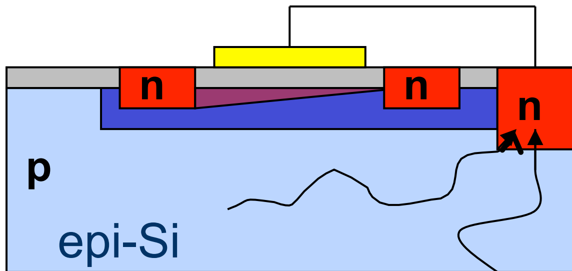
– non standard double-sided process
– simple, one stage amplifier
+ large signal, fast collection
+ wafer size sensors possible



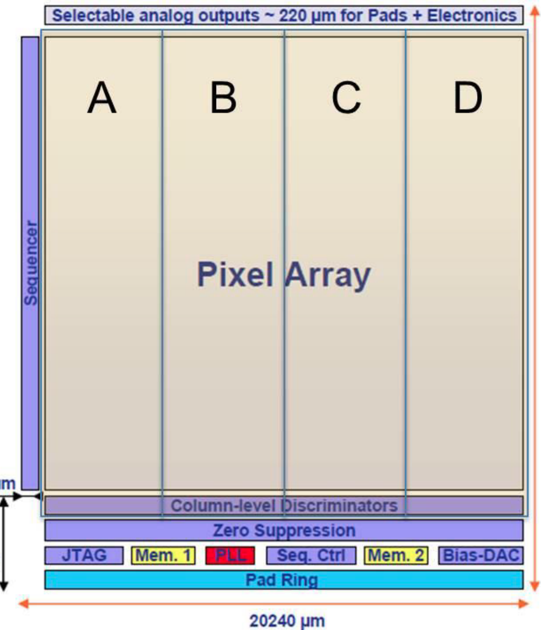
87) 365-377

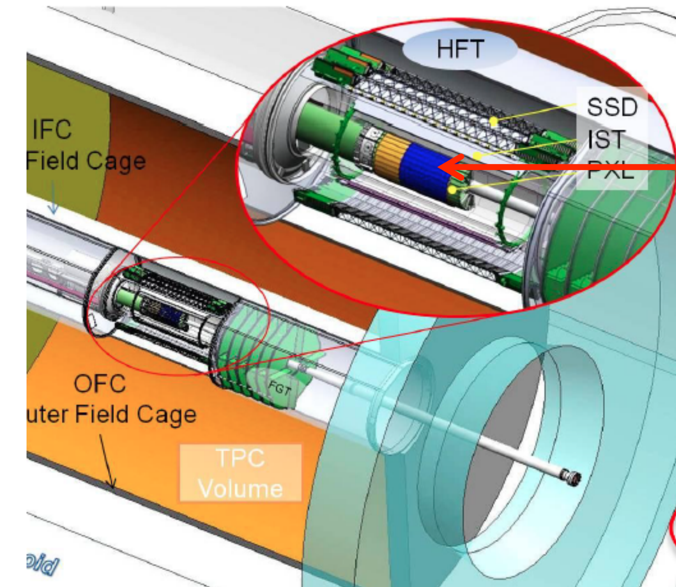
+ **no expensive bump bonding**
+ **very thin (50 µm resp. 75 µm) → ~0.2% x/X_0**
+ **small pixels (20x20 resp. 50x75 µm²)**
+ **low power → less cooling**
– **radiation hardness**
– **R/O speed**

Monolithic Active Pixel Sensors (MAPS)



- **MAPS – epi**
  state of the art MIMOSA (IPHC)
  no NMOS in active area

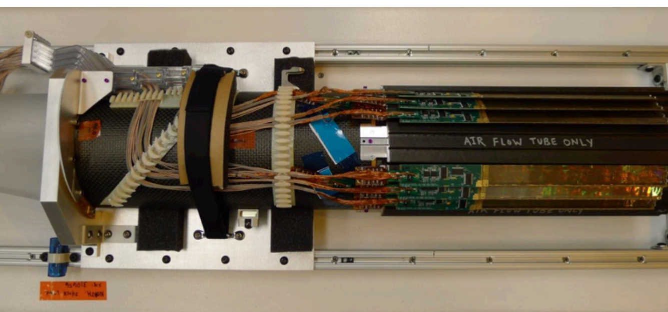




a real detector
STAR@RHIC

CMOS circuitry

- 350 nm CMOS
- < 30 µm pixels
- 0.37% X_0
- 50 µm thick
- frame time < 200 µs



engineering run detector works!
also: some lessons learned
15/27 ladders ok
Ready for data taking soon in 2014

MAPS for ALICE (2018) and for the ILC (20xx?)

ALICE

10.7m²

Beam pipe — Inner Barrel — Outer Barrel

outer barrel — inner barrel

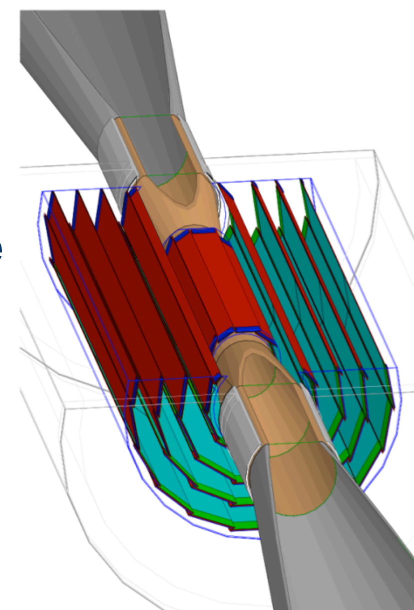
see talk by Petra Riedler

specs

Parameter	Inner barrel	Outer barrel
Max. silicon thickness	50 µm	
Intrinsic spatial resolution	5 µm	30 µm
Chip size	15 mm × 30 mm ($r\phi \times z$)	
Max. dead area on chip	2 mm ($r\phi$), 25 µm (z)	
Max. power density	300 mW/cm²	100 mW/cm²
Max. integration time	30 µs	
Max. dead time	10 % at 50 kHz Pb–Pb	
Min. detection efficiency	99 %	
Max. fake hit rate	10^{-5}	
TID radiation hardness[a]	700 krad	10 krad
NIEL radiation hardness[a]	10^{13} 1 MeV n_{eq}/cm^2	3×10^{10} 1 MeV n_{eq}/cm^2

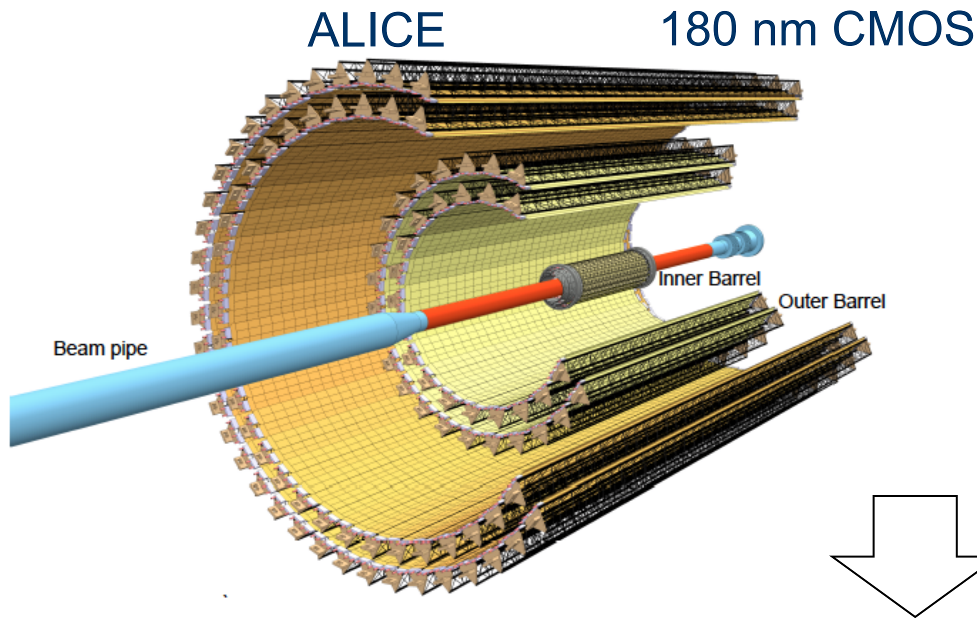
[a] This includes a safety factor of ten

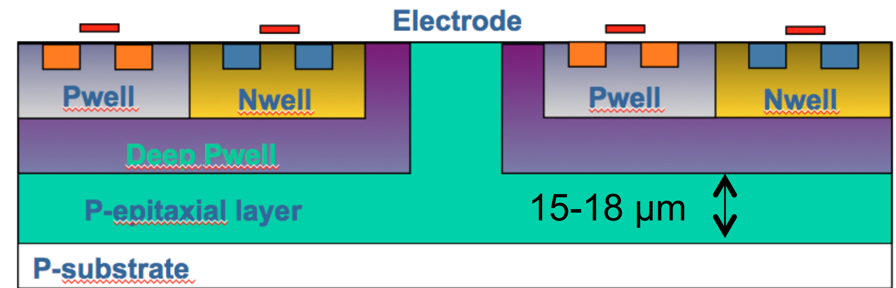
current baseline also for ILC pixels



MAPS for ALICE (2022) and for the ILC (20xx?)

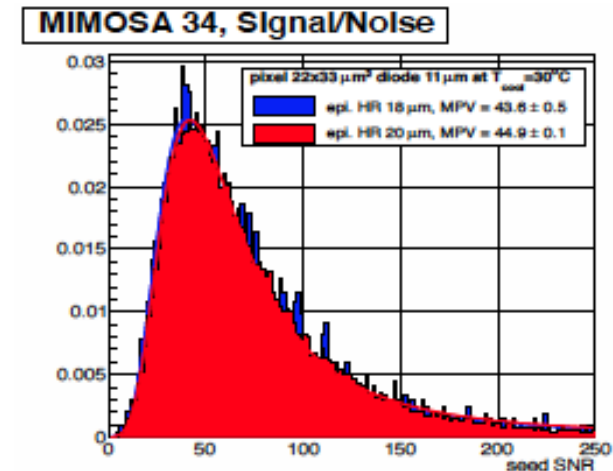
ALICE 180 nm CMOS





- 6 metal layers
- epi layer between ≳ 1 kΩcm, 15-18 µm
- Deep Pwell shielding

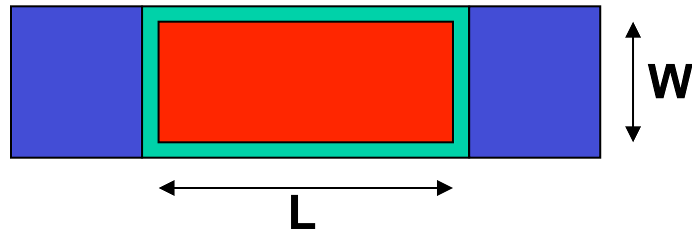
- **MISTRAL/ASTRAL** (IPHC Strasbourg)
  - MIMOSA type, rolling shutter archit. w/ column parallel readout
  - pixel size 20x30µm, integration time ~30µs, ~250mW/cm^2
  - ASTRAL: in-pixel discr. & binary R/O, 10µs frame time, ~150 mW/cm^2
- **CHERWELL** (RAL)
  - 128 pixels organized in strixels, each w/ discriminator, read out in parallel
  - pixel size 20x20µm, integration time ~30µs, ~100mW/cm^2
- **ALPIDE** (CERN-INFN-Wuan)
  - each pixel has its own amplifier and discriminator, data driven R/O
  - pixel size 28x28µm, R/O time ~2-3µs, <100mW/cm^2

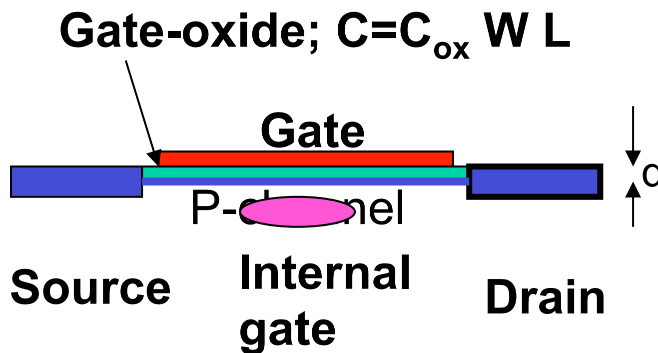


TowerJazz 180 nm HR-epi (1 kΩcm), epi layer up to 40 µm thick

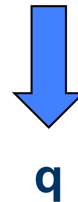
DEPFET Pixels

How does a DEPFET work?





A charge q in the internal gate induces a **mirror charge** αq in the channel (α <1 due to stray capacitance). This mirror charge is compensated by a change of the gate voltage: $\Delta V = \alpha\, q / C = \alpha\, q / (C_{ox}\, W\, L)$ which in turn **changes the transistor current I_d**.



q

FET in saturation:

$$I_d = \frac{W}{2L}\mu C_{ox}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right)^2$$

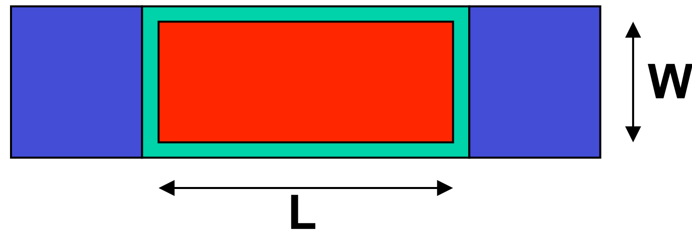
I_d: source-drain current
C_{ox}: sheet capacitance of gate oxide
W,L: Gate width and length
μ: mobility (p-channel: holes)
V_g: gate voltage
V_{th}: threshold voltage

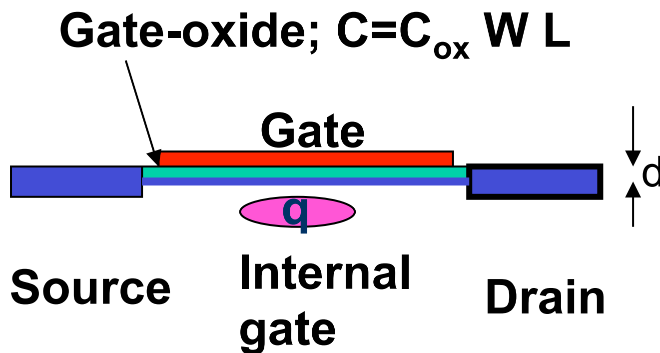
Conversion factor:

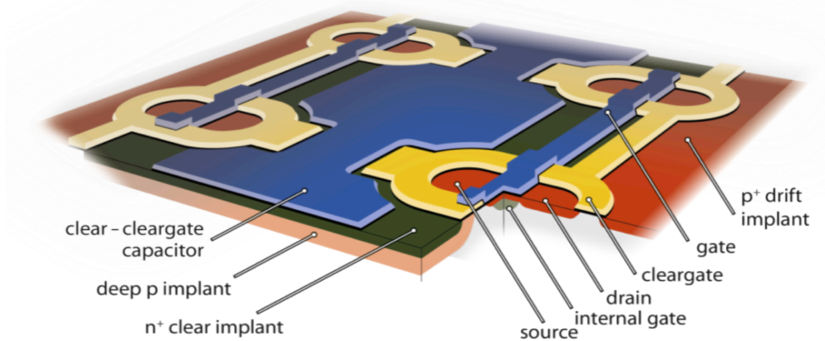
$$g_q = \frac{dI_d}{dq_s} = \frac{\alpha\mu}{L^2}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right) = \alpha\sqrt{2\frac{I_d\mu}{L^3WC_{ox}}}$$

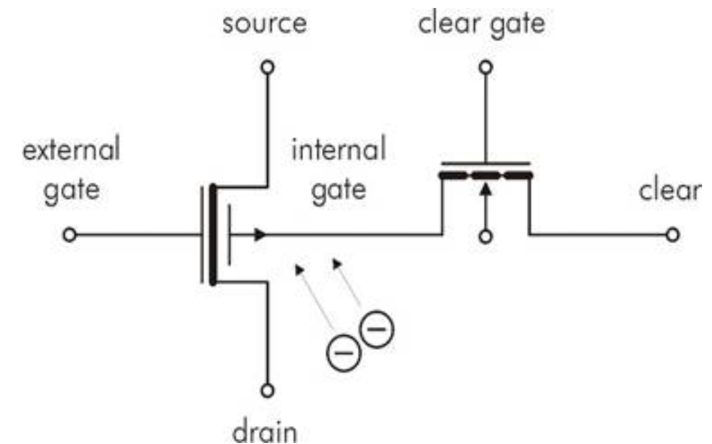
$$g_m = g_q = \alpha\frac{g_m}{WLC_{ox}} = \alpha\frac{g_m}{C}$$

How does a DEPFET work?









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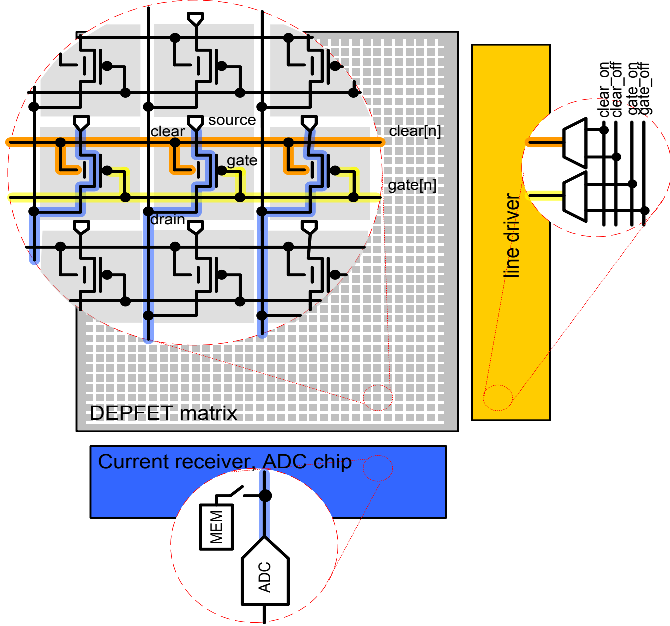
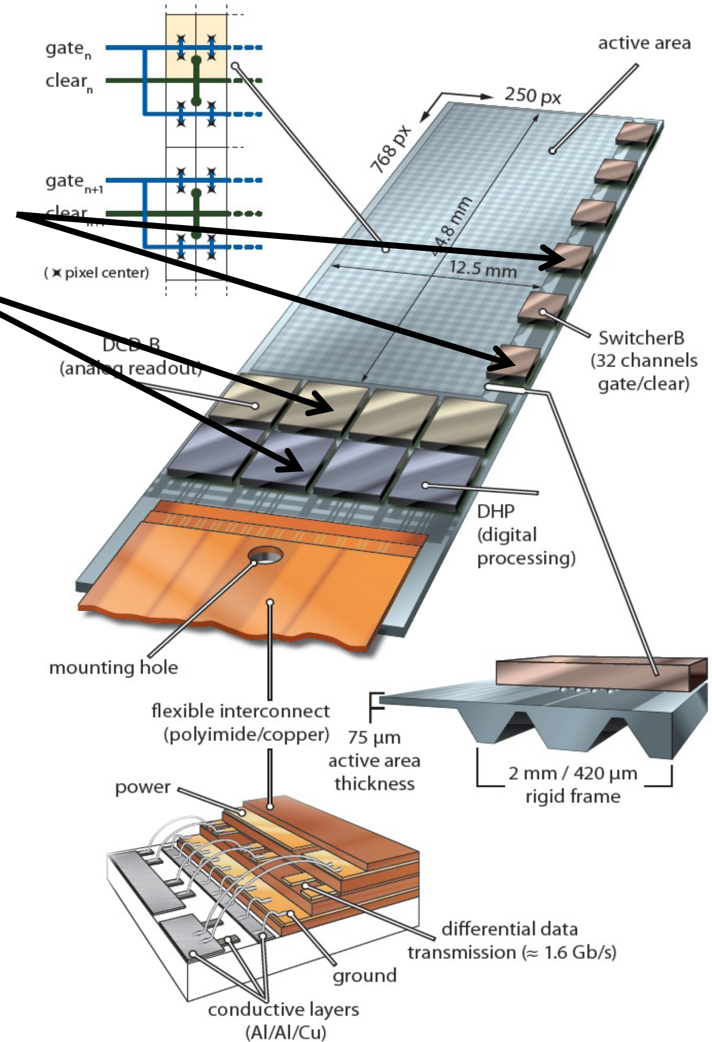
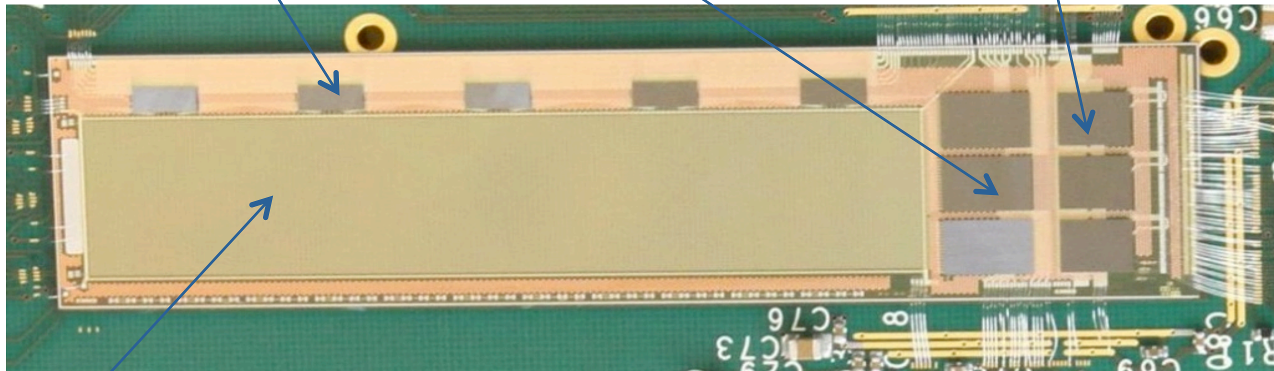
- Internal amplification $g_q \sim 500\ \mathrm{pA/e^-}$
- Small intrinsic noise
- Sensitive off-state, no power consumption

DEPFET PXD @ Belle II @ SuperKEKB



- DEPFET pixel transistors arranged in a matrix
- row wise select and clear column wise readout
- 100 ns per row
  20 µs per frame

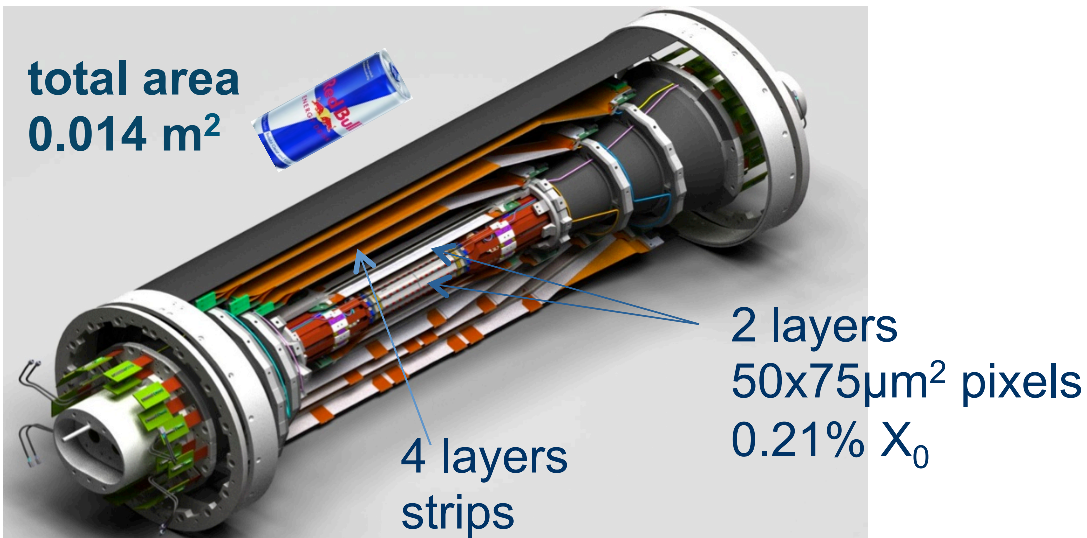


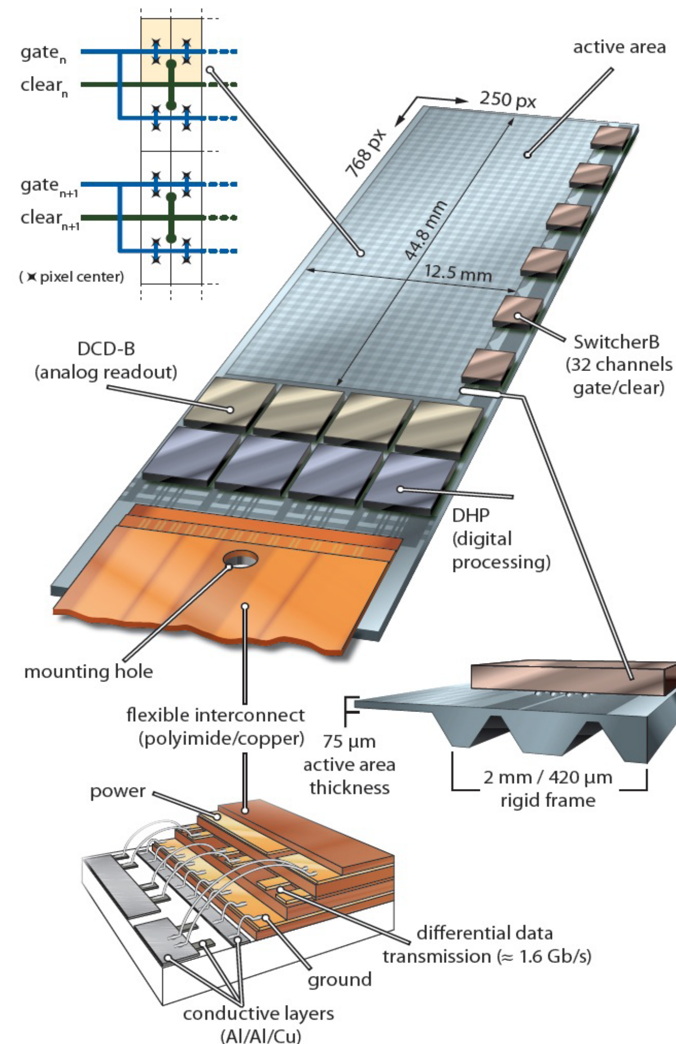


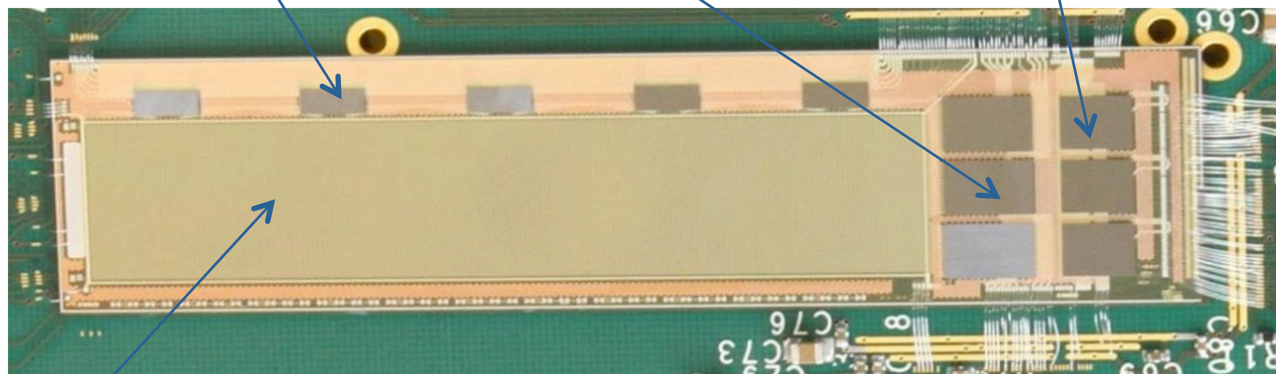
full-size module prototype

DEPFET PXD @ Belle II @ SuperKEKB

2-layer pixel vertex detector (PXD)





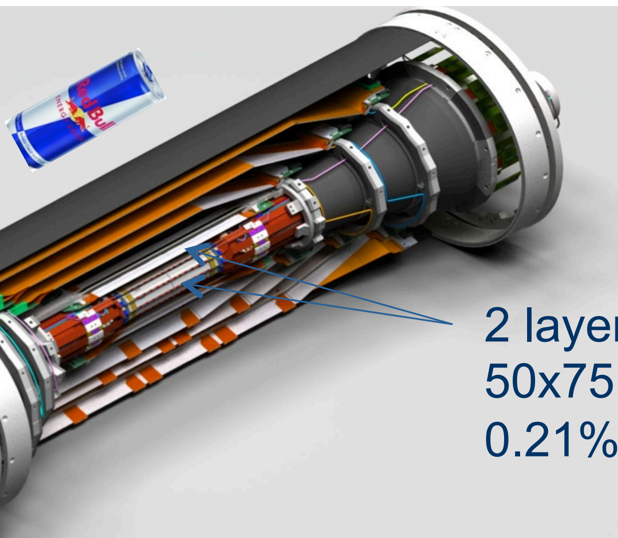


full-size module prototype

DEPFET PXD @ Belle II @ SuperKEKB

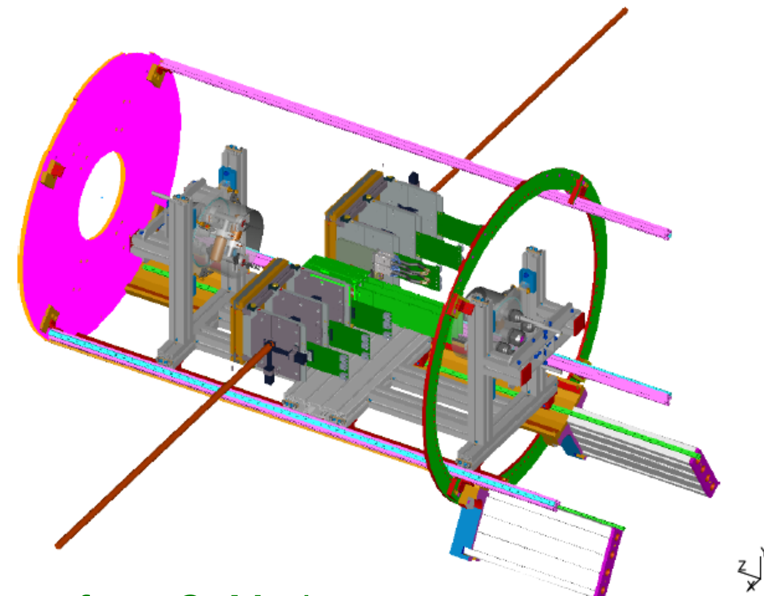
2-layer pixel vertex detector (PXD)

total area
0.014 m²



2 layers
50x75μm² pixels
0.21% X_0

combined test beam
pixels + strips (Jan 2014)

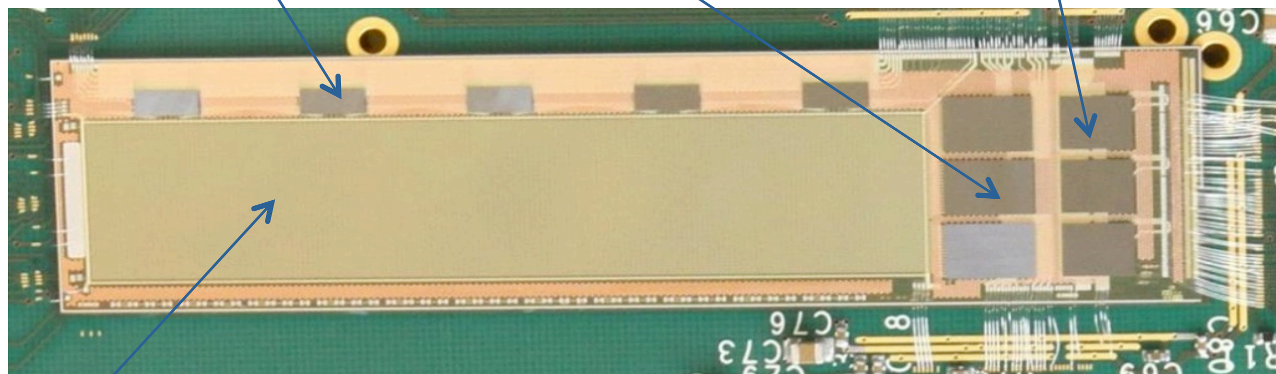


from C. Marinas

switcher chips

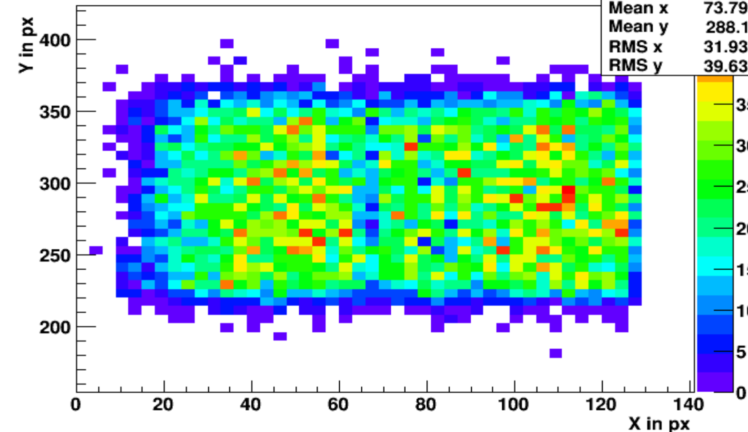
current digitizer chips

data processing chips



DEPFET sensor

full-size module prototype

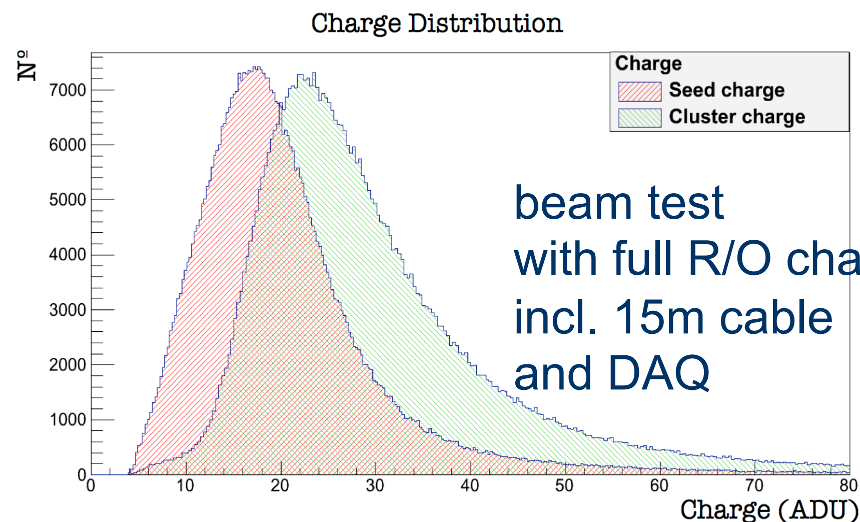


DEPFET PXD @ Belle II @ SuperKEKB

2-layer pixel vertex detector (PXD)

total area
0.014 m²

2 layers
50x75μm² pixels
0.21% X_0

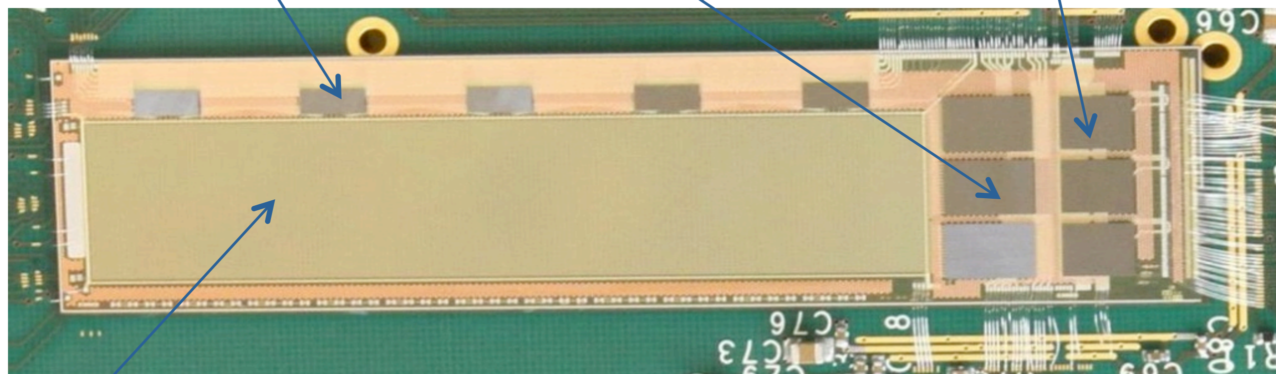


beam test
with full R/O chain
incl. 15m cable
and DAQ

switcher chips

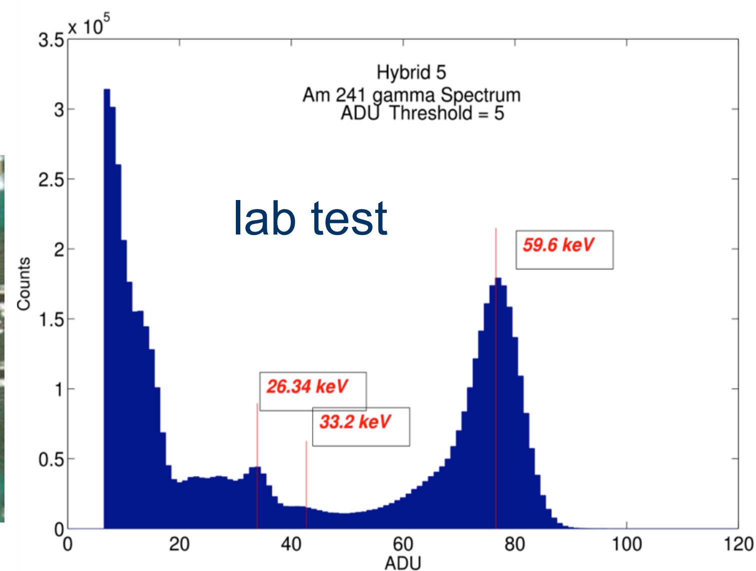
current digitizer chips

data processing chips



DEPFET sensor

full-size module prototype



lab test

Reality

	semi-monolithic MAPS/DEPFET
• good S/N	➢ OK? / YES
• µm space resolution	✓ but ~1 µm is tough
• ~ns time resolution	➢ slow rolling shutter
• > 10 MHz / mm^2 rate capability	➢ < 1 MHz/mm^2
• radiation hard to 1 Grad	➢ < 10 Mrad
• radiation length per layer < 0.2% x/X_0	✓ but tough
• all in one monolithic pixel "chip"	○ not yet

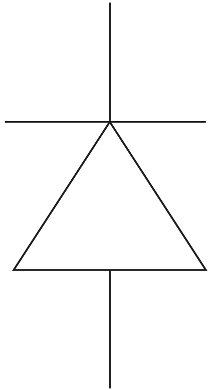
HV and HR - Monolithic CMOS Pixels

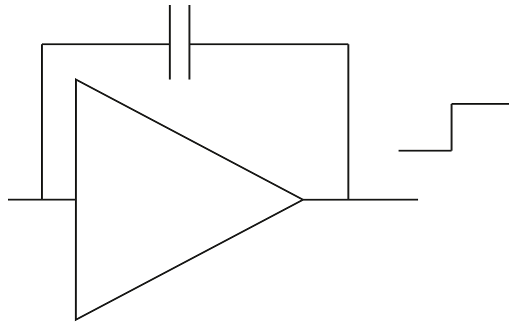
... conventional MAPS (on epitaxial Si) not suited for pp @ LHC

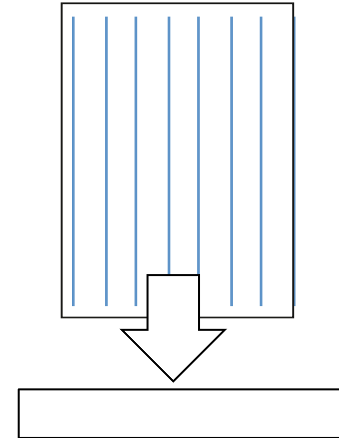
... generate depletion layer under CMOS layer

... functionality wise MAPS with high resistivity epi material
have the same target: full CMOS on a (thin) depleted layer

growing dollaboration:
Bonn, CERN, CPPM, Geneva, Glasgow, Göttingen, Heidelberg, Liverpool, LBNL, ...





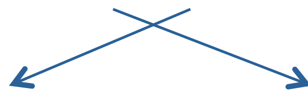


pixel-
sensor

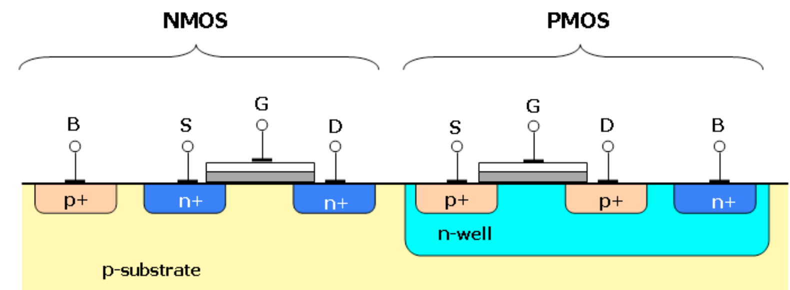
chip: pixel cell: amplifier, discriminator ...
o(100) transistors

chip: column/region architecture buffers, periphery ...
o(>100M) transistors ...
requires full CMOS
i.e. pMOS and nMOS in circuit

signal ∝ depletion depth

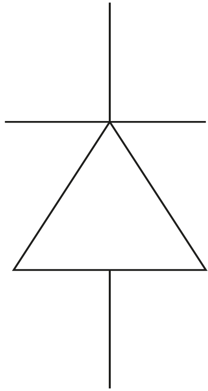


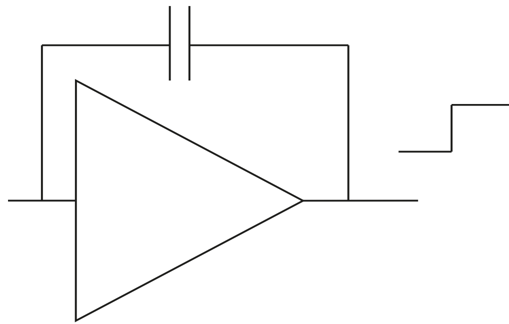
$$d \sim \sqrt{\rho \cdot V}$$



I. Peric et al. ⟷ T. Hemperek et al.

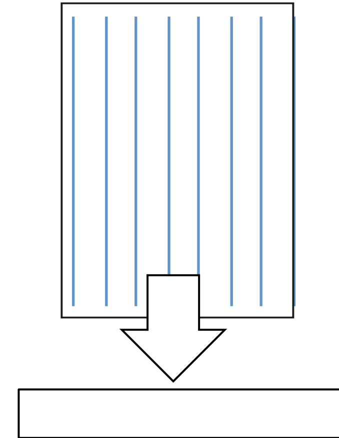
HV-CVMOS ... approach to generate depletion depth





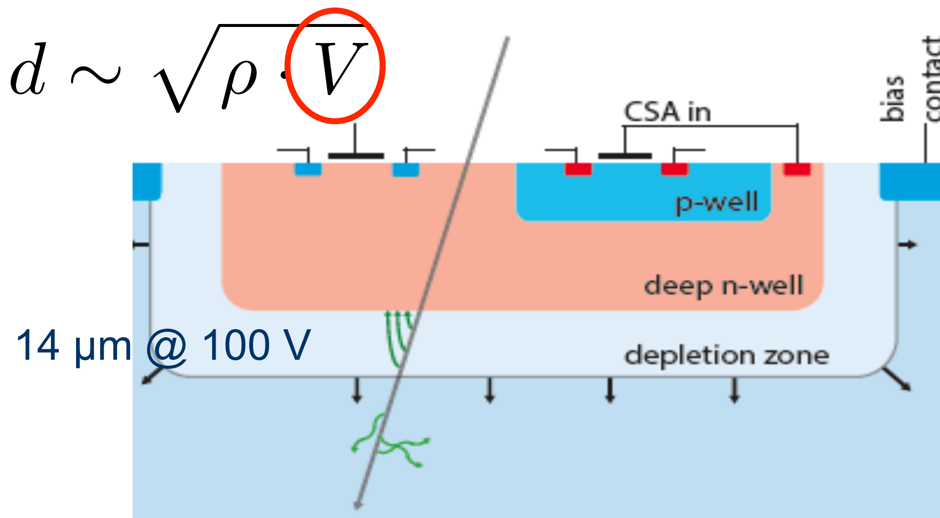
pixel-
sensor

chip: amplifier, discriminator ...
o(100) transistors



chip: column architecture
buffers, periphery ...
o(50M transistors) ...

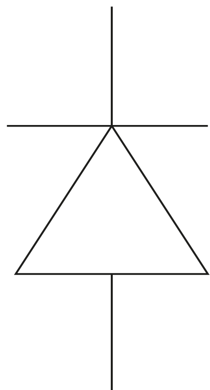
$$d \sim \sqrt{\rho \cdot V}$$



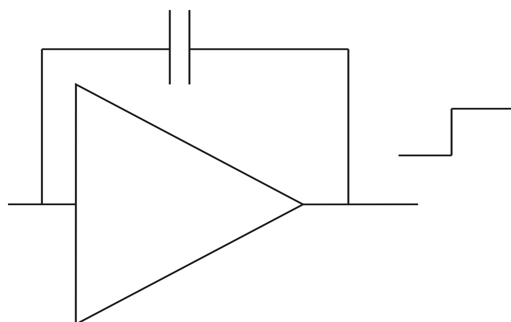
14 µm @ 100 V

I. Peric et al.
NIM A582 (2007) 876-885
NIM A731 (2013) 131-136

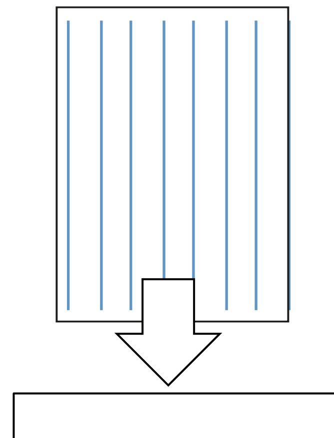
HR-CVMOS ... approach to generate depletion depth



pixel-
sensor

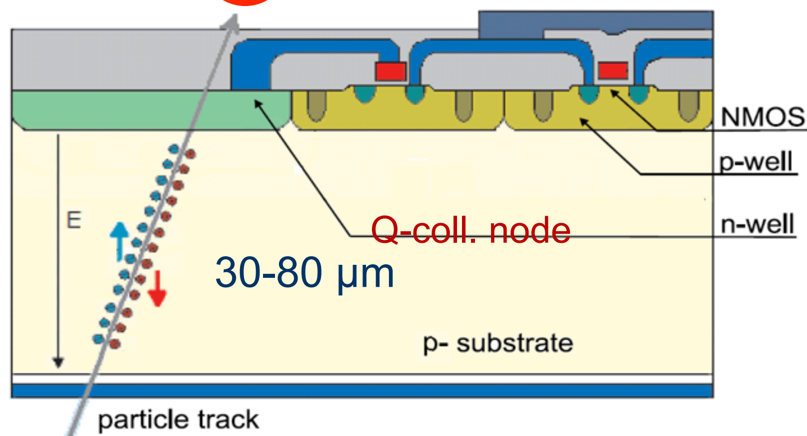


chip: amplifier, discriminator ...
o(100) transistors



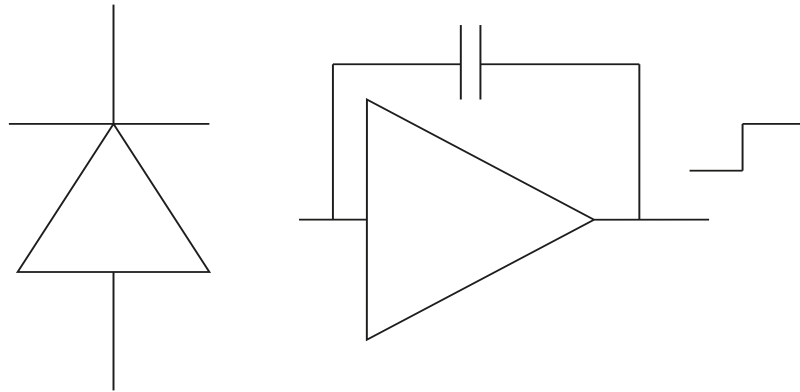
chip: column architecture
buffers, periphery ...
o(50M transistors) ...

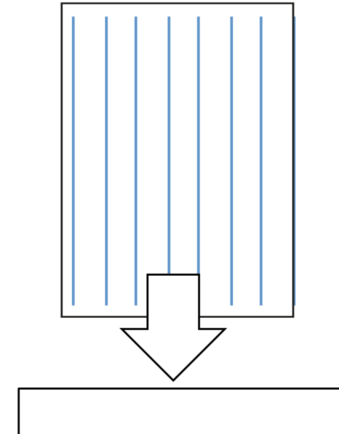
$$d \sim \sqrt{\rho \cdot V}$$



T. Hemperek et al.,
http://indico.cern.ch/getFile.py/access?resId=1&materialId=slides&confId=273886

CCPD – approach (capacitively coupled pixel detector)

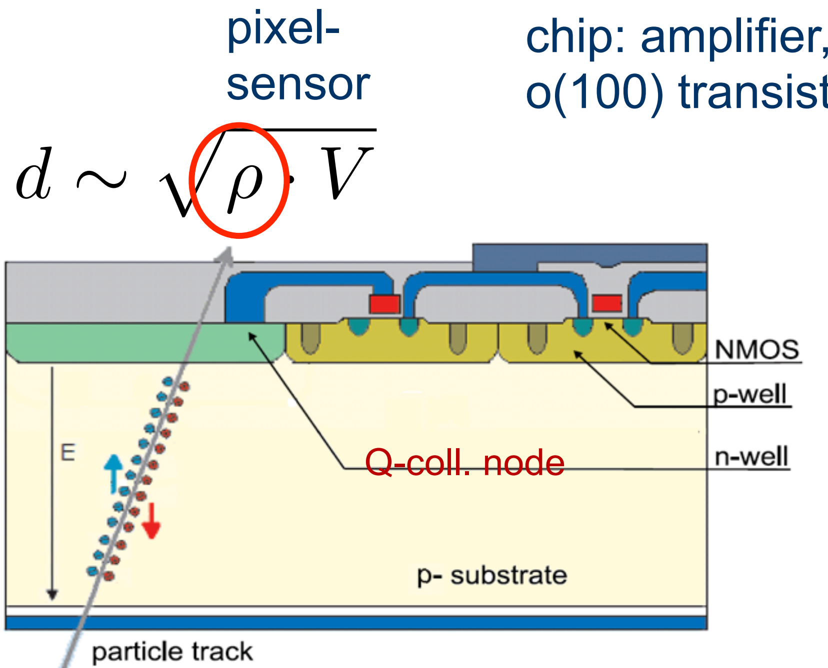




pixel-
sensor

chip: amplifier,
o(100) transist

$$d \sim \sqrt{\rho \cdot V}$$

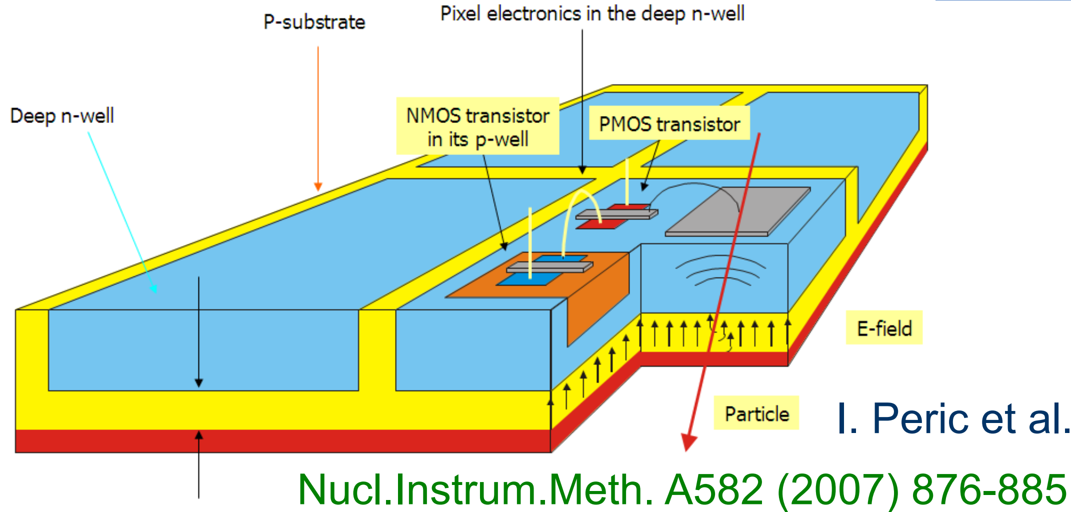


CCPD (see talk I. Peric, Friday):
AMS 180 nm -> EPROS, LFOUNDRY, others
... replaces sensor

- ✓ first amplification stage in sensor
- ✓ Q-collection by drift (different to conv. MAPS)
- ✓ thin sensor
- ✓ indications of radiation hardness for HL-LHC
- × d ~ o(10 µm) in HV-CMOS ... but may be enough
- ✓ larger o(50 µm) ... with HR-CMOS

... capacitance not easily small

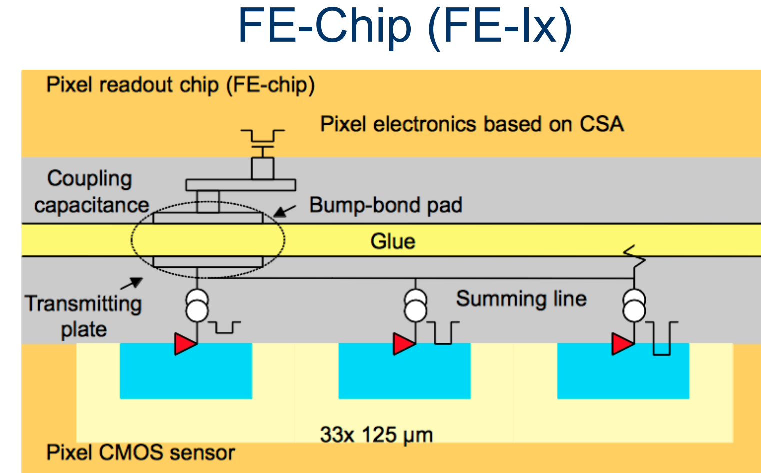
CCPD – approach (capacitively coupled pixel detector)



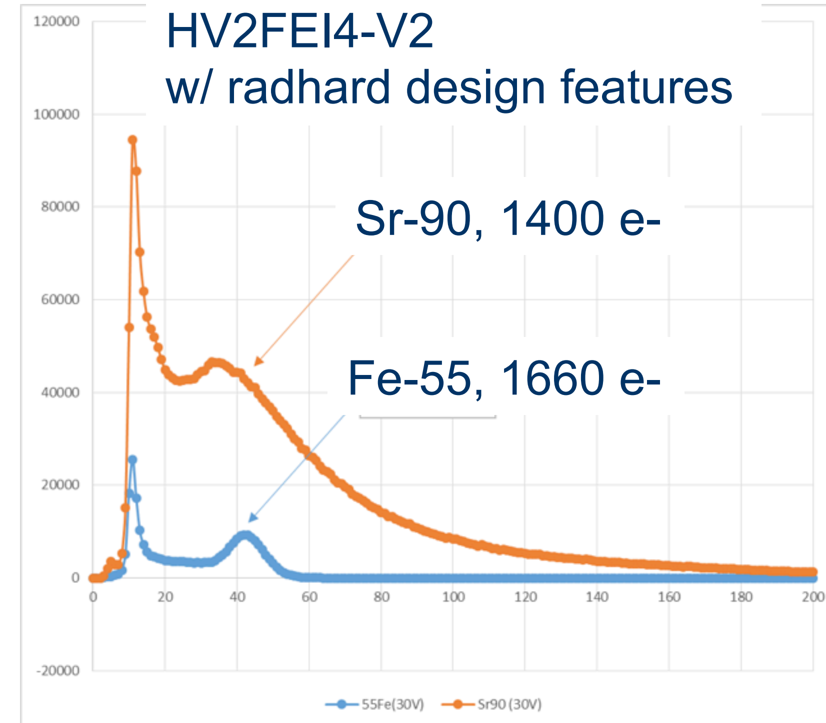
I. Peric et al.

Nucl.Instrum.Meth. A582 (2007) 876-885

FE-Chip (FE-Ix)



- AMS 180 nm HV process (p-bulk) ... 60-100 V
- deep n-well to put pMOS and nMOS (in extra p-well)
- some CMOS circuitry possible (ampl. + discr.)
- ~10-20 µm depletion depth → 1-2 ke signal
- various pixel sizes (~20x20 – 50x125 µm^2)
- several prototypes
- also strip like geometries possible
- replaces „sensor“ (amplified signal) in a „hybrid pixel“: any bonding (bump, glue, other...)
- big advantage: industrial CMOS process
- ☹ electrical contacts through wire bonds
- indications of radiation hardness to ~10^{16} n_{eq} / cm^2

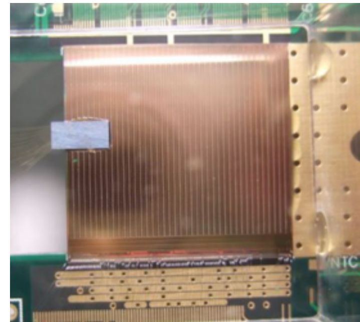


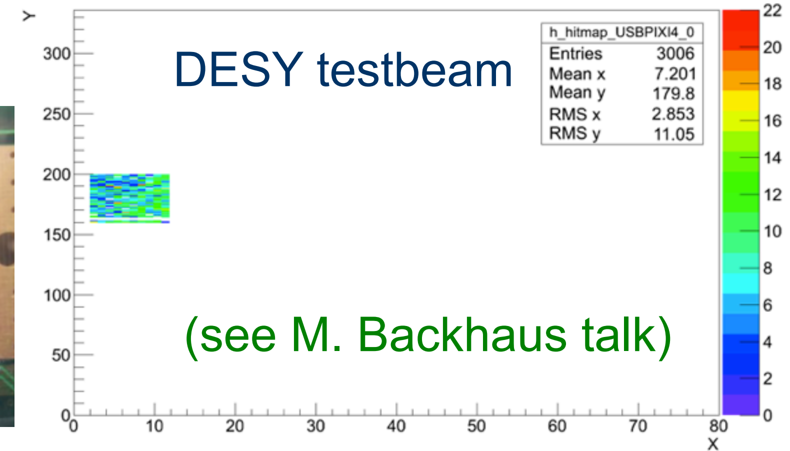
CCPD with HV-CMOS

see talks by I. Peric/M. Backhaus (Friday)

preliminary irradiation tests: using reactor neutrons 1×10^{15} and 1×10^{16} n_{eq}/cm^2
also with protons and X-ray (862 Mrad !)

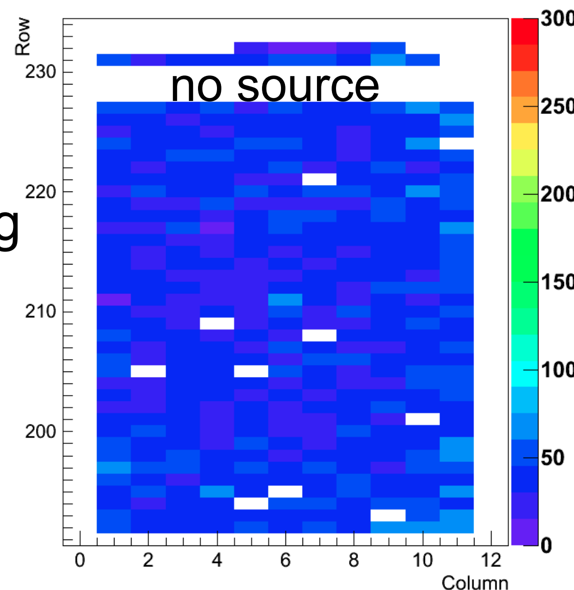
HV2FEI4 glue bonded to FEI4
and irradiated to 1×10^{15} n_{eq}/cm^2

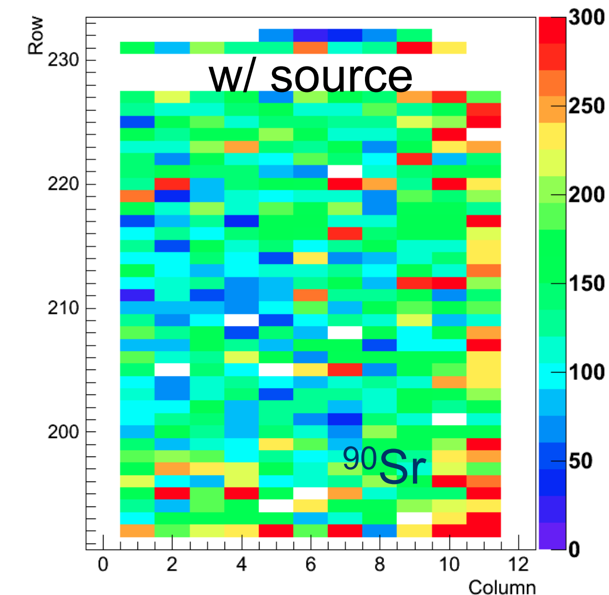




1×10^{16} n_{eq}/cm^2

- @RT after ~30 days / annealing
- source scan with ~25 V bias
- still alive, noise occ. ~10^{-10}, not yet clear if this can be claimed as radiation resistant to this level

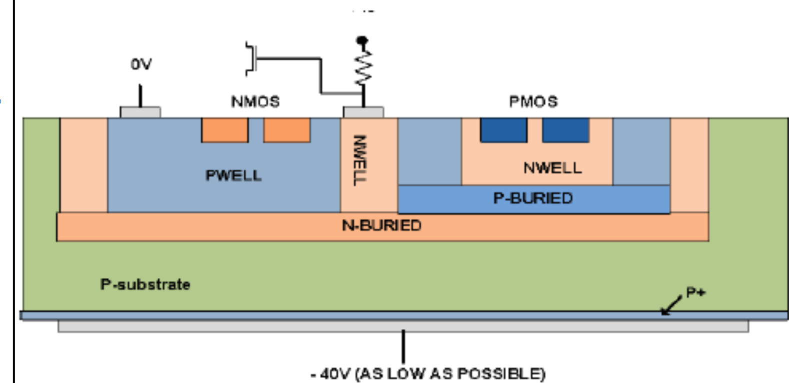




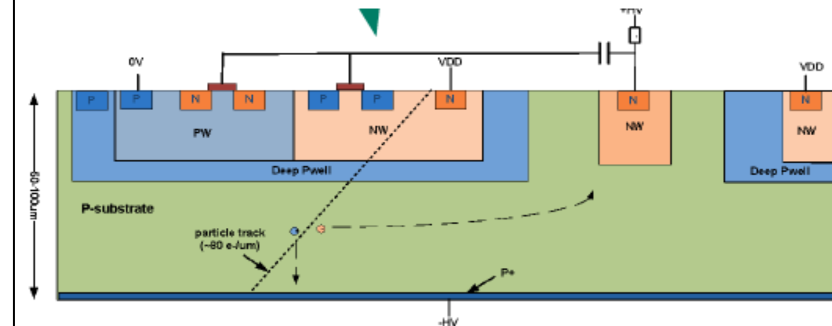
HR-CMOS (not yet CCPDed)

- needed

  - **high resistivity** substrate material vendor or costumer supplied
  - (several) **deep implants** for Q-collection and isolation (wells)
  - **backside processing** for thinning and back contact
  - (also **strip-like geometries are** possible)



standard with addn'l backside contact & high resistivity -> >50 µm depletion depth and full CMOS logic



sideward drift to small collection diode

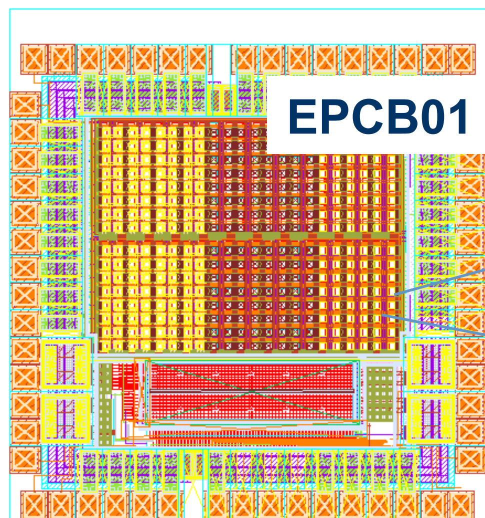
- addressed vendors

  - Vendor A: 150nm, 2kΩ-cm n-bulk, **50µm depl.** → MPW submitted Q4 2012
  - Vendor B: 180nm, 1kΩ-cm p-bulk + epi (various), → submitted Q1 2013
  - Vendor C: 180nm, SOI HV proc.,100Ωcm p-bulk, → MPW submitted Q1 2013
  - Vendor D: 130nm, 3kΩ-cm p-bulk → MLM (**full wafers**) Q1 2014
  - Vendor E: 150nm, 2- 5 kΩcm p-bulk, **>50 µm depl.** → MLM to be subm. Q2 2014

T. Hemperek, H. Krüger (+ I. Peric, P. Pangaud et al. on Vendor D)

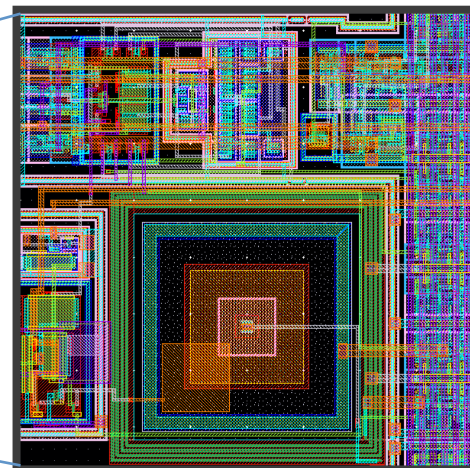
HR-CMOS

~200 transistors in pixel
real matrix operation



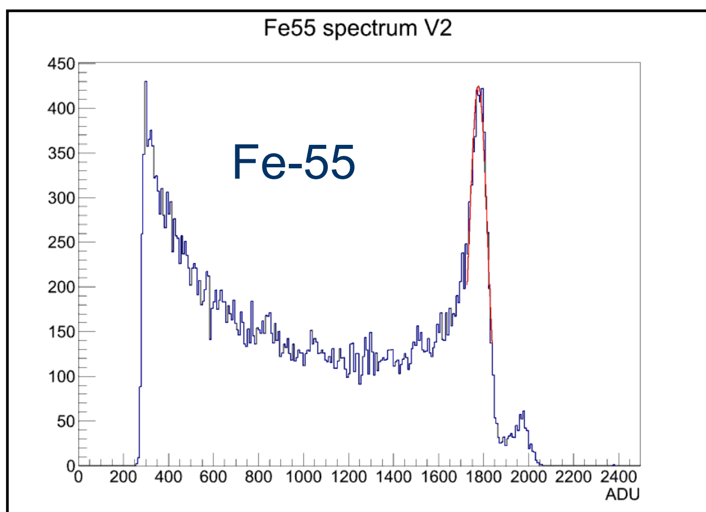
Vendor A

352 pixels
40×40 μm²



M. Havranek
T. Hemperek
(Bonn)

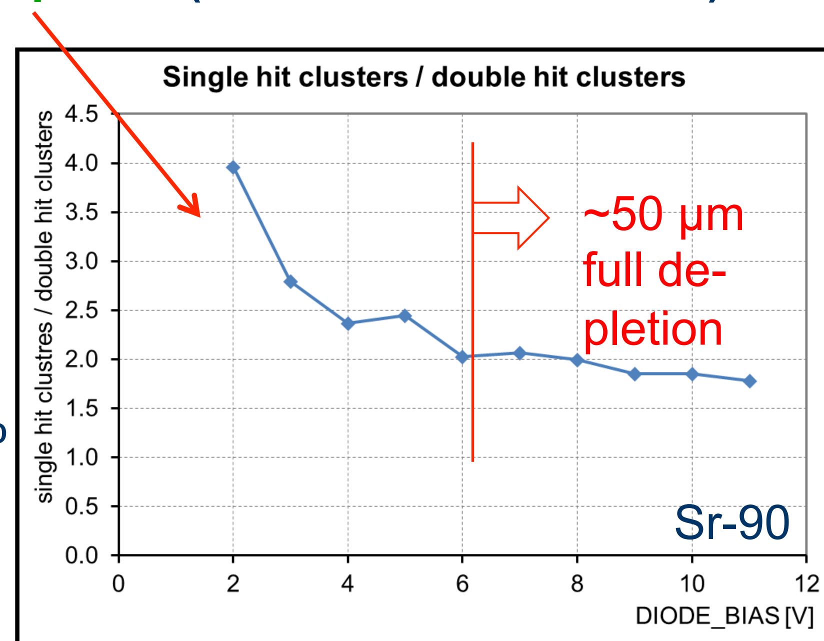
50μm, back side processed, full CMOS, fully depleted (>2kOhm-cm substrate)



good
noise (~30 e)
and
thres. disp. (~80 e)

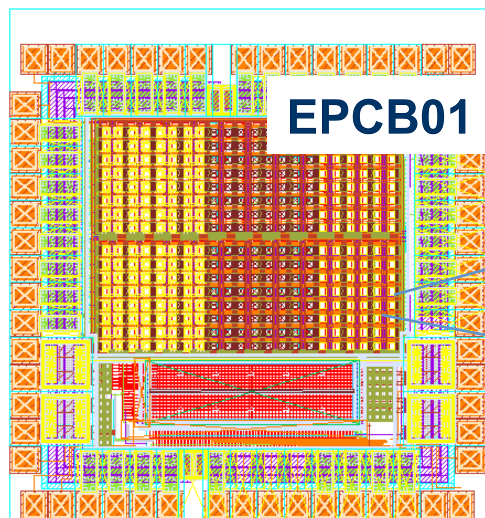
gain variation ~10%

full depletion
from cluster size
saturation

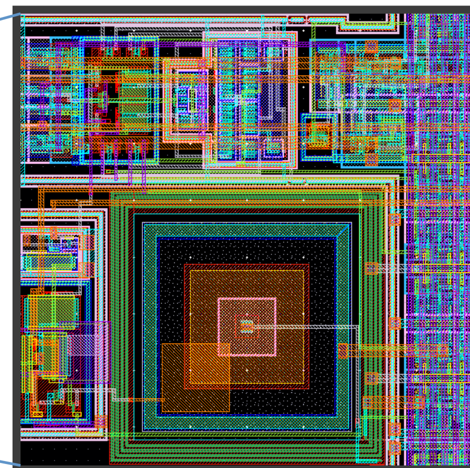


HR-CMOS

~200 transistors in pixel
real matrix operation



352 pixels
40×40 μm²

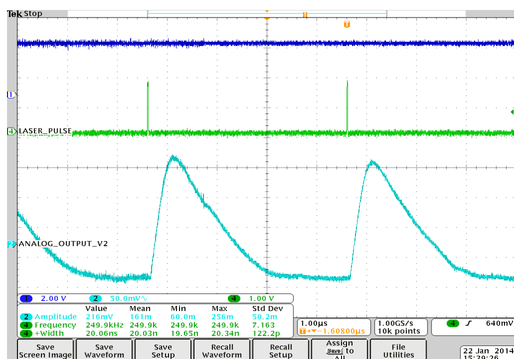


50μm, back side processed, full CMOS, fully depleted (>2kOhm-cm substrate)

Laser Scan

T. Obermann (Bonn)

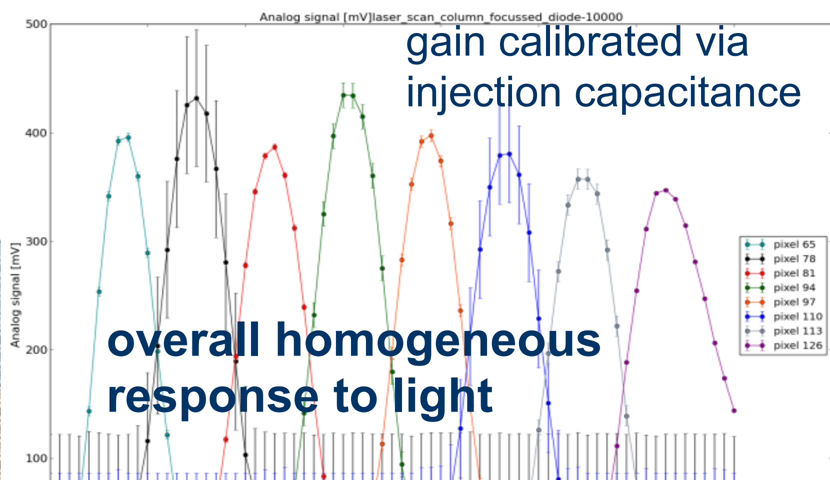
full depletion voltage ~10V
leakage current ~20 nA



V1 — resistor — V2 — diode — V3

7	8	23	24	39	40	55	56	71	72	87	88	103	104	119	120	135	136
6	9	22	25	38	41	54	57	70	73	86	89	102	105	118	121	134	137
5	10	21	26	37	42	53	58	69	74	85	90	101	106	117	122	133	138
4	11	20	27	36	43	52	59	68	75	84	91	100	107	116	123	132	139
3	12	19	28	35	44	51	60	67	76	83	92	99	108	115	124	131	140
2	13	18	29	34	45	50	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	141
1	14	17	30	33	46	49	[illegible]	65	78	81	94	97	110	113	126	[illegible]	142
0	15	16	31	32	47	48	63	64	79	80	95	96	111	112	127	128	143
344	343	328	327	312	311	296	295	280	279	264	263	248	247	232	231	216	215
345	342	329	326	313	310	297	294	281	278	265	262	249	246	233	230	217	214
346	341	330	325	314	309	298	293	282	277	266	261	250	245	234	229	218	213
347	340	331	324	315	308	299	292	283	276	267	260	251	244	235	228	219	212
348	339	332	323	316	307	300	291	284	275	268	259	252	243	236	227	220	211
349	338	333	322	317	306	301	290	285	274	269	258	253	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
350	337	334	321	318	305	302	289	286	273	270	257	254	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
351	336	335	320	319	304	303	288	287	272	271	256	255	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

resistor — diode
V6 — V5

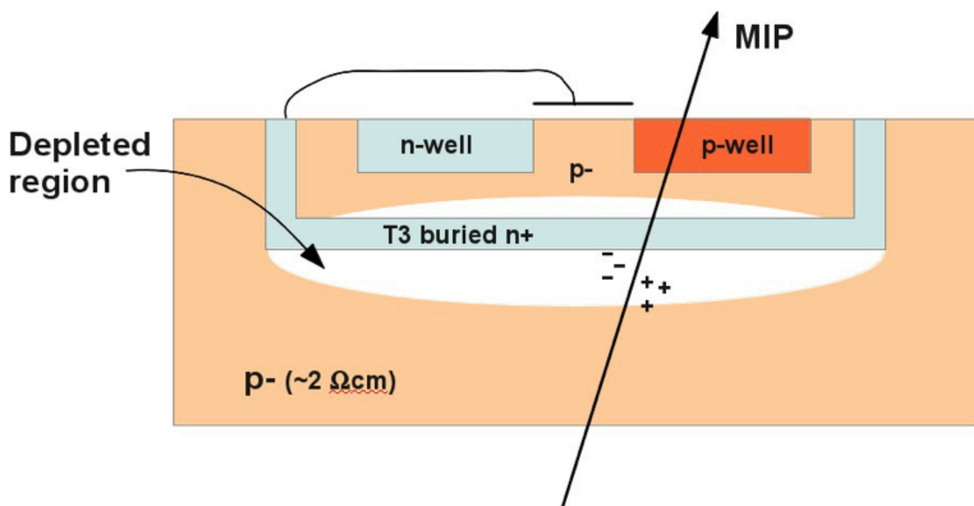


gain calibrated via injection capacitance

overall homogeneous response to light

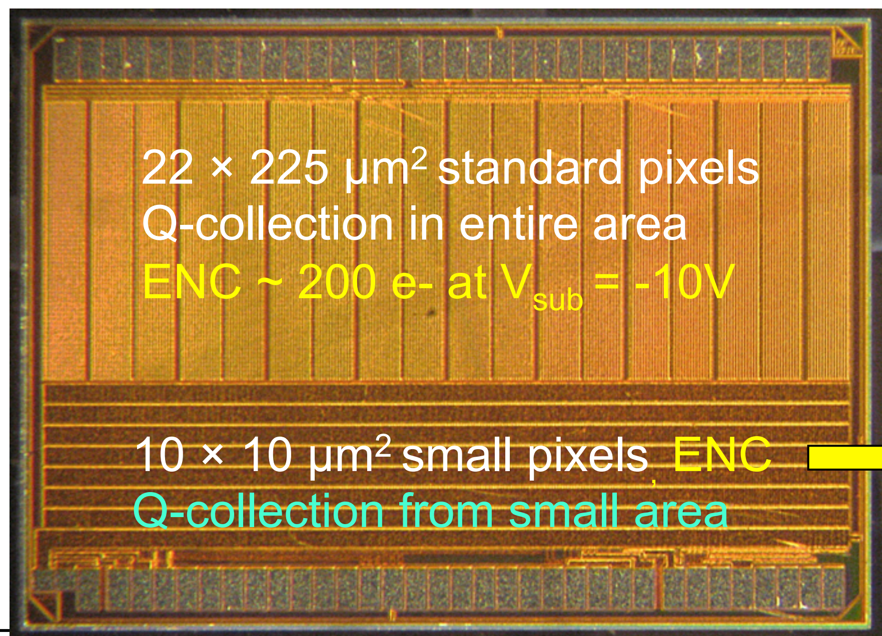
radiation hardness?
100 Mrad X-ray -> CMOS electronics ok
$>10^{14}$ cm^{-2} neutrons (Ljubiljana soon)

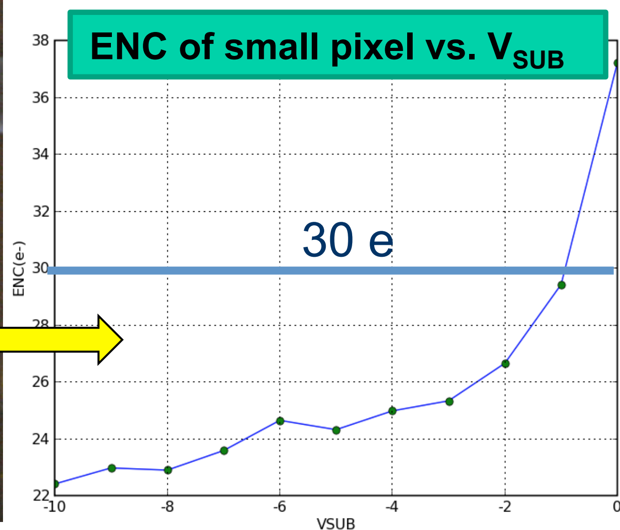
T3MAPS: partial depletion, full CMOS (LBNL)



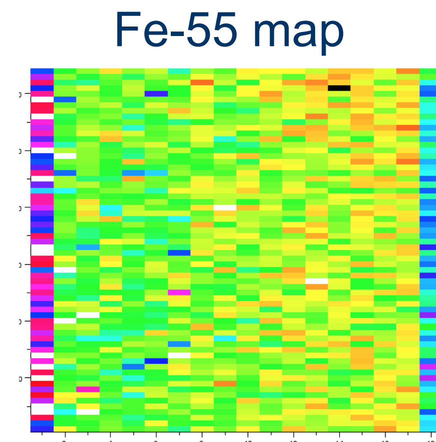
A. Mekhaoui, M. Garcia-Sciveres at al.

- use IBM 130 nm process (same as for FE-I4) offering also buried N-well in p-substrate to create depletion region and serve as Q-collecting electrode
- ✓ Q-collection by drift → rad. hardness
- ✓ full use of CMOS and synthesized logic
- × rel. large capacitance
- × low res. bulk → small depl. region (~5 μm)
- × perhaps more x-talk sensitive (n-well node)
- radiation program has started



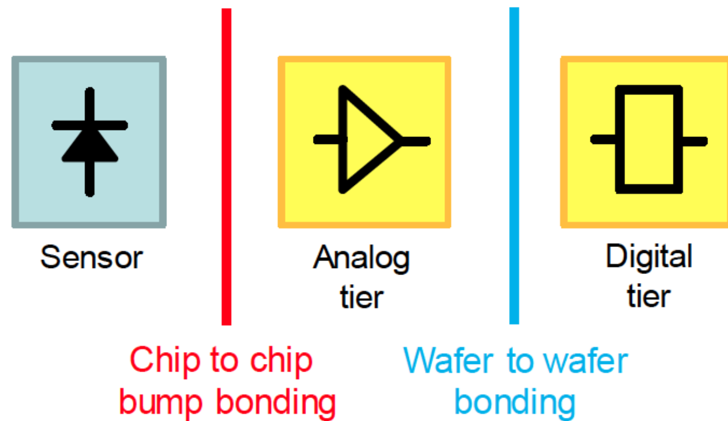


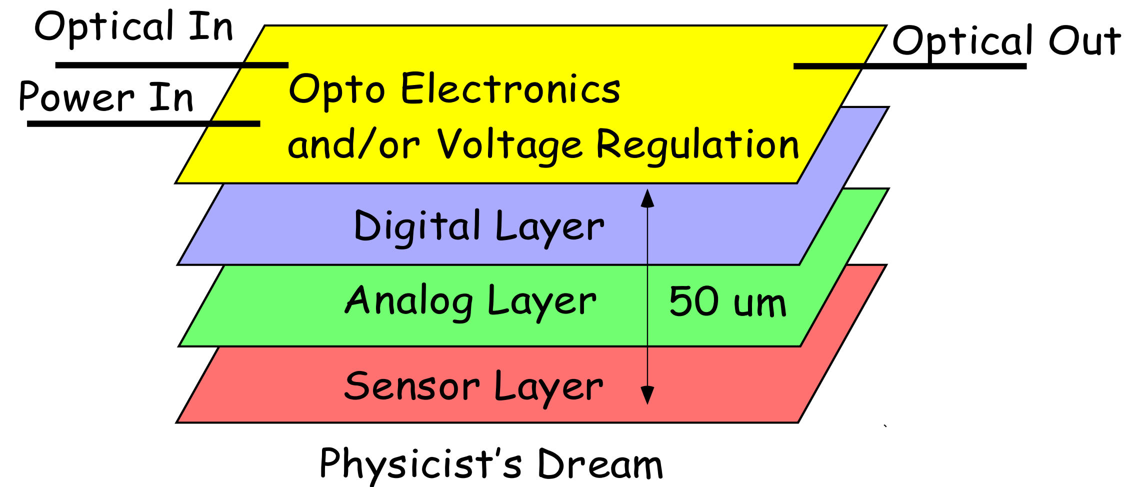
Fe-55 map



3D integration …

… various CMOS layers





3D integration promises

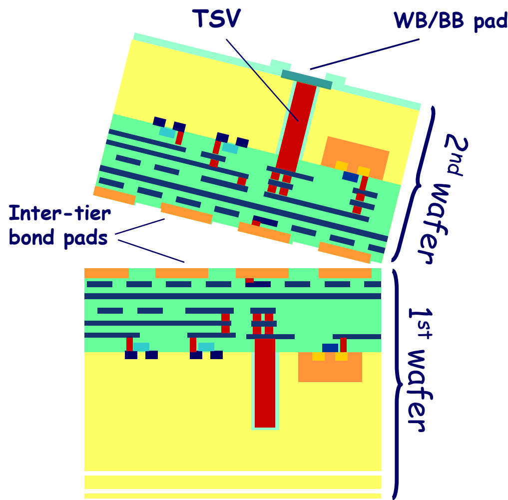
- higher granularity (smaller pixel size)
- lower power
- large active over total area ratio
- dedicated technology for each functional layer

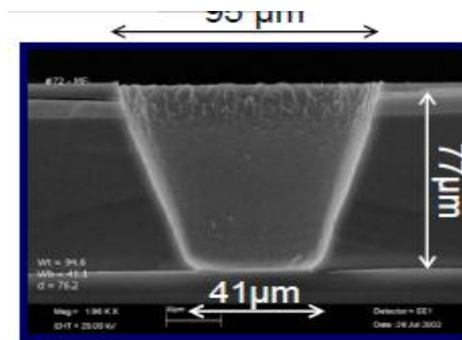
prototyping with

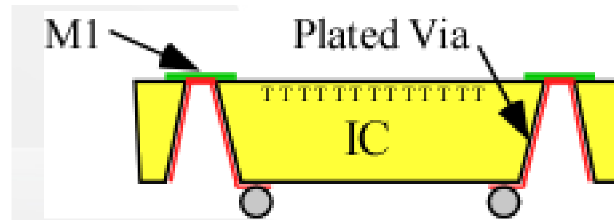
- **LAPIS Semic.**
- **MIT LL**
- **Tezzaron/ Chartered**

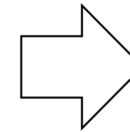
3D integration …

within **AIDA** network WP3



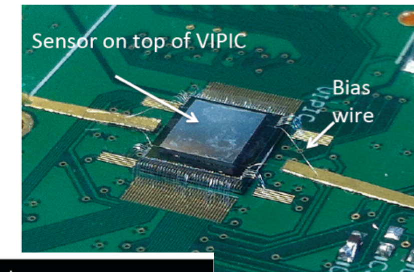


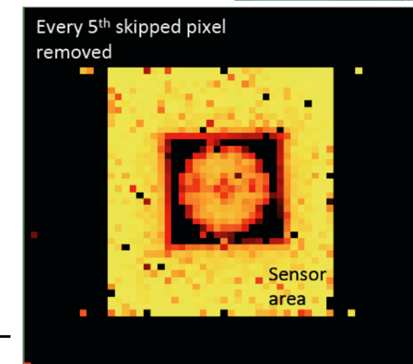




FE-I3 operated through TSVs (^{241}Am)

M. Barbero, T. Fritzsch, L. Gonella, F. Hügging et al., JINST 7 (2012) P08008





120V
ing 2 sources
Fe 5.9keV (mask not
oto)

VIPIC

various approaches

- from (comparatively simple) post-processed TSVs with fairly large pitch, based on ATLAS FE-chips
- to via first/middle multi-Tier approaches (applied within the CMOS process plus post-processing) (CPPM/Bonn/ MPI)
- to first working 3D-integrated chip (R. Yarema et al, FNAL), VIPIC -> photon science

Conclusions

The "brink to a new era" currently looks like …

- for HL-LHC (pp collisions) at the innermost layers
  - hybrid pixels possibly with some 3D integration will be able to cope with radiation and rate levels ... perhaps also DMAPS/CCPDs?
  - with hybrid pixelsmaterial will not easily go below 1% X_0 per layer
- for (almost all) other applications in HEP or Heavy Ions
  - thin materials
  - high integration
  - costs (especially for large area applications) will dominate the issue.
- CMOS pixels in whatever variants
  - "smart" sensor bonded to dedicated digital chip ... or ...
  - fully monolithic ... or ...

  open a new field which may even range into high radiation applications with lots of room for R&D in the coming years

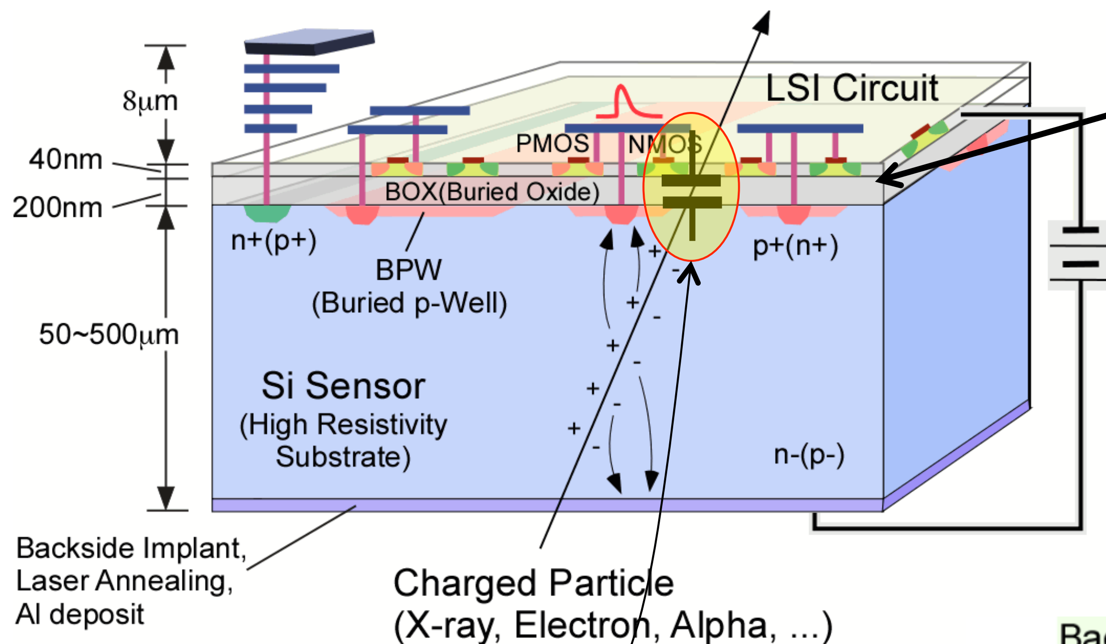
backup

VIPIC (Vertically Integrated Photon Imaging Chip)

- The VIPIC is designed to quickly count the number of hits in every pixel and read out the # of hits, and addresses in a dead timeless manner.
- To achieve the desired speed requires a sparsified digital readout, where only the pixels which have registered a hit are read out.
- To implement the sparsified readout requires a digital design which would not fit in the desired pixel size of 80 x 80 um along with the analog circuitry.
- Thus design was split into analog and digital design layers of equal area to meet the pixel size requirement.
- This required a large number (25) of signals to be passed between the analog and digital section of every pixel (over 100,000/chip)
- Chip operates in 2 modes
  - Timed Readout of # of hits and addresses at low occupancy (~ 10 photons/cm^2/10 usec)
  - Imaging – alternating 5 bit counters read out # of hits in each time slot without addresses (less data output without addresses)

CMOS on SOI ... Silicon on Insulator

the scheme



thick burried oxide (BOX)

LAPIS Semicond. (formerly OKI)

principle challenges

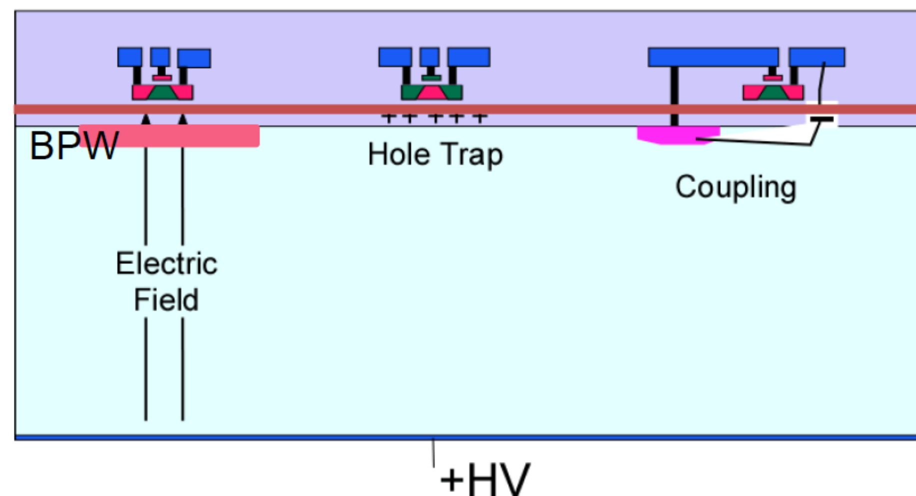
- back gate effect
- radiation resistance
- x-talk

so far:

several cures tried:

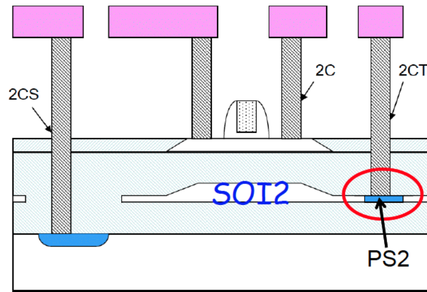
- buried p-well
- nested wells
- double SOI → current asset

- also: stitching possible
- also: vertical integration (in process)



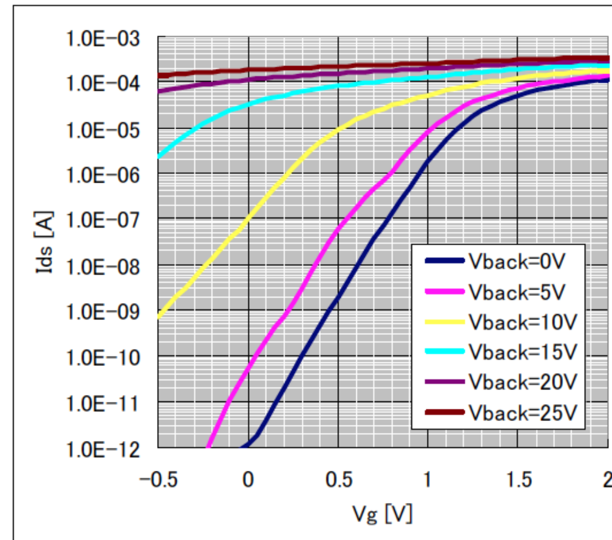
Double SOI

Yasuo Arai (Vertex 2013)

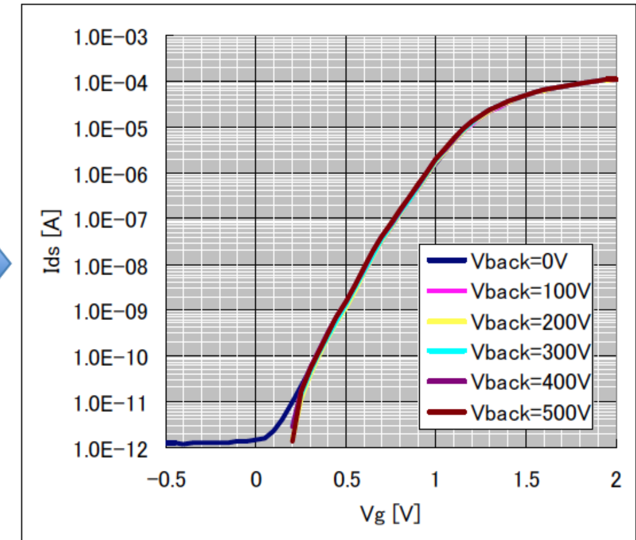


- Back Gate Effect is fully suppressed
- rad. hardness still not easy

a) Middls-Si Floating



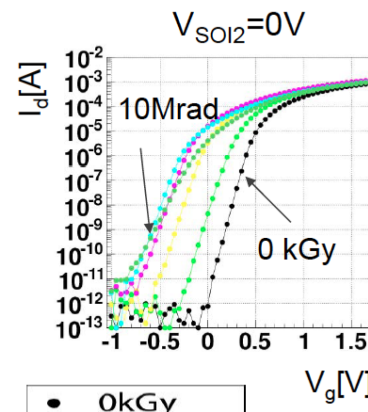
b) Middle-Si = GND

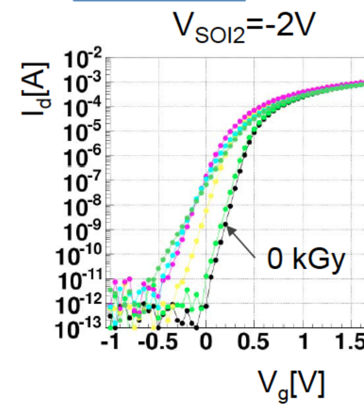


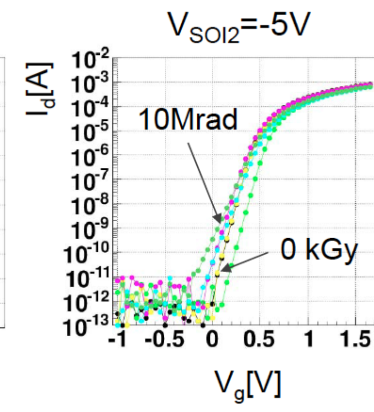
NMOS

L/W =0.35um/5um

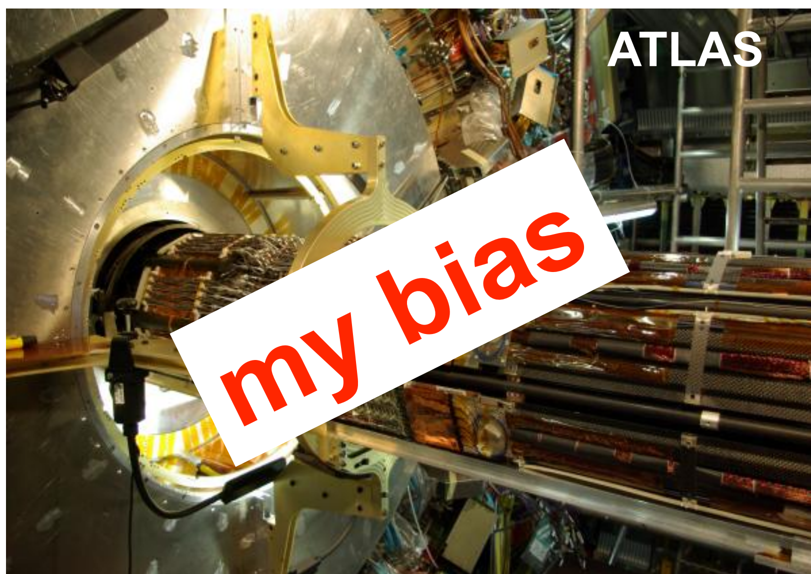
●	0kGy
●	0.5kGy
●	1kGy
●	2kGy
●	5kGy
●	10kGy
●	20kGy
●	100kGy

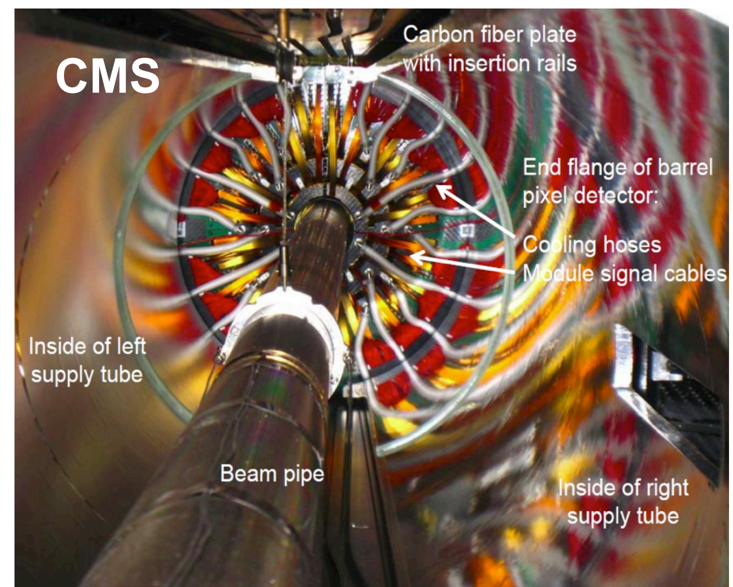




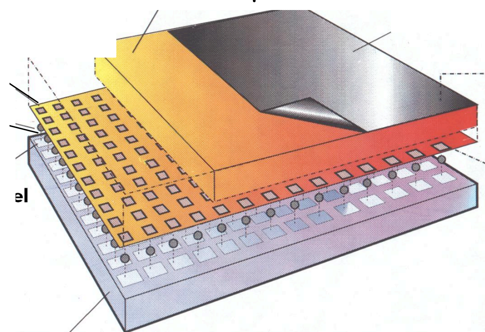


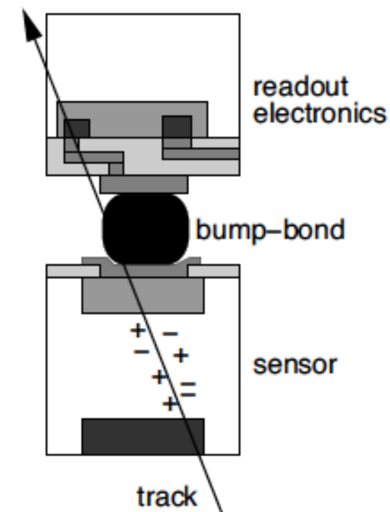
Today's "state of the art" of running detectors





all based on
"Hybrid Pixel Detectors"

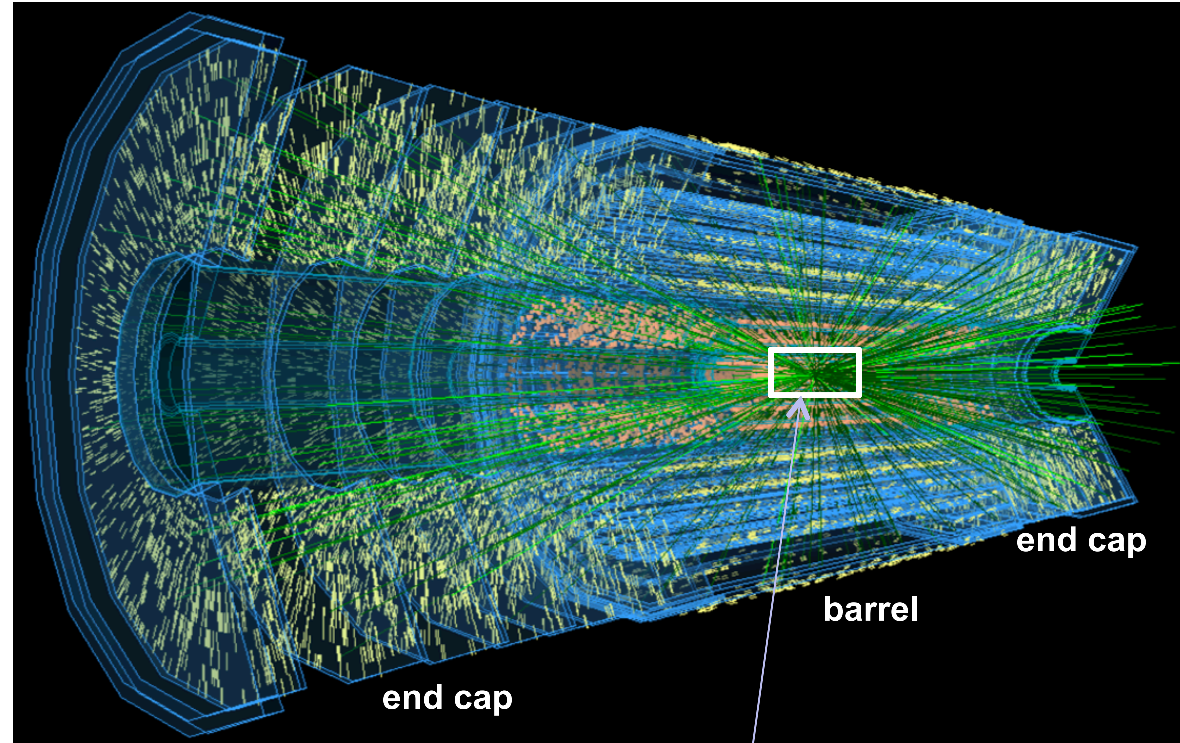




Challenges for the LHC upgrades

Increased luminosity requires

- higher hit-rate capability
- increased granularity
- higher radiation tolerance
- lighter detectors



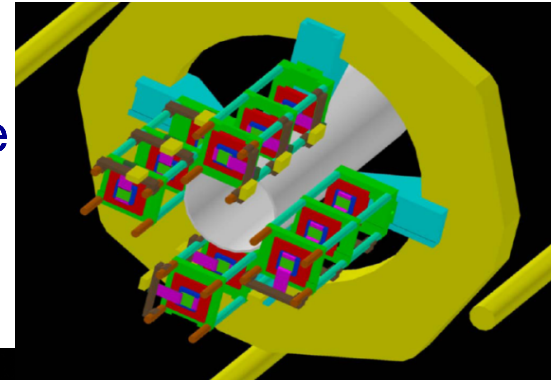
we are here

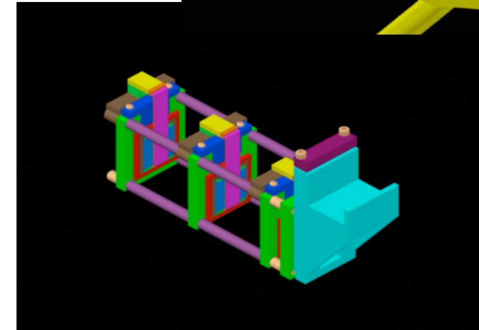
Radiation hardness and rate increase compared to now

- phase 0 (2015) ≈ × 5
- phase 1 (2018) ≈ × 5-10
- phase 2 (2023) ≈ × 10-30

DBM – Diamond Beam Monitor

- radiation hard due to
  - 5x larger band gap than Si ⇒ no leakage current
  - strong lattice (x2 stronger than Si) ⇒ less NIEL damage





- low Z

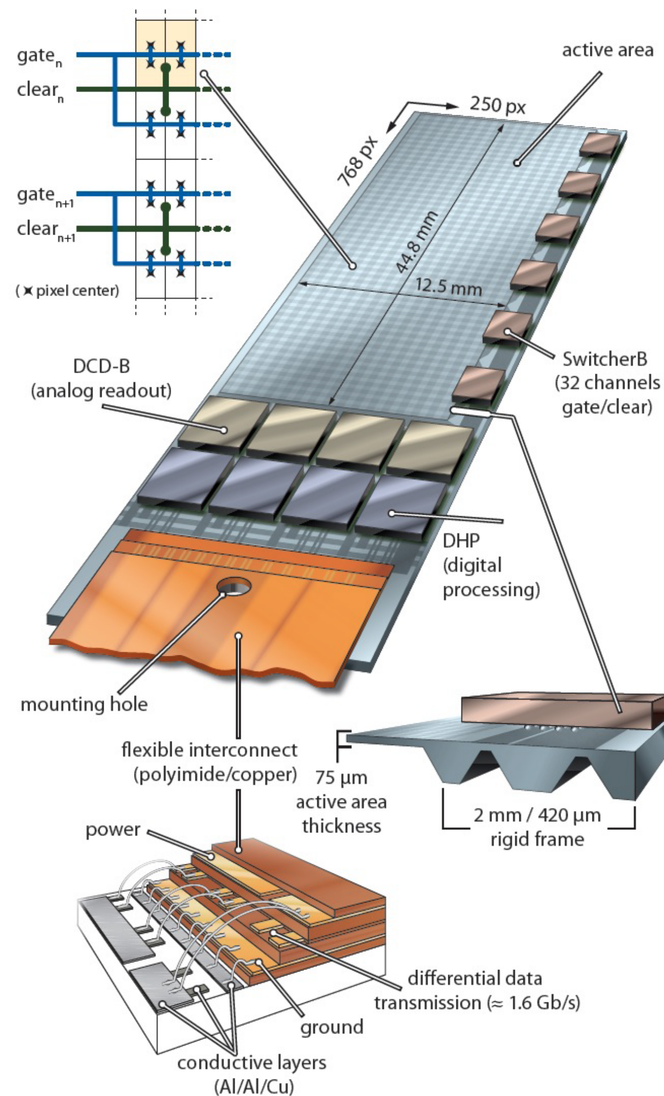
- first pixel use in ATLAS:
  Diamond Beam Monitor (DBM) – 24 telescopes

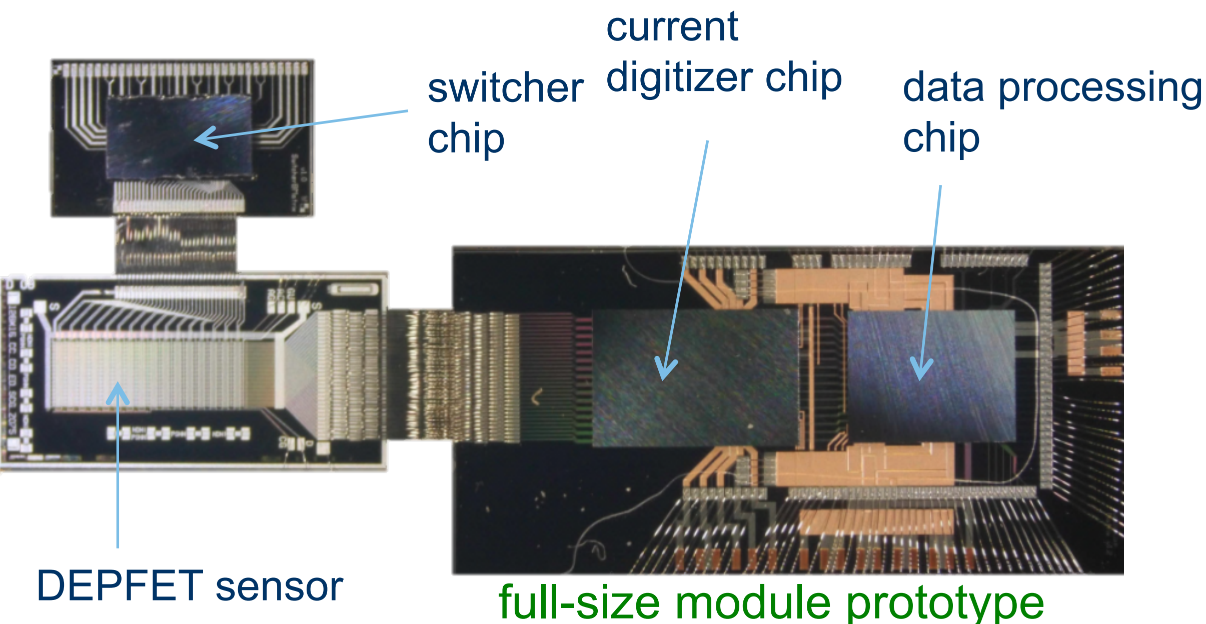
η = 1.4
1106 mm
617 mm
560 mm
η = 2.2
275 mm
149.6 mm
88.8 mm
R=0 mm
DBM
2720.2 2505
2710
2115.2
1771.4
1399.7
1299.9
1091.5 934 848
853.8
650 580
495
400.5
z=0 mm
SCT end-cap
TRT end-cap
Pixel
end-cap
Pixel barrel

DEPFET PXD @ Belle II @ SuperKEKB

2-layer pixel vertex detector (PXD)

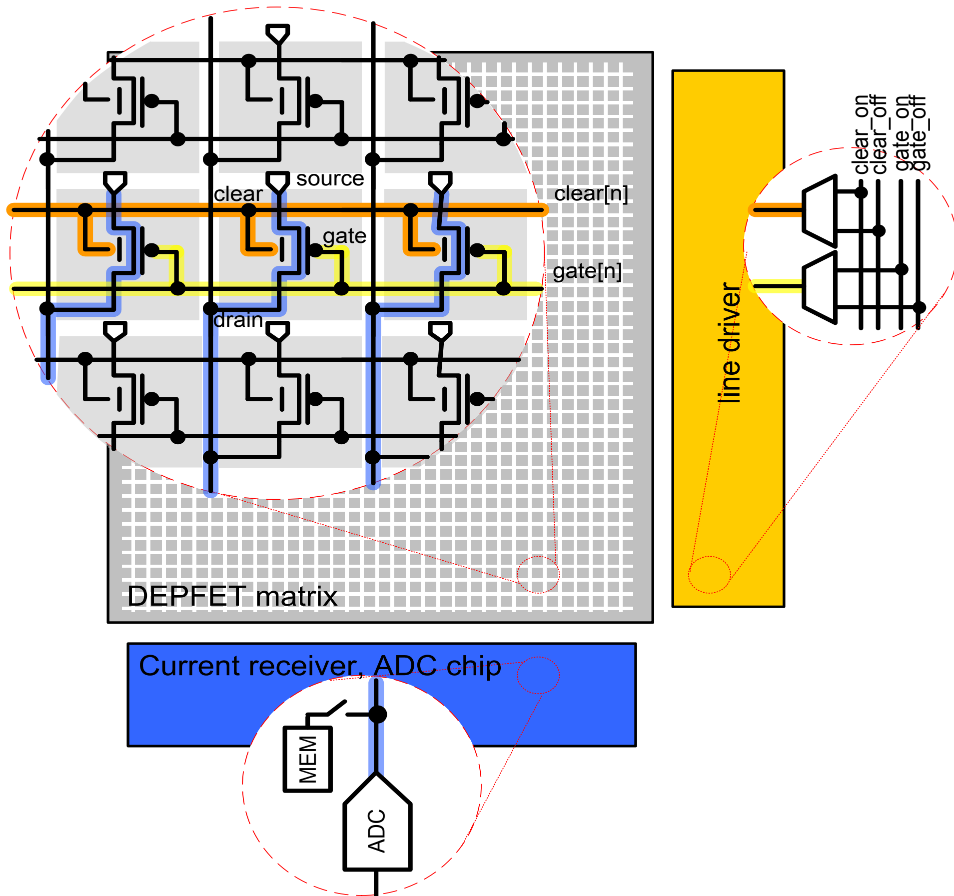
2 layers
50x75μm² pixels
0.21% X_0





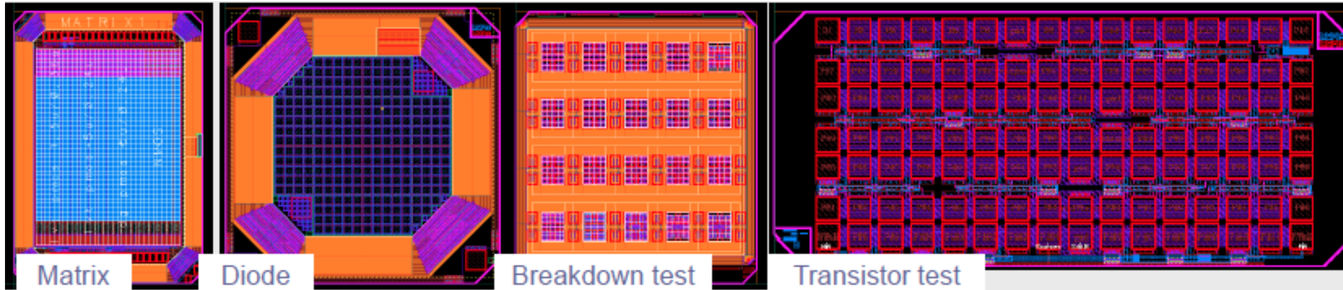
full-size module prototype

DEPFET pixel array



- DEPFET pixel transistors arranged in a matrix
- row wise select -> column wise readout of transistor (drain) currents
- Gate and clear lines need a steering chip
- Long drain readout lines to keep material out of the acceptance region
- 100 ns per row
  20 µs per frame

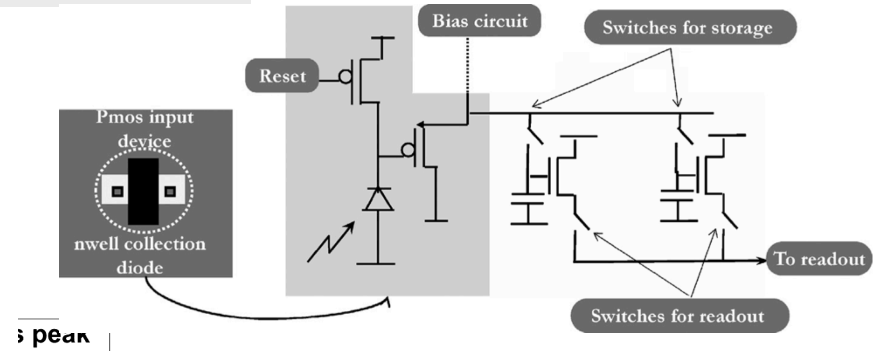
HR-CMOS pixels

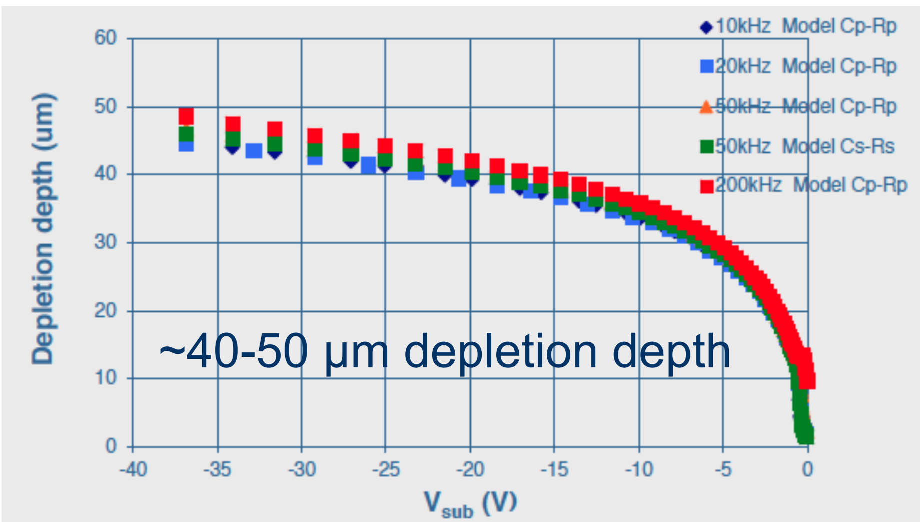


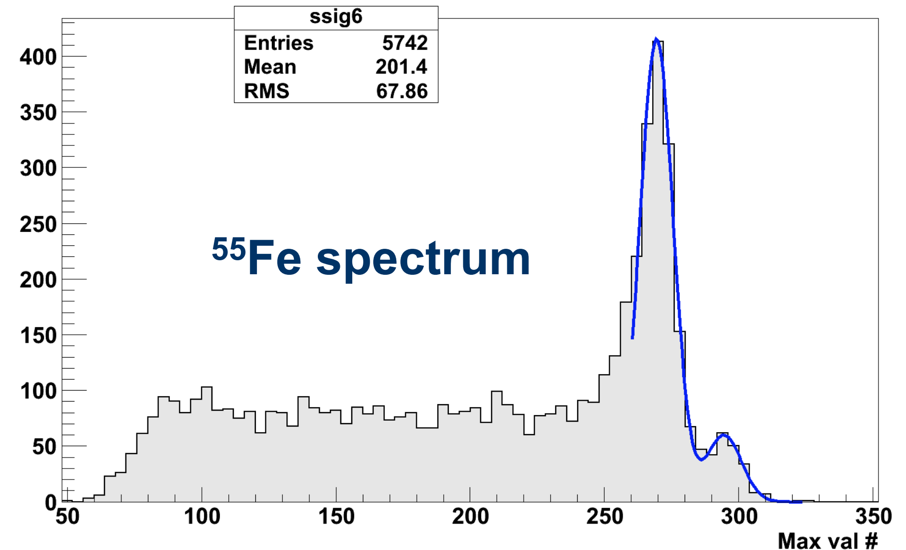
LePIX (Walter Snoeys et al.) IBM 90 nm
... exploring the high resistivity route (> 0.5 kΩ cm)
NIM A 718 (2013) 288-291

radiation tolerance: > 10^{14} n_{eq}/cm^2 and 10 Mrad

2 transistors in pixel







3D Integration

Cu-Cu bonding (Tezzaron)

Wire
Bond pads

2nd wafer

12 um

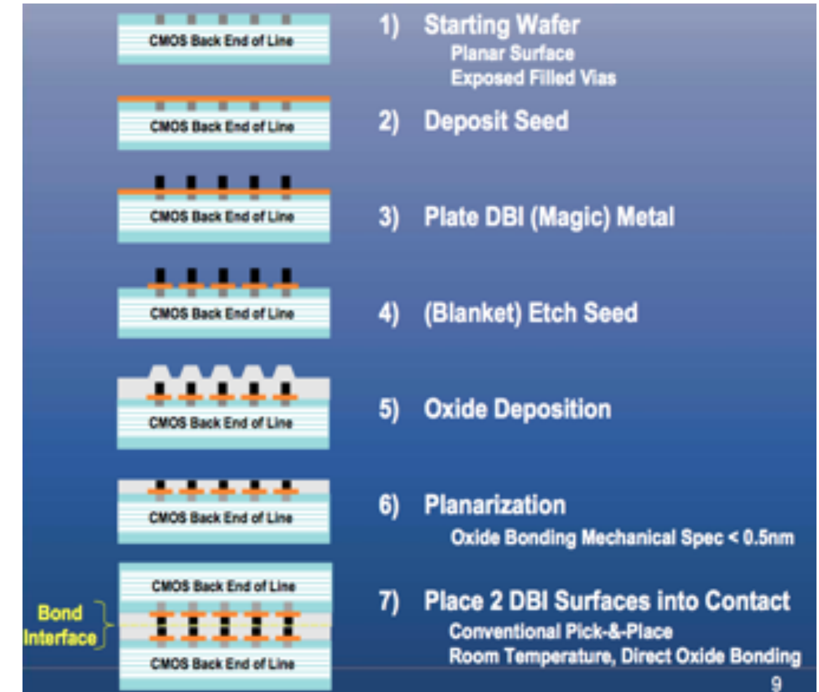
1st wafer

tier1 tier2

3D bonding

rotational and transitional misalignment

Oxide-Oxide bonding (Ziptronix)

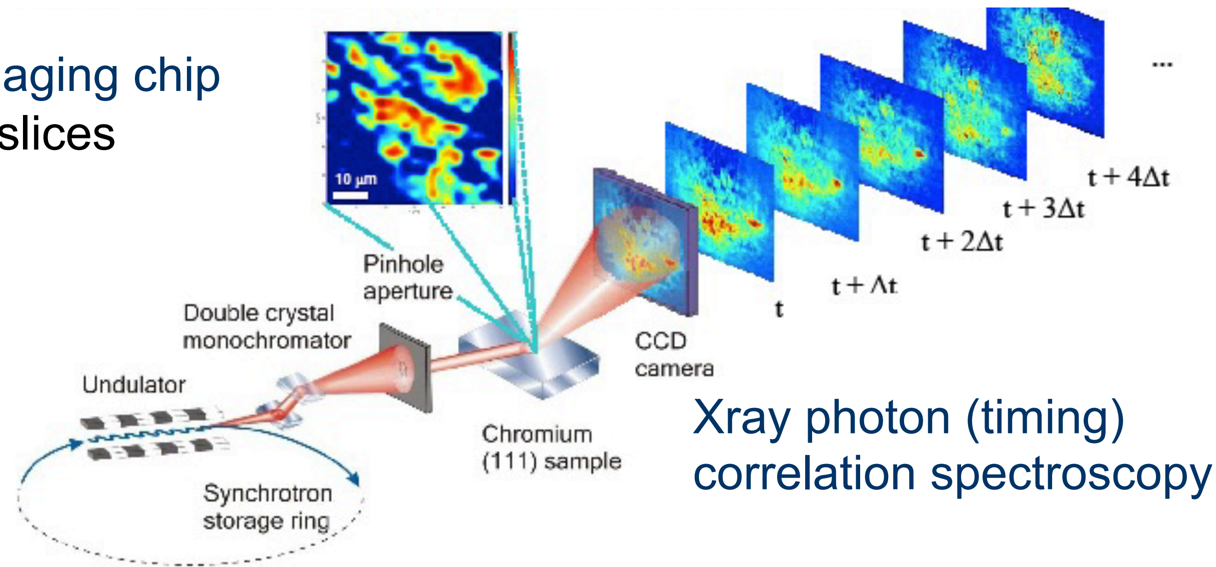


wafer level stacking and bonding has been
a painful (4 year) experience (Ray Yarema, Vertex2013) ... but ... finally

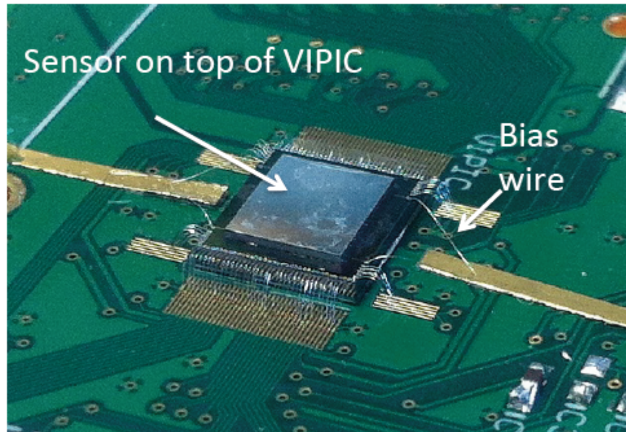
3D integration: A FIRST working chip with 3D integration for imaging

a working 3D integrated chip ...

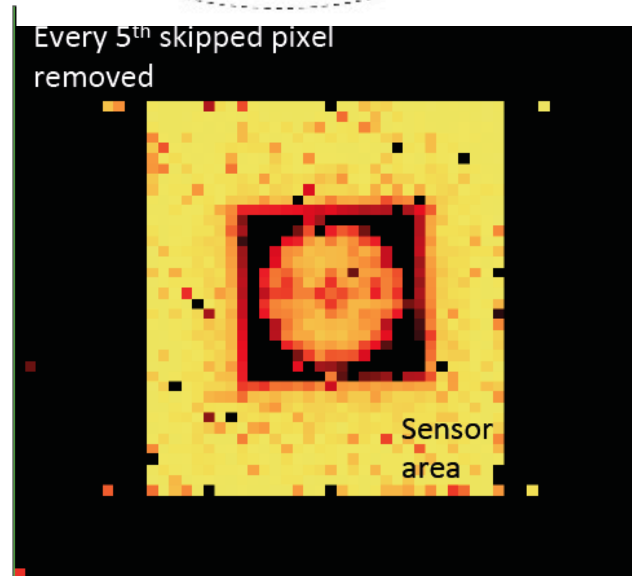
- VIPIC vertically integrated photon imaging chip
- goal: buffer and readout image time slices w/ dead time less readout
- output time stamped information
- circuitry needed would else not fit in cell area



Xray photon (timing) correlation spectroscopy



- Detector biased at 120V
- Detector tested using 2 sources ^{109}Cd 22keV and ^{55}Fe 5.9keV (mask not shown in above photo)



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