

Radiation-hard Active Pixel Sensors for HL-LHC Detector Upgrades based on HV-CMOS Technology

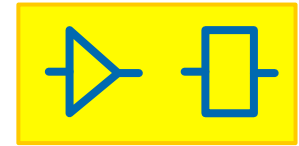
Malte Backhaus – on behalf of the ATLAS Smart CMOS Pixel collaboration

Outline

- HV2FEI4 introduction
 - “Sensor”
 - Readout chip
- Lab results
- Test beam results
- Irradiation results
- Outlook
 - Alternative submissions
 - Summary
 - ATLAS Smart CMOS Pixel Collaboration



Sensor

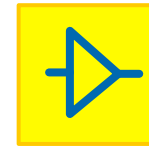


FE chip

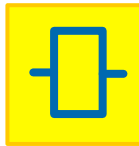
Chip to chip
bump bonding



Sensor



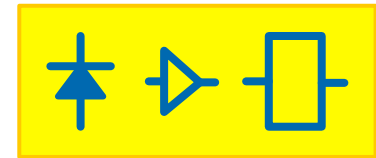
Analog
tier



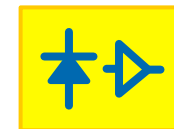
Digital
tier

Chip to chip
bump bonding

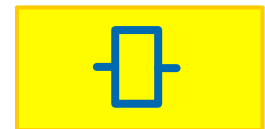
Wafer to wafer
bonding



Diode + Amp + Digital



Diode +
full analog
processing

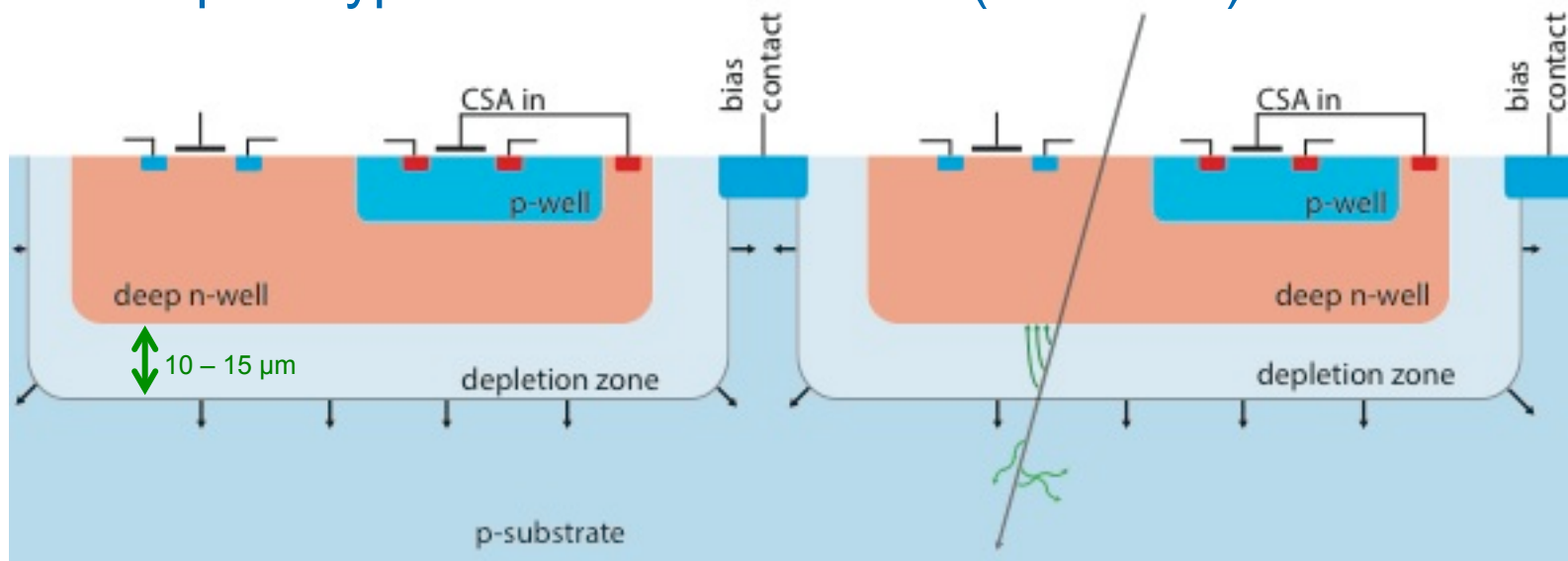


Digital only FE
chip

Wafer to wafer
bonding

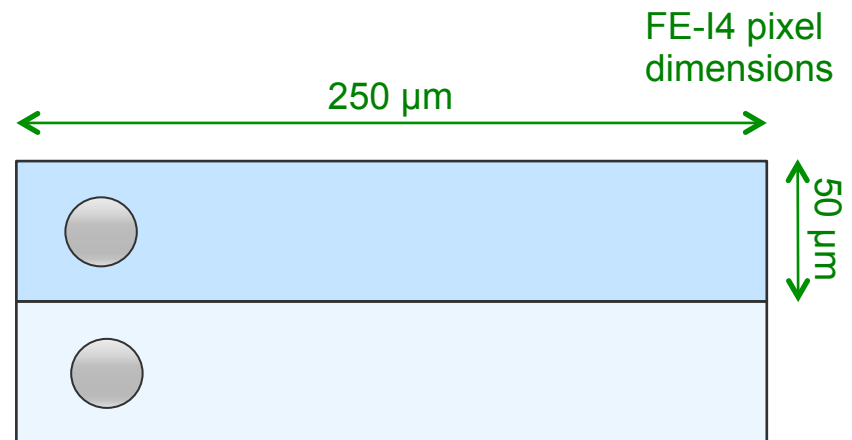
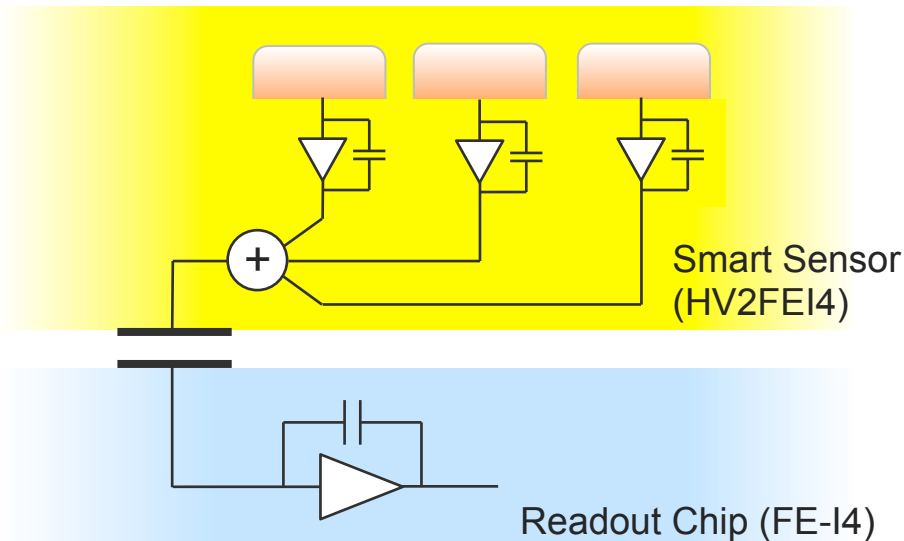
HV2FEI4 Concept

- Use bulk of commercial HV/HR-CMOS process as sensor
- Deep n-well → collection electrode
 - PMOS transistors unshielded from charges → design constraints
 - p-well used for NMOS transistors
- AMS prototypes in characterization (HV2FEI4)



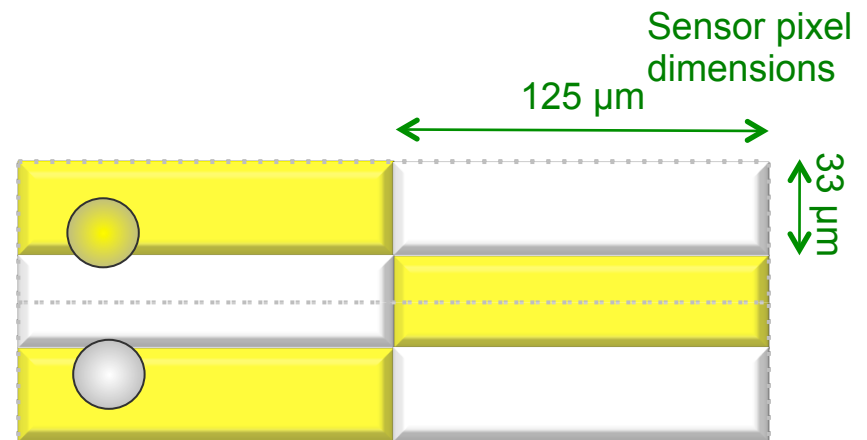
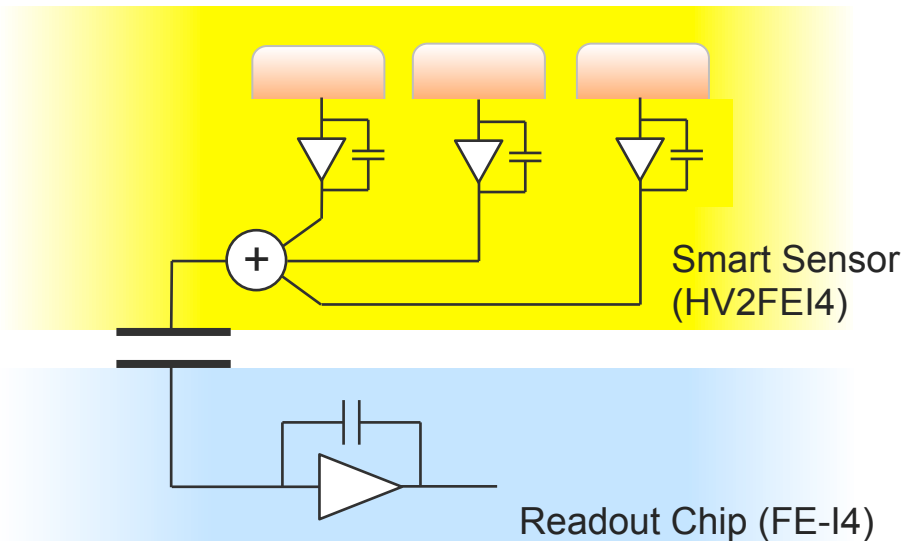
HV2FEI4 Sensor

- Limited logic implementation in sensor:
 - CSA + Discriminator
 - Adjustable sub-pixel output pulse (for AC coupled signal to FE)
 - Adding of sub-pixel pulses



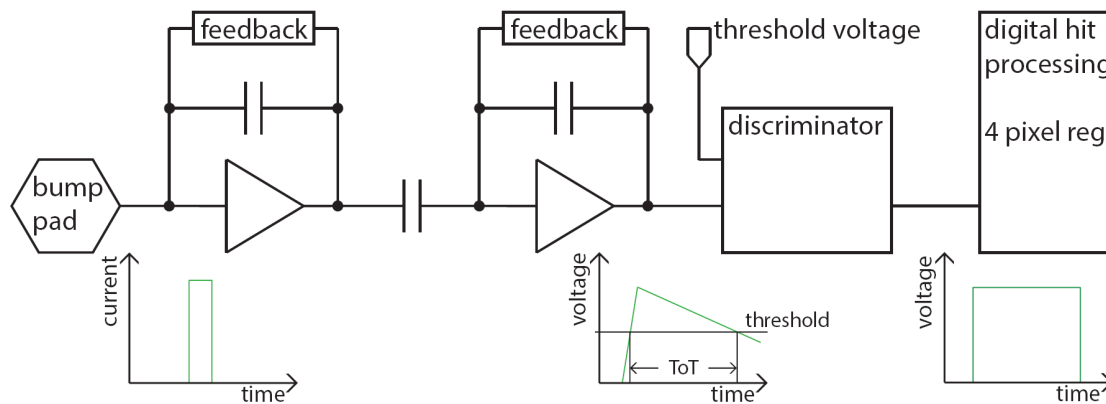
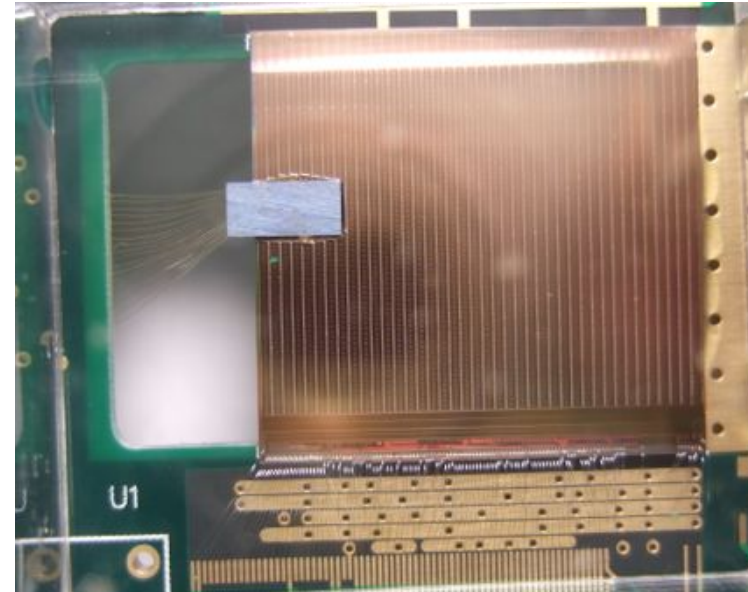
HV2FEI4 Sensor

- Limited logic implementation in sensor:
 - CSA + Discriminator
 - Adjustable sub-pixel output pulse (for AC coupled signal to FE)
 - Adding of sub-pixel pulses
- Six sub-pixels connect to two FE pixels



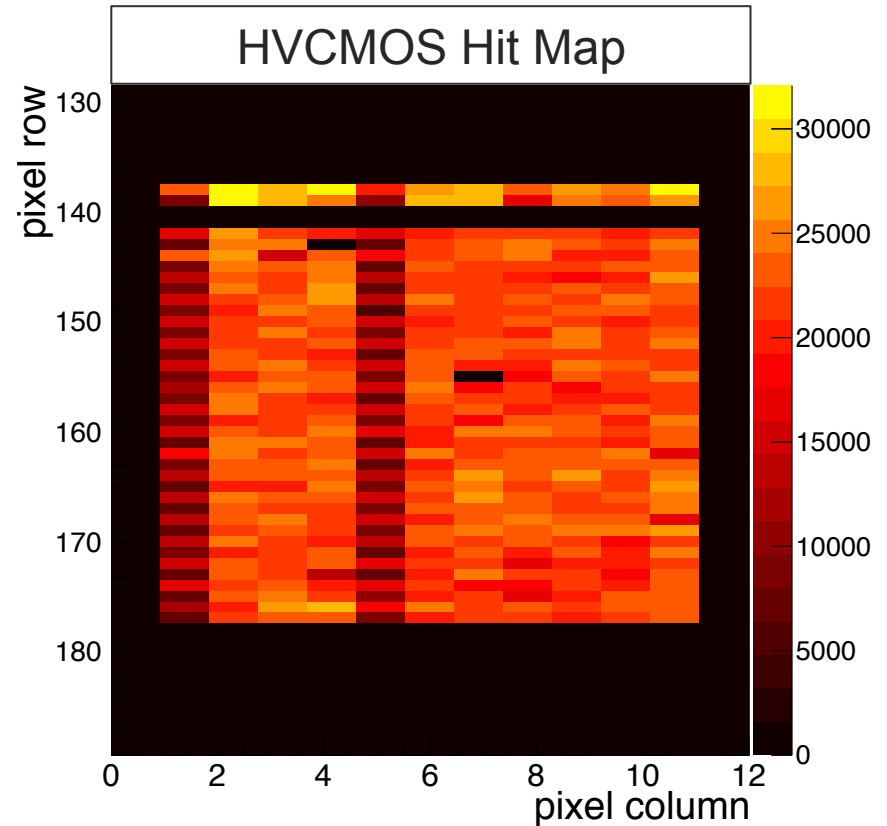
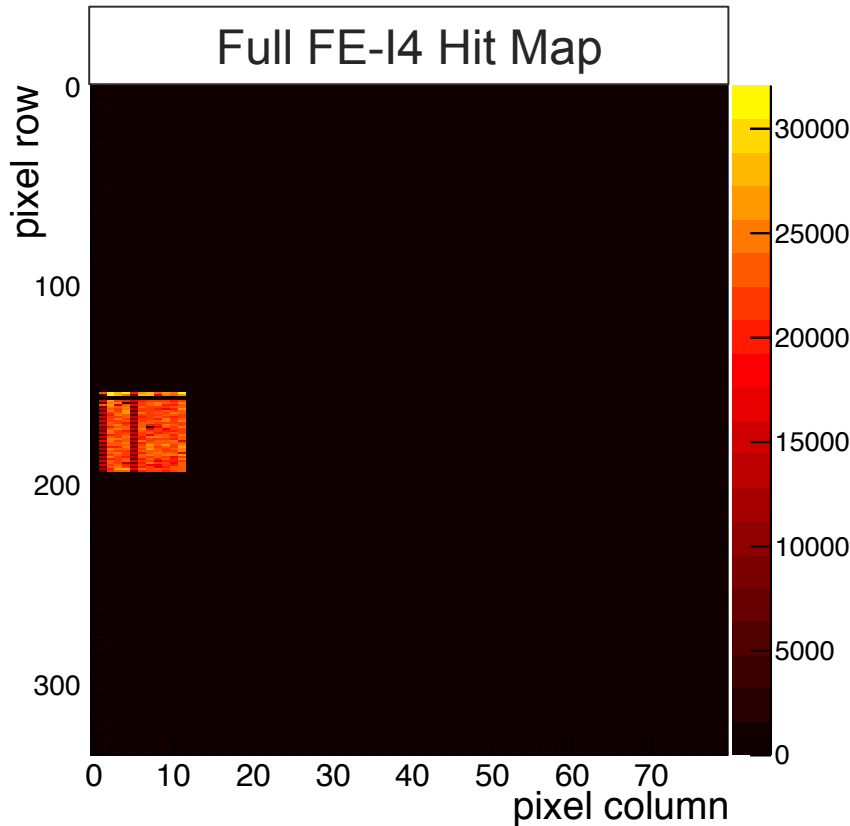
Readout Chip – FE-I4

- Use IBL readout chip: FE-I4
- Huge complexity
- Designed for passive sensor
- Pixel size $50 \times 250 \mu\text{m}$
→ area of 3 „sensor“ chips
- „Smart sensor“ glued to FE-I4
- Analog information (TOT)
→ Can be used for sub-pixel decoding



Source Scan Occupancy

^{90}Sr

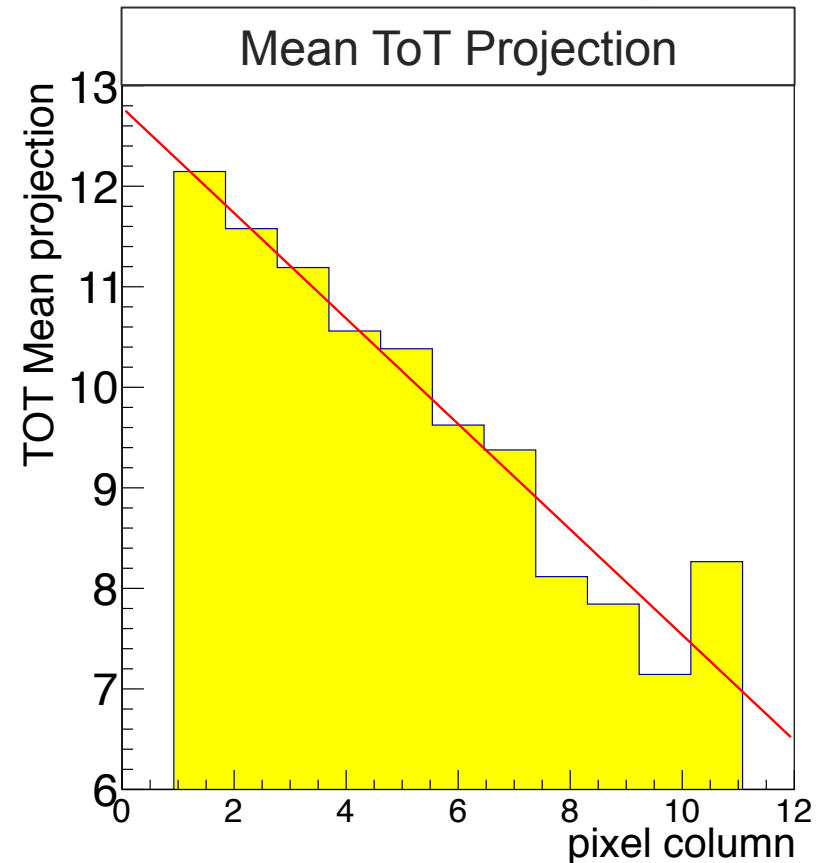
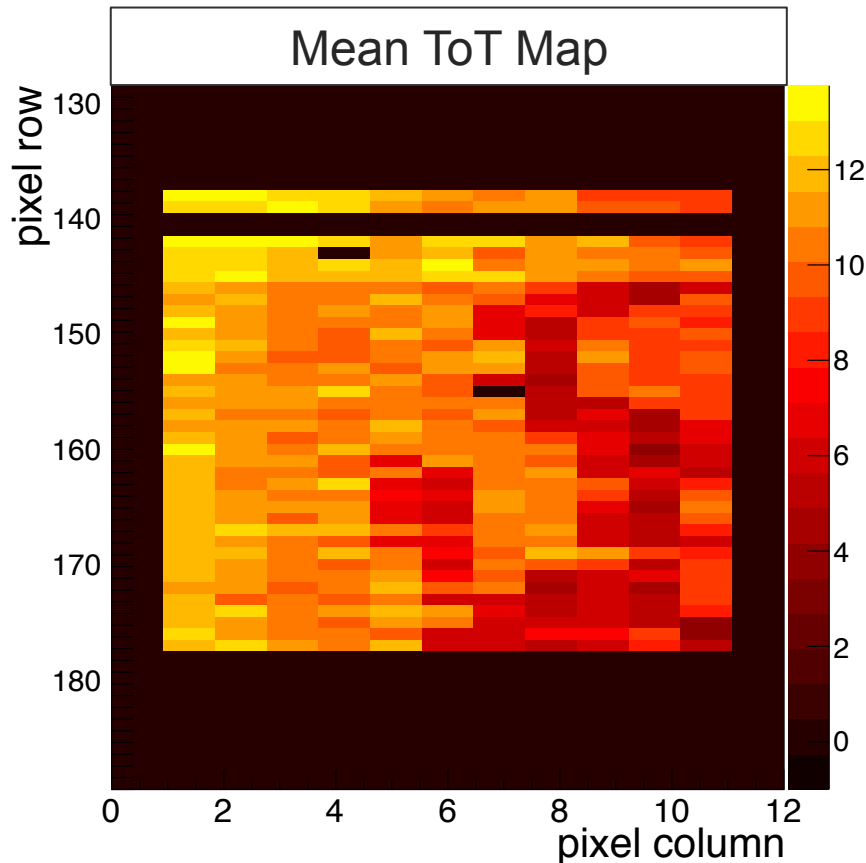


→ Full FE-I4 pixel matrix active

→ Charges generated in sensor transmitted to FE-I4 (AC coupled)

AC Coupled Signal Transmission

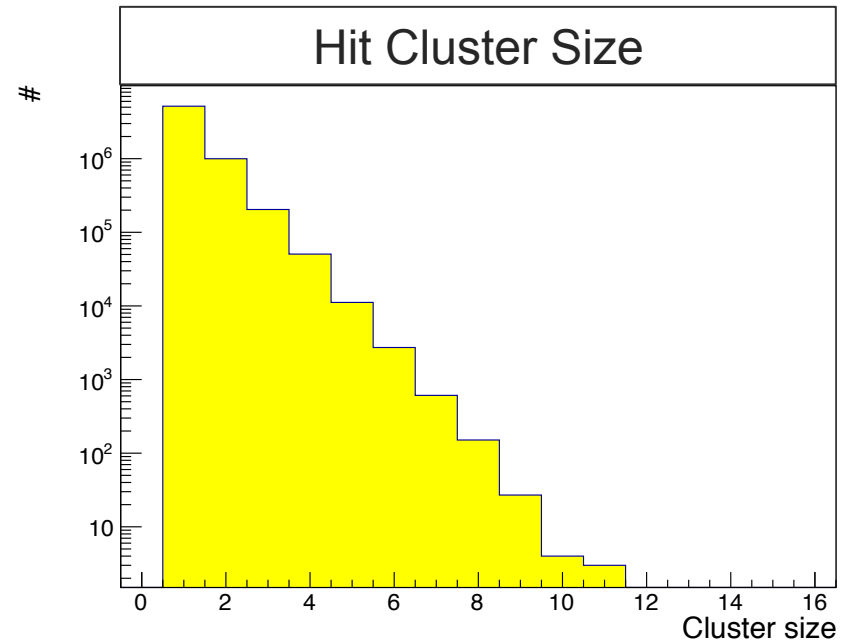
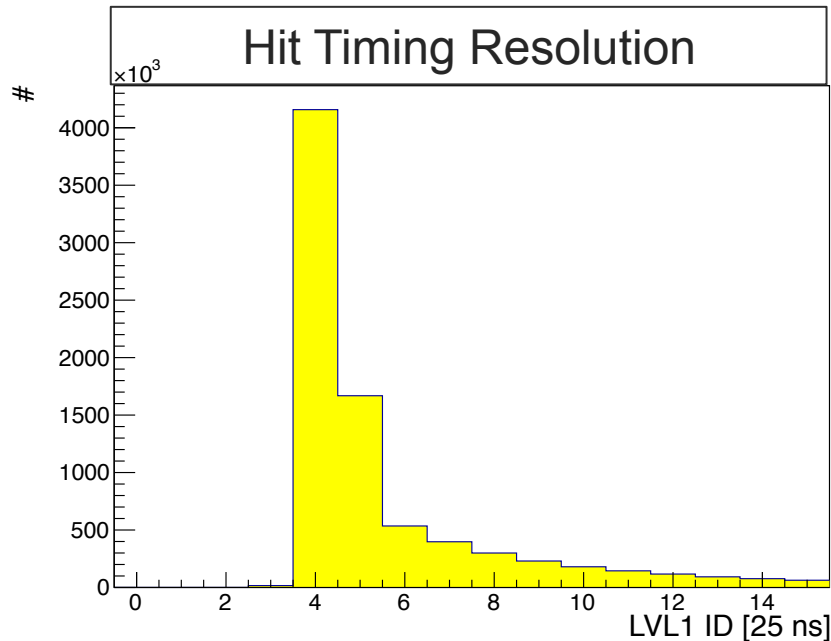
90Sr



- ToT indicator for AC coupling strength
- Tilt of sensor or output pulse amplitude

Source Hit Timing and Cluster

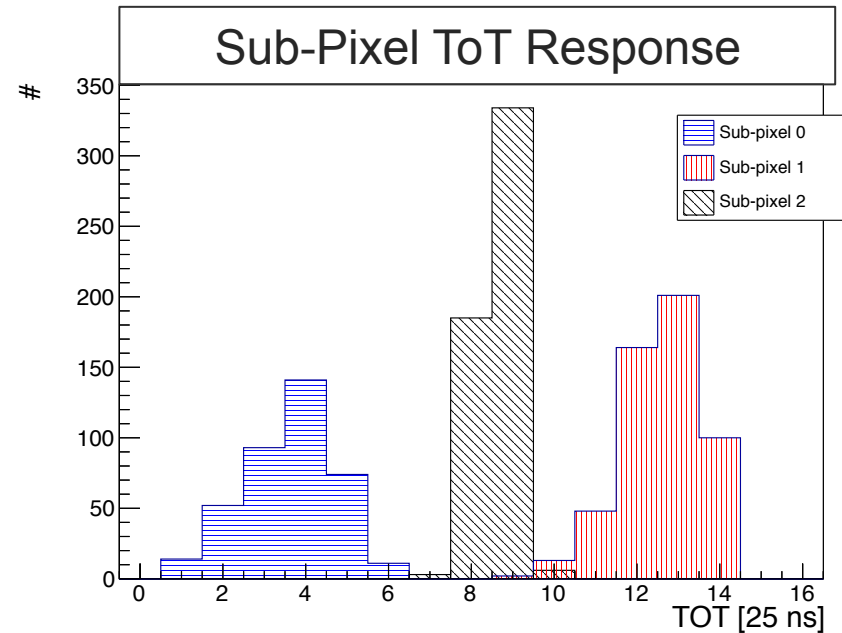
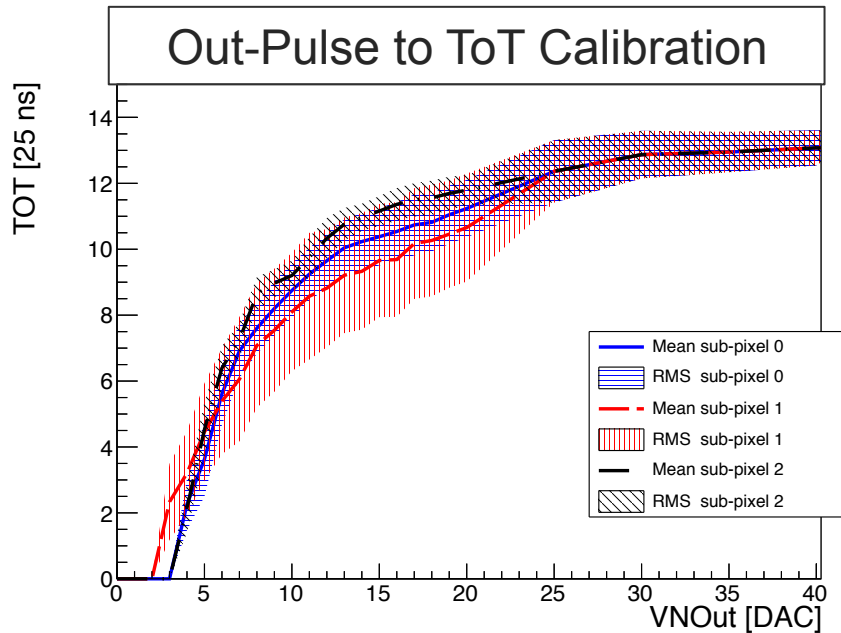
90Sr



- Hits with significant delay recorded, time-walk sources present twice
- Sub-pixel resolution + dedicated algorithm mandatory for investigation
- Large hit clusters present

Sub-Pixel Resolution

- Convolved scans possible with new HVCMOS support in USBpix
- Puls adding disabled, test charge injections



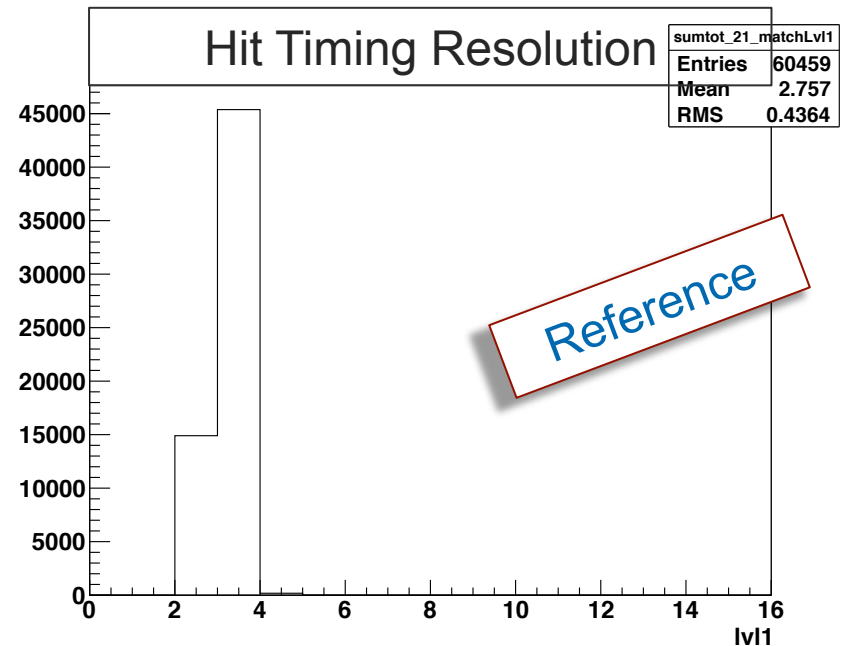
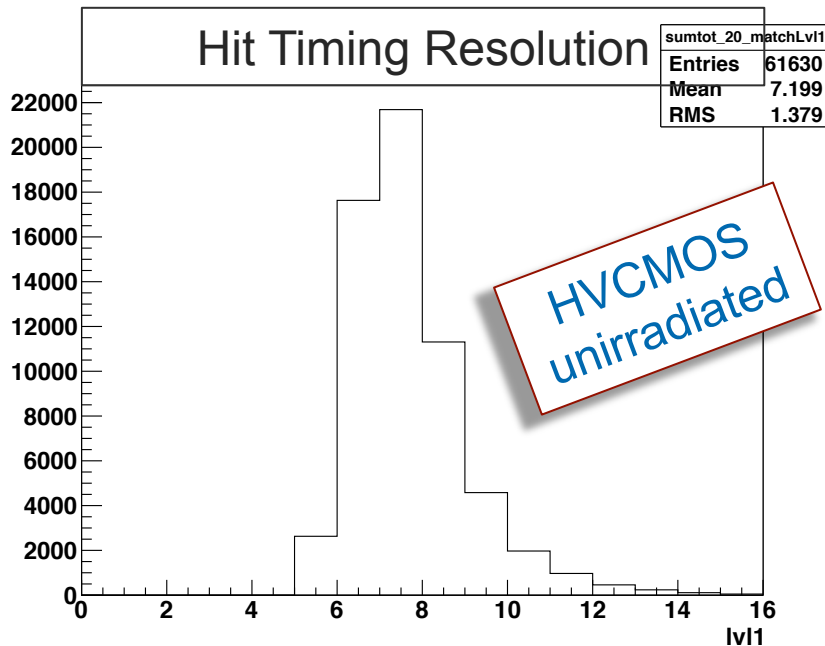
- Distinct ToT peaks → sub-pixel resolution demonstrated
- Tuning algorithm and test beam necessary for spatial resolution measurement

Test Beam Results – Introduction

- Tuning algorithm for “full matrix sub-pixel reconstruction” under development
 - Single test system for “smart sensor + FE-4” mandatory
 - USBpix integration
 - No sub-pixel reconstruction serious challenge for test beam measurements (temporally):
 - Alternating pixel connection pattern → challenging alignment
 - Sub-pixel resolution mandatory for in-pixel efficiency measurements
- **Careful** conclusions on radiation hardness from test beam / lab results, although very promising (Samples “alive” after up to $10^{16} n_{eq} \text{ cm}^{-2}$)

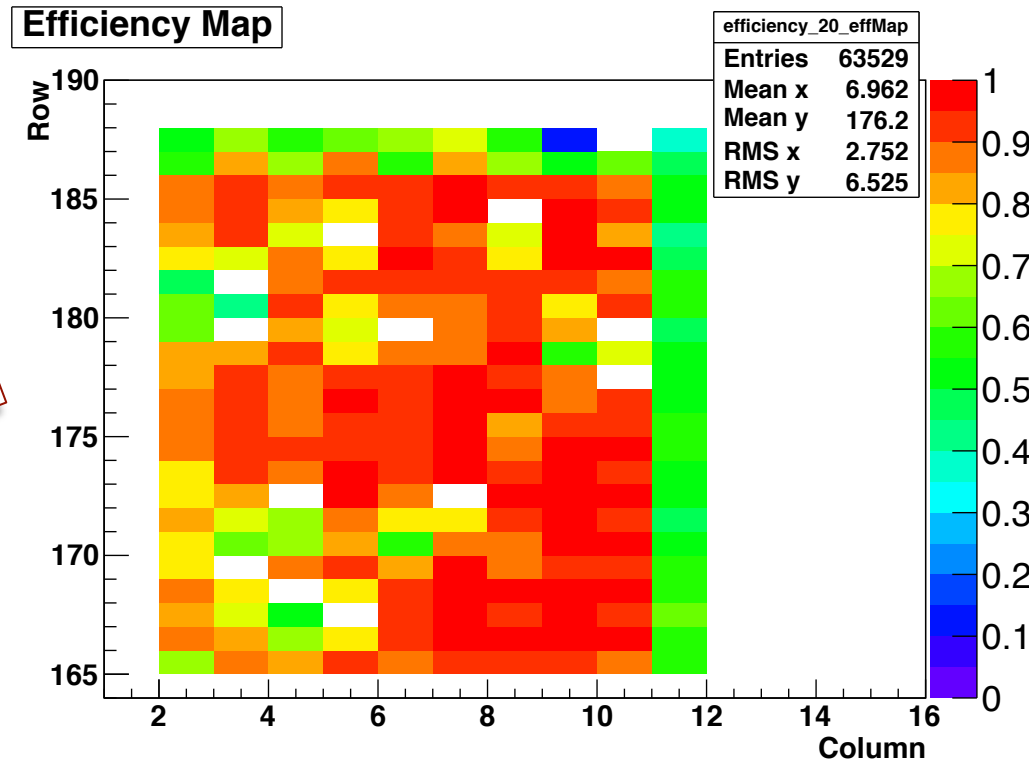
Test Beam Results – Timing Resolution

→ DESY test beam, 4 GeV e



→ Hits with delayed detection

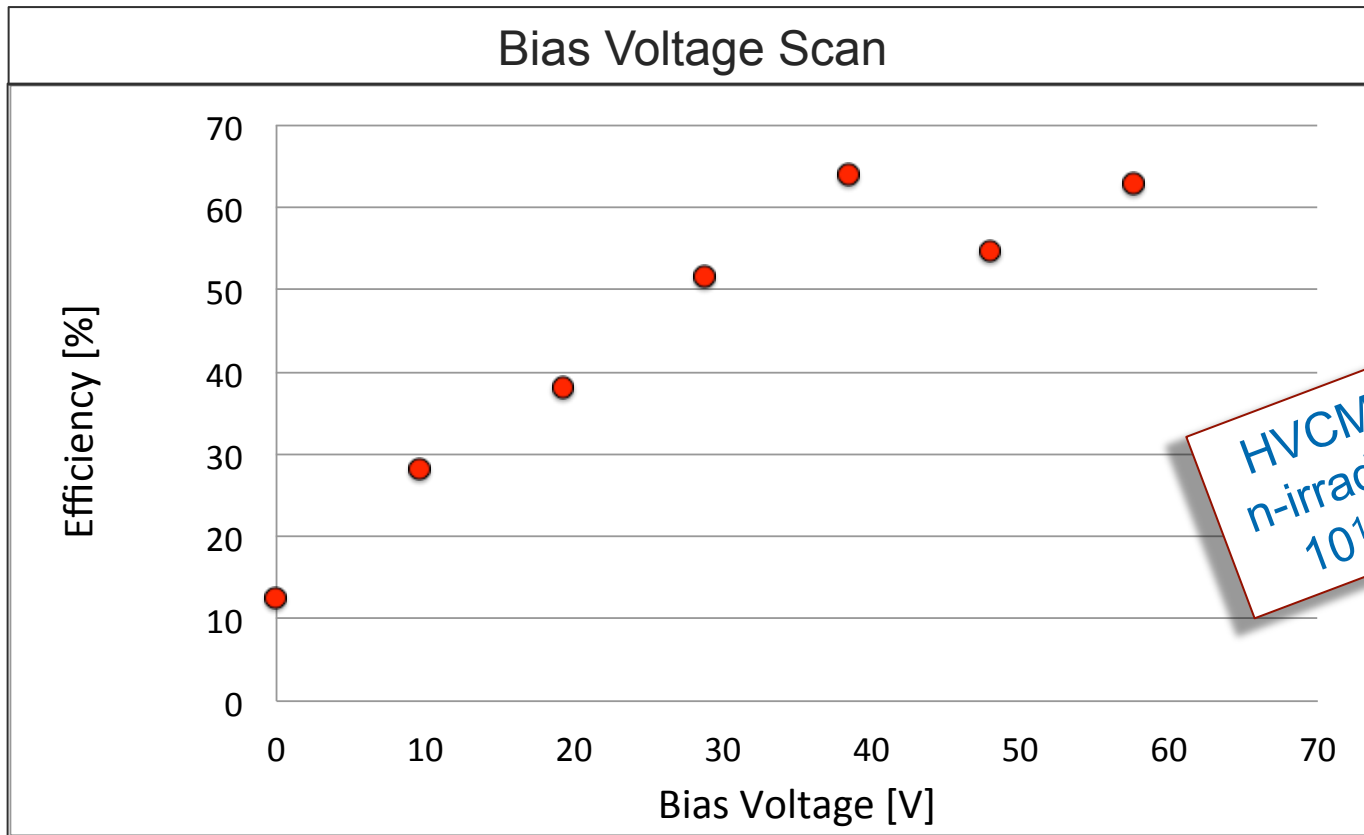
Test Beam Results – Mean Efficiency



HVCMOS
unirradiated

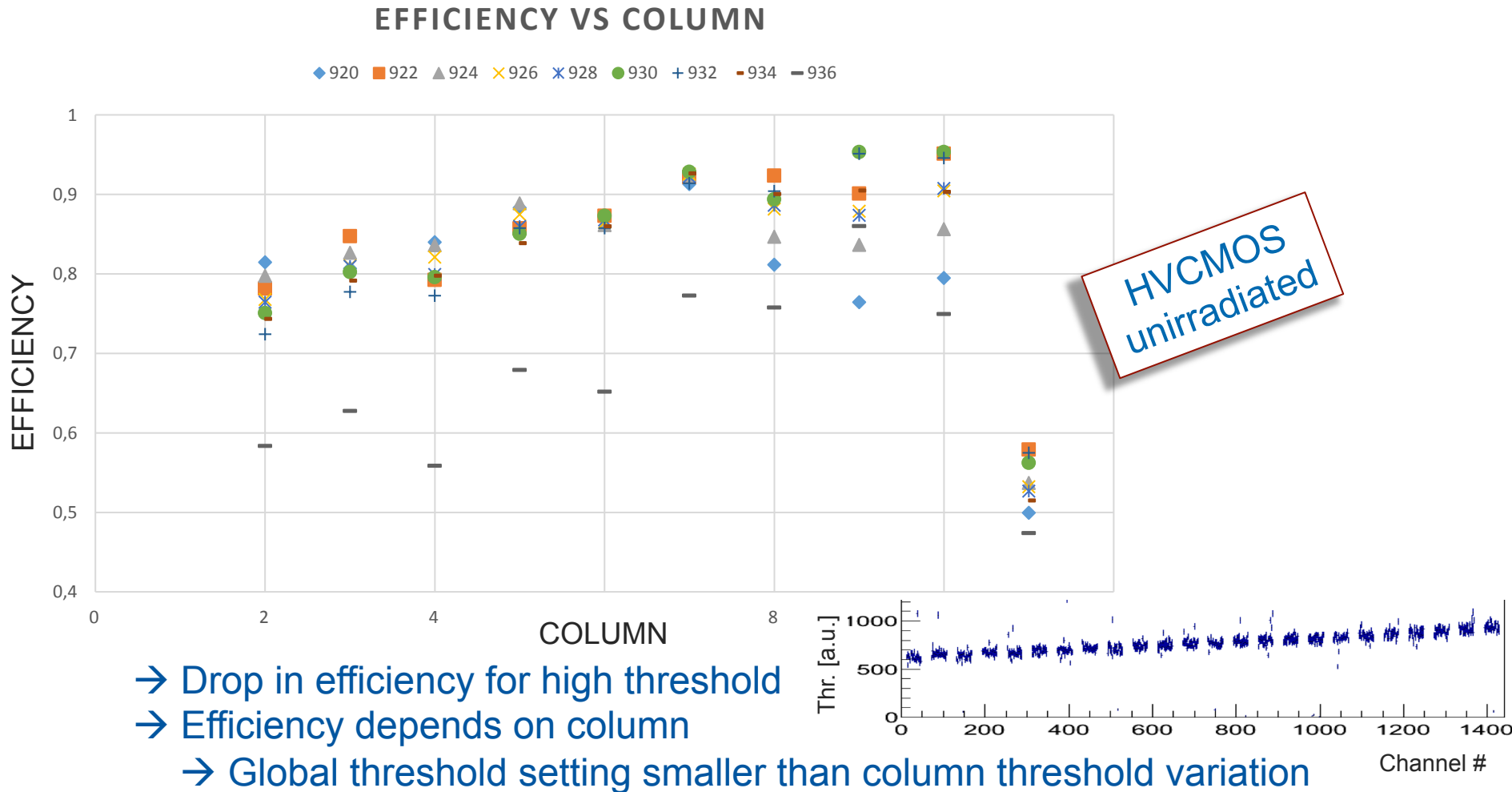
- Reduced efficiency at edges and around dead pixels to be investigated
- Again column dependency → Powering of HVCMOS columns

Test Beam Results - Scans

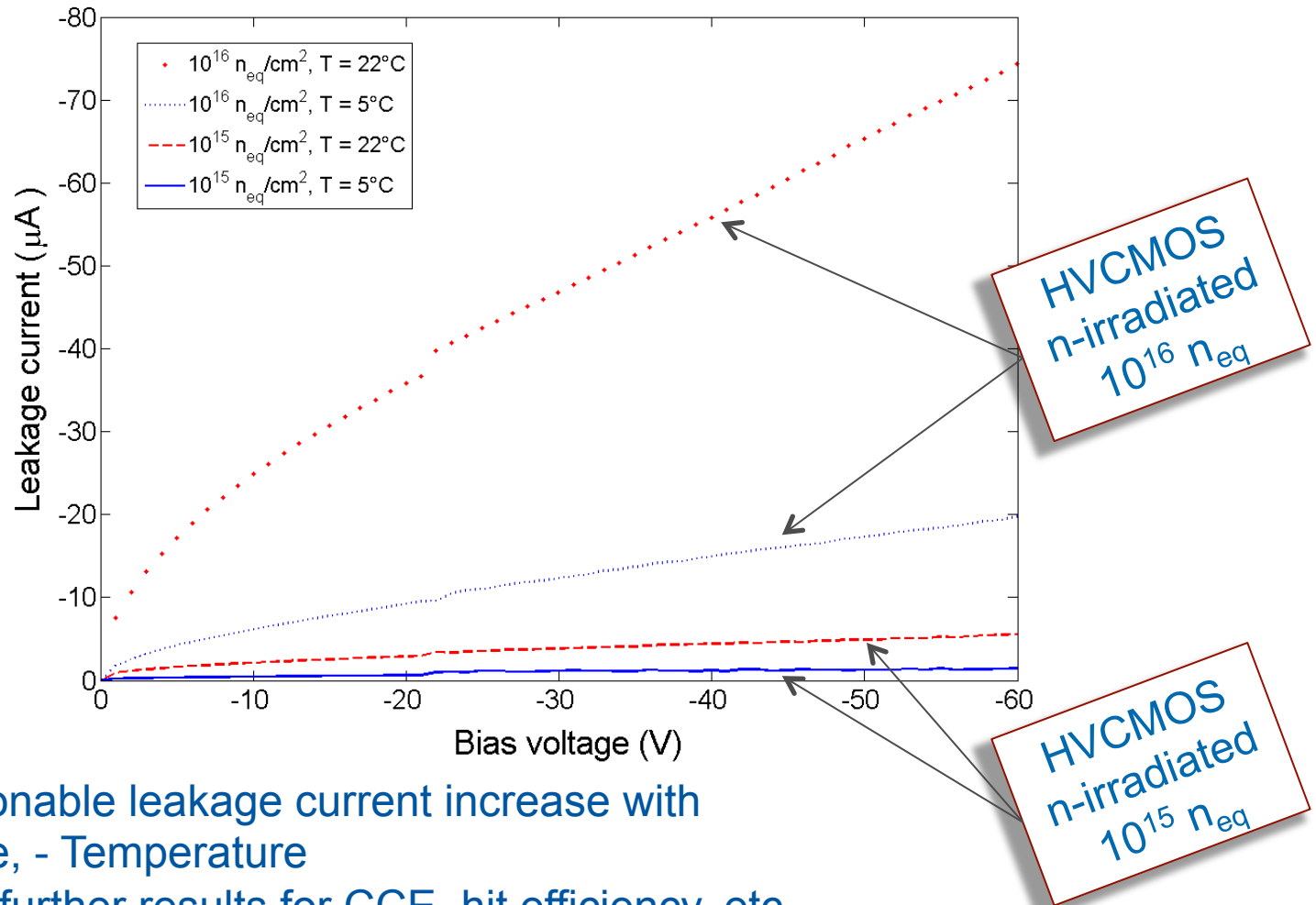


→ Bias voltage increases efficiency

Test Beam Results – Column Efficiency

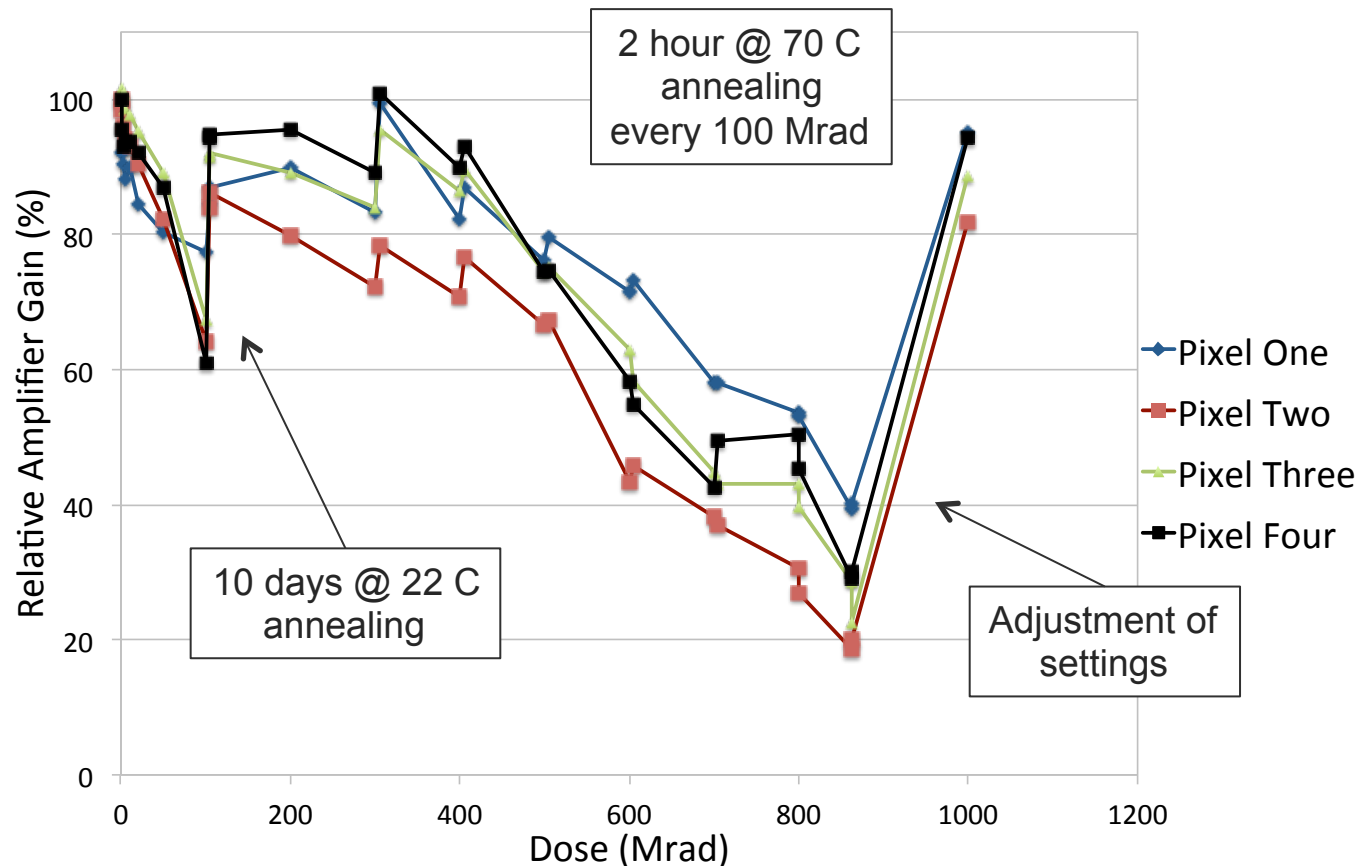


Irradiation Studies – Bulk Damage



- Reasonable leakage current increase with
 - Dose, - Temperature
- Need further results for CCE, hit efficiency, etc.

Irradiation Studies – Electronics



- Decrease of Preamplifier gain with irradiation
- Annealing periods observable
- Parameter tuning recovers to 90 % gain after ~ 900 Mrad

Smart CMOS Pixel Submissions Overview

Submissions targeting R&D with FE-I4 readout

HVCMOS:

- AMS 180 nm – V1: First prototype In test
- AMS 180 nm – V2: Radiation hard electr. design In test

HRCMOS:

- GF 130 nm: First prototype In test
- LFoundry 150 nm: First prototype In design
(→ march/april 2014)

Conclusions

- Promising **HVCMOS** and **HRCMOS** prototypes submitted and in hand
- Large step towards **on sensor analog signal processing + digital FE**
- AC coupled signal transmission demonstrated
 - Research on gluing techniques started
- Sub-pixel resolution possible
 - Detailed characterization to come
 - Complicated tuning and reconstruction algorithms under development
- Radiation hardness of process very promising
 - Physics hits detected after several hundred Mrad (not shown here)
 - Radiation hard electronics for LHC environment feasible
- **A lot achieved – more work ahead!**



ATLAS Smart CMOS Pixel Collaboration

- **University of Bonn:**
L. Gonella, T. Hemperek, T. Hirono, F. Hügging, J. Janssen, H. Krüger, T. Obermann, N. Wermes
- **LBNL:**
M. Garcia-Sciveres
- **CERN:**
M. Backhaus, M. Capeans, S. Feigl, S. Fernandez-Perez, M. Nessi, H. Pernegger, B. Ristic
- **University of Geneva:**
S. Gonzales-Sevilla, D. Ferrere, G. Iacobucci, A. La Rosa, A. Miucci, D. Muenstermann
- **University of Göttingen:**
M. George, J. Grosse-Knetter, A. Quadt, J. Rieger, J. Weingarten
- **University of Glasgow:**
R. Bates, A. Blue, C. Buttar, D. Hynds
- **University of Heidelberg:**
C. Kreidl, I. Peric
- **CPPM:**
P. Breugnon, P. Pangeaud, S. Godiot-Basolo, D. Fougeron, F. Bompard, J.C. Clemens, J. Liu, M. Barbero, A. Rozanov